Ö2.1

```
library ieee;
use ieee.std_logic_1164.all;
entity C2_1 is
  port (X  : in  integer;
        Z  : out integer);
end C2_1;

architecture A2_1 of C2_1 is
begin
  Z <= X + 10;
end A2_1;
```

Ö2.2

```
library ieee;
use ieee.std_logic_1164.all;
entity C2_2 is
  port (X,
        Y  : in  std_logic;
        Z  : out std_logic);
end C2_2;

architecture A2_2 of C2_2 is
begin
  Z <= X and Y;
end A2_2;
```

Ö2.3

```
library ieee;
use ieee.std_logic_1164.all;
entity C2_3 is
  port (X0,
        X1 : in  std_logic;
        Z  : out std_logic);
end C2_3;

architecture A2_3 of C2_3 is
begin
  process (X0, X1)
    subtype select_type is std_logic_vector (1 downto 0);
  begin  -- process
    case select_type'(X0 & X1) is
      when "00"|"10"|"11"  => z <= '1';
      when others          => z <= '0';
    end case;
  end process;
end A2_3;
```

Ö2.4

```
library ieee;
use ieee.std_logic_1164.all;
```

```
entity C2_4 is
  port (X0,
        X1,
        X2 : in  std_logic;
        Z  : out std_logic);
end C2_4;

architecture A2_4 of C2_4 is
begin
  Z <= X0 xor X1 xor X2;
end A2_4;
```