

# COMPARATIVE STUDY OF LOW-VOLTAGE PERFORMANCE OF STANDARD-CELL FLIP-FLOPS

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## ABSTRACT

The static single-phase D flip-flop is the basic memory element in the standard cell based design methodology for digital integrated circuits. In low-power high-speed performance designs, pipelining in conjunction with voltage scaling has proven to be an efficient approach to achieve the targeted low-power performance. The efficiency of the flip-flop at low power supply voltages will therefore play an increasingly important role. In this paper a comparison of the efficiency of six different D flip-flops operating at different voltages are presented and discussed. All circuits in this paper have been designed in a 0.6  $\mu\text{m}$  CMOS technology and the results have been obtained from analog simulation. This study shows that power savings are possible in power-driven synthesis by including different flip-flops that are based on different design styles in the standard cell library.

## 1. INTRODUCTION

Power consumption appears to have become one of the most important design issues in digital CMOS design for an increasing number of electronic products. High performance ICs (Integrated Circuits) are nowadays defined by their computational capability and power consumption. High performance ICs are integrated in mobile systems, such as cellular telephones and portable multimedia terminals, where the energy resources are limited by batteries. From the user's perspective, battery lifetime is important.

The dominating component of the total power consumption is the dynamic power consumption ( $P_{dyn}$ ). It can be approximated with the expression:

$$P_{dyn} = \frac{1}{2} \cdot \alpha \cdot C_L \cdot V_{dd}^2 \cdot f$$

where  $P_{dyn}$  is the power consumed when a gate is switching the capacitive load of its output,  $\alpha$  is the probability of a signal transition within a clock period,  $C_L$  is the switched capacitance,  $V_{dd}$  is the power supply voltage and  $f$  is the clock frequency. From this expression it can be seen that lowering the power supply voltage is an efficient

way to reduce the power consumption. One approach called *architecture-driven voltage scaling* [1] is to increase the parallelity of the operations by introducing pipeline registers in the data-paths. In timing-constrained designs the reduced power supply voltage leads to larger logic delays and additional pipeline registers are needed to obtain the specified cycle time. These extra registers constitute a functional overhead that also increases the power consumption. In order to keep the overhead low, efficient flip-flop design is essential when operating at low power supply voltages.

The synthesis-based design methodology is the most widespread one in digital design today. The design description is given in a HDL (Hardware Description Language) such as VHDL and is taken to a gate-level netlist by an automatic logic synthesis tool. The gates in the netlist are then mapped to predefined cells from a standard cell library. Modularity and robustness are the essential issues in this standard cell approach. In order to model the interfaces to the cells in a simple and uniform way, constraints will be set on the design of the predefined cells. For the design of the flip-flops that are to be included in a standard cell library, the following four design criteria must be fulfilled. First, the flip-flops have to be fully static in order to provide robust operation and not impose any restrictions on the lowest allowable clock frequency. Second, the clock signal has to be single-phase. This will facilitate the automated design process supported by CAD-tools for logic synthesis, static timing analysis, and automatic clock tree synthesis. In addition, most HDL-descriptions are written with single-phase clocking in mind. Third, single-ended data inputs are required. Fourth, all the primary inputs of the flip-flop cell must only be connected to gate-terminals of transistors. Source- or drain connections are not well suited for the timing calculations based on RC-models, which are used by the CAD-tools.

The introduction of the true single-phase (TSPC) latch by Yuan et al. [2] in 1987 has been followed by a long series of works presenting new circuit topologies for both static and dynamic latches and flip-flops. The objectives here have been to improve the speed performance or

power consumption. The relative improvements are often demonstrated through comparisons to the circuit techniques that are for the moment best. Larger comparative studies gather a number of different types of flip-flops and the evaluations are made on a common base providing a fair comparison. The study by Ghannoum et al. [3] compares different types of dynamic TSPC-latches and proposes a set of evaluation criteria for latches. An analysis of power consumption in latches and flip-flops is given by Svensson et al. [4]. In the paper [5] by Stojanovic et al. a set of rules for consistent performance estimation and power consumption is proposed for flip-flops and these rules have been applied in a comparative study of different flip-flops.

In the comparative study presented in this paper, we take into account the four design criteria outlined above when designing the flip-flops used in the comparison. With these considerations, which are necessary in standard cell design, the performance and power figures will show different compared to the original designs. The main contribution of this paper is to point out that having a set of flip-flops included in the standard cell library with different power dissipation characteristics may have significant influence on the total power consumption in power-driven synthesis.

The outline of the paper is as follows: The next section describes the circuit-level implementations of the flip-flops that are evaluated. After that, the simulation setup is described. This is followed by results and conclusions.

## 2.FLIP-FLOP DESIGN

As for all standard cells, the flip-flops must be designed in a way that they conform to the modeling techniques used by the CAD-tools in which the cell library is put to use. For digital CMOS circuits, the delay calculation can be greatly simplified by using RC-models without sacrificing significant accuracy. The RC-model assumes an output signal of a gate driven from  $V_{dd}(V_{ss})$  via the on-resistance of a pMOS (nMOS) transistor chain for a low-to-high (high-to-low) signal transition. The gate-load consists of a distributed RC-line, modeling the interconnections, with a discrete capacitance at the end of the interconnection modeling the input impedance of the connected gates. Thanks to the high input resistance of the MOS-transistor gate terminal the load of a logic gate, where the inputs are connected to the gate terminals of the MOS-transistors, is accurately modeled as a discrete capacitance. Logic gates with pass-transistor inputs are not compatible with the delay modeling technique described above. Here the input impedance consists of a RC-network residing inside the logic gate and the input impedance can therefore not be modeled as a discrete

capacitance. A few of the flip-flops evaluated in this paper have pass-transistors on the data inputs. For these, inverters have to be included in the logic gate in order to adapt to the delay modeling technique. Some flip-flops have differential data inputs. Local inversion of the data is also needed to obtain single-ended data inputs. Other single-phase flip-flops may require the inverse of the clock signal that is produced by local inversion of the clock signal.

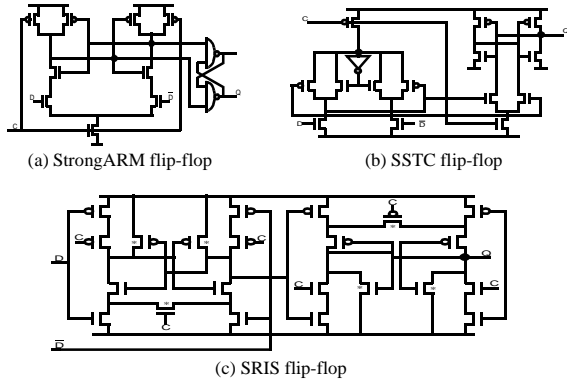
The different adaptations outlined above do all require additional inverters located inside the flip-flop cell. Flip-flops in CMOS are designed in a master-slave configuration. In general, the master-slave stages can be designed either as two identical stages clocked on different phases of the clock signal or designed as an n-stage followed by a p-stage (or arranged in the opposite order). The latter solution often requires differential data inputs and the former solution requires local inversion of the clock signal. Master-slave configurations will have a power-overhead that is dependent on the switching activity on the data signals and for configurations with local inversion of the clock signal the power-overhead is independent of the data.

In this paper, we have selected the most promising flip-flop designs that have been presented in the literature over the years. We have also included the traditional flip-flop design that is often used in standard cell libraries to serve as a reference design. The remaining part of this chapter briefly presents the investigated flip-flop designs.

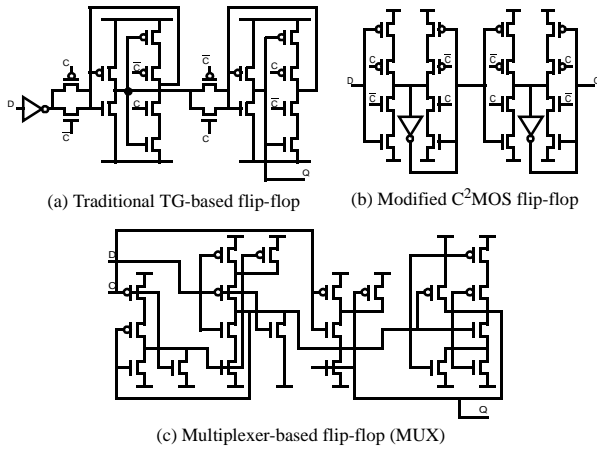
Three flip-flops with differential data inputs are investigated. A self-timed master-slave configuration, shown in Figure 1a, designed for the StrongARM processor [6] is composed of a pre-charged sense-amplifier stage followed by a set/reset stage keeping the previously latched value. The Static Single Transistor Clocked (SSTC) flip-flop [7], shown in Figure 1b, is composed of a p-latch followed by an n-latch. By having only two clocked transistors its local clock power dissipation can be kept low. The Static Ratio-Insensitive Latch (SRIS) [7], shown in Figure 1c, is built from a p- and an n- latch.

Three different types of flip-flops using local inversion of the clock signal are investigated. The traditional flip-flop based on transmission-gates (and sometimes referred to as the PowerPC master-slave flip-flop) [8] is constructed from two identical latch stages that are clocked on different clock phases, see Figure 2a. The modified C<sup>2</sup>MOS flip-flop, shown in Figure 2b, is quite similar to the previous flip-flop and the main difference is that the input transmission-gates of each of the latches are designed as C<sup>2</sup>MOS structures [9]. An entirely combinational solution based on multiplexers [10], shown in Figure 2c, is a single-phase and single-ended data flip-flop constructed of two multiplexers with opposite inversion of

one of the inputs.



**Fig. 1:** Differential data flip-flops



**Fig. 2:** Two-phase clocked flip-flop

### 3. PERFORMANCE CHARACTERIZATION

Setting up the experiment for a fair comparison of different design styles involves many considerations. Besides a common technology, transistor sizing, input transition times, loading conditions, and data input sequences are important parameters that must be controlled in a simulation setup. In comparative studies like the ones presented in this paper, it is possible to control all these parameters. It is, however, necessary to limit the number of parameters that shall be altered. In this chapter, we define the simulation conditions and motivate the limitations made.

The objective is to characterize the speed and power performance down to low power supply voltages. All flip-flops are characterized from 3.0V down to the lowest pos-

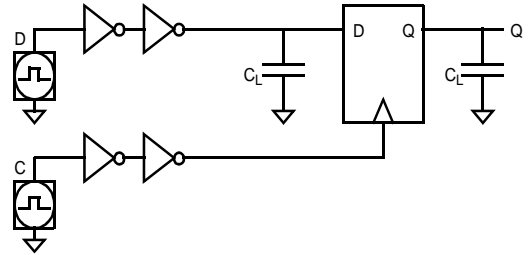
sible voltage. The measurement for the speed of the flip-flop is minimum D-Q delay [5], which is the minimum delay from input D to output Q. D-Q delay is defined as:

$$t_{DQ} = t_{setup} + t_{CQ} = \frac{t_{CQ,HL} + t_{setup,HL} + t_{CQ,LH} + t_{setup,LH}}{2}$$

where  $t_{CQ,HL}$  ( $t_{CQ,LH}$ ) is high-to-low (low-to-high) clock-to-output propagation delay and  $t_{setup,HL}$  ( $t_{setup,LH}$ ) is high-to-low (low-to-high) setup time.

The sources of power dissipation associated with a flip-flop are the following. The *internal power dissipation* is the power dissipated in the transistors inside the flip-flop excluding the power for switching the external load. The *local clock power dissipation* is the external power dissipation in the clock buffer that is needed for clocking the flip-flop. The *local data power dissipation* is the power dissipation in the driving gate of the data input of the flip-flop.

The simulation test bench is depicted in Figure 3. Input signals to the flip-flop are driven by inverters that are driven by ideal voltage sources. In this way, realistic transition times on the input signals of the flip-flop are generated. The output is loaded with a capacitance value corresponding to the input capacitance of two minimum sized inverters ( $C_L$ ). In order to take into account the transition time degradation from the fanout, the data inputs signal is also loaded with  $C_L$ . The power consumption for switching the external capacitors is excluded from the power figures presented in the next chapter.



**Fig. 3:** The simulation test bench

The dynamic power consumption is data-pattern dependent and is directly proportional to the switching activity  $\alpha$ . The flip-flop has two inputs that cause the switching capacitance to charge and discharge. The switching capacitance that is related to the switching of the clock signal is independent of the switching of the data signal. This fact motivates the study of the three separate sources of power dissipation described above. Additionally, it is of interest to study the power dissipation for different types of input data patterns. In this work, we use the standard patterns defined in [5]. The maximum power dissipation is reflected by applying the pattern ...01010

...( $\alpha = 1$ ). The average power dissipation is achieved by applying a pseudo-random sequence ( $\alpha = 0.5$ ). Minimum power dissipation is reflected by using either the sequence ...11111...( $\alpha = 0(1)$ ) or ...00000... ( $\alpha = 0(0)$ ).

The speed and power performance is of course dependent on the way the transistor sizing has been made. The designs may be optimized for speed, low-power operation, or a trade-off between these. In this work each CMOS-stage is designed to give approximately symmetric switching characteristics. The technology is a  $0.6\mu\text{m}$  CMOS with threshold voltage of  $V_{tn0}=0.8\text{V}$  and  $V_{tp0}=-0.95\text{V}$ .

## 4.RESULTS

In this section the results of our comparative study of the six types of flip-flops are presented.

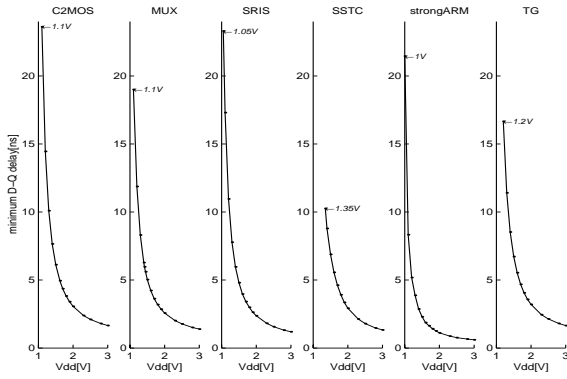


Fig. 4: Minimum D-Q delay under voltage scaling

Figure 4 presents the minimum D-Q delay of each flip-flop for different power supply voltages. The voltages marked out with an arrow are the lowest possible power supply voltages of the flip-flops. As we can see, the minimum D-Q delay for all flip-flops decreases as the power supply voltage increases. The results reasonably follow the equation:

$$T_d \sim \frac{C_L V_{dd}}{\mu C_{ox} (W/L) (V_{dd} - V_t)^2}$$

where  $T_d$  is the delay of the flip-flop,  $\mu$  is the electron mobility,  $C_{ox}$  is the gate capacitance per unit area, and  $V_t$  is the threshold voltage.

We can see that StrongARM can work correctly for power supply voltages down to 1.0V and SRIS works down to 1.05V, yet SSTC is not able to function below 1.35V. All the other ones have the lowest possible power supply of 1.1V. We also see that for the delay, StrongARM

has the best performance of all flip-flops over all voltages.

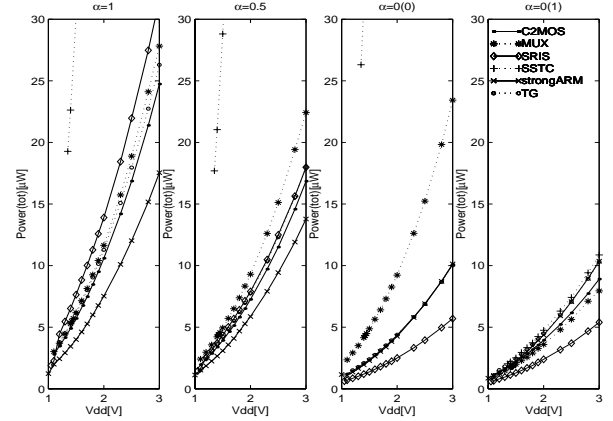


Fig. 5: Power consumption for different  $\alpha$

Figure 5 shows the dynamic power dissipated by each flip-flop when we scale the power supply voltage. The figure is divided into four sub-plots for the different switching activities. Please notice that here we only show the power in the range from  $0\mu\text{W}$  to  $30\mu\text{W}$ . Thus some of the data of SSTC are cut off. The figure clearly shows the quadratic relationship between the power supply voltage and the power dissipation.

We can see here that different flip-flops do not follow the same order in power consumption when the switching activity is different. Especially when  $\alpha = 1$ , SRIS consumes more power than all the other flip-flops (excluding SSTC). When  $\alpha = 0$ , SRIS becomes the one which consumes the least power. Moreover, when  $\alpha = 1$  and  $\alpha = 0.5$ , StrongARM consumes the least power, but when  $\alpha = 0$ , StrongARM no longer performs that well as when the switching activity is higher. However, the power consumption of StrongARM is not as sensitive to the switching activity as the other flip-flops.

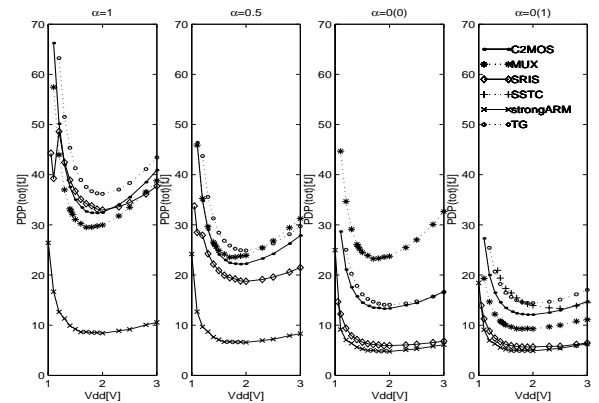


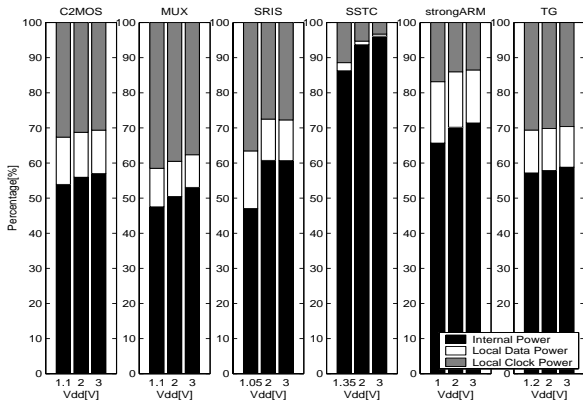
Fig. 6: PDP for different  $\alpha$

Figure 6 shows the power-delay product (PDP) of flip-flops when we scale the power supply voltage. The figure is divided into four sub-plots for different switching activities. The trend of the PDP, while the power supply voltages are scaled, reasonably follows the relationship:

$$PDP(V_{dd}) = T_d \times Power$$

$$\sim \frac{C_L V_{dd}}{\mu C_{ox}(W/L)(V_{dd} - V_t)^2} \times \frac{1}{2} \alpha C_L V_{dd}^2 \sim \frac{V_{dd}^3}{(V_{dd} - V_t)^2}$$

It can be seen from Figure 6 that StrongARM is quite insensitive in PDP for different switching activity, and the PDP is lower in comparison to all the other flip-flops. We can also see that the performance of SRIS, when the switching activity drops to zero, is nearly as good as that of StrongARM. From the previous discussion and results shown in Figure 5, we can see that it will be beneficial to use SRIS instead of StrongARM in non-time-critical paths when the switching activity is low.



**Fig. 7:** Contribution of different sources of power dissipation

Figure 7 shows where the power is dissipated in percentage. Here we notice that StrongARM is the one whose local clock power dissipation takes a smaller portion than the other ones. This means the power dissipated in the clock buffers is rather small, which makes StrongARM the most efficient one.

## 5. CONCLUSIONS AND DISCUSSIONS

From the results we have presented, it is clear that there is a large difference in performance of the flip-flops. Thus it is highly motivated to include cells based on different design styles so that the synthesis tools can make power optimization by choosing the appropriate flip-flop from the library. Here, we summarize our comparative study of the flip-flop as follows:

1. The power supply voltage can be scaled down to

approximately 1.5V without much sacrifice in delay.

2. StrongARM is the flip-flop with smallest delay and works at the lowest  $V_{dd}$  in comparison to other flip-flops. SRIS is the second best one.

3. The flip-flop with the best overall performance is the StrongARM. It has the lowest power consumption for all switching activities and the lowest for medium to high switching activities. It has the lowest PDP for all switching activities which indicates that it is suitable to be used in time critical paths. StrongARM is insensitive to differences in switching activities.

4. For low switching activities, SRIS consumes nearly half the power compared to StrongARM. For high switching activities, SRIS consumes nearly double the power compared to StrongARM.

The final conclusion of our comparative study is that flip-flops included in the cell library should be based on both StrongARM and SRIS structures.

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