A Static Single-Phase Clock D-Latch for UV-Programmable Floating-Gate MOSFET Circuits

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Abstract - **In this work we present a static single-phase clock D-latch in floating-gate technique. The D-latch contains only six transistors, which makes it the most efficient one reported in literature. It is designed to operate in the subthreshold region. Its performance has been characterized by SPICE simulations for a 0.6 μm CMOS process and a power-supply voltage of 800 mV. Its maximum clocking frequency is 45 MHz and the power-delay product (PDP) is 28 fJ, which is at least two orders of magnitude lower than its counterparts operating in strong inversion.**

1. INTRODUCTION

For applications such as wearable computers, distributed sensor nodes, RFID (Radio Frequency IDentification) transponders, and implantable electronic devices, ultra-low power consumption is paramount and speed is less important. At the cost of speed performance, new levels of power reductions can be achieved by operating the digital circuits in the subthreshold region [1]. Their power-delay product is reduced up to two orders of magnitude and the maximum speed is three to four orders of magnitude lower compared to circuits operating in strong inversion [2].

Shifting the threshold voltage (v_T) of the MOS-transistors is an efficient method to decrease the large degradation in speed when operating at low voltages. It is desirable to be able to use standard CMOS processes, which makes it necessary to use post-fabrication techniques for the threshold-shifting. By using floating-gate transistors, the threshold voltage can be shifted by controlling the charge deposited on a floating gate. Logic gates using floating-gate transistors are well suited to be implemented as linear threshold elements (*LTE*) [3]. The circuit topology of these elements provides a simple programming mechanism [7] and results in efficient circuits for logic gates, especially for those with a large number of inputs [4].

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In the work presented in this paper we target UV-programmable floating-gate (FGUVMOS) transistors. By using this technique, the deposition of charge on the floating gate (also called *programming of the transistor*) can be accurately controlled. In addition, recent development in logic gate design makes the FGUVMOS promising to be used in complex digital integrated circuit designs [5].

For automated digital ASIC (Application-Specific Integrated Circuit) design, the design primitives are standard-cells. Here, the modularity and robustness of these cells are essential issues. For latches this means that they have to be static in order to not impose any restrictions on the lowest allowable clock frequency. A single-phase clocking scheme eliminates the problems with clock skew between multiple phases. In addition, by avoiding local inversion of the clock, unnecessary power dissipation can be avoided. In this paper we present an efficient FGUVMOS implementation of a static single-phase D-latch built with only six transistors. The previously reported static latch in FGUVMOS contains ten transistors [6].

The rest of the paper is organized as follows: Section 2 gives first a brief introduction to the FGUVMOS technology and then the circuit design of the proposed D-latch is described. Section 3 presents the simulation results of speed and power consumption of the latch. Finally conclusions are given in section 4.

2. FGUVMOS D-LATCH CIRCUIT

2.1. FGUVMOS transistors

The floating-gate transistors are implemented in a standard digital CMOS technology. Because each input signal is coupled through a designed capacitance, a double-poly process is preferred for efficient realization of the capacitors.

As the symbols for the n- and p-type FGUVMOS transistors shown in Figure 1a) and c) indicate, the FGUVMOS transistors are composed of two devices: a MOS-transistor and a capacitor. The input signal is applied at the *control gate* (V_{CG}). The MOS-transistor gate terminal voltage (V_{FG}) is during programming set to an offset value. By offsetting the floating gate, the control gate is experiencing a shift in the threshold voltage. The programmed value is stored on the floating-gate thanks to

there is virtually no leakage from the floating-gate. During normal operation, the transistors are electrically symmetric with respect to source and drain terminals.

In order to deposit charge on the floating gate, a UV-activated conductance will provide a path from the drain of the transistor to the floating gate. The UV-activated conductances, denoted G_{UV}, are shown for pMOS and nMOS transistors in Figure 1b) and d) respectively. A UV-activated conductance is implemented by an opening in the passivation in a region partially covering the drain and the gate of the transistor. The UV-hole is indicated as a circle in the symbol of the FGUVMOS-transistor. Programming is done by applying the programming voltages (V_+ and V_- in Figure 3b) on the drain-terminals during UV-exposure. For more details on the design and programming of FGUVMOS-transistors please refer to the work by Berg et al. [7,8].

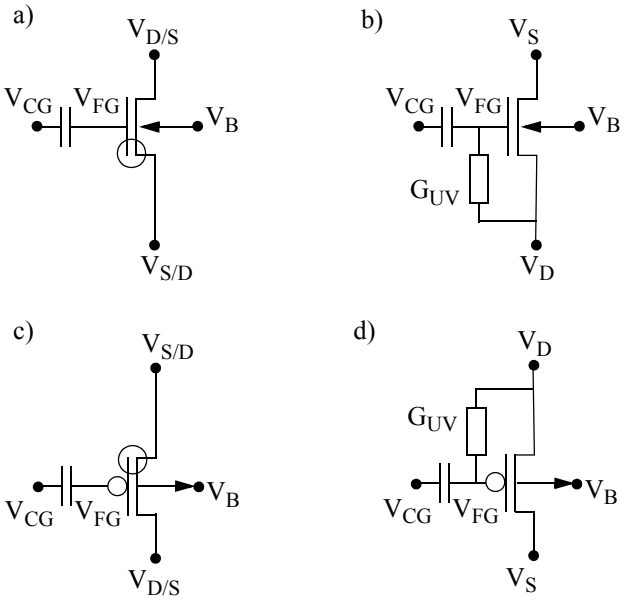

Fig. 1: FGUVMOS transistors, a) and b) nMOS, c) and d) pMOS

For ultra-low power operation the FGUVMOS transistors will operate in the subthreshold region. For the CMOS technology we target, it means that the power supply voltage is equal or less than approximately 800 mV. In the subthreshold region, the drain-source current (I_{DS}) can be approximated as:

$$I_{DS} = I_0 e^{\frac{V_{FG}-V_S}{nU_T}} \cdot \left(1 - e^{-\frac{V_{DS}}{U_T}}\right) \cdot (1 + \lambda V_{DS}) \quad (1)$$

Where I_0 is the zero-bias current, U_T is the thermal voltage, λ is the parameter for channel-length modulation, and n is the subthreshold current parameter.

If transient effects are neglected, the instantaneous voltage on the floating-gate (V_{FG}) is:

$$V_{FG}(t) = V_{FG0} + w \cdot (V_{CG}(t) - V_{CG0}) \quad (2)$$

Where V_{FG0} is the initial value of the floating-gate, V_{CG0} is the initial value of the control-gate, and w is the capacitive coupling factor for the control-gate signal.

The capacitive coupling factor can be described as:

$$w = \frac{C_I}{C_G + C_I}$$

The capacitive coupling is illustrated in Figure 2. The value of the input capacitor (C_I) is determined by the designer. The gate capacitance (C_G) is the capacitance from the floating-gate to the source. C_G comprises also all the different parasitic capacitances associated to the gate-terminal of the MOS-transistor.

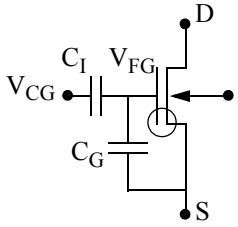

Fig. 2: Capacitive coupling of the signal to the floating-gate

The factor w is a parameter that can be controlled by the designer in order to determine to what extent the input signal shall affect I_{DS}.

2.2. Circuit Design of Gates in FGUVMOS

In general, Boolean functions are implemented by a complementary pair of multiple-input FGUVMOS-transistors as depicted in Figure 3a. Each input signal is coupled by the weight w and the weighted input voltages are summed at the floating-gate node. For the functional analysis we can assume that the transistors are in saturation mode. Furthermore, the normal way to operate the gate is around an equilibrium condition where the output voltage $V_{OUT} = V_{DD}/2$ when all input voltages are set equal to $V_{DD}/2$. A set of pairs of initial floating-gate voltages (V_{FG0n}, V_{FG0p}) fulfils this condition and each of them will result in different transistor currents I_{BEC}. The equilibrium currents for the pMOS and nMOS can be written as:

$$I_{BECn} = I_0 e^{\frac{V_{FG0n}}{nU_T}}; \qquad I_{BECp} = I_0 e^{\frac{V_{DD}-V_{FG0p}}{nU_T}} \quad (3)$$

Where $I_{BECn} = I_{BECp} = I_{BEC}$ for the equilibrium condition. From (3) it is evident how the transistor currents can be adjusted by selecting the programming voltages.

For a multiple-input gate we can write the transistor

currents as:

$$I_{DSn} = I_{BEC} \cdot e^{\frac{1}{nU_T}\sum_{i \in N} w_i \cdot \left(V_i - \frac{V_{DD}}{2}\right)} \quad (4)$$

$$I_{DSp} = I_{BEC} \cdot e^{\frac{1}{nU_T}\sum_{j \in P} w_j \cdot \left(\frac{V_{DD}}{2} - V_j\right)} \quad (5)$$

By having binary input signals, we can assume that $V \in \{0, V_{DD}\}$. Let us use binary values $b \in \{0, 1\}$ to represent the input values such that $V = b \cdot V_{DD}$. The weights to the nMOS and pMOS are denoted W_n and W_p respectively. Where $W_n = \{w_i, i \in N\}$, $W_p = \{w_j, j \in P\}$, and N and P are the sets of inputs to the nMOS and pMOS transistor respectively. Let us denote the exponents in (4) and (5) as $k \cdot e_n$ and $k \cdot e_p$ respectively. Where $k = V_{DD}/(nU_T)$ and

$$e_n = \sum_{i \in N} w_i \cdot \left(b_i - \frac{1}{2}\right), \quad (6)$$

$$e_p = \sum_{j \in P} w_j \cdot \left(\frac{1}{2} - b_j\right) \quad (7)$$

The exponents e_n and e_p are used to describe the function of the FGUVMOS circuit as a linear threshold function:

$$out = \begin{cases} 1 \text{ if } & e_p > e_n \\ 0 \text{ if } & e_p < e_n \\ - \text{ if } & e_p = e_n \end{cases} \quad (8)$$

The threshold function given in (8) together with the equations for the weighted sums, given in (6) and (7), are used for determining the weights for the input signals in order to get the desired logic function for the LTE.

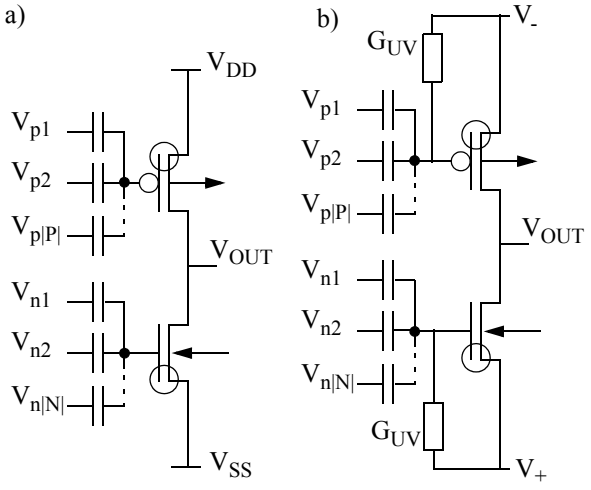

Fig. 3: FGUVMOS LTE; a) in operational mode, b) in programming mode

2.3. Static D-latch in FGUVMOS

Dependent on the value of the clock signal (*C*), a D-latch can be in one of two operational states; transparent or opaque. In the transparent state the output signal (*Q*) follows the input signal (*D*). In the opaque state the output is kept constant. There are basically two ways to implement a D-latch in CMOS. The first type is based on transmission-gates and will therefore not be possible to implement using linear threshold elements. The second type is based on combinational feedback. A commonly used solution is to use a 2-1 multiplexer with feedback [9]. However, a 2-1 multiplexer cannot be directly implemented by one single LTE stage. Since a single LTE stage is not based on primitive logic operations, arbitrary sum-of-products cannot be implemented. Therefore two LTE stages are required.

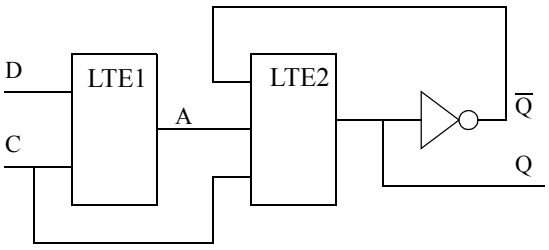

Fig. 4: Overview for the D-latch structure

The first stage (LTE 1) is designed to enable a write of a '1' in the latch. Its function and the weights, required for the function, is given in Figure 5.

z	*C*	*D*	e_p(7)	e_n (6)	*A*
0	0	0	0.5	-0.5	1
0	0	1	0.5	0.056	1
0	1	0	0.0385	-0.0556	1
0	1	1	0.0385	0.5	0

$P = \{z, C\}$ $N = \{C, D\}$
$W_p = \{w_z, w_{Cp}\} = \{(7/13), (6/13)\}$
$W_n = \{w_{Cn}, w_{Dn}\} = \{(4/9), (5/9)\}$

Fig. 5: Design of LTE 1

The second stage (LTE 2) is included in the feedback loop. Its function is to decide whether the input value should be passed on to the output (Q) or the output should remain the same. The logic function and the weights are given in Figure 6. The inverter in the feedback is also based on a LTE. The input *z* is an constant-zero input that is used to weaken the other inputs of the same transistor by increasing the total floating-gate capacitance. The weights give relations between the values of the different

coupling capacitors and the capacitance values are selected based on the CMOS technology used and the design constraints. For the simulation results presented in this paper we have used a 0.6 μm CMOS process with double poly. The capacitance values are set to be approximately five to ten times larger than the gate-capacitance of the MOS-transistors that are approximately 3 fF. The designed capacitances are then in the range from 15 fF to 35 fF.

z	A	C	$\overline{Q}$	e_p (7)	e_n (6)	Q^+
0	0	0	0	-	-	-
0	0	0	1	-	-	-
0	0	1	0	0.5	-0.083	1
0	0	1	1	0.5	0.167	1
0	1	0	0	0	-0.167	1
0	1	0	1	0	0.083	0
0	1	1	0	0	0.250	0
0	1	1	1	0	0.5	0

$P = \{z,A\}$, $N = \{A, C, \overline{Q}\}$
$W_p = \{w_z, w_{Ap}\} = \{(1/2),(1/2)\}$
$W_n = \{w_{An}, w_{Cn}, w_{\overline{Q}}\} = \{(4/12), (5/12),(3/12)\}$

Fig. 6: Design of LTE 2

3. RESULTS

The performance of the D-latch has been obtained through circuit simulations in SPICE. Parasitic capacitances included have been extracted from layout. The maximum speed at a power supply voltage of 800 mV is 45 MHz. The average power consumption expressed as Power-Delay Product (PDP) is 28 fJ and the Energy-Delay Product (EDP) is $1.7 \cdot 10^{-22}$ Js.

The transient simulation in Figure 7 shows the output (Q) with full swing from V_{SS} to V_{DD}.

Q

D

C

Fig. 7: Simulation of D-latch

4. CONCLUSIONS

Research over one decade has shown that the FGUV-MOS technology is useful for both analog and digital circuits operating in the subthreshold region. The work has mainly been focused on bringing forward new efficient circuit topologies and to develop the FGUVMOS technology. The overall objective of our work is to develop basic building blocks that are robust and can be UV-programmed in a simple way. The latch, proposed in this paper, fulfils these requirements. The same structure can be used for latches with opposite polarity and in a pair they can be used in a single-phase Master-Slave Flip-Flop.

5. REFERENCES

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