

Behavioral Simulation of Power Line Noise Coupling in Mixed-Signal Systems using SystemC

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Abstract

This paper presents methods for early quantification of digital to analog noise coupling at behavioral level. The methods enable designers to both verify the behavior of their mixed-signal architecture and its sensitivity to noise coupling. The high-level noise coupling simulation models are implemented as extensions to SystemC.

1. Introduction

The integration level of electronic systems is constantly increasing, both on chip and package levels. When a complete system is integrated on a single chip or package, it will usually compromise both analog and digital functional blocks. In the integration of digital and analog circuits, potential noise coupling from the digital logic to sensitive analog nodes needs to be carefully considered. Noise generated by digital circuits is coupled over the power distribution network and through the substrate of the package or chip [1]. Quantification of the noise coupling and the degradation this causes to system performance needs to be assessed very early in the design cycle in order to avoid costly and time consuming re-design at a later stage. Accurate predictions of the noise coupling effects normally need very low-level simulations to be carried out [2][3]. Circuit level simulation however implies very long simulation times, something which quickly becomes a problem with increasing circuit and system complexity. None of the existing approaches allows the quantification of noise coupling at an architectural level [4], in a top-down design flow. The methods presented in this paper enable a designer to quantify the noise coupling effects at the early stage of architectural explorations. The noise source models for the different circuit blocks of the system can be modeled to be data dependent, hence the noise

coupling simulation will be very similar to the real system. By enabling fast evaluation of different architectures, the system designer can find analog and digital architectures with low sensitivity to interference and generating only low levels of harmful interference, respectively. Early quantification of the digital to analog noise coupling can also give valuable information to the floor planning of the chip.

The methods for quantifying and verifying noise coupling that are described here are implemented as extensions to SystemC [5], which is a worldwide initiative to develop a system design language that is able to model hardware (both analog and digital), abstract communication and software constructs. SystemC modeling language is captured in C++ classes, which makes it an excellent platform for research since there is no overhead associated with building extension to the modeling and simulation methods in SystemC, as would be the case for a compiled approach. Since SystemC supports incremental design refinement, the model can be used on different abstraction levels, preventing long design flow iterations.

We have organized the paper as follows. Section 2 present the modeling and simulation extensions for high-level noise coupling simulation and comparison of the simulation accuracy. Finally, in Section 3, we conclude the paper.

2. High-level simulation of noise coupling

SystemC version 4.0 will support modeling and simulation of mixed-signal systems. The work to achieve this has started in both academia [6] and by the SystemC consortium [5]. The idea behind the simulation methods proposed in this paper is to extend the behavioral mixed-signal modeling and simulation methods to also include the simulation of noise coupling between analog and digital blocks, as shown in Figure 1. The simulation of the noise coupling is based on abstract models of power supply

current for both analog and digital blocks together with a model of the power distribution network. Future extensions to the proposed method will also include models for substrate coupling and will not be discussed further in this paper.

In a top-down design flow supporting modeling and simulation of noise coupling, the mixed-signal behavioral models of the blocks in the system are initially developed and simulated. When these models have been developed and verified, the models for simulation of the noise coupling can be added to the simulation. The functional simulation will work exactly as in the previous case, the difference being that the simulation models for the power consumption are added to each block in the system, (i_1 - i_4) in Figure 1. The behavior of each current source can be individually modeled, e.g. it could be recorded from a SPICE simulation, it could include data dependency, or it could be a statistical model. Each current source is connected to the model of the power distribution network in the extended test bench, which is used for simulation of the noise coupling as shown in Figure 1. The simulation can either be used to analyze the noise at a certain point of the power distribution network or the noise voltage can be fed directly into the analog behavioral model. Thus, the noise coupling effect on the system behavior can be directly simulated.

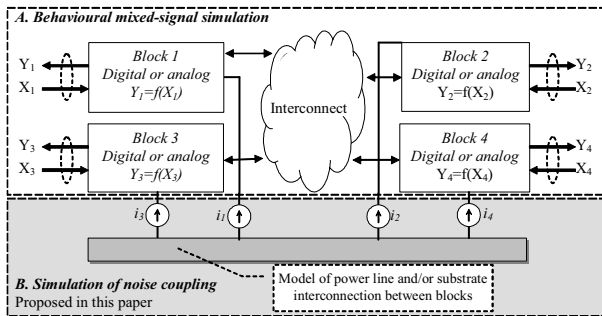


Figure 1. Overview of the noise coupling modeling and simulation extensions.

2.1 Mixed-signal noise coupling wrapper

The model for the power supply current in a functional block is implemented as a wrapper that adds simulation ports that are simulation clock, power supply and ground. In addition, the wrapper adds a current source for the power supply. The wrapper is illustrated in Figure 2.

The actual implementation of the wrapper in SystemC is made as macro definitions that are instantiated in the code of each block. The interface is added by including `NC_SIM_PORTS` in the code of the block, as illustrated by the counter example in Figure 2. The user configures the wrapper by defining the update period, *timestep*, of the simulation clock, *sim-clk*. The triggering condition of the

current source is defined by adding `NC_CURRENT_SOURCE` in the constructor of the block with a standard SystemC sensitivity list, as shown in Figure 2. The behavior of the current source is entered as a SystemC process, which is written as a C++ method.

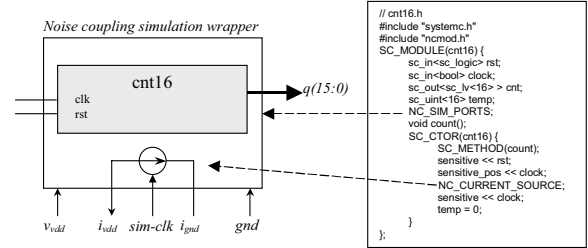


Figure 2. Noise coupling simulation wrapper.

2.2 Modeling the power distribution network

In CMOS, long interconnects can be seen as distributed RC lines and can be accurately modeled by cascaded discrete RC-stages [7] with a certain serial resistance and a capacitance to ground. The electrical model for the wire is given in a) RC-based model for wires and b) the interfaces for the system SystemC model., where i_m represents the power supply current for a functional block as described in Section 2.1 and C_{comp} represents the component capacitance toward the substrate.

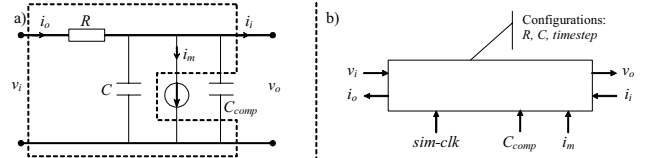


Figure 3. a) RC-based model for wires and b) the interfaces for the system SystemC model.

The time-discrete evaluation of currents and voltages for the RC-stage requires some considerations concerning the relation between the RC-factor of the interconnect and the selected simulation *timestep*. The power distribution model needs to handle three different cases: (1) *timestep* is smaller than the RC-factor $R \cdot C$, (2) *timestep* and the RC-factor are of the same magnitude ($timestep \approx R \cdot C$) and (3) *timestep* is larger than the RC-factor. Case 1 and 3 used the following equations:

$$\begin{aligned}
 \text{Case 1: } & \begin{cases} \Delta v_o = \frac{\Delta(i_m + i_i) \Delta t}{C} \cdot \gamma_1 \\ \Delta i_o = i_n + \frac{\Delta v_o}{R} \end{cases} \\
 \text{Case 3: } & \begin{cases} \Delta v_o = \Delta i_o \cdot R \\ \Delta i_o = \Delta(i_m + i_i) \Delta t \cdot \gamma_2 \end{cases}
 \end{aligned}$$

Where γ_1 and γ_2 are damping factors set to 1.0. Δt is the *timestep* of the simulation. For case 2 same equations are used but the damping factor is set to the function $\gamma_n = f_n(R, C, \Delta t)$, which is similar to the methods presented

by Brambilla et al. [8]. This ensures stable simulation models for all values of *timestep*. By using the same modeling technique, an RCL model of a wire can be built.

In Figure 4 simulation results from these three cases are shown. The simulation setup consists of three cascaded RC-stages. Current pulses on i_m , representing currents in the power supply for the blocks, are injected in stage two and three. The output voltage v_o and output current i_o of each stage are plotted. The component values are set to $\tau_{RC} = 2$ ns for all stages and the simulation time is set to 100 ns. For a *timestep* much smaller than the RC-factor (100 ps), the simulation results are very close to the results from SPICE and these cannot be distinguished from each other in the plot.

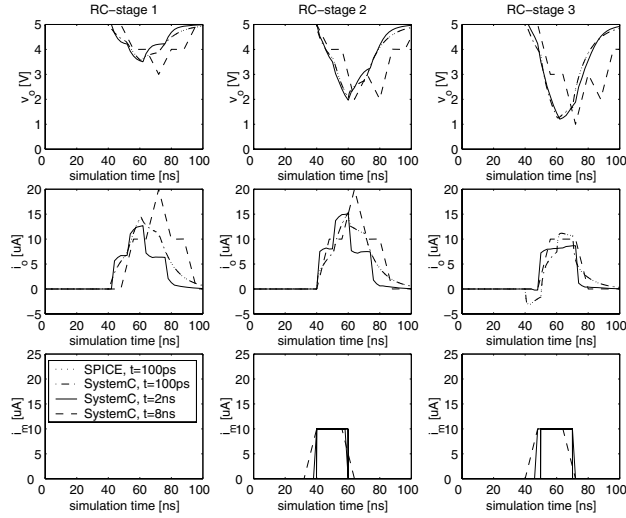


Figure 4. SystemC vs. SPICE simulation results.

For larger timesteps the accuracy will drop and, as can be expected, the error will increase in amplitude and time. For the case of a *timestep* equal to 8 ns (four times the RC-factor) this is clearly shown.

The relative mean error estimates for the three cases are made according to:

$$Rme[\%] = \frac{\sum (|V_{SystemC} - V_{SPICE}| \cdot \Delta t)}{\sum (|V_{SPICE}| \cdot \Delta t)} \cdot 100$$

The results of these error estimations are shown in Table 1. The SPICE simulation that is compared with the SystemC simulation cases has a *timestep* of 100 ps.

Table 1. The relative mean error estimations of v_o for the three cases vs. the SPICE plots.

<i>timestep</i>	RC-stage 1	RC-stage 2	RC-stage 3
100 ps	0.046 %	0.084 %	0.111 %
2 ns	1.807 %	1.945 %	2.523 %
8 ns	3.928 %	5.503 %	11.005 %

The presented model has its limitations. The actual update period in the model is $T_{update} = (2n-1) \cdot timestep$, where n is the number of RC-stages. This causes a problem for large numbers of n , since the *timestep* has to be very short, and this in turn causes long simulation times.

3. Conclusions

We have presented a simulation method for quantification of noise coupling over power distribution networks at behavioral level. The simulation model consists of two parts, a noise coupling wrapper for behavioral blocks and a noise-coupling block for interconnection. The wrapper captures the power consumption behavior of the functional block and can be captured as a data dependent current source (CS), a CS captured from SPICE data or statistical modeled CS. The interconnection block models the power distribution network and its accuracy compared to SPICE is in the range of 99.9% down to 90% depending on the update frequency of the synchronous dataflow. Both the noise-coupling wrapper and the interconnection block are implemented in SystemC as synchronous dataflow and are both compatible with the normal SystemC description style.

4. References

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