A SYSTEMC EXTENSION FOR BEHAVIORAL LEVEL QUANTIFICATION OF NOISE COUPLING IN MIXED-SIGNAL SYSTEMS

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ABSTRACT

We present a method, based on SystemC, for quantification of noise coupling in mixed-signal systems, called BeNoC. Presented method facilitates seamless quantification of both power distribution network and substrate noise coupling at behavioral level. The main contribution of this approach is the integration of noise coupling simulation with behavioral functional simulation. Starting from a behavioral model of the system, captured in SystemC, we add wrappers to each block in the behavioral model. These wrappers add an estimated power consumption model for each block, which is triggered by events in the behavioral simulation. The noise coupling simulation is then done by connecting the different blocks according to a virtual layout and technology parameters. The resulting noisy substrate or noisy power distribution network can then be fed back into the behavioral model. Thus, effects on the system behavior can be analyzed. In this paper we focus on noise coupling over the power distribution network and to demonstrate the usability of the noise coupling simulation technique. The simulation results are compared with circuit simulations in SPICE.

1. INTRODUCTION

The integration level of electronic systems is constantly increasing, both on chip and package levels. When a complete system is integrated on a single chip or package, it will usually compromise both analog and digital functional blocks. In the integration of digital and analog circuits, potential noise coupling from the digital logic circuits to sensitive analog nodes needs to be carefully considered. Noise generated by digital circuits is coupled over the power distribution network and through the substrate of the package or chip [1]. Quantification of the noise coupling and the degradation this causes to system performance needs to be assessed very early in the design cycle in order to avoid costly and time consuming re-design at a later stage. Accurate predictions of the noise coupling effects normally need very low-level simulations to be carried out [2],[3]. Circuit and device level simulation however also implies very long simulation times, something that quickly becomes a problem with increasing circuit and system complexity. None of the existing approaches allows the quantification of noise coupling at an architectural level [4] of a top-down design flow.

There are a variety of macro models for simulating power distribution networks and substrates. In the case of power distribution networks, there are two different models currently dominating in simulation research [5]. The first is the simple RC model shown in Figure 1a, which works for $t_r > 2T_0$, where t_r is the waveform transition time of the clocked signal coupling onto the power distribution network and T_0 is the time of flight [6]. However, when t_r decreases below $2T_0$, this model have to be expanded to include an inductance in series with the RC model. This model is shown in Figure 1b.

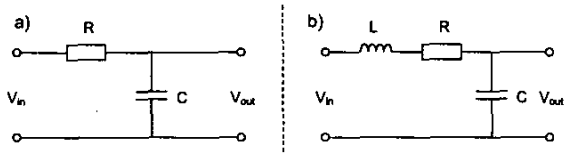

Figure 1. a) RC model for simulating power distribution networks. b) RLC model for use when $t_r < 2T_0$.

In the case of substrate modeling, there is a larger variety of models, ranging from models with high precision to models with short simulation time. The model that seems closest to a device simulation consists of a substrate mesh with cubical mesh blocks which each has parallel capacitances and resistances connected from each side of the block to a center node in the mesh block [7]. A simplified version of this model discards the capacitances and only calculates the remaining resistive network [1]. Another simplification to reduce simulation time is to reduce the mesh partitioning in the (x,y) plane [8]. In the z direction the mesh sizes on the surface of the simulated substrate can also be smaller than the mesh sizes further down [1]. A more abstract model that has gained ground is the concept of a single ground node at the bottom of the substrate and terminal nodes on the surface [9]. Within this concept there is a variety of models used. Closest to the layout level there are models which incorporates capacitances between wells and substrate and between poly and substrate. In addition to these capacitances, a complex resistive network can also be incorporated to increase accuracy in the simulations [10]. A more common and more abstract way of modeling with a single ground node is just to connect a resistance to the ground node from every terminal and resistances between the terminals [11]. Even in these models, simplifications are common, mostly by using variants of Delaunay triangulations to reduce the resistive network and, as a consequence, reduce the simulation time [12]. These models have all been developed for simulation of noise coupling on a layout level, though.

The methods presented in this paper enable a designer to quantify the noise coupling effects and to explore various schemes to combat the self-generated interference during architectural design space exploration. It differentiates itself from

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other approaches, found in the literature, through the integration of the behavioral simulation together with a high-level model of the noise coupling. Hence, the method enables investigation of the dynamic effects of the noise coupling without having to design the circuits. This is achieved by combining a behavioral simulation in SystemC [13] with a high-level noise coupling simulation done off-line in SPICE. The noise coupling part is added to the behavioral SystemC model by applying a wrapper to each behavioral block. The noise coupling is simulated using the behavioral model, with wrappers, together with technology parameters and a virtual layout that connects the substrate and power distribution network between the blocks. By enabling fast evaluation of different architectures, the system designer can find analog and digital architectures with low sensitivity to interference and generating only low levels of harmful interference, respectively. Early quantification of the digital to analog noise coupling can also give valuable information to the floor planning of the chip.

Next section positions the presented method in a top-down design flow. The modeling method is described in section 3. Section 4 demonstrates the simulation method by using the method for design space exploration of a dental photon counting X-ray pixel array. This design example is also used to compare the accuracy of the simulation results with real circuit simulations. Finally, we summarize the paper.

2. DESIGN FLOW

The proposed noise coupling model is a proposed addition to architectural exploration stage of a top-down design flow for mixed-signal systems, as depicted in Figure 2. The noise coupling simulation starts from a behavioral model, which is extended by applying the noise coupling simulation wrapper to the behavioral model. The simulation wrappers add technology parameters, power consumption and power supply interconnect to all functional blocks in the system.

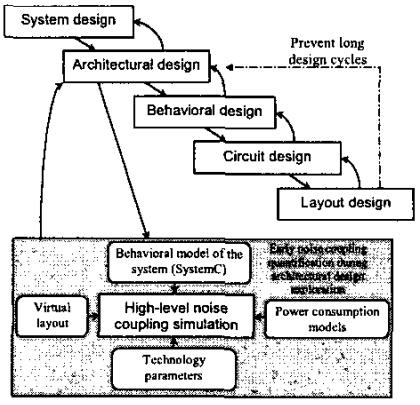

Figure 2. Proposed addition to a top-down based design flow for mixed signal systems.

3. MODELING

The model for the power supply current in a functional block is implemented as a wrapper that adds simulation ports: simulation clock, power supply and ground. The wrapper is illustrated in Figure 3.

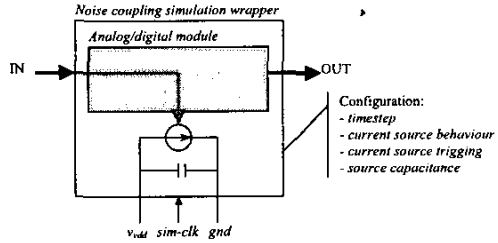

Figure 3. Mixed-signal noise coupling wrapper.

The actual implementation of the wrapper in SystemC is made as macro definitions that are instantiated in the code of each block. The interface is added by including *NC_SIM_PORTS* in the code of the block, as illustrated by the counter example in Figure 4. The user configures the wrapper by defining the update period, *timestep*, of the simulation clock, *sim-clk*. The trigging condition of the current source is defined by adding *NC_CURRENT_SOURCE* in the constructor of the block with a standard SystemC sensitivity list, as shown in Figure 4. The behavior of the current source is entered as a SystemC process, which is written as a C++ method.

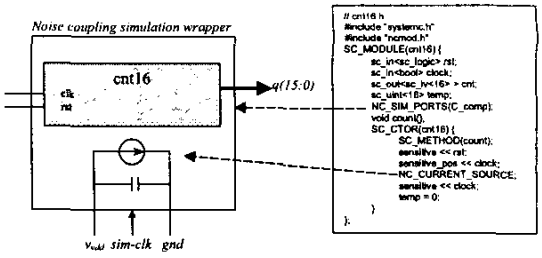

Figure 4. Example of noise coupling simulation wrapper.

The noise coupling wrappers are connected by entering a virtual layout of the system, as shown in Figure 5. In the current version, the virtual layout is entered in the SystemC description. This is simply done by connecting the blocks with the selected wire model, which is completed with technology parameters. From this description a SPICE netlist is generated. This includes the power distribution network and the noise behavior of each block in the system. The noise behavior is recorded during behavioral simulation and included as piece wise linear (PWL) current sources in the generated SPICE netlist. Currently the noise coupling simulation is done off-line. To enable feedback of the noise into the behavioral simulation, the two simulations must be done simultaneously. This integration is left for future work.

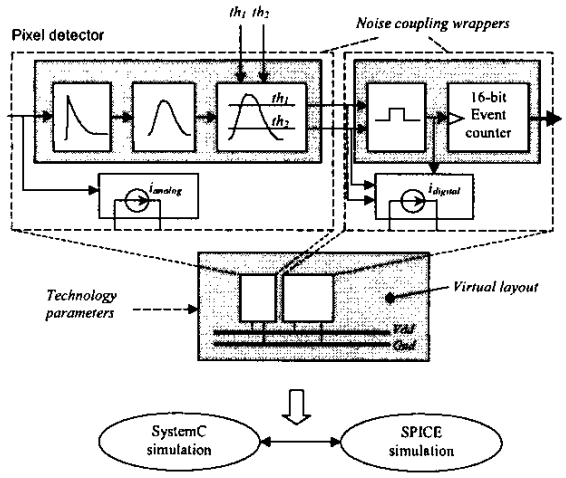

Figure 5. Organization of the behavioral and noise coupling simulation.

4. ARCHITECTURAL EXPLORATION

Sub-micron technology has enabled X-ray imaging with image sensors composed of photon-counting pixels [14]. In these image sensors each pixel is implemented as a single channel radiation detector, which means that each X-ray photon that is detected in the pixel is counted. The architecture of the pixel is depicted in Figure 5. The number of counts will represent the pixel value. An event is processed such that when the photon hits the detector, the photon energy is converted into a charge pulse that is integrated by a pre-amplifier. This is then pulse-shaped, i.e. a band-pass filter is applied on the signal. The height of the filtered signal represents the photon energy. The pulse is counted if the energy is between the two threshold levels in the window discriminator. The window discriminator is implemented with two comparators. This enables X-ray color imaging and gives increased sensitivity. Another advantage with a photon counting image detector is that the image is directly captured in digital form and thus no analog to digital conversion is needed during readout.

Each pixel comprises three to five hundred transistors, which accentuates the problem with tight integration of sensitive analog circuits and digital logic. To quantify the noise coupling effects for the image sensor requires long design and simulation times if carried out at circuit level. We have chosen the photon counting image sensor as a test vehicle to demonstrate the effectiveness of our proposed high-level simulation methods. In the test setup we have used a small fraction of the image sensor where we simulate 16 adjacent pixels (4 × 4 pixels).

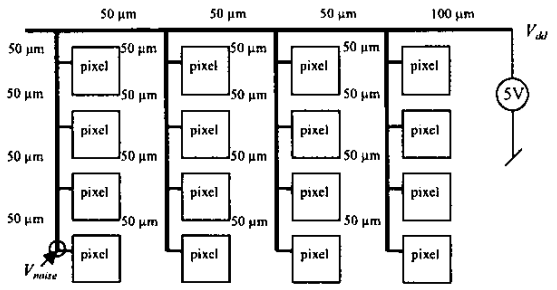

Figure 6. 4x4 array of photon counting pixels used as test vehicle for evaluation of the noise coupling simulation.

The test structure is organized as a 4 x 4 pixel array with a pixel size of 50 µm, as depicted in Figure 6. It is simulated using both the BeNoC model and circuit simulation. The test case is limited to 16 pixels to enable verification with SPICE.

To save area for the active pixel elements in the image sensor, we have evaluated a single power supply. This means that we have the same power supply for both the analog and the digital circuits. We have also selected power distribution network routing, as shown in Figure 6, using a fork structure, which is connected to a power supply with a 100 µm wire. Four cases are evaluated: two different power distribution network widths (1µm, 5µm) for two different digital architectures. The first digital architecture (LFSR) is a synchronous linear feedback shift-register and the second one is a LFSR with an asynchronous pre-scaler [16].

Counter	*Line width*	V_{noise}			*Simulation time [min]*	
		Circuit	*BeNoC*	*diff*	*Circuit* [1]	*BeNoC* [1]
LFSR	1	3.1mV	3.0mV	3%	55.44	0.20+0.06
	5	0.53mV	0.51mV	4%	58.57	0.21+0.06
Prescale	1	0.59mV	0.54mV	9%	56.46	0.19+0.06
	5	0.14mV	0.11mV	17%	56.59	0.20+0.06

Table 1. Evaluation of mixed-signal architectures using the BeNoC and comparing the simulation results with SPICE. Simulation time is measured on an [1]UltraSparc-10 300MHz (BeNoC time is divided into behavioral simulation + SPICE simulation). The test case was simulated for 2 µs.

Each pixel is modeled as a synchronous dataflow in SystemC and connected to a detector. The detector is based on statistical models of the time between two events and the energy level for each event that correspond to a dental application [17]. In the simulations the power distribution network is modeled using an RC wire model. In the circuit simulation only the digital part of the pixel is simulated and it uses the same R and C values as in the BeNoC simulation.

Technology parameters that were used for these simulations:

- Wire capacitance: 0.045 fF/μm^2
- Wire resistance: 150m$\Omega/\square$.

Table 1 shows that the noise coupling simulation is approximately two orders of magnitude faster, for this example, with an acceptable error for the simulation result. Although this is impressive, the main point with this approach is that the simulation can be done long before the circuits have been designed. As for most high-level design methodologies, the quality of the estimations highly affects the accuracy of the noise coupling simulation.

5. SUMMARY

For ongoing research to improve BeNoC, we are developing methods for capturing the virtual layout and simulating the substrate noise coupling. We are also experimenting to use SPICE as a simulation engine for noise coupling part (both the power distribution network and substrate), concurrent to the SystemC behavioral simulation.

In this paper we have shown that the high-level noise coupling simulation methods can be used to quantify different noise coupling parameters in a mixed-signal system. In this paper we have limited the approach to noise coupling over the power distribution network. We have demonstrated the noise coupling methods for a photon-counting X-ray image sensor (4 × 4 pixels) design. The result from this simulation is compared with SPICE simulations of the whole pixel array. The high-level model of the image sensor was captured in SystemC as synchronous dataflow. Separate power models for the digital and analog parts were added to the high-level model of each pixel.

The quantified noise coupling can be used to compare different pixel architectures, to generate constraints for analog designers, give hints on the design of the power distribution network, and the noisy power supply can be fed directly into the behavioral model to simulate its effects on the pixel behavior. In this way, strategies for the power distribution network can be evaluated and the required constraints on the power supply rejection ratio (PSRR) can be tested and verified.

6. ACKNOWLEDGEMENTS

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