Annual Report for the Research Platform on Electronic Devices, Sensors and Systems

2000-07-01 to 2001-06-30

Mitthögskolan

2001-06-30

Content

1. Introduction

This report describes the work within the research platform on electronic Devices, Sensors and Systems, at Mitthögskolan during 2000-07-01 to 2001-06-30. The report presents our research results, our recruitment initiatives and our various information activities. The ambition is to provide interesting information about the project status and show the positive and stimulating environment that the platform support has provided for our research. It is not possible to describe each detail in our research results in this report. The details can be found in the publications submitted. We will also describe the work on building a new cleanroom laboratory for research on semiconductor devices. The new cleanroom will be officially opened at the June 11, 2001 and is of strategic importance for the research within this platform.

2. Research results

The research result will be presented for each work package and for the interdisciplinary panoramic X-ray unit separately.

2.1. Device simulation

The research on device simulation consists of three main activities, Monte Carlo simulation of carrier transport in bulk semiconductors, Monte Carlo simulation of semiconductor devices and macroscopic modeling of semiconductor sensors and devices. These activities are closely related but involve different types of research goals. The study of basic carrier transport in bulk material is of large importance in order to understand the basic properties of a semiconductor material. This knowledge can then be used to study different kind of device structures. The accuracy of the bulk model is determining the accuracy of the device simulation. The bulk Monte Carlo model is also used to extract transport parameters for modeling of large device structures.

2.1.1. Study of carrier transport in bulk semiconductors

The research in this field has mainly been directed towards the carrier transport in SiC polytypes. Silicon Carbide is a semiconductor that recently has attracted a lot of attention due to its high breakdown field and high thermal conductivity. These characteristics make it a very promising material for high field and high temperature applications.

The SiC polytypes are very challenging materials to simulate with the Monte Carlo method. They require that several fundamental and scientifically important questions are addressed that go beyond the standard Monte Carlo procedure considerably. This makes the SiC polytypes especially interesting for modeling purpose and allows us to further develop the Monte Carlo simulation model beyond what is state of the art today.

The knowledge we gain by studying the SiC polytypes will also be used to address more conventional semiconductors like GaAs and silicon.

2.1.1.1. Study of electron transport in bulk 3C-SiC

3C-SiC is a cubic SiC polytype that can be grown on silicon substrates. There are a considerably interest in developing high frequency MESFET devices in 3C-SiC. There

are predictions of Thertz operation in 3C-SiC in the literature. However, in order to fully understand the potential of 3C-SiC as a semiconductor the charge transport properties has to be studied carefully. During the fall 2001 we have implemented 3C-SiC into our Monte Carlo simulator. The new model is based on first principles where the ab initio wave functions have been used to calculate scattering rates and impact ionization transition rates. The only empirical data used are two coupling constants for the acoustic and the non-polar optical phonon scattering. The model provides good agreement between simulations and experiments as can be seen in fig. 2.1.1 where the mobility as a function of temperature is presented. In fig. 2.1.2 the velocity versus electric field is presented which shows that 3C-SiC has a saturation velocity close to 2 x 10^7 cm/s.

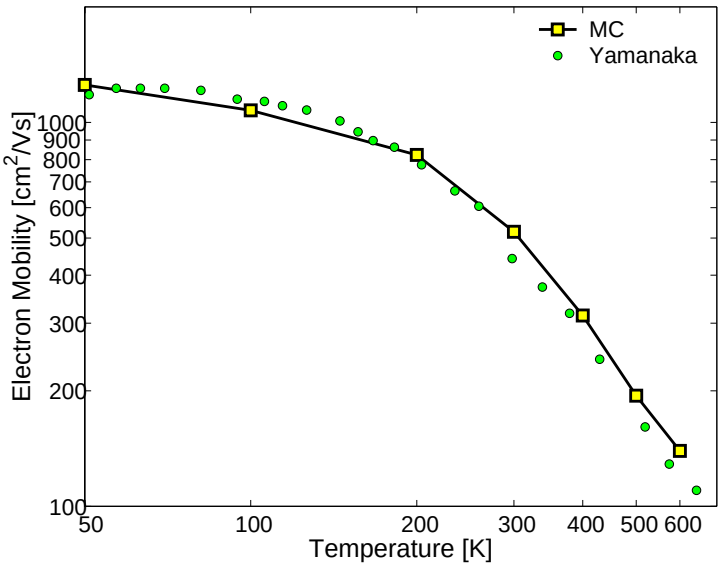

Fig. 2.1.1. Comparison between simulated and measured electron mobility in 3C-SiC.

In fig 2.1.3 the electron initiated impact ionization coefficients are presented together with experimental results for silicon. The results for 3C-SiC holes have also been included. Our simulation results show that electrons dominate the impact ionization process in 3C-SiC. This is the opposite behaviour compared to 4H-SiC and 6H-SiC which is a very important results since it is usually assumed that the holes dominates the impact ionization in all SiC polytypes.

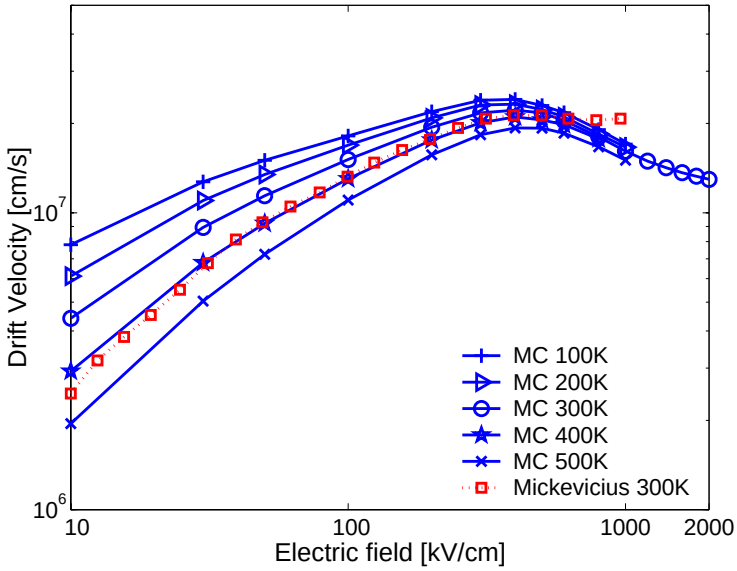

Fig. 2.1.2. Drift velocity as a function of electric field in 3C-SiC.

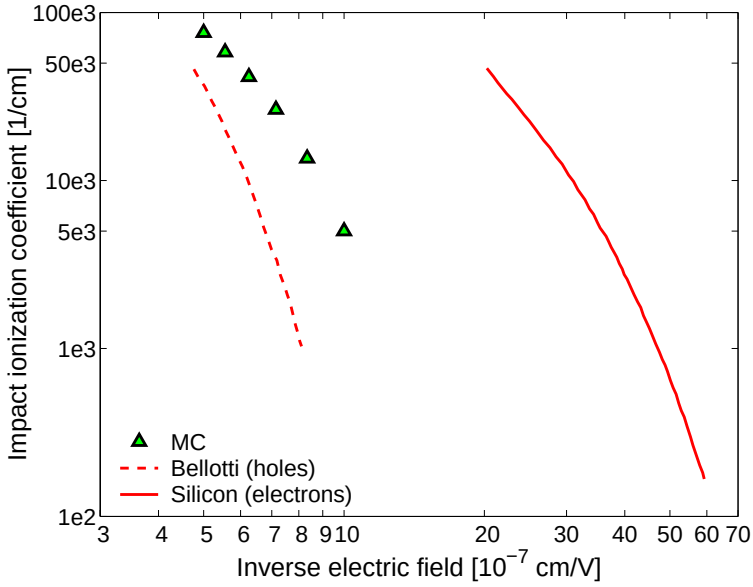

Fig. 2.1.3. Comparison of the electron initiated impact ionization coefficients for 3C-SiC electrons (holes) and silicon electrons.

2.1.1.2. Study of high field hole transport in bulk 4H-SiC

The impact ionization in hexagonal SiC polytypes is dominated by hole initiated impact ionization events. There are two different measurements available in the literature of the impact ionization coefficients in 4H-SiC. These two experimental results differ by a

factor of 5. The temperature dependence of the hole initiated impact ionization has been found to be negative.

During 1999 and 2000 we presented the first Monte Carlo results on the high field transport of the 4H-SiC polytype [sim1, sim3]. In this study we found several very interesting hole transport properties which we are currently trying to understand using a completely new modeling approach. Our Monte Carlo results were in good agreement with the latest measurement found in the literature using a so-called EBIC (electron beam injected current) method. This method is considered to be very accurate and avoids problems related to large defect densities. In order to simulate the hole transport in 4H-SiC we developed a new simulation approach. In this approach we went beyond the standard Monte Carlo method and introduced very accurate scattering models. We also included a first approximation to multi-band transport, which turned out to be extremely important in simulation of hole transport in hexagonal SiC polytypes. In our work we showed that multi-band transport (band to band tunneling during drift) really occur and is very important to consider. Neglecting this phenomenon results in very low impact ionization coefficients, far from any experimental observation.

We are currently working on a more accurate band to band tunneling model. The first results from this new model will be presented at the SISPAD´01 in Athen this autumn [sim18]. In fig. 2.1.4 the results from the new model is compared with the experimental data available in the literature. Notice the large difference in impact ionization coefficients with and without the band to band tunneling.

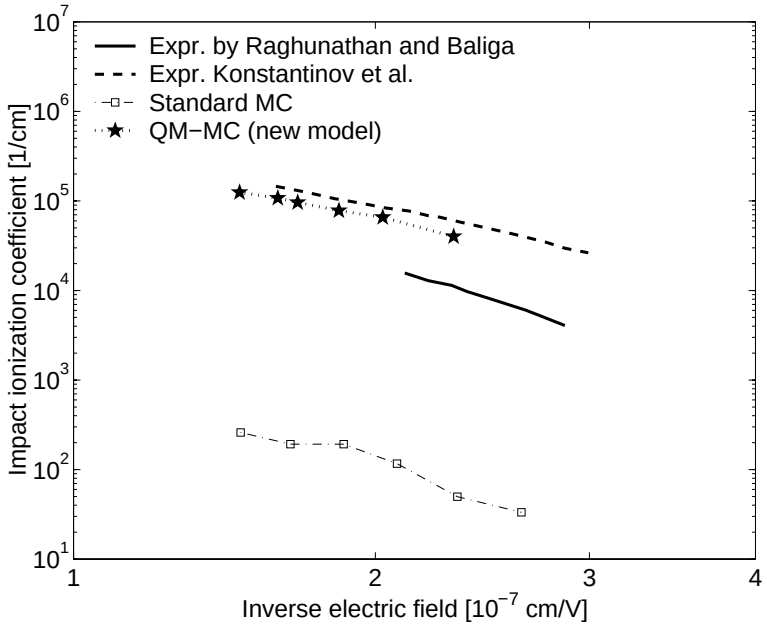

Fig. 2.1.4. Impact ionization coefficients for holes in 4H-SiC as a function of inverse electric field.

2.1.1.3. Implementation of zincblende semiconductor materials in our Monte Carlo framework

One of the long-term research goals that the simulation group has is to develop a completely general Monte Carlo simulator that may be used to simulate arbitrary semiconductor devices and materials. The overall architecture of our simulation program is developed with this goal in mind. The first type of materials that was implemented had hexagonal crystal structure. Our ambition is to incorporate other crystal structures as well. However, this is a long-term project and it will be important to really perform detailed simulations on each material that we address. Two visiting scientists from Politecnico di Torino has been working on the implementation of GaAs in the simulator during the autumn 2000. This work was finished in the beginning of 2001. However, some tuning of the model is still needed in order to provide accurate simulation results.
In addition to the work on GaAs we have implemented a full model for silicon (both electrons and holes). In fig. 2.1.5 to 2.1.7 different transport properties of silicon has been compared to experimental data or results from the IBM MC model Damocles available in the literature. The accuracy of the model is well in parity with the Damocles simulator developed by IBM research at York Town Heights.

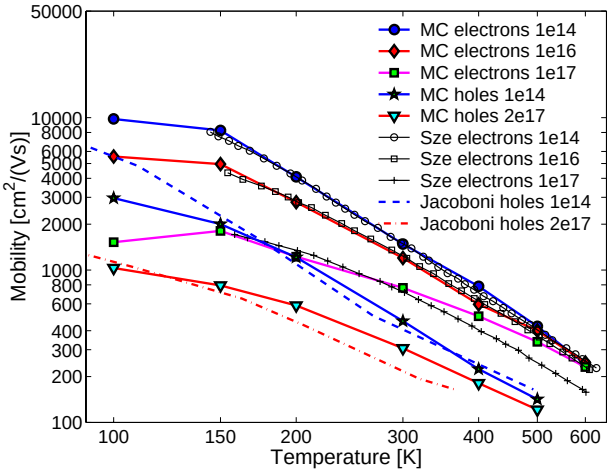

Fig. 2.1.5. Comparison between measured and simulated electron and hole mobilities as a function of temperature.

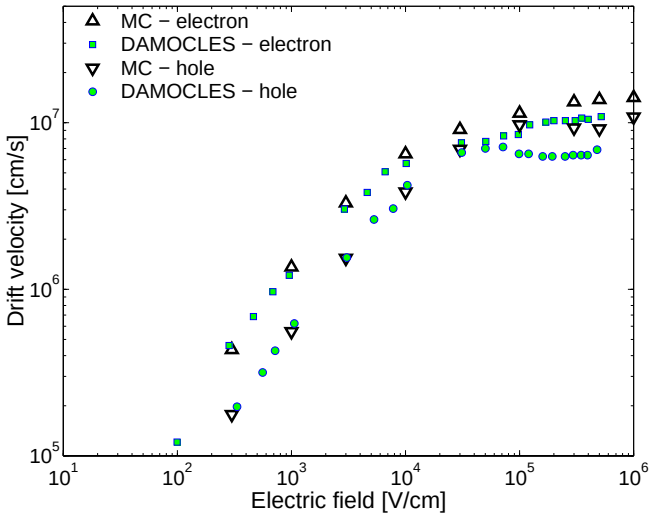

Fig. 2.1.6. Comparison of electron and hole velocity as a function of electric field obtained by our MC model and the IBM model Damocles.

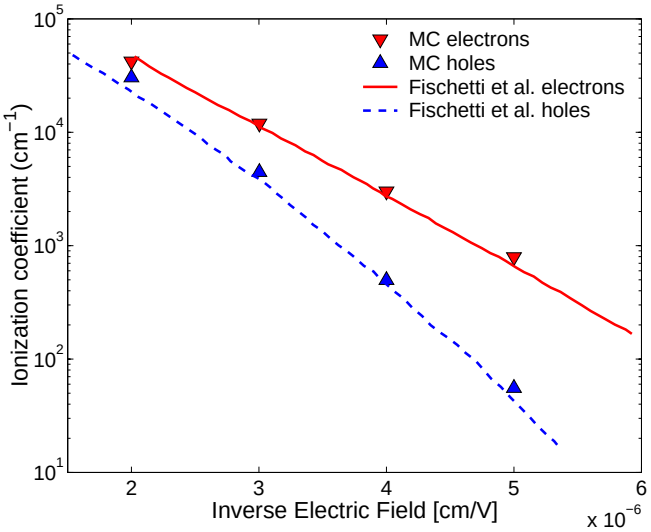

Fig. 2.1.7. Comparison of electron and hole initiated impact ionization coefficients as a function of inverse electric field obtained by our MC model and the IBM model Damocles.

2.1.1.4. New algorithms for selection of final state after scattering

When a carrier (electron or hole) moves in a semiconductor crystal, the movement is interrupted by scattering events, which practically instantaneously change the movement direction. In a Monte Carlo simulation it is necessary to have models for as well the calculation of scattering probability as selection of final state for the carrier after scattering. The final state selection has to consider the dependency of the difference in wave vector between the original and final state, which is varying depending on the type

of scattering mechanism. It also has to consider the overlap between the carrier wave functions for original and final state. We have implemented a new algorithm for the selection of final state, based on the rejection method, which is a general method to obtain an arbitrary distribution of random number. The advantage with the new algorithm is that it results in a reduced number of calculations of the overlap, which is computationally heavy to perform. I.e. it is possible to do a more accurate calculation in shorter time. The improvement is especially important for high-energy simulations. A paper that presents the new algorithm and compares it with older has been submitted to "Simulation - Practice and Theory".

The rejection method has been crucial in the improvement of final state selection for ionized impurity scattering according to Ridley's third body rejection method. This improvement has been necessary in order to get good agreement between experimental values for doping dependence of mobility in silicon and the corresponding values obtained from Monte Carlo simulation.

2.1.1.5. A study of anisotropy of bulk and surface electron transport in 4H and 6H-SiC

The two SiC polytypes 4H and 6H differ largely in anisotropy. The electron mobility in 6H is about five times higher in the plane perpendicular to the crystal axis than in the crystal axis direction. In 4H the electron mobility in the crystal axis direction is about 20 percent higher than in the perpendicular plane. We have made a study of the consequences of this anisotropy for transport, that is neither parallel to the crystal axis nor to the perpendicular plane. The study covers both bulk transport and transport in crystal-semiconductor interfaces.

An interesting result in the case of bulk transport is that in "sloping" transport directions, the actual electron movement has a component perpendicular to the electric field. If a device is arranged with a current in one of these directions, it will result in the build up of at perpendicular potential difference. The effect is similar to the Hall effect, but no magnetic field is required. A new semi-empirical model of the interface is used in the surface transport study. It is necessary due to the step-formed morphology of the surface, which is caused by the departure from the symmetry planes. We present simulated characteristics for mobility and field-velocity relations in the planes that generally are used when cutting the crystal. These characteristics show that 6H-SiC has better transport properties for MOS devices. Our study has been presented at the E-MRS Spring Meeting and will be printed in the conference proceedings.

2.1.2. Modeling of high speed, high power and sensing devices

In this section we will describe our work related to advanced device modeling using state of the art transport models such as full band ensemble Monte Carlo algorithms, hydrodynamic transport equations and drift-diffusion models. Our strategy is to utilize our Monte Carlo model as a reference and to extract transport parameters for different materials and device structures. For well-known semiconductors like silicon and GaAs

we are using established models available in the literature to investigate various device characteristics and to optimize a device design according to certain constraints.

2.1.2.1. Evaluation of different transport models for simulation of SiC MOSFETs

One of the merits of silicon carbide processing technology is that the material can be thermally oxidised to form SiO_2. The quality of the oxide is vital for MOS applications. Due to its higher mobility and lower dopant ionisation energy, the 4H-SiC polytype is the favoured over 6H-SiC. Despite these drawbacks 6H-SiC is preferred for MOSFET applications. Experiments have shown that 4H-SiC has lower channel mobility. The lower mobility is believed to originate from a different position for the interface traps relative conduction band edge. Nevertheless, a wide range of MOS devices has been fabricated in both polytypes.
SiC is a new and highly anisotropic material and therefore very difficult to simulate. The existing carrier transport models need to be investigated and updated to give a correct behaviour of sub-micron devices in SiC. The device simulation program MEDICI contains a module for anisotropic materials. This module in combination with the drift-diffusion (DD) and hydrodynamic (HD) transport model has been used to simulate a deep sub-micron MOSFET in both polytypes. The results were compared with those from MC simulations.
Several SiC material parameters have not been measured. In the case where the parameters are lacking, Monte Carlo simulations of the bulk properties have been used to extract the transport parameters for the DD and HD models.
The results of the simulations are presented in Table 2.1.1. The 4H polytype gives the highest values in transconductance g_m and unity current gain f_T, which is in agreement with the degree of anisotropy for the two polytypes. Compared to the MC results the DD model gives f_T values that are lower, whereas the HD model gives higher values. The DD model gives g_m values that are close to the MC model, but the HD model overestimates it. Also, when it comes to current levels the DD gives better agreement than the HD model, which overestimates the current considerably. The HD model is very CPU demanding, therefore it is more “time saving” to use the DD model since the accuracy of the results are very good. The results have also been compared to a Si version of the MOSFET, with the same gate length, threshold voltage and bias conditions as the corresponding SiC device.

Table 2.1.1. Device performance for the simulated Si, 4H- and 6H-SiC MOSFET.

T [K]	**4H-SiC**						**6H-SiC**						**Si**			
	f_T [GHz]			g_m [mS/m]			f_T [GHz]			g_m [mS/m]			f_T [GHz]		g_m [mS/m]	
	DD	HD	MC	DD	HD	MC	DD	HD	MC	DD	HD	MC	DD	HD	DD	HD
300	173	204	191	657	706	612	128	157	139	422	455	425	126	176	465	578
500	142	165	160	531	566	500	95	116	105	294	317	310	107	139	400	468

2.1.2.2. Evaluation of different transport models for simulation of SiC MESFETs

A high frequency vertical MESFET structure in 4H and 6H-SiC has been studied using three different transport models; a full band Monte Carlo model, an anisotropic drift-

diffusion model and an anisotropic hydrodynamic model. The macroscopic models assume the same anisotropy at low and high electric fields. The hydrodynamic model used assumes a constant value for the energy relaxation time.

In a device with a one-dimensional current flow, the drift-diffusion and the hydrodynamic models describe the device well at electric field not exceeding $3 \cdot 10^5$ V/cm. At high electric fields the effects of the negative differential mobility observed in Monte Carlo simulations become significant, resulting in higher drain-current in the high-level model simulations.

In a device with a two dimensional current flow, the alternating behavior of the anisotropy in 4H-SiC must be accounted for in the high-level transport models.
The energy relaxation time is dependent on the electric field and anisotropy in 4H as well as 6H-SiC. In a device with a varying electric field, the hydrodynamic model used is not able to resolve carrier heating in a correct way. This shows that both the field dependency and the anisotropy of the energy relaxation time in 4H and 6H-SiC have to be considered in simulation of two-dimensional devices operated close to breakdown.

2.1.2.3 Optimization of SiC MESFET devices

The geometry of both vertical and lateral MESFETs for high frequency and high power operation, have been optimized, using iterative 2-dimensional simulations. Relevant parasitics are included in the simulations to reveal the performance of realistic devices. A comparison of the vertical and lateral MESFET for use in both low and high-power microwave applications is also presented.

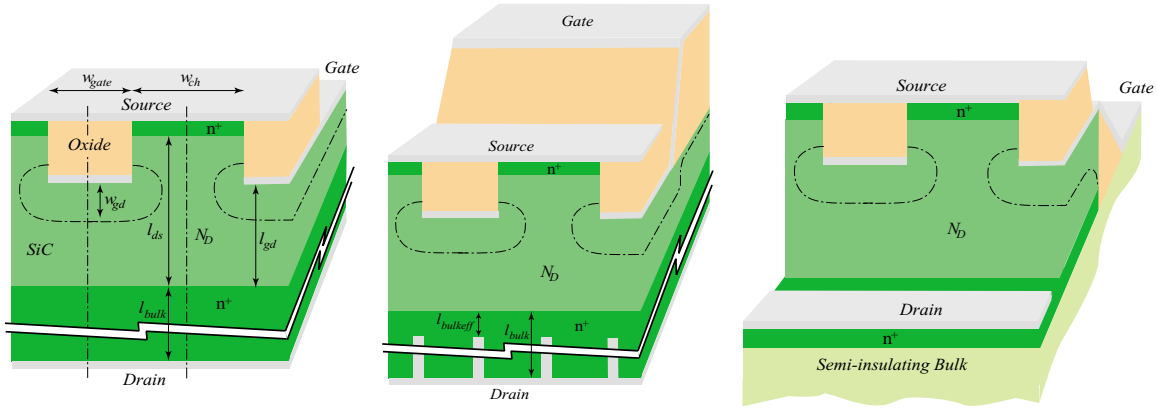

Fig 2.1.8 Two different way to improve the performance of the vertical SiC MESFET.

With the technology used today lateral MESFET on semi-insulating substrate is the best candidate for high-frequency low-power devices. The vertical MESFET is limited by inherent parasitics such as a high gate pad capacitance and bulk resistance and the optimization shows that for vertical MESFETs, using a standard technology, it is difficult to achieve higher f_T than already is achieved in a fabricated state of the art device.

The vertical MESFET is however a better candidate for high power applications and shows better driving capabilities compared to a lateral MESFET in its frequency range of operation.
The vertical MESFET can be improved by reducing the parasitics in the device (see Fig 2.1.8.). This can be achieved both by reducing the effective bulk thickness and increase the gate-pad to bulk spacing. A device like that gives better high frequency and high power performance compared to both vertical and lateral MESFETs (see Fig 2.1.9). This device is well suited as a discrete microwave power device. An optimized 4H-SiC improved vertical MESFET have P_{max} = 13 W at f_{match} = 10 GHz.

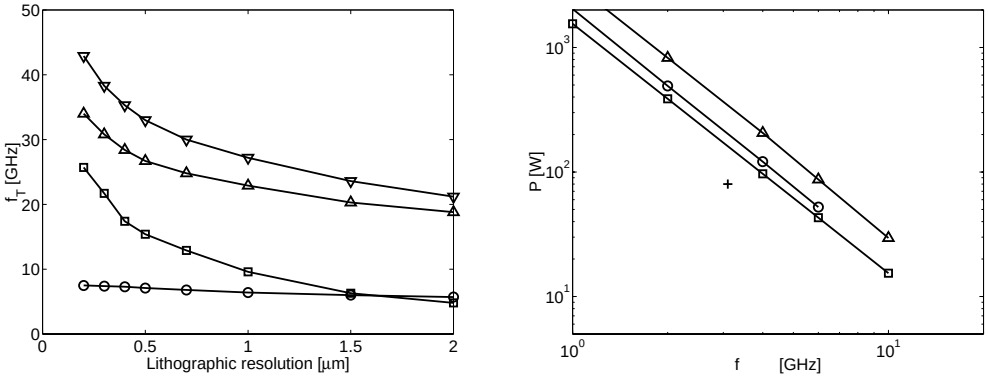

Fig 2.9 Optimized device performance. To the left, f_T as function of lithographic resolution and to the right, P_{max} as function of frequency for different types of MESFET devices. (o) - Normal vertical MESFET, (□) - Lateral MESFET, (Δ) - Vertical MESFET with reduced effective bulk thickness and increased gate-pad bulk spacing, (∇) - Vertical MESFET on semi-insulating substrate.

Vertical MESFETs can also be realized on semi-insulating substrates and in this case reaching higher frequencies, and the highest f_T obtained in the optimization for a 4H-SiC device is 50 GHz. As this device is completely realized in the epitaxial layers two-dimensional effects is important and the device should be designed with multiple short channels to minimize the influence of distributed drain-resistance. One more advantage with this structure over normal vertical MESFETs is the possibility to integrate multiple devices on the same chip.
The development of 2H-SiC substrates would be an advantage for SiC device performance, mainly for vertical devices where the performance can be increased with ≈ 20 % but also for lateral devices (≈ 5 %).
We have established a good agreement between simulations and measurements both for f_T and the power density and the reliability in the results are therefore expected to be good.

2.1.2.4. Simulation of X-ray absorption in a scintillator/oxide/semiconductor material system

The imaging properties of X-ray pixel detectors depend on the quantum efficiency for X-rays, the generated signal for each X-ray photon and the distribution of the generated signal between different pixels. In a scintillator coated device the signal is generated both

by X-ray photons captured in the scintillator and X-rays captured directly in the semiconductor. The signal-to-noise ratio (SNR) in the image is then a function of the number of photons captured in each of these processes, and the yield of each process in terms of electron-hole pairs produced in the semiconductor. The light spreading within the scintillator primarily determines the spatial resolution. In a pure semiconductor detector the signal is generated by one process only, and the SNR in the image is proportional to the number of X-ray photons captured within the sensitive layer. The spatial resolution is affected by the size of the initial charge cloud generated in the semiconductor and any diffusion of carriers between the point of interaction and the readout electrode. We have developed a model for the imaging properties of scintillator coated X-ray imaging detectors. Simulations using the Monte Carlo program MCNP have verified the model. We also have developed a new program for the transport of the generated light photons to the semiconductor. The combined results from these two simulations have then been used to simulate the charge transport in the semiconductor. For this purpose the commercially available device simulation program MEDICI was used.

2.1.2.5. Simulation of the imaging properties of scintillator coated X-ray pixel detectors

The combination of the three programs described in the previous section was used to analyze the resolution (MTF) and noise properties (SNR) of three emerging CMOS pixel detector structures, two different pn-junction structures and a phototransistor. The simulations show that the detector with a small sensitive depth has better resolution and noise properties. This result is in good agreement with what can be expected from theoretical model that has been developed. However, the phototransistor showed the highest MTF. The reason is the very short base-emitter junction length that contributes to the amplified main signal. We have demonstrated that this framework can be used to address large pixel arrays (>108 pixels) allows full control over detection of X-ray photons and charge transport effects.

2.2. Sensor technology

2.2.1. X-ray pixel detectors

During 2000-07-01 to 2001-06-30 the research on X-ray pixel detectors have mainly been theoretical performed within the simulation work package. A large part of the experimental efforts has been devoted to building a new cleanroom laboratory. This work will be presented in section 2.2.3.

2.2.2. Readout electronics for X-ray pixel detectors

Various integrating CMOS active pixel sensor (APS) imager prototypes have been designed, fabricated and successfully tested [sens1]. The devices were made to investigate the characteristics of different pixel architectures, and to evaluate their performance as an alternative to the currently dominating CDD based systems in dental X-ray imaging. The opto-electrical performance of photo-diodes type pixels and a phototransistor pixels were measured. The phototransistor pixels showed the highest sensitivity to light compared to the photo-diode pixels because of its transistor action.

However, its high dark current limits its reliability as a candidate in this application. Therefore a dark current cancellation technique was implemented and showed a significant leakage current cancellation [sens2]. Further improvement of the device will be worked on. The APS pixels whose photo-sensing elements are the photodiodes showed much lower sensitivity than the phototransistor pixels, but exhibited much lower direct detection for X-ray. The enhancement of the sensitivity of the photodiode sensor was achieved by implementing a preamplifier in the pixel. The measured results confirmed an improved optical sensitivity of the APS [sens3]. The imaging properties of scintillator coated CMOS pixel detector was simulated and characterised for two photdiode type pixels. Signal-to-noise (SNR) and Modulation Transfer functions were simulated and the results were reported [sim8].

The design of readout electronics for radiation sensors is driven mainly by small area and low power consumption. Several motivations suggest that most of the applications can benefit from the use of ASIC readouts in place of discrete solutions. CMOS technology is an attractive technology for fabricating such ASICs, particularly if a high level of integration is desired.
In radiation measurement applications wherein event counting technique is used,, the charge sensitive amplifier (CSA) is widely used at the front-end because its conversion gain is independent of the detector anode capacitance variation. CMOS technology offers many advantages over other technologies in implementing these amplifiers because of the high input impedance of the MOSFET transistor and its readily available inexpensive prototyping.
A typical analog processing channel for radiation measurement using event counting technique consists of a preamplifier, shaping amplifier, a single channel /or window discriminator or an ADC. The charge sensitive amplifier (CSA) is widely used at the front-end because its conversion gain is independent of the detector anode capacitance variation. The main amplifier-shaper, on the other hand, should ideally satisfy many requirements. It should amplify the pulse with negligible distortion and so should have sufficient linearity and a large enough bandwidth.
The goal is to design a complete photon counting circuit on a pixel for X-ray imaging. The pixel accommodates the analog-processing channel in addition to a 16-bit counter. The analog part consists of a preamplifier, an amplifier-shaper and a single channel analyzer.
We have introduced a new biasing techniques for the charge sensitive amplifier (CSA) - shaper topology to implement a feedback resistance in the Megaohm range using a MOSFET [sens5]. This technique used a mirroring circuit to stabilize the operation of the feedback transistor over process and temperature variations. Various design techniques for a photon counting pixel detector readout devoted to whole pixel design, window discriminator and noise reduction methods have been proposed [sens6, sys7, sys19].
The sensor technology group has also been involved with the detector research group at Glasgow University in an ion beam profile project [sens7]. Our contribution was in the design of the ASIC readout.

2.2.3. Development of new research infrastructure (cleanroom laboratory)

2.2.3.1. Background

The processing of sensors for radiation detection is one of the mainstays in the experimental research in semiconductor physics at mitthögskolan. However, the experimental resources have been located at KTH-Kista in Stockholm, 400 km from Sundsvall. Since a process to get through one batch can take about 1 months, it have been necessary for researchers from mitthögskolan to have double accommodation in Stockholm and Sundsvall respectively. Moreover, the fabrication of sensors needs special processing equipment, which was difficult to implement in the present activities at KTH. The decision to build a new clean room was of that reason not far away since a new building where planned at the campus in Sundsvall. A 200m^2 cleanroom was built for semiconductor processing and for analyses of metallic species in ground water, an activity that belongs to the department of chemistry. The cleanroom was ready to be equipped in the beginning of January of 2001.

2.2.3.2. Activities

The purchasing of new equipment started already in the spring 2000 and continued in the autumn. Equipment for semiconductor processing has unfortunately long delivery time. Delivery time in the order of 5 months or longer is not unusually. Sture Höijer from the department of administration has been very helpful in preparing the documents to manage the rules for EU-purchasing.
In December 2000 was Krister Aldén employed as a cleanroom-engineer. Krister have experience from cleanrooms at LM Ericsson AB (subμ-factory) and Mitel Semiconductor AB. Kristers good relationship with Ericsson and Mitel gave as a result that we have been able to get tree used maskaligner for free. We have also bought an used implanter (Varian DF4) very cheap and got a lot of spare parts as well as a plasma stripper and a HMDS-furnace. Moreover, From Mitel we have bought two used dry etchers for 1/10 of the market price (Tegal 901e and 903e) and one instrument for thin film thickness measurement. The two dry etchers differ in electrode distance, which make the one with shorter distance more suitable for anisotropy etching. The equipment have been dismantled and transported by us four times to Sundsvall. The used equipment's we have got are now in an overhauling process and some worn out parts have to be replaced.

We have purchased storages for chemicals, benches for equipment, wet benches, protecting clothes, expendable items, and chemicals for processing. The two tree stack quartz-tube furnaces was accepted after source inspection and is now installed and running. The purchased electron-beam evaporator is going to be delivered in the beginning of august. The installation of the evaporator in august finish the C-montage (connection of cooling water etc) in the cleanroom for this time. Process implementation is now initiated for installed equipment and test batches are running. The alarm system has been expanded to switch of the hydrogen bottle if a leakage occurs in the exhaust of the furnaces or a leakage occurs in the gas storeroom. Also an alarm detector for BF_3 have been implemented. A visit at the Ångström laboratory in Uppsala have been done to discuss our risk analyse plan from theirs perspective. Our risk analyse plan must be put together as fast as possible and sent in to the community. Education and maintenance of

the cleanrooms infrastructure have been given for us (exhaust and drainage of acid and solvent, ventilation system, vacuum system, clean water system, and alarm system). A vacuum course for semiconductor processing have been carried out and finished. We also planned to give a experiment in fabrication of pn-diodes for the students, reading the semiconductor physics at mid sweden university.

We have had visitors both from high school and adult education in the cleanroom and the expectation is an increasing interest in reading at Mid-Sweden University.

2.3. System design

The research on system design consists of four main activities: low-power design of electronics, video signal processing, rapid hardware prototyping, and design of pixel detectors. These activities are closely related, but involve different types of research goals.

2.3.1. Low-power design

The research in low-power digital design has been developed into two branches. The first one is about general design methods and design automation for low power. This work is focused on low-power finite-state machines (FSMs) and dynamic power management as the method for power reduction. The work has been going on since 1999 and it has been financed by this platform. We have published four papers since project start, e.g. [sys9]. The other branch is directed towards application specific techniques for low power design. The application area is video processing systems with high requirements on both low power consumption and high speed performance. This activity just has been started (spring 2001). This activity is partly described in this section and partly in the section called “Video and image signal processing”.

2.3.1.1. A mixed synchronous/asynchronous implementation architecture

A new approach to partitioned FSMs with mixed synchronous/asynchronous implementation architecture has been developed [sys13]. This work introduces a new model for designing partitioned finite-state machines (FSMs). The proposed model implies an implementation style that is based on a mixed synchronous/asynchronous state memory. The total state of the partitioned FSM is based on a global state and a local state. The local states reside in state memories that are updated synchronously at a clock edge. The global state is updated asynchronously, initiated by any of the sub-FSMs in the partition. The main objective is to provide a design model that enables low-power FSM design with low area overhead. The work includes procedures to transform the original monolithic FSM description to a description suitable for mixed synchronous/asynchronous implementation. Future directions for development or investigation of implementation architectures, performance, design automation, applications, and low-level optimizations for designs based on the proposed design model have been outlined.

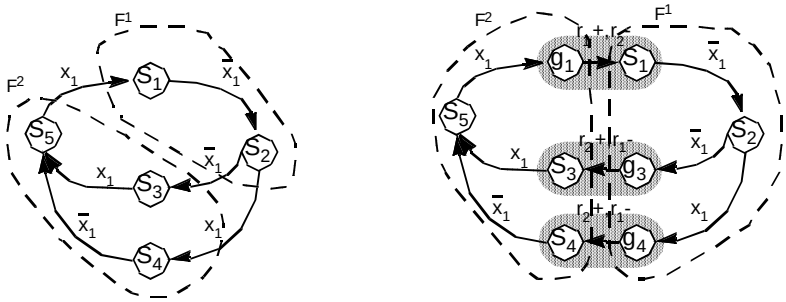

Fig. 2.3.1. Example of partitioned FSM, with state partition indicated in the left graph and the coupled states indicated in the right graph.

Several interesting problems related to this design model have been identified. We find it important to continue developing this approach because it is unique (no other group is working on it), the potential reduction in power consumption seems to be large, and it may be useful for applications other than FSMs. Continuation of this work is well suited as a PhD-thesis project.

2.3.1.2. Comparative study of low-voltage performance of standard-cell Flip-flops

The static single-phase D flip-flop (DFF) is the basic memory element in the standard cell based design methodology for digital integrated circuits. In low-power high-speed performance designs, pipelining in conjunction with voltage scaling has proven to be an efficient approach to achieve the targeted low-power performance. The efficiency of the flip-flop at low power supply voltages will therefore play an increasingly important role. In this work a comparison of the efficiency of several D flip-flops operating at low voltages are presented and discussed [sys15]. The results have been obtained from analog simulation in Powermill. This study indicates that power savings are possible in power-driven synthesis by including different flip-flops that are based on different design styles in the standard cell library.
Power consumption characterization of flip-flop circuits requires extensive simulations. For each level of power supply voltage, the delay characteristics and power consumption for different data input patterns must be simulated. A simulation environment for power and delay characterization of digital CMOS circuits has been developed. The objective is to provide the designer with automated characterization procedures. This simulation environment can be seen as a wrap-around Powermill that is an analog simulator with features for monitoring the power consumption in the circuit. It is based on scripts in Matlab and Perl.

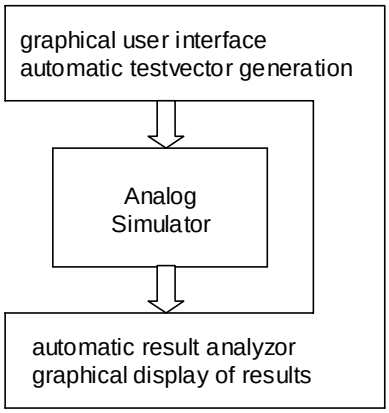

Fig. 1.3.2. Simulation environment.

2.3.2. Video and image signal processing

In this activity, we study the implementation, both hardware and software, of video signal processing algorithms and systems. The activities in this work package are done in close cooperation with industrial partners.

2.3.2.1. Spatial and temporal video enhancement filter

2.3.2.1.1 Algorithm improvement

This project presents an improved algorithm targeting real-time noise reduction in digitized video using spatio-temporal filtering techniques. The noise reduction device is a spatio-temporal filter using information from both the spatial and the temporal domain of the video sequence that is to be filtered. The filter core is accessing seven frames at a time from an uncompressed RGB video stream and produces an uncompressed RGB video stream as an output. The proposed algorithm allows extensive parallelism suitable for FPGA or ASIC implementation. We can show that a significant performance, up to 17% improvement can be achieved with the refined algorithm without increasing the implementation cost in terms of area and timing for both ASIC and FPGA technology [sys1, sys4].

One of the improvements is the refined shot-noise detection function that gives a more efficient way to handle impulse noise. As a consequence by the nature of this function it provides an efficient tool to repair block-loss of transmitted frames and also restoration of mechanical film defects. Fig. 2.2. shows the previous presented function marked with green color, and the new one in gray.

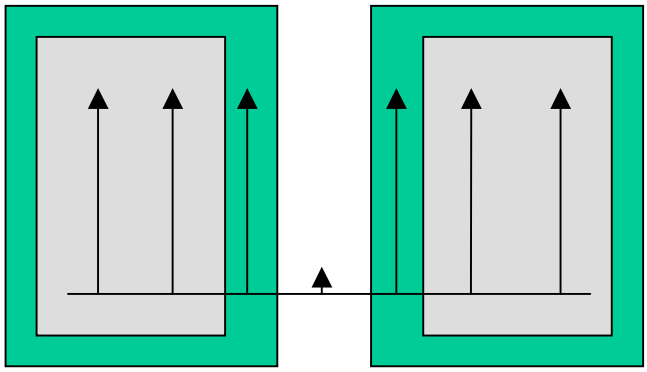

Fig. 2.2.3. Previous and refined shot-noise function in green and gray respectively.

2.3.2.1.2 Hardware implementation
Design of a device for real-time noise reduction in digitized video using temporal filter techniques targeting ASIC implementation. The noise reduction device is a three-dimensional filter using both spatial and temporal information from the video sequence that is to be filtered. The input format of the video stream is uncompressed RGB and the filter is accessing seven image frames at a time. An implementation of the video filter has been designed [sys1]. The chip area of 19.5 mm^2, 96 I/O-signals, 71 MHz I/O frequency for real-time filtering in a 0.6 µm CMOS process and standard cell implementation approach.

To investigate the implementation cost for FPGA-technology we implemented both versions of the algorithm and concluded that we managed the timing constraints without any increased use of recourses [sys4].

2.3.2.1.3 Software implementation
In the D-level course *Embedded System Design - 5p,* a group of students have implemented the spatial/temporal video filter algorithm on a software platform as a design project. The selected software platform is an Intel based PC-platform utilizing the MMX instruction set of the processor. The project has resulted in an implementation that takes 70 clock cycles to process a pixel. Thus, a PAL video stream would be filtered in real-time on an Intel or AMD MMX enabled processor with an operating frequency over 700 MHz. Hopefully, these results will be presented as a conference presentation later this year.

What still needs to be solved, and was out of the scope project, is the I/O for the video stream. That is, solve how the filter is fed with a video stream from a disk or frame grabber.

2.3.2.2. Image reconstruction of panoramic X-ray image sequences

A master's thesis done by Patric Thelander has been presented during the spring [sys11]. The goal for this work was to do a problem formulation and a case study of image reconstruction algorithms.

2.3.2.2.1 Acquisition

The acquisition setup contains a X-ray tube with a SAR648 as sensor, a rotating table built on a precision rotator with a universal motion controller/driver (Fig. 2.3.3.) and a program named Xray 3D composed especially for taking a certain amount of pictures related to the rotation degree.

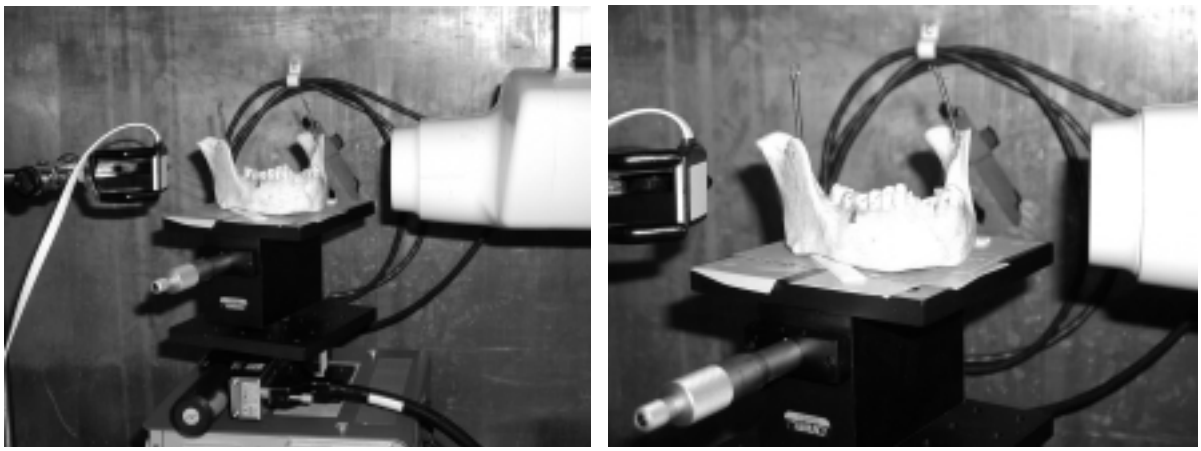

Fig. 2.3.3. Image acquisition setup.

2.3.2.2.2 Image reconstruction

Different reconstruction algorithms were tested. One that reconstruct the panoramic image through summation of a several sample images and another that combines summation and median selection of images. The developed and tested algorithm is described in Fig. 2.3.4. and the result from this algorithm is shown in Fig. 2.3.5.

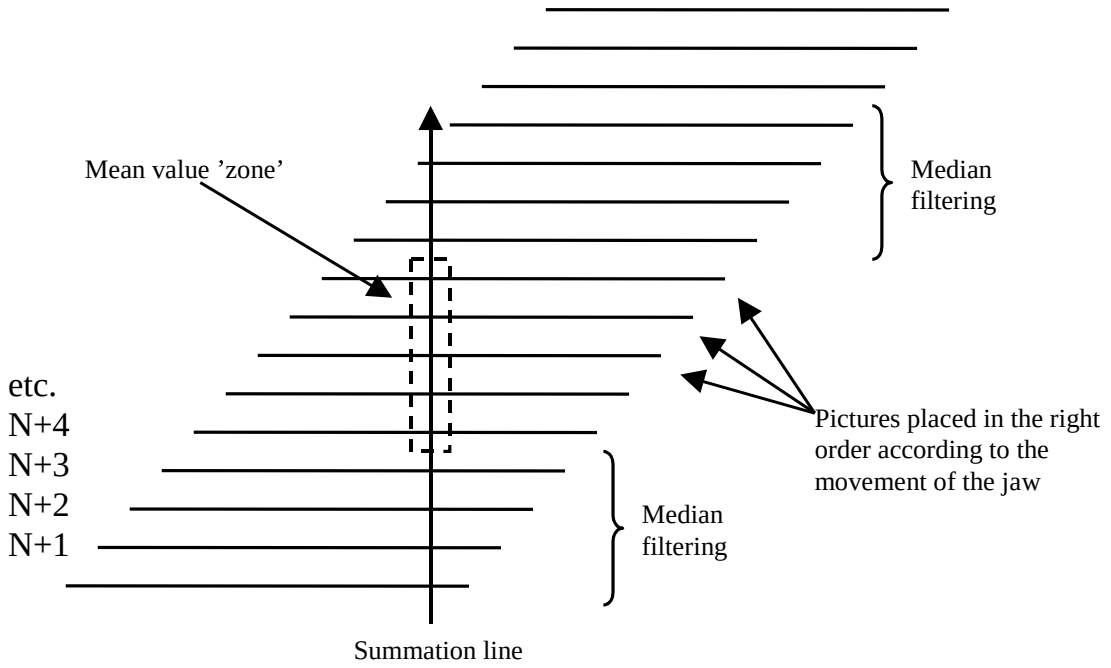

Fig. 2.3.4. The hybrid filter.

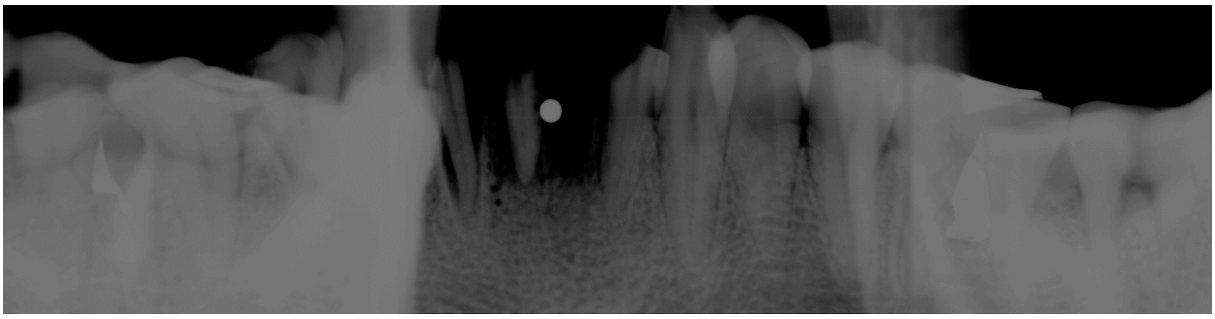

Fig. 2.3.5. Result from the hybrid reconstruction, mean value of frames 5-15 of total 50 frames.

2.3.2.2.3 Conclusions

The main results from this work were the definitions of bottlenecks in the panoramic imaging system. The most important research problems found in this work were:

- The movement of the acquisition setup. That is, how should the image sensor and the radiation source move for best image acquisition?
- Find an automatic movement estimation algorithm. That is, an algorithm that automatically finds the movement in both sides of the jaw and thus enable auto focus.
- How many pictures per degree have to be captured for the selected algorithm?
- Analysis of the distance between the jaw and the source.

2.3.2.2 Algorithms and architectures of the VLSI for mobile multimedia terminals.

This activity will start up during the summer of 2001. The plan is to complete necessary pre-studies in the beginning of December 2001 in order to set up long-term research goals in this area. Today one PhD student is engaged in this project.

2.3.3. Environment for rapid prototyping

One major challenge for prototyping of video processing systems is the large amounts of data which these systems typical process. The large amounts of data, one or several video frames, must be processed by the system at the predefined frame-rate imposed by the video standard. These requirements introduce hard real-time constraints on the interfaces to the system and internally in the system. Another issue that needs to be researched is the methods for rapid development of video processing system prototypes.

2.3.3.1. Analysis of real-time constrains for prototyping environment

A PC based hardware prototyping platform is very appealing for the user of the system due to: its user friendliness, the high availability of hardware prototyping platforms, it is cheap, and it is a widely spread and well-known architecture. We have preformed a theoretical analysis of the bus and storage communication [sys5, sys6]. From the derived results we have analyzed the limitations of this architecture with respect to real-time prototyping of image and video signal processing algorithms. Achieved results have been verified through simulations of the existing bus architectures, as seen in Fig. 2.3.6. We can show a number of possible architectures that supports different types of prototyping configurations for prototyping of video-systems up to the emerging HDTV quality.

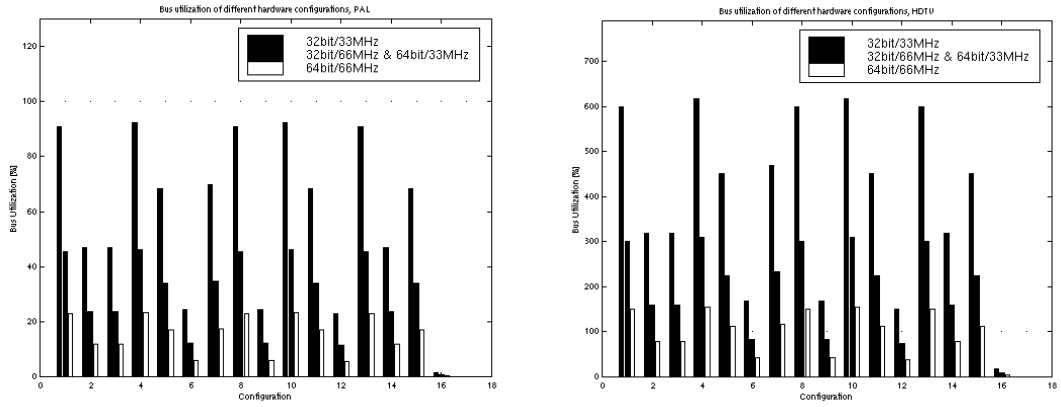

Fig. 2.3.6. Analysis and simulation results, describes bus utilization for HDTV and PAL respectively.

2.3.3.2. Development of hardware prototyping environment

We have developed a hardware prototyping environment for development of real-time video processing systems. This environment is composed of a hardware prototyping board from Nallatech and a PC equipped to feed the prototyping board with test data.
Our intention in this project is to improve this environment further and add design tools/methods to aid the designer in the development of video processing systems.

2.3.3.2.1 Test of hardware prototyping environment

To enable rapid development of video processing functions we need a number of generic standard functions to handle input- and output data. Real-time grabbing of video is one

part that is crucial. This part has been tested and evaluated, the function is satisfactory so far. Large frame-store is required to efficient use available data, especially required for the video filter presented above. Currently a physical-level SDRAM controller is under design and test.

2.3.3.3. Object oriented hardware modeling of video systems

During 00-01 has Benny Thörnberg done his Bachelor' thesis on evaluating C++ based hardware design methodologies. The evaluation targeted video processing systems.

By the addition of constructs for modeling electronic systems, well-known sequential programming languages like C/C++ can be used for hardware simulation and synthesis. The languages themselves lack all the necessary mechanism for such parallelism, though it can be added by means of a class library. The development in this area is driven by the huge competence that exists for these languages. There is also a need for a test strategy, applicable throughout the whole design process from algorithm down to register level, which is another good reason to go for C/C++. A spatio temporal video filter, characterized by high requirements on computation, memory size and bandwidth, is chosen for a case study. Oacpi and SystemC are examples of specification methods based on object oriented class libraries. The thesis intends to evaluate and compare the modeling, simulation and hardware synthesis capabilities of these two class libraries within the chosen case study [sys12, sys18]. The results point out SystemC to be the most suitable specification language for this application. Comparison results have been summarized in Table . The thesis also outlines some ideas of a parameterized memory model to support a more general video-processing algorithm.

PARAMETER	OCAPI	SYSTEMC
Simulation scheduler	Linear programming	Real time kernel
Models needed for simulation	Design, test bench and parts of the simulator	Design and test bench
Resolved signals for memory interface	No (implicit)	Yes
Supports hierarchical design	No	Yes
Explicit support for memory hierarchies	No	No
Memory usage for 576 x 705 sized frames (PAL)	325 Mb	43 Mb
Simulation performance, RTL-model 120x200 frame	95 [sec./frame]	515 [sec./frame]
Hardware synthesis	Transformations and external tool	Compiler
Lines of code	4160	2670

Table 2.3.1. Comparison of modeling and simulation capabilities for the video filter.

2.3.3. Photon counting pixel detectors

The system design group has during the year been involved in the design aspects of a photon counting pixel detector. The activities have been focused on the digital parts of the pixel detector. Problem formulations for the digital blocks have been signal integrity and chip area. During this year, two design blocks have been studied: the clock generator in the discriminator and the event counter, see Fig. 2.3.7.

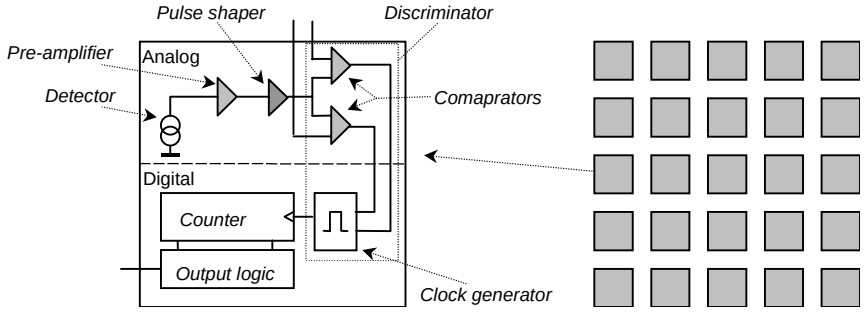

Fig. 2.3.7. Pixel detector and pixel array for photon counting X-ray image sensors.

2.3.3.1. Discriminator design

High spatial resolution of pixel arrays puts hard constraints on the circuit area. Area-efficient solutions for both analog and digital circuits are needed. In addition, the mix of analogue and digital circuits on a small area will make the analog part subjected to digital noise. In this work an all-digital window discriminator (ADWD) for photon counting pixel detectors has been developed [sys7]. The ADWD reacts upon the events generated by the integral discriminators and conditionally generates a clock pulse for input pulses with energy levels within the defined window.

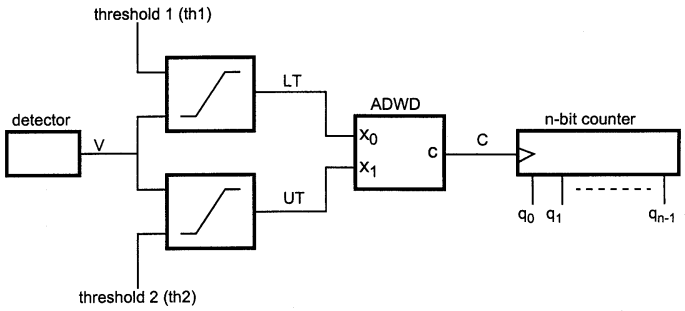

Fig. 2.3.8. A simpliefied block diagram of the photon counting pixel.

Our solution is event-driven and does not rely on external or internal timing references. Results from analog simulations give minimum resolution time of 100 ps and shortest time between two consequtive pulses of 600 ps that the ADWD can detect. A full-custom implementation contains 22 transistors with a circuit area of 350 μm^2, see Fig. 2.3.9.

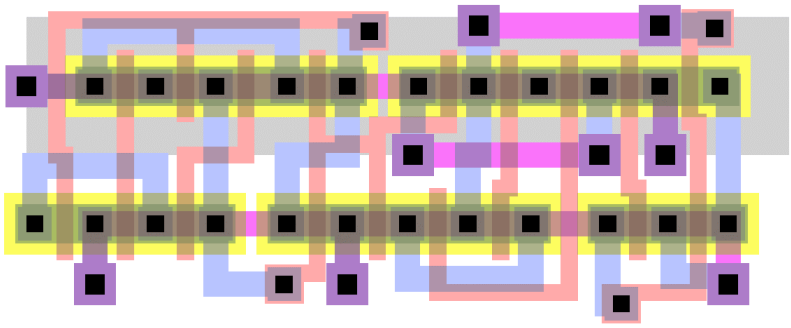

Fig. 2.3.9. Layout of the ADWD module in a 0.6 µm CMOS process.

2.3.3.2. Counter design

Photon counting in image sensors removes the need for AD converters since the method is based on counting discrete events. This introduces a problem with digital interference since the digital and analog parts are closely integrated into the same small pixel area. Additionally, there can be close to one million pixels integrated onto the same image sensor chip. This and the close integration of the digital and analog parts will require careful considerations regarding the noise inject into the analog signal flow due to digital switching. The established implementation styles of the event counter in a photon counting pixel detector is to use a linear feedback shift register (LFSR) as an event counter. With an LFSR as counter, the readout function will almost comes for free since the LFSR is easily converted into a shift register.

The proposed low-power counter architecture use the simple fact that rounding 3.452±0.2 to 3.45±0.2 adds only a small error. That is, we allow truncation in the pixel but keep the same dynamic range for collecting events. The truncation is done by splitting the counter into two parts, see Fig. 2.3.7: one prescaler that divide the counting frequency to the event counter and one event counter. The event counter is implemented with an LFSR and the prescaler with an asynchronous counter.

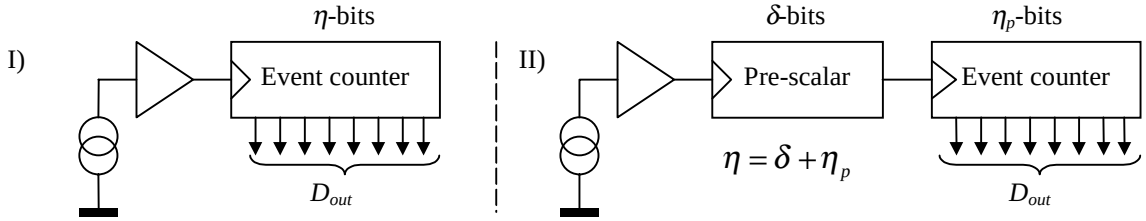

Fig. 2.3.10. Two different architectures for a photon counter in a pixel detector.

Through analysis of the event counter size that is needed to fulfil a signal to noise ratio, SNR, constraint we got following relation between the SNR and event counter size, D_{out}:

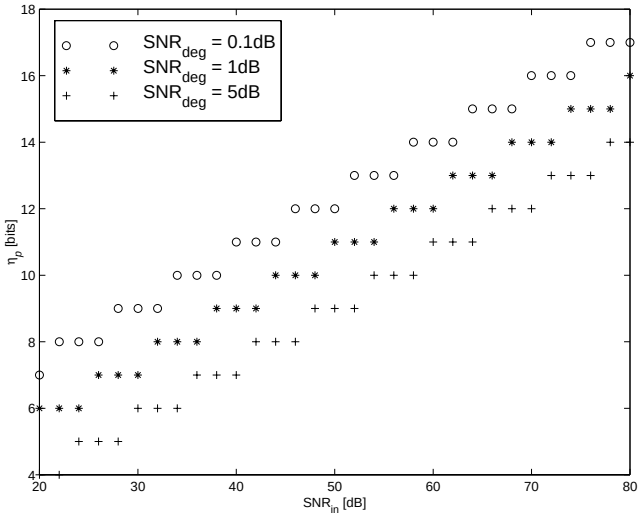

Fig. 2.3.11. Plot of η_p vs the SNR_{in} for different SNR_{deg} constraints.

We have also show that the peak current for a typical event counter can be decreased by a factor of 5 with our architecture compared to the established architecture, see Fig. 2.3.12. and Table 1. [sys14].

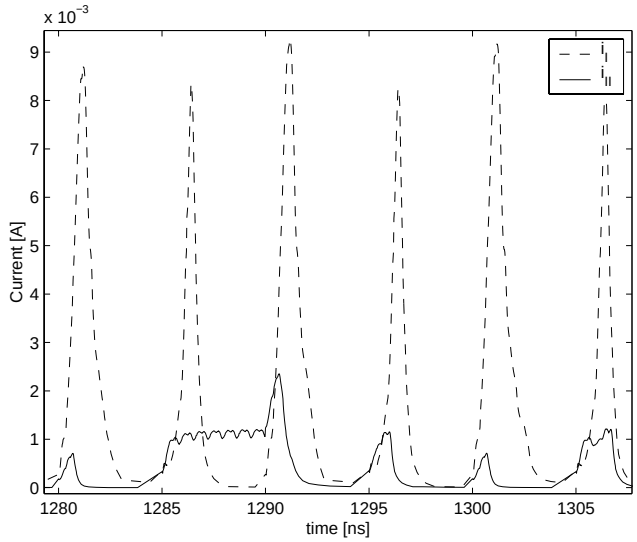

Fig. 2.3.12. Plot of power supply current for the 16-bit counter of both type I and II. Worst case current for the type II counter.

Table 1.3.2. Comparisons between power supply current and *di/dt* for a type I and type II counter.

	Type I	Type II	Ratio (I/II)
Max current	13.3 mA	2.4 mA	5.54
Mean current	2.5 mA	0.66 mA	3.79
Max di/dt	22.8 mA/ns	3.99 mA/ns	5.72
Mean di/dt	2.51 mA/ns	0.57 mA/ns	4.46

2.4. Interdisciplinary research activity

2.4.1. Simulation of the noise to signal ratio in a scintillator coated CMOS pixel sensor

This simulation requires integration of two different simulation packages, MCNP and MEDICI. MCNP is a very advanced Monte Carlo simulator of the interaction of high-energy photons with matter and MEDICI is a commercial semiconductor simulator with optical interface. The simulation takes into account both the signal generated in the scintillator and the signal from the X-ray photons absorbed in the CMOS sensor directly. To perform this type of simulation a new intermediate simulation program that combines MCNP and MEDICI has been developed. The combination of these three programs was used to analyze the resolution and noise properties of three emerging CMOS pixel detector structures.

2.5. The panoramic imaging system

During the first year of the project we have been discussing the amount of practical engineering work, that should be performed related to the panoramic X-ray demonstrator. After careful considerations we have decided to limit the ambition in the engineering area. This allows us to focus on the scientific challenges involved in the demonstrator. These can be listed as

- Gaining fundamental knowledge about operation and limitations of high performance image sensors
- Design and optimisation of a high performance image sensor
- Design of fast and efficient readout electronics
- Design and evaluation of image reconstruction algorithms

This strategy limits the engineering ambition to set up counting and integrating sensors for panoramic imaging, using low speed data communication between the computer host and the sensor. The requirement of high speed for the final “product” will be secured though detailed studies of the sensor in an experimental test bench that allows verification without full design of a “product”.
The results related to the panoramic imaging system are presented in sections 2.1.2.5, 2.2.2, 2.3.2.2 and 2.3.3.

3. Recruitment

The recruitment activities have been directed towards ensuring senior competence, and to increase the number of PhD students within the three main research groups. We are trying to synchronize the recruitment in such a way that the new PhD students will be ensured to have good guidance by the senior staff. This is achieved by first employing senior researchers and then PhD students. The following recruitment have been made during the second year of the project:

- Mr. K. Aldén
  - Mr. Aldén has been employed as a laboratory technician (cleanroom).
- Prof. M. Breidne
  - Adjunct Professor in optoelectronics.
- Dr. B. Oelmann
  - Bengt Oelmann finished his PhD degree in June 2000. The support from this platform makes it possible for him to stay as a senior researcher within the system design group.
- BSc. U. Englund
  - Master student working on semiconductor simulation.
- BSc. P. Thellander
  - Master student working on image reconstruction of panoramic X-ray image sequences.
- MSc. B. Norlin
  - Started to work within the platform in the sensor technology research group.
- BSc. B. Thörnberg
  - Started to work within the platform in the system design research group.
- MSc. X. Shang
  - Started to work within the platform in the system design research group.

4. Information activities

In this section we have listed all the information activities within the platform from 1999-07-01. In this way a better overview of the information activities is obtained.
The information activities can be divided into three different categories.

- Dissemination of research results within the international scientific community.
  - The 1st International Workshop on Radiation Imaging Detectors was organized by the research group at Mitthögskolan in June 1999.
  - We participated in the conference committee of the same conference previous year in Freiburg, Germany.
  - We are participating in the conference committee of the same conference this year in Sardinia, Italy.
  - The results obtained within this research platform have been presented on several international research conferences.
    - The International Conference on Silicon Carbide and Related Materials, Research Triangle 1999, North Carolina, USA
    - The IMACS conference on Monte Carlo Methods, Varna, Bulgaria
    - The 1st International Workshop on Radiation Imaging Detectors, Sundsvall, Sweden
    - The 2nd International Workshop on Radiation Imaging Detectors, Freiburg, Germany
    - The IEEE International Conference on Electronics, Circuits and Systems, Cyprus.
    - European Conference on Circuit Theory and Design, Stresa, Italy

  - The IEEE Norchip Conference, Oslo, Norway
  - IEEE Nordic Signal Processing Symposium, Kolmården, Sweden
  - Nuclear Science Symposium 2000, Lyon, France
  - The 19th Nordic Semiconductor Meeting, Copenhagen, Denmark
  - Computers in Power Electronics, 2000, Blacksburg, Virginia USA
  - Diamond and Related Material, 2000, Porto, Portugal
  - High Temperature Electronics, 2001, Oslo, Norway
  - European Material Research Symposium, Strassburg, France
  - International Symposium on Information Theory and Its Applications, Hawaii, USA.
  - The IEEE Norchip Conference, Åbo, Finland

- Dissemination of research results within the Mid-Sweden region.
  - The research work within the platform has been addressed by the following regional media
    - Sundsvalls Tidning, 2000-06-07
    - Sveriges Television, Mittnytt, 2000-06-07
    - Radio Västernorrland, 2000-06-07
    - Sundsvalls Tidning, 2000-09-19, The profile application.
- Dissemination of research results within Mitthögskolan
  - The research within the platform has been presented in different internal channels.
    - Annual report of the Department of Information Technology and Media
    - Official opening of the research center developed in cooperation between SCA and Mitthögskolan.
    - Project presentations at Mitt-Forum, which is a conference on regional development of the Mid-Sweden area.

5. Summary

This report has presented the research results obtained within the platform on Electronic Devices, Sensors and Systems at Mitthögskolan. The most important research results obtained in this platform are:

- A new Monte Carlo model for charge transport in complex materials have been developed and applied to study carrier transport in SiC polytypes.

- The effect of using different transport models applied to simulation of SiC devices have been studied and the fundamental limitations of the models have been clarified.

- A new iterative optimization strategy for MESFET transistors have been developed and applied to SiC MESFETs

- A numerical model for the interband tunneling in hexagonal semiconductors have been developed.

- Our MC simulation program as been updated to include accurate models for high field carrier transport in silicon and GaAs.

- A new approach to simulate scintillating X-ray image detectors has been developed.

- Integrating CMOS readout prototype circuits for dental x-ray imaging have been designed and fabricated. Successful results from the circuits being hybridized to scintillating x-ray sensors were obtained. On the other hand, new circuit design methods for preamplifiers, shapers, discriminators and digital counter to be implemented in photon counting pixel electronics have been investigated and tested by simulation. A complete photon counting pixel circuit is currently under development.

- A first version of a readout ASIC for ion beam profiling has been fabricated and successfully tested after being assembled with the complete system. A second improved version of the design is underway. The work is done in collaboration with Glasgow University.

- A new cleanroom facility for experimental research on semiconductor devices and sensors has been established.

- A Master's thesis with the title "A prestudy in rapid prototyping for video signal processing algorithms" (Håkan Norell) has been produced.

- A Master's thesis with the title "*Panoramic X-ray Image Reconstruction - Problem formulation and case study*" (Patric Thelander) has been produced.

- A Bachelor's thesis with the title *Ocapi versus SystemC - A case study comparing two specification methods for object oriented hardware design*" (Benny Thörnberg) has been produced.

- A profile application to KK-foundation with the title "Centre for Multimedia Technology" has been produced [sys17].

- Started a co-operation between the research group in Teleinformatics and the system design group. The co-operation will hopefully be formalized in three KK-foundation projects with the title "Adaptive video transmission over heterogeneous networks" [sys16].

- Analysis and design of digital parts in a photon counting pixel detector.

5.1. Milestones

5.1.1. Device simulation

Research milestones:	Date:	Status
Drift-diffusion simulation of a Silicon X-ray detector	Febr. 2000	Done
Monte Carlo simulation of a 6H-SiC MOSFET for high temperature electronics	March 2000	Done
A new Monte Carlo model for high field hole transport in 4H-SiC	June 2000	Done
Implementation of GaAs in our Monte Carlo simulation program	July 2000	Done
Implementation of algorithms for absorption of electromagnetic radiation and high energy particles	Jan. 2001	Done
Monte Carlo simulation of a Silicon X-ray detector	Jan. 2002	Done
Monte Carlo simulation of GaAs, Si and SiC X-ray detectors	July 2002	

5.1.2 Sensor technology

Research milestones:	Date:	Status
Assessment of the time dependence of the X-ray response for LEC, VPE and doped GaAs layers.	Nov. 1999	Done
CMOS prototype readout circuit whith on-chip photodiodes for X-ray imaging using scintillating layers.	April 2000	Done
Theoretical study of the properties of a GaAs detector with horizontal depletion field.	May 2000	Done but not reported
Simulation of the UV-response of detectors made from other materials than silicon.	June 2000	Done but not reported
Comparison of GaAs and CdTe detectors on the same read-out chip.	June 2000	Done
Test set-up to collect images for verification of image reconstruction algorithms for panoramic images using a standard intra-oral system.	June 2000	Done
Panoramic images of a dental phantom reconstructed from a set of single shot images taken in a test jig.	Nov. 2000	Done
First MEDIPIX2 system for photon counting	Mar 2001	
Dental images taken at different photon energies	Jun 2001	
First prototype of the Scintillating Guides Screen in our cleanroom	June 2001	
A reliable process for detector fabrication in our cleanroom	Oct 2001	
Study of colour X-ray imaging in dental applications	Dec 2001	
Photon counting High speed, dual polarity readout circuit for panoramic imaging (first prototype)	Dec. 2001	
Optimised structure of the Scintillating Guides Screen	June 2002	

5.1.3. System design

Research milestones:	**Date:**	**Status**
Panoramic images of a dental phantom reconstructed from a set of single shot images taken in a test jig.	Jan 2001	Done
Analysis of real-time parameters of a hardware prototyping environment for real-time video and image prototyping.	July 2000	Done
Selection of a prototyping environment hardware prototyping of video and image signal processing systems	July 2000	Done
Implementation of prototyping environment	June 2001	Done
Investigation of incremental refinement design methods for prototyping development based on C++ modelling and synthesis.	June 2001	Done
Low power Finite-State Machines	Aug. 1999	Done

6. References

See Appendix A.

Appendix A

List of publications

Device simulations:

[sim1] H-E. Nilsson, E. Bellotti, M. Hjelm, K. F. Brennan, "A comparison between different Monte Carlo models in simulation of hole transport in 4H-SiC", Mathematics and Computers in Simulation, Vol. 55, No. 1-3, pp. 199-208, 2000

[sim2] K. Bertilsson, H-E. Nilsson, C. S. Petersson, "Simulation of anisotropic breakdown in 4H-SiC diodes", Proceeding of Computers in Power Electronics -2000, Virginia Tech, Blacksburg, Virginia, USA, 16-18 July 2000

[sim3] E. Bellotti, H-E. Nilsson, K. F. Brennan, P. P. Ruden, R. Trew, "Monte Carlo calculation of hole initiated impact ionization in 4H-SiC", J. Appl. Phys., Vol. 87, No. 8, 2000

[sim4] K. Bertilsson, E. Dubaric, G. Thungström, H-E. Nilsson, C. S. Petersson, "Simulation of Low Atmospherical Noise Four-Quadrant Position Sensitive Detector", Nuclear Instruments and Methods in Physics Research Section A, Vol. 466, Issue 1, pp. 183-187 (June 2001)

[sim5] K. Bertilsson, E. Dubaric, H-E. Nilsson, M. Hjelm, C. S. Petersson, "Monte Carlo Simulation of vertical MESFETs in 2H, 4H and 6H-SiC", Diamond and Related Materials, No. 10, 2001, pp 1283-1286

[sim6] K. F. Brennan, E. Bellotti, M. Farahmand , H-E. Nilsson, P. P. Ruden and Y. Zhang, "Monte Carlo simulation of noncubic symmetry semiconducting materials and devices", Trans. on Elec. Dev., Invited, Vol. 47, p. 1882, 2000

[sim7] E. Dubaric, C. Fröjdh, H-E. Nilsson, C. S. Petersson, "Resolution and Noise Properties of Scintillator Coated X-ray Detectors**"** Nuclear Instruments and Methods in Physics Research Section A, Volume 466, Issue 1, pp. 178-182 (June 2001)

[sim8] E. Dubaric, C. Fröjdh, M. Hjelm, H-E. Nilsson, M. Abdallah, C. S. Petersson, "Monte Carlo Simulations of the Imaging Properties of Scintillator Coated X-ray Pixel Detectors" Presented at the Nuclear Science Symposium 2000, Lyon, France (Oct. 2000) (Submitted to IEEE Trans. On Nuclear Science)

[sim9] E. Dubaric, K. Bertilsson, H-E. Nilsson, "Simulations of submicron MOSFETs in 2H-, 4H- and 6H-SiC", proceedings of NSM'01, Copenhagen, Denmark

[sim10] E. Dubaric, K. Bertilsson, M. Hjelm, H-E. Nilsson "A Comparison of Different Transport Models and Their Effects in Simulations of a 100 nm MOSFET in 6H-SiC" Submitted to IEEE Trans. on Electron Devices

[sim11] K. Bertilsson, H-E. Nilsson, M. Hjelm, C. S. Petersson, P. Käckell, C. Persson, “The Effect of Different Transport Models in Simulation of High Frequency 4H-SiC and 6H-SiC Vertical MESFETs”, Solid-State Electronics, Vol 45 (5), 2001, pp. 645-653.

[sim12] K. Berilsson, H-E. Nilsson, “Optimization of 2H, 4H and 6H-SiC MESFETs for High Frequency Applications”, Presented at Nordic Semiconductor Meeting 2001

[sim13] K. Bertilsson, M. Hjelm, H-E. Nilsson, C. S. Petersson, “Monte Carlo Simulation of 4H and 6H-SiC short channel MOSFETs”, (To be Presented at HITEN 2001)

[sim14] K. Bertilsson, H-E. Nilsson, “Optimization of 2H, 4H and 6H-SiC high-speed vertical MESFETs”, (To be presented at Diamond 2001)

[sim15] M. Hjelm, H.E. Nilsson, "Methods for Anisotropic selection of final states in the Full Band Ensemble Monte Carlos Simulation Framework", submitted for publication in Simulation Practice and Theory.

[sim16] M. Hjelm, K. Bertilsson, H.-E. Nilsson, "Full band Monte Carlo study of bulk and surface transport properties in 4H and 6H-SiC", submitted for publication in proceedings of E-MRS Spring Meeting, Juny, 2001.

[sim17] H-E. Nilsson, A. Martinez, U. Sannemo, "Numerical Study of Bloch Electron Dynamics in Wide Band-Gap Semiconductors", submitted for publication in proceedings of E-MRS Spring Meeting, Juny, 2001.

[sim18] H-E. Nilsson, A. Martinez, M. Hjelm, E. Bellotti, K. Brennan, "Monte Carlo simulation of multi-band carrier transport in semiconductor materials with complex unit cells", submitted for publication in the proceedings of SISPAD'01, Sept., 2001.

[sim19] H-E. Nilsson, A. Martinez, E. Ghillino, U. Sannemo, E. Bellotti, M. Goano, "Numerical calculation of hole band-to-band tunneling in GaN and SiC", submitted for publication in J. Appl. Phys.

[sim20] A. Martinez, U. Lindefelt, M. Hjelm, H-E. Nilsson,"A Monte Carlo Study of Low Field Transport in Al Doped 4H-SiC", submitted for publication in proceedings of E-MRS Spring Meeting, June, 2001.

[sim21] A. Martinez, H-E. Nilsson, U. Lindefelt, “A study of band to band tunneling with application to high-field transport in hexagonal SiC polytypes”, Materials Science Forum Vols. 353-356, pp. 487-490, 2001

[sim22] P. P. Ruden, E. Bellotti, H-E. Nilsson, K. F. Brennan, “Modeling of Band-to-band tunneling transitions during drift in Monte Carlo transport simulations”, J. Appl. Phys., Vol. 88, No. 3, p. 1488-1493, 2000

Sensor Technology:

[sens1] Munir A. Abdalla, C. Fröjdh, C. S. Petersson, “A CMOS APS for dental X-ray imaging using scintillating sensors”, Nuclear Instruments And Methods-A 460 (2001) 197 - 203.
[sens2] Munir A. Abdalla, E. Dubaric, C. Fröjdh, C. S. Petersson,” A Scintillator-coated Phototransistor Pixel Sensor with Dark Current Cancellation”, To appear in the Proceedings of "The 8th. IEEE International Conference on Electronics, Circuits and Systems (ICECS'2001)- Malta, Sept.2001.
[sens3] Munir A. Abdalla, C. Fröjdh, C. S. Petersson, “ An integrating CMOS APS for X-ray imaging with an in-pixel preamplifier”, Nuclear Instruments And Methods-A 466 (2001) 232 - 236.
[sens5] M. A. Abdalla, C. Fröjdh, C. S. Petersson, “A New Biasing Method for CMOS Preamplifier-Shapers”,
Proceedings of "The 7th. IEEE International Conference on Electronics, Circuits and Systems (ICECS'2K)", Lebanon, Dec.2000.
[sens6] M. A. Abdalla, C. Fröjdh, C. S. Petersson, “An All-analog Time-walk Free SCA for Event Counting Pixel detectors”, Accepted in the 5th WSES/IEEE CSCC2001-Crete, July 2001.
[sens7] M. S. Passmore, M. A. Abdalla, J. van den Berg, C. Fröjdh, D. Livingston, J. Marchal, V. O'Shea, M. Rahman, K. M. Smith, “ Active Pixel Detector for Ion Beam Profiling”, Manuscript

System design:

[sys1] Håkan Norell, Bengt Oelmann and Youshi Xu, "Spatio-Temporal Noise Reduction ASIC for Real-Time Video Processing", *Proceedings of the IEEE Nordic Signal Processing Symposium*, 2000.

[sys2] A. Jantsch, S. Kumar, I. Sander, B. Svantesson, J. Öberg, A. Hemani, P. Ellervee, M. O'Nils, "Comparison of Six Languages for System Level Descriptions of Telecom Systems", *Electronic Chips & Systems Design Languages*, edited by Jean P. Mermet, Kluwer Academic Publisher, ISBN 0-7923-7311-1, March 2001.

[sys3] Mattias O'Nils and Bengt Oelmann, "Using CoWare in a Course on Design of Embedded HW/SW System", In *Proceedings of the 18th IEEE Norchip Conference*, 2000.

[sys4] Håkan Norell, Bengt Oelmann, and Youshi Xu, "Spatio-Temporal Noise Reduction algorithm targeting Real-Time Video Processing," In *Proceedings of the International Symposium on Information Theory and Its Applications*, 2000, Hawaii, USA.

[sys5] Håkan Norell, Bengt Oelmann, Mattias O'Nils, "Requirement Analysis of Reconfigurable Hardware Prototyping Platforms for Real-Time Video Applications", In *Proceedings of the 18th IEEE Norchip* Conference, 2000.

[sys6] Håkan Norell, "A prestudy in rapid prototyping for video signal processing algorithms", Master's thesis, Mitthögskolan, Dec. 2000.

[sys7] Bengt Oelmann, Munir Abdalla and Mattias O'Nils, "An all-digital window discriminator for photon counting pixel detectors", In *IEE Electronics Letters,* Vol.37, No.6, March 2001, p.373-4.

[sys8] Mattias O'Nils, Axel Jantsch, "Device Driver and DMA Controller Synthesis from HW/SW Communication Protocol Specifications", *In Design Automation for Embedded Systems*, Vol. 6, No. 2, Kluwer Academic Publisher, 2001.

[sys9] Bengt Oelmann, Kalle Tammemäe, Margus Kruus, Mattias O'Nils, "Automatic FSM Synthesis for Low-Power Mixed Synchronous/Asynchronous Implementation", to appear in *VLSI Design: An International Journal of Custom-Chip Design*, Simulation, and Testing, 2001.

[sys10] Johnny Öberg, Mattias O'Nils, Axel Jantsch, Adam Postula, Ahmed Hemani, "Grammar-based Design of Embedded Systems", *Journal of Systems Architecture*, Elsevier, Vol.47, No.3-4, April 2001, p.225-40.

[sys11] Patric Thelander, *Panoramic X-ray Image Reconstruction - Problem formulation and case study*, Master's thesis, Mid Sweden University, March 2001.

[sys12] Benny Thörnberg, *Ocapi versus SystemC - A case study comparing two specification methods for object oriented hardware design*, Bachelor's thesis, Mid Sweden University, June 2001.

[sys13] Bengt Oelmann, *Design Model for FSM Based on Mixed Synchronous/ Asynchronous State Memory*, Internal report, Mid Sweden University, May 2001.

[sys14] Mattias O'Nils, Munir Abdalla, Bengt Oelmann, *Analysis of Digital Switching in Photon Counting Pixel Detectors*, Internal report, Mid Sweden University, May 2001.

[sys15] Xue Shang, Bengt Oelmann, "A Comparative Study of Low-Voltage Performance of Standard Cell Flip-Flops", Accepted to *8th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2001)*, Malta, 2001.

[sys16] M. O'Nils, B. Oelmann, Y. Xu, T. Zhang, *Adaptive video transmission over heterogenous networks*, Project proposal.

[sys17] Research Profile Proposal - Centre for Multimedia Technology.

[sys18] B. Thörnberg, M. O'Nils, "Analysis of Modeling and Simulation Capabilities in SystemC and Ocapi using a Video Filter Design", Accepted *to Forum on Design Languages*, Lyon, Sept. 2001.

[sys19] M. O'Nils, M. A. Abdalla, B. Oelmann, “Low digital interference counter for photon counting pixel detector”, Manuscript.

This report has been read and acknowledged:

Prof. Kenway Smith

……

This report has been read and acknowledged:

Prof. Åke Öberg

……

This report has been read and acknowledged:

Prof. Trond Ytterdal

……

This report has been read and acknowledged:

Prof. Ingmar Höglund

……

This report has been read and acknowledged:

Prof. Sture Petersson

……