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Experimental Setup for UV-Programming of Floating-Gate MOS Circuits

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Abstract - **In this paper the experimental equipment for UV-programming of floating-gate circuits are presented along with initial results on concurrent UV-programming of digital floating-gate circuits. It is demonstrated that concurrent UV-programming is possible when using real-time reconfigurable gates (Universal Gates). It is also shown that openings in the passivation, enabling UV-programming, works two years after fabrication of the chip.**

I. INTRODUCTION

Circuit implementations of Boolean functions using Linear Threshold Elements (LTE), based on the floating-gate technique, has proven to be efficient in standard CMOS technologies. For example, Shibata et al. [1] have demonstrated that a configurable block of only 22 transistors could represent 512 Boolean functions of eight variables. The work on digital floating-gate circuits has been taken one step further by Berg and Lande, e.g. in [2, 3] by developing techniques for operating them at power supply voltages below the threshold voltages of the MOS devices by offsetting the floating gate voltages using UV-programming. The circuits, called FGUVMOS, have very low-power consumption and reasonable good speed performance [3]. In order to make large scale designs with FGUVMOS, identical LTE-elements used throughout the design are preferred for concurrent one-time UV-programming of the entire chip or wafer. In the work by Aunet a Universal Gate is proposed that can be configured to six different Boolean functions [4].

In this paper we present the experimental equipment set up to perform UV-programming and DC characterization. Having techniques for concurrent UV-programming is crucial in order to enable VLSI integration of gates based on FGUVMOS. For us the overall objective here is to develop UV-programming techniques for concurrent programming of Universal Gates in multi-gate designs.

The outline of the rest of the paper is as follows. Section 2 briefly introduces the UV-programmable floating-gate circuits. Section 3 describes the experimental equipment. In section 4 we present examples of concurrent programming of FGUVMOS gates.

II. FGUVMOS CIRCUITS

A. FGUVMOS Transistors

The floating-gate transistors are implemented in a standard digital CMOS technology. Because each input signal is coupled through a designed capacitance, a double-poly process is preferred for efficient realization of the capacitors.

As the symbols for the n- and p-type FGUVMOS transistors shown in Figure 1a) and c) indicate, the FGUVMOS transistors are composed of two devices: a MOS-transistor and a capacitor. The input signal is applied at the *control gate* (V_{CG}). The MOS-transistor gate terminal voltage (V_{FG}) is during programming set to an offset value. By offsetting the floating gate, the control gate is experiencing a shift in the threshold voltage. The programmed value is stored on the floating-gate thanks to there is virtually no leakage from the floating-gate. During normal operation, the transistors are electrically symmetric with respect to source and drain terminals.

In order to deposit charge on the floating gate, a UV-activated conductance will provide a path from the drain of the transistor to the floating gate. The UV-activated

conductances, denoted G_{UV}, are shown for pMOS and nMOS transistors in Figure b) and d) respectively.

A UV-activated conductance is implemented by an opening in the passivation in a region partially covering the drain and the gate of the transistor. The UV-hole is indicated as a circle in the symbol of the FGUVMOS-transistor. Programming is done by applying the programming voltages (V_+ and V_- in Figure 2b) on the drain-terminals during UV-exposure. For more details on the design of FGUVMOS-transistors please refer to the work in [3].

B. Linear Threshold Elements

Boolean functions are implemented by Linear Threshold Elements (LTE). The LTE:s are implemented by complementary pair of multiple-input FGUVMOS-transistors as depicted in Figure a. Each input signal is coupled by the weight *w* and the weighted input voltages are summed at the floating-gate node. By having the transistors operating in the subthreshold region, the transistor currents can be written as: $I_{DSn} = I_{BEC} \cdot e^{k \cdot e_n}$; $I_{DSp} = I_{BEC} \cdot e^{k \cdot e_p}$ where $k = V_{DD}/(nU_T)$, $e_n = \sum_{i \in N} w_i \cdot (b_i - 1/2)$ and $e_p = \sum_{i \in P} w_j \cdot (1/2 - b_j)$.

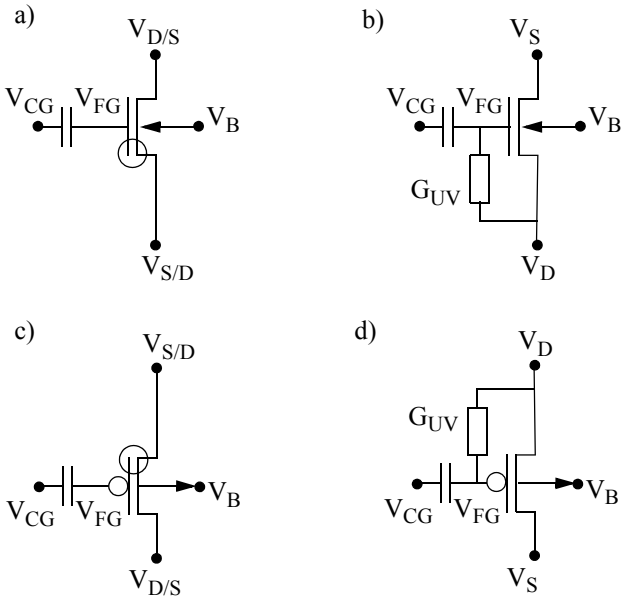

Fig 1: FGUVMOS transistors, a) and b) nMOS, c) and d) pMOS

Where *N* and *P* are the sets of binary inputs to the nMOS and pMOS transistors respectively and I_{BEC} is the transistor currents under the equilibrum condition where the inputs and output are all $V_{DD}/2$. The input signal coupling factor *w* is $C_I/(C_I + C_G)$ where C_I is the design capacitor and C_G is the MOS gate capactiance. The exponents e_n and e_p are used to describe the function of the LTE:

$$out = \begin{cases} 1 \text{ if } & e_p > e_n \\ 0 \text{ if } & e_p < e_n \end{cases}$$

The circuit topology of the floating-gate implementation of Linear Threshold Elements is suitable for UV-programming. As can be seen in Figure , there is a conducting path G_{UV} directly from the power supply lines to the floating nodes. This makes it possible to apply the programming voltages (V_- and V_+) in the programming mode.

C. Universal Linear Threshold Elements

To efficiently do concurrent UV-programming of all gates on the chip, it is preferable that the implementation of all LTEs are identical. In [4] a re-configurable LTE for floating-gate implementation is presented. By having one input, *W*, setting the Boolean function of the gate, the floating-gate voltages can be same for all gates and still having Boolean functions making it a complete logic family.

The gate in Figure 3 can be configured as 3-input NOR ($W=V_{dd}$), 3-input NAND ($W=V_{ss}$), and $\overline{\text{CARRY}}$ ($W=V_{dd}/2$).

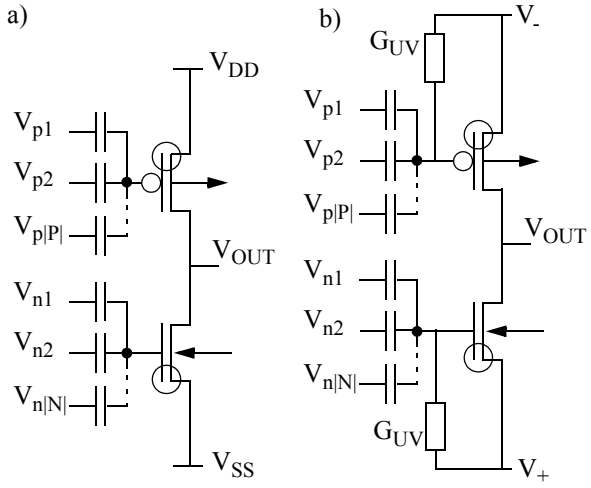

Fig. 2: FGUVMOS LTE; a) in operational mode, b) in programming mode

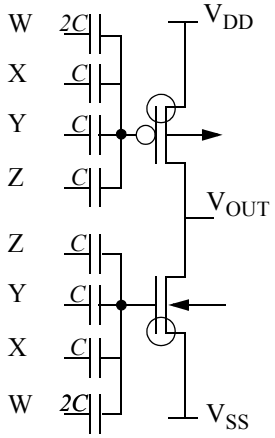

Fig. 3: Function of a Universal LTE (P5N5)

III. EXPERIMENTAL SETUP

The experimental setup was designed to carry out automated UV-programming and DC characterization needed for evaluating the circuits during programming. As shown

in Figure 4, all equipment is contained in a box and the measurment is all computer controlled and accessed through the computer terminal. The electrical requirements are to measure and control low voltages and currents. The circuits are operated at low voltages that are close to the threshold voltages of the MOS devices which means that they always are below 1V. Characterizing single digital gates operating in subthreshold region requires current measurements in the range of pico to nano amperes. As depicted in Figure 5, most part of our setup is built on PCI-based cards, from National Instruments, in the computer.

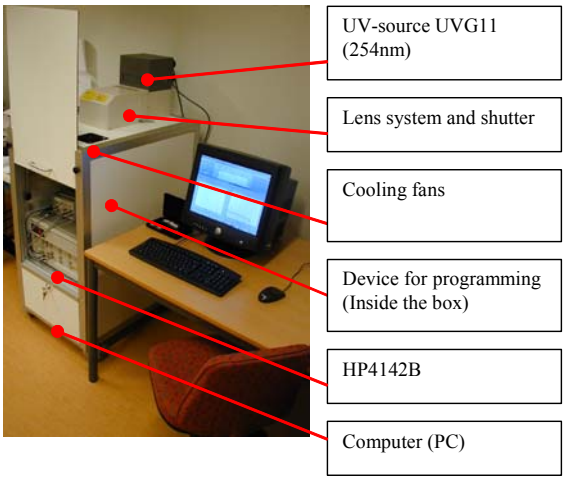

Fig. 4: Experimental setup

The PCI-6704 has 16 voltage and 16 current output channels of 16 bit resultation each. For the voltage channels, the absolute accuracy is maximum +/- 1mV. For voltage measurements the PCI-MIO-16XE50 card is used. It provides 16 input channels of 16 bits resolution each. The input range of the inputs is programmable. For our measurements the input range of +/- 1V is sufficient and gives us the absolute accuracy of 0.28mV. For high-resolution current measurements in the nano-ampere region there is no PCI-card on the market that fulfills the requirements. Therefore we use a GPIB instrument from Hewlett-Packard (HP4142B) that gives us current measurments with a 20fA resolution.

In order to automate the UV-programming, the UV-exposure and cooling of the *device under programming* (DUP) must be controlled from by the computer. The PCI-MIO-16XE50 card has eight digital channels of which two are used for controlling the shutter to the UV-lamp and the cooling fan. The SC-2050 card splits the analog and digital channels where the digital go to the relay box ER-8.

The DUP is mounted on a general testfixture Printed Circuit Board (PCB) that can be used for all test chips in JLCC84 packages. Open lid package is required to make it possible to expose the UV activated conductances. Customization of the testfixture is made by wire-wrap interconnections of the I/Os of the chip to the desired channels. The testfixture is mounted on a shelf inside the box that can be adjusted vertically to vary the distance to the UV-source.

The software for controlling the programming procedures are implemented using LabView from National Instruments. The post-processing and graphical presentation of measurment data is carried out in Matlab that is invoked from the LabView programs.

The implemented UV-programming procedure, that is slightly modified compared to the one described in [2] can be summarized by the following steps:

1. **Set the desired power supply voltage V_{dd}**
2. **Apply the programming voltages at the power supply rails, V_- at V_{dd} and V_+ at V_{ss} and Start UV-exposure.** The supply rails are used to provide the programming voltages and the circuit is then reversed biased.
3. **Terminate the programming by stop the UV-exposure after specified time.**
4. **Set the power supply voltages for normal operation of the gate. Measure the DC transfer characteristics.**
5. **If the switching threshold voltage of the gate is outside the targeted range then adjust the programming voltages and go to step 2.**
6. **Terminate the programming.** The programming is completed when the switching threshold point has converged to the targeted value.

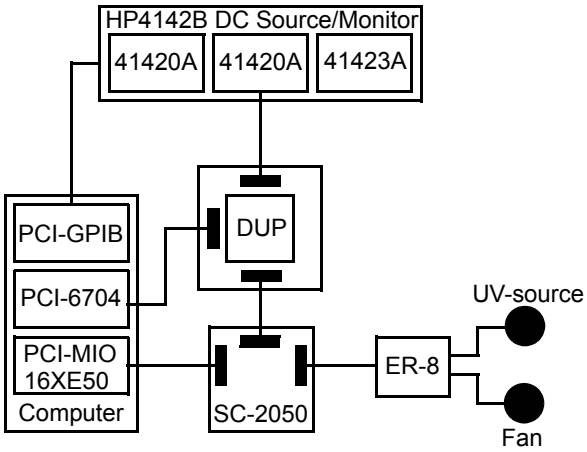

Fig. 5: Programming and measurement equipment

IV. EXPERIMENTS

We have made measurements on a prototype chip and in this paper we present the initial results on concurrent programming of two Universal gates, shown in Figure 3.

The two elements to be concurrently programmed are connected during programming as depicted in Figure 6. All inputs to the first element is shorten and makes it work like an inverter. The output of the first element is fed to the W-input of the second element and will therefore configure the second element. Under normal operation this two-stage circuit is intended to work as a full-adder with the first stage computes the carry ($W=V_{dd}/2$) and the second stage computes the sum of the inputs X, Y, and Z. This is a full-adder based on four transistors only.

In Figure 7, the DC transfer function is shown for the two elements. The gate voltage (V_G) is swept from 0 to V_{dd}, that is 0.8V, and the output of the first element (V_1) is as for an inverter since all inputs are shorted.

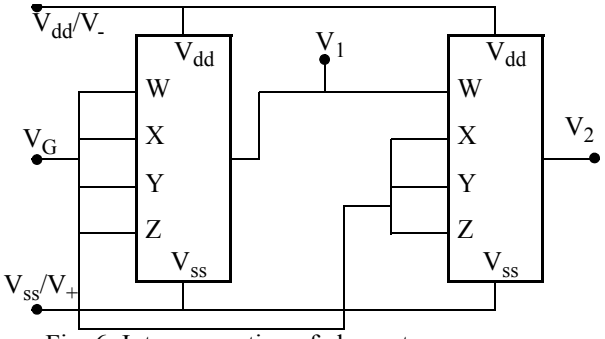

Fig. 6: Interconnection of elements

The function of the second element is configures by the *W*-input. When $W=V_{dd}$ its function is NOR3 and when $W=V_{ss}$ its function is NAND3. From Figure it can be seen that the second element goes low when the input voltage reaches 0.15V which corresponds to one single input voltage of 0.45 that is approximately $V_{dd}/2$. With this switching point the Boolean function is NOR3. As the first element's output goes low, the seceond element will be set to be a NAND3 function. The output of the second element will go low when all inputs are approximately 0.7V which correponds to to the NAND3 function. The output voltage of the first element is here for measured data and the output voltage from the second is computed and shows the expected behaviour of the second element.

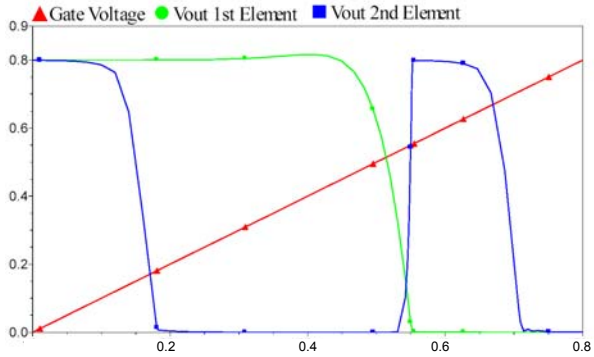

Fig. 7: DC transfer function of the two elements

Figure 8 show the DC characteristics of both first and second elements during programming. Compared to Figure , it can be seen that the DC characteristics of the second does not reach the ideal characteristic.

V. CONCLUSIONS

In this paper we have demonstrated how an experimental setup for automated UV-programming of digital floating-gate circuits is designed. For programming, the FGUVMOS circuits are relying on that the UV-hole remains over time. Our experiments have been carried out circuits stored at room temperature for two years and no degradation with respect to programmability has been observed. We have used it for concurrent programming of two gates. It has been demonstrated that concurrent programming is possible. The measurements revealed that the input signal coupling factor (w) of the gates was to low. In our coming prototype chip the input capacitors (C_I) have been made larger to overcome this problem.

VI. REFERENCES

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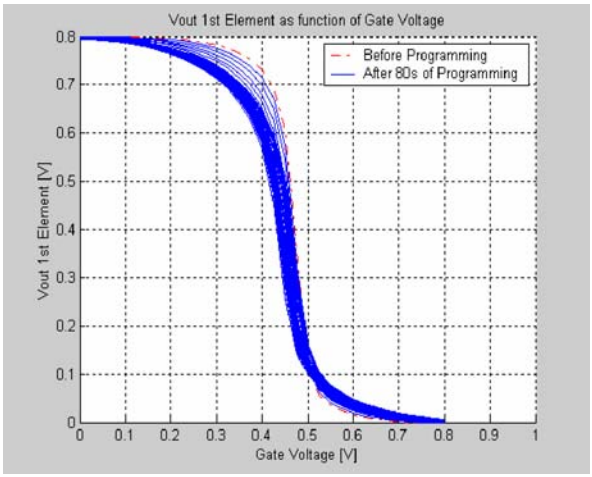
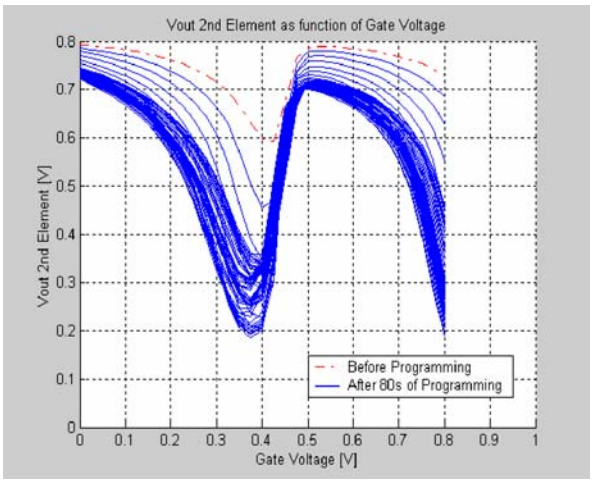


a) Transfer function of the 1st element



b) Transfer function of the 2nd element

Fig. 8: Voltages and currents during programming