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Trading Speed and Power for Reduced Substrate Noise from Digital CMOS Circuits

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Abstract - **In a mixed analogue/digital system, the state-changes of digital circuits generate switching noise that is transferred through the substrate and the power-lines to sensitive analogue nodes. This work investigates how trade-offs with speed and power consumption can be used to decrease this substrate noise. Six different digital CMOS design techniques have been simulated and compared with respect to their trade-off possibilities. The simulations result show how speed and power can be traded for lower digital switching noise by selecting a suitable design technique and power supply voltage.**

Keywords: Substrate noise, noise reduction, switching noise, mixed-signal, low-power, low-noise.

I. INTRODUCTION

In mixed-signal circuits like Analogue-to-Digital converters (ADC) and photon-counting pixel detectors (PCD), the analogue and digital parts are often required to be located closely together. This is mainly caused by two reasons. For ADCs the analogue parts needs to be near the digital parts in order to minimize the amount of injected noise into the wires. In PCDs each pixel has its own analogue and digital parts and the pixels should be as small as possible to get high resolution. This requires the analogue and digital parts to be close. As a result of these requirements, the noise generated from the switching digital parts must be as low as possible. It is impossible to completely avoid the switching noise effects on the analogue parts but they must be reduced as much as possible to be able to meet hard design specifications.

There are several ways that switching noise is spread in a circuit. Through electromagnetic interference, power supply lines and the circuit's substrate. This article has focus on the noise spread in the substrate, substrate noise [1], and how it can be reduced.

There exist several methods to reduce noise already. Guard rings and increasing the distance between circuits are two examples. These methods are not good for mixed-signal applications like ADCs and PCDs because of their need of high circuit density. Instead an application specific choice of circuit design technique can be used to trade-off circuit performance for reduced switching noise. This article gives a comparison of how different design techniques can use trade-offs with area, power consumption, and gate delay to reduce the digital switching noise.

Normally the analogue circuits set the limit to a mixed-signal system's performance and the digital circuits have a lot of over-capacity. This over-capacity gives the designer a margin to do trade-offs with for example power consumption and gate propagation delay against noise. Knowledge about possible trade-offs to achieve reduced substrate noise will be increasingly important when low levels of digital noise is required.

When different circuits on a chip are integrated more and more closely to each other, the substrate cannot be seen as an ideal isolator between them. The substrate is then required to be included as a circuit model in simulations. The substrate is often modelled as an RC-link where the resistive part comes from the doped silicon material and the capacitive parts are originating from the reverse biased p-n junctions between the source, drain or n-well and the bulk substrate [1].

Analysis and comparative studies of certain techniques for low-noise and low-power have been done previously. For example Current Steering Logic (CSL) has been compared with Folded Source Coupled Logic (FSCL) [2]. That paper compares the two logic families with respect to propagation delay and current spikes in the power supply line and it proposes some design guidelines for the techniques. In another article [14], CMOS has been compared to FSCL with respect to switching noise, power-delay product and power supply scaling at high frequencies.

In contrast to previously published work in the sub-

strate noise research field, this article focuses on how design trade-offs with area, power consumption and gate delay can be performed to reduce the substrate noise. The main contribution of this article to this research field is that it shows how a proper choice of design technique together with trade-offs in performance can reduce the substrate noise significantly.

The article is based upon a comparative study of six different circuit techniques. Simulations show that when performance trade-offs are possible, large reductions in switching noise can be achieved with a good choice of design technique.

II. DIGITAL CIRCUIT TECHNIQUES

The digital circuit techniques compared in this article are the most frequently used design techniques for low-power and low-noise. Compared techniques are ordinary static CMOS, Dynamic Threshold CMOS (DTMOS) [4, 5], Current Steering Logic (CSL) [3, 6, 7, 8], Reduced Supply Bounce CMOS (RSBMOS) [9, 10], MOS Current Mode Logic (MCML) [11, 12, 13] and Folded Source Coupled Logic (FSCL) [14, 15, 16]. The circuit topology for digital inverters in these techniques are shown in Figure 1.

A. Method

The comparisons are based on an n-well 0.6µm process technology with an epi-layer substrate. Digital inverter gates have been designed in all the different technologies and the transistors sizes are tuned to achieve approximately equally fast rise- and fall-times (for 3.3V power supply). To get an approximative value of the circuits' areas a layout from each of the inverters have been designed. Of course the circuit's layout and area will be dependent on the designer so it is impossible to determine the area exactly and there is no single circuit layout that is the best. The layouts used in the simulations described in this paper represent a typical designer's layouts and are not optimized with respect to area.

To measure the switching noise, a substrate contact with an area of $1.5\mu m^2$ is placed 10µm from the gate to become a reception point. The potential changes in this contact have then been observed in the simulations as injected substrate noise.

The substrate is modelled with resistive and capacitive couplings that are added to the inverter circuits in Spice. The substrate resistances from all terminal nodes to the reception point and to the grounded bulk are taken into account.

The resistances in the substrate are distributed and to perform simulations in Spice equivalent lumped substrate resistances have been extracted with a program called SubSPACE [19]. The mathematics behind the SubSPACE resistance extraction is described in [17].

In addition to the extracted resistances there are also junction capacitances between the p-doped substrate, the n-well and the doped drain and source terminals. These capacitances have been calculated with the junction

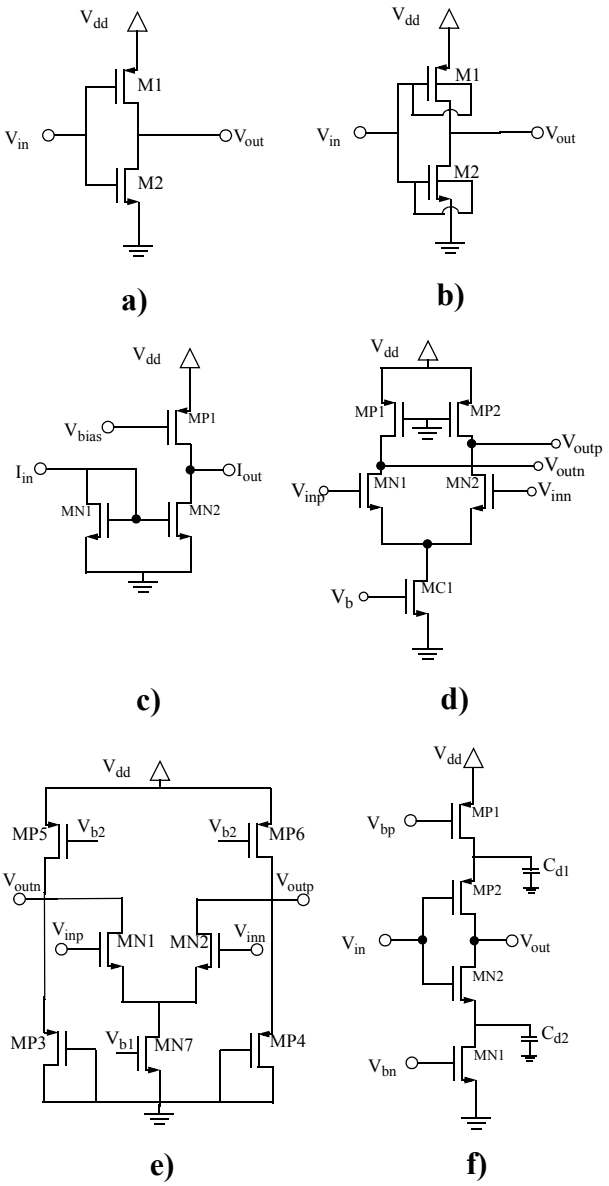

Fig. 1: Inverters implemented in different circuit techniques. a) CMOS b) DTMOS c) CSL d) MCML e) FSCL f) RSBMOS.

capacitance equation and at nodes where the potential varies, the capacitance is integrated between the lowest and highest potential [18].

The circuits including substrate resistances and capacitances have been simulated in Spice. The RC-model used in the simulations has been identical for all the inverters to ensure that simulations results can be compared. Figure 3 shows how substrate resistances and capacitances are connected in the substrate. This model is used in the Spice simulations. R1 and R3 are resistances connected to the grounded bulk and R2 is the resistance between the two terminal nodes. C1 and C2 are the junction capacitances between the n+ doped terminals and the p-epi substrate.

III. SIMULATIONS AND RESULTS

The simulations have been performed in Spice with a 0.6µm process technology on an epi-layer p-substrate. All of the inverters have been simulated with capacitive load

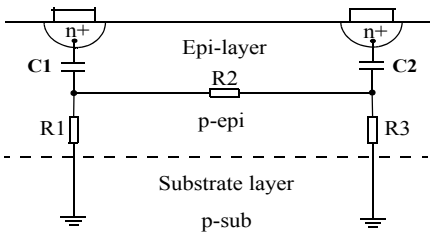

Fig. 2: Substrate model between two terminals.

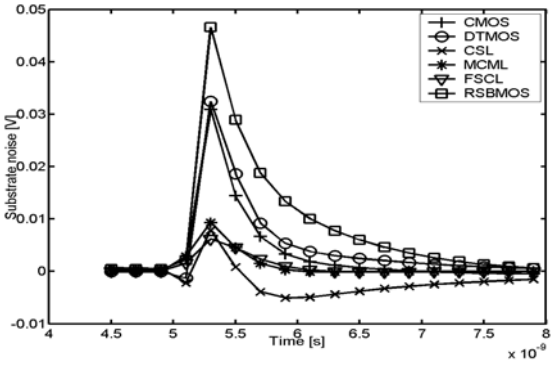

Fig. 4: Positive substrate noise peaks at 3.3V power supply and 10µm distance from the inverter.

of 10fF at the output. The areas of the inverters designed in the different techniques are shown in Figure 3. Performances have then been compared with the performance of a static CMOS inverter.

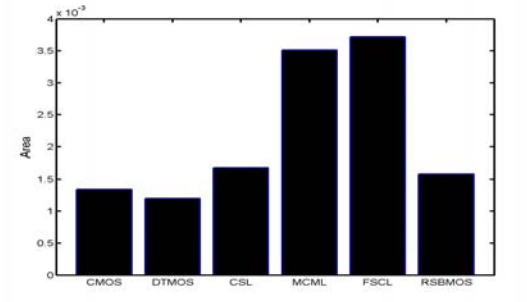

Fig. 3: Inverter area in different techniques.

The Spice simulations show that there are very large differences in digital noise generation between the circuits. Figure 4 shows the positive switching noise peaks at the terminals 10µm away from the circuits when the power supply is 3.3V. As can be seen, the FSCL shows the lowest noise generation and its peak-to-peak substrate noise is less than one sixth of the CMOS peak-to-peak substrate noise. All the techniques do not have the same signal voltage swing and taking into account that the signal voltage swing for FSCL is much lower than for CMOS the noise reduction is less. At 3.3V power supply, CMOS has a signal swing of 3.3V when FSCL has a swing of only 0.76V. The relative substrate noise compared to the voltage swing for FSCL is around 1.35%. For CMOS is that figure 2.07%.

A large advantage of the FSCL and the MCML techniques is that they are differential techniques and have a considerably lower input/output swing than the other logic styles. A disadvantage is that they have static power consumption so they are not suitable for low-power designs at

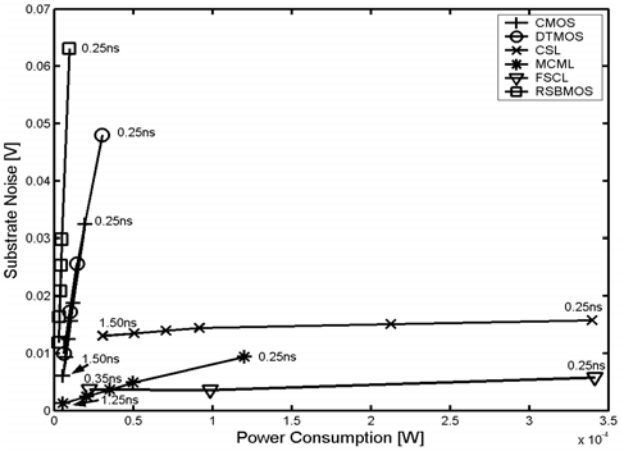

Fig. 5: Substrate noise vs. Power consumption. Gate delay is written as parameter.

low frequencies. At high frequencies, the dynamic power consumption will dominate. The total power consumption will then be comparable to the other design techniques.

To get a good picture of how trade-offs can be made between gate delay, power consumption and the substrate noise, Figure 5 is a plot of how the switching noise varies with the power consumption and the gate delay. The power supply is taken as a parameter that varies between 1.1V - 3.3V and the gate delay variations are between 0.25ns - 1.5ns. Figure 6 shows the plots in the lower regions of Figure 5 more in detail.

The simulations show that several design trade-offs with performance are possible in order to reduce the substrate noise. By looking at the plots in Figure 5 it can be seen that the design techniques mainly form two groups. One group is characterized by low power consumption and very varying substrate noise depending on gate delay (CMOS, DTMOS and RSBMOS). The other group is characterized by high power consumption in combination with quite low substrate noise that does not vary very much with gate delay (CSL, FSCL and MCML).

MCML is a good choice of design technique when the area is of less importance and the circuit should be relatively fast. MCML has considerably lower substrate noise than CMOS, DTMOS and RSBMOS (at the same gate delay) and the power consumption is also less than for FSCL and CSL. This makes MCML a generally good design technique if the performance requirements are not extreme in any direction.

When the switching frequency is not important RSBMOS is a good choice. Then the substrate noise is low in combination with very low power consumption and a small area.

CMOS and DTMOS shows low generated substrate noise if the gate delay is allowed to be larger than around 1ns. This makes them a good choice for circuits that does not have to be extremely fast or low-power consuming.

Where high power supply voltage is required (e.g. 3.3V) and the substrate noise is required to be very low, the FSCL technique is useable. It has high power consumption and a large area but the circuit will be very fast and have low substrate noise.

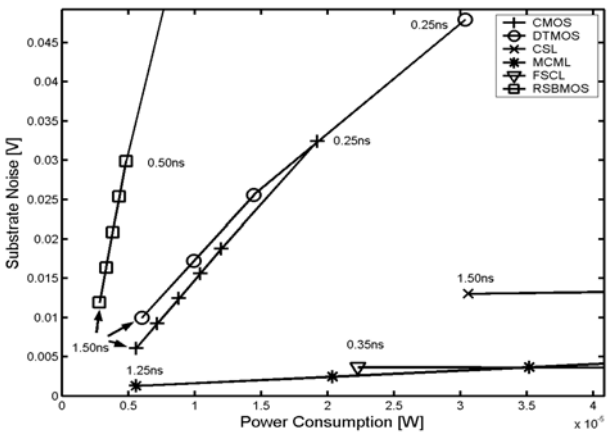

Fig. 6: Substrate noise vs. Power consumption. Detaild plot of Figure 5.

IV. CONCLUSIONS

When considering 3.3V power supply the peak noise voltage for the CSL technique shows the smallest substrate noise relatively to the voltage swing. When power supply scaling is allowed there are possibilities to do design trade-offs and choice of design technique in order to reduce the substrate noise.

In design of mixed-signal systems like an ADC or PCD the knowledge of possible performance trade-offs are very useful. The designs can then be optimized in performance with respect to lower the substrate noise.

This article contributes to extend the knowledge of how circuit area, power consumption and gate delay can be traded-off for a reduction in the substrate noise. The most common digital design techniques for low-power have been compared with. The simulations show that significant reductions in substrate noise can be achieved by selecting the best design technique and power supply under specific design constraints.

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