

Low Power Design of Mixed Synchronous/Asynchronous Finite State Machine

Cao Cao and Bengt Oelmann

PROJECT DESCRIPTION

The motivation of this project is:

- Low power is a primary concern for portable devices to lengthen the battery life. e.g, laptop, mobile phone.
- The Finite State Machine (FSM) almost exists in all integrated circuits and often consumes much power.

The objective of this project is:

- Develop effective algorithm and architecture for FSM low power design.
- Implement the optimization algorithms in a CAD-tool to enable automatic optimization of FSMs.

INTRODUCTION

In a CMOS circuit, generally, the switching activity of the gate output contributes most to the total power dissipation.

For FSM low power design, partitioning technique proves to be effective for reducing switching activity. That is, partition the original FSM into several smaller sub FSMs and only one of them is active at a time.

However, two issues are often introduced:

- Increased area overhead of state memory by separate sub FSM encoding.
- More power consumption by crossing transitions between different sub FSMs in the synchronous design.

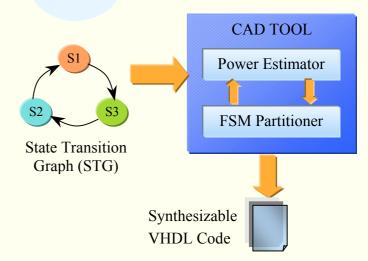
METHODS/THEORY

The project provides a solution towards the problems above:

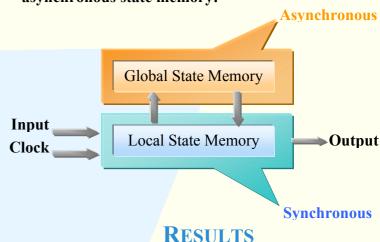
- All sub FSMs share the same local state memory with distinguished codes in the global state memory.
- Asynchronous communication is used for crossing transitions of sub FSMs.

This mixed synchronous/asynchronous design is still behavioural equivalent to the synchronous circuit and thus avoid the complexity of total asynchronous ones.

Flow graph of our tool:



Architecture of the mixed synchronous/ asynchronous state memory:



- Previous related work shows the potential of mixed synchronous/asynchronous design.
- A prototype of this CAD tool has been established from reading STG to create synthesizable VHDL file.
- Final result will be obtained at the end of this year.

FUTURE WORK

- Further algorithm development for power optimisation with area constraint.
- Use the CAD tool for optimising real-world designs such as microprocessor and DSP.