A simple charge sensitive preamplifiers for experiments with a small number of detector channels

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Abstract– **We present a Charge Sensitive Preamplifiers, CSP, based on a very simple design. The CSP consists of an input transistor and a Differential Amplifier, DA, in the second stage. The circuit does not make use of a cascode connection to load the input transistor, to minimize the supply voltage, with a consequent reduction of power dissipation. In addition, only two active devices, a transistor and an Operational Amplifier, are needed where discrete components are used. By exploiting both the inputs of the DA and thanks to a simple resistive network used to load the input transistor, stability, noise and dynamic performances can be met applying a few very simple mathematical rules.**

I. Introduction

Charge sensitive preamplifiers, CSP, are one of the key element of many detector readouts. Different circuit configuration has been suggested for their implementation. The traditional configuration is based on the cascode connection to load the low noise selected input transistor [1], [2], [3], [4], [5]. One simplified schematic of the traditional CSP is shown in Fig. 1. Transistor Q_1 cascodes J_1. The configuration results in single stage. The gain is developed across the impedance of the current generator I_1. The output load is driven by the buffer Q_2. The feedback is closed between the input and the output by capacitance C_F and resistor R_F. A capacitance, C_C, shunts I_1 and is responsible for the dominant pole. Additional poles are present given by the input transistor, located at high frequencies thank to the small input impedance of Q_1, and from the output buffer stage. This single stage amplifier is implemented with a few numbers of transistors. The value and location of the poles determine the stability of the circuit as a function of the detector capacitance. Compensating capacitance C_C must be chosen to accommodate the proper frequency behaviour.

This basic topology has been widely exploited in the implementation of monolithic Si-JFET, Si-Bipolar and CMOS processes [6], [7], [8], [9], [10], [11], as well as in III-V and hetero-structures processes [12], [13], [14].

A very large open loop gain is obtained if the load of the input transistor is amplified by a Differential Amplifier, DA, or a very large gain Operational Amplifier, OA, to form a two stages structure. When this is done the cascode connection is often missed, to avoid voltage shifts. Dynamic performance and the second stage noise deserve particular attention in this case. Such kind of solution has been already studied [15], [16]. Fig. 2 is the simplified diagram of the two stages CSP. Also for this case we included the compensation network composed of R_C and C_C, that is necessary to compensate for the poles due to the input transistor and to the DA.

In this work we present a new solution for the frequency compensation of the two stages CSP of Fig. 2, having the DA in the last stage of amplification. By exploiting the two inputs of the DA and a network composed of four resistors we will show that it is possible to select properly the working condition of the CSP for both concern noise and dynamic performances.

In the following section we will illustrate the principle of operation of the circuit solution and the experimental results obtained.

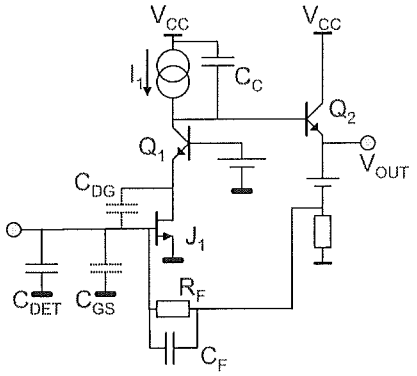

Fig. 1: Traditional CSP circuit configuration.

II. The New Compensation Solution

A. The standard compensation of the 2-stages CSP

Let's begin by analyzing the loop gain of Fig. 2. The Return Path, RP, of the network around the DA is, at frequency greater than $1/C_C R_C$, given by:

$$\frac{1}{RP} \approx -\frac{C_F + C_{DET} + C_{GS} + (1 + g_m R_C) C_{DG}}{C_F} \frac{1}{g_m R_C}. \quad (1)$$

In the above eq. g_m is the trasconductance of J_1 and the presence of the input pole of J_1 has been neglected, supposed to be located at frequency large enough (at first approximation

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$g_m/(C_F+C_{DET}+C_{GS}+C_{GD})$). The loop gain is the product, T, of RP and A(s), the open loop gain of the DA:

$$T = RP\,A(s). \quad (2)$$

As known, in closed loop condition the gain is proportional to the term -T/(1-T), and the divergence of the CSP is avoided, and stability is guaranteed, if the phase spread of RPA(s) is smaller than π (normally less than $3\pi/4$ is the limit considered) at the frequency where |RPA(s)|=1. This condition can be met if |1/RP| is much greater than 1, that implies |A(s)| large, with a consequent small spread of the phase of A(s), that degrades with frequency. Unfortunately the speed of response of the CSP slows down when 1/RP is large. A compromise has therefore to be found.

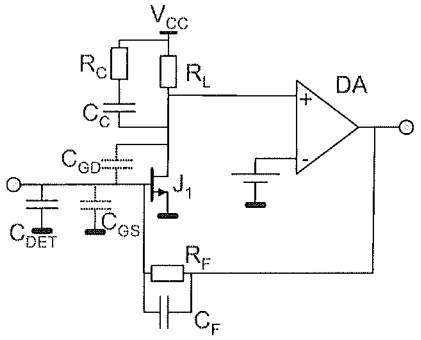

Fig. 2: Schematic diagram of the two stage CSP.

We can see a practical example for illustrative purpose. Let's consider the JFET J_1 of Fig. 2 able to match a detector having a dynamic impedance of about 500 pF. TABLE I shows a hypothetical conditions for the set-up.

TABLE I:
Set-up parameters for an example calculation.

C_{GS} (pF)	C_{GD} (pF)	g_m (mA/V)	C_{DET} (pF)	C_F (pF)
350	210	150	500	500

In Fig. 3 the plots of |A(s)| and |1/RT| are shown. Simulation has been carried out using Symbolic Math®[1] from MatLab. The interception of the two curves results in the unity value for the loop gain. At this frequency the phase, also shown in Fig. 3, is asked to have covered a span smaller than π. In Fig. 3 an OP27 has been considered as DA. An additional pole has to be added given by the presence of a finite value for the output impedance of the OP27, about 50 Ω, and the capacitance in series with it. Compensating capacitance C_C and resistance R_C of Fig. 2 has been set to 200 nF and 15 Ω respectively. This way at frequencies large enough the inverse of the return path rises to about 1.8, allowing the phase margin to become 45° at |T|=1. If the compensation were not set the value of 1/RP had the value of 0.43 and the network break into oscillation due the presence of the three considered poles. The noise of the DA adds to the input series noise with an attenuation factor that is only 2.25 V/V ($=g_mR_C$) at large frequencies. The preamplifier works well, but two limitations must be addressed. It is necessary to take care of the contribution to the input noise from the DA at high frequencies. This reflected noise does not depend on the trasconductance of J_1, above certain limits, since the product g_mR_C has un upper limit for stability requirements.

[1] Symbolic Math is a trademark of The MathWorks, Inc.

B. The new compensation network for the 2-stages CSP

We tried to avoid the limitation at large frequencies of the compensation network of Fig. 2. To do this we have exploited both the inputs of the DA. The resulting network is shown in Fig. 4. Resistors R_C and R_D take a fraction of the voltage developed across R_A and R_B to the inverting node of the DA.

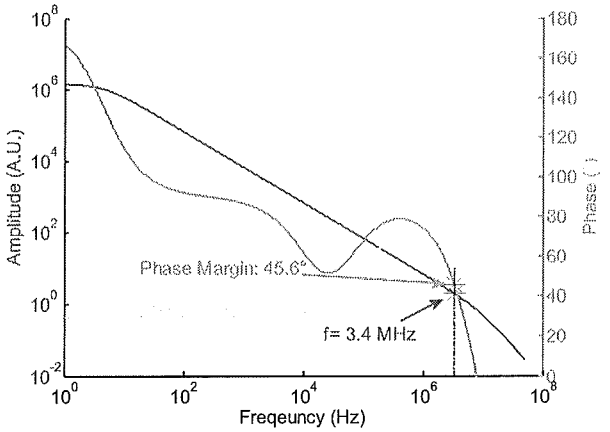

Fig. 3: Magnitude of |A(s)| (continuous line) and |1/RT| (dashed line) (left axis) and phase of A(s)RT (right axis) for the CSP of Fig. 2.

So far, the signal current of J_1 is made partially common mode. DA differential input is given by:

$$V_+ - V_- = -\left[R_B + \frac{R_A R_C}{R_A + R_C + R_D}\right] g_m V_i = -R_{Eq} g_m V_i. \quad (3)$$

We have that R_{Eq} is not equal to the impedance that loads the drain of J_1. This impedance, responsible for the Miller effect, is instead:

$$R_{Miller} = R_B + R_A \| (R_C + R_D). \quad (4)$$

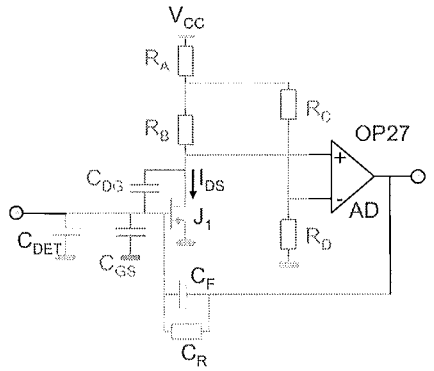

Fig. 4: The CSP of Fig. 2 with the new compensating network.

A noticeable difference in the return path is now obtained from (3) and (4). Eq. (1) now changes to:

$$\frac{1}{RP} = -\frac{C_F + C_{DET} + C_{GS} + (1 + g_m R_{Miller}) C_{DG}}{C_F} \cdot \frac{1}{g_m R_{Eq}} \approx \frac{C_{DG}}{C_F} \frac{R_{Miller}}{R_{Eq}} \quad (5)$$

The feedback capacitance C_F and the JFET characteristics can be chosen to match the detector performances and the experimental requirements, while the stability conditions can be satisfied by setting the proper ratio R_{Miller}/R_{Eq} from (3) and (4).

Moreover, we have two further degrees of freedom in selecting the four resistors that connect the drain of J_1 to the DA inputs. We can exploit them to determine the biasing drain current, I_{DS}, and the drain to source voltage, V_{DS}, of J_1. This can be done by considering that at DC, due to the large gain, $V_+ \approx V_-$. Solving the DC condition we get:

$$I_{DS} = \frac{R_C}{R_A R_C + R_B (R_A + R_C + R_D)} V_{CC} \qquad V_{DS} = \frac{R_B R_D}{R_C} I_{DS} \quad (6)$$

From (6), (3) and (4) we can solve for the 4 resistors as a function of the DC and dynamic constraints:

$$R_A = \frac{V_{CC}(R_{Miller} - R_{Eq})}{(R_{Miller} - R_{Eq}) I_{DS} + V_{DS}} \qquad R_B = \frac{R_{Eq} V_{DS}}{(R_{Miller} - R_{Eq}) I_{DS} + V_{DS}}$$

$$R_C = \frac{V_{CC}(R_{Miller} - R_{Eq}) I_{DS} R_{Eq}}{[(R_{Miller} - R_{Eq}) I_{DS} + V_{DS}]} \cdot \frac{1}{V_{CC} - V_{DS} - R_{Miller} I_{DS}} \qquad R_D = \frac{V_{CC}(R_{Miller} - R_{Eq})}{V_{CC} - V_{DS} - R_{Miller} I_{DS}} \quad (7)$$

From (7) a broad range of conditions can be satisfied. There is only an upper limit on the Miller resistance:

$$R_{Miller} < \frac{V_{CC} - V_{DS}}{I_{DS}} \quad (8)$$

The expression for RP in (5) says that the frequency response of the circuit can be fitted with a very large choice. We have to limit the possible range by imposing adequate noise performances. The noise of the DA is reflected to the CSP input with an attenuation of $g_m R_{Eq}$. An adequate large value for this resistor allows minimizing the DA contribution. Since the dynamic performance is dependent on the ratio R_{Miller}/R_{Eq} we can increase this ratio trying to maintain R_{Eq} at an adequate value. Let's consider again the example specified in TABLE I. We set a bias voltage, V_{DS}, and channel current, I_{DS}, at 3 V and 5 mA respectively for our JFET and the supply voltage, V_{CC}, equal to 10 V. Then we select R_{Miller} of 1 KΩ and R_{Eq} of 100 Ω. The result shown in Fig. 5 is obtained with a phase margin of about 63°. The value of R_A is 1200 Ω, that of R_B 40 Ω, R_C 300 Ω and R_D 4500 Ω. Fig. 6 shows the simulated impulse response. As can be seen the expected overshot is about 4.5 %. A CSP has been developed having the characteristics of TABLE I. The input JFET used to match the detector were a parallel combination of two SNJ3600 from Interfet, that results, at the considered operating point, in a trasconductance, g_m, of about 0.15 A/V, and channels capacitances C_{GS}=350 pF and C_{GD}=208 pF, as measured with the technique described in [17]. Impulse response of the implemented CSP is in Fig. 7. The result is consistent with the simulation.

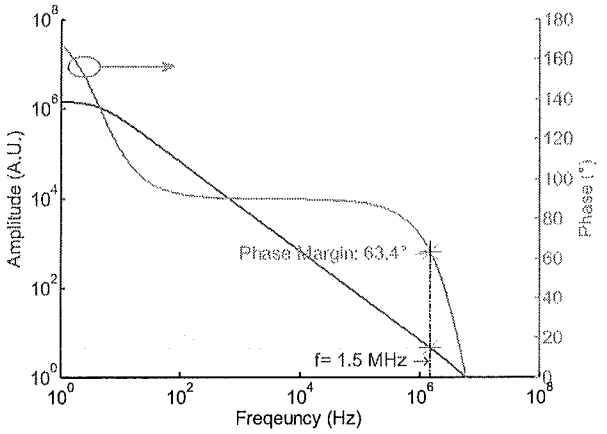

Fig. 5: Magnitude of |A(s)| (continuous line) and |1/RT| (dashed line) (left axis) and phase of A(s)RT (right axis) for the CSP of Fig. 4.

The proposed compensation technique allows obtaining a good frequency response with a large reduction coefficient of the noise of the DA.

A complete analysis implies the study of the noise coming from the network resistors and the parallel noise of the DA. The calculation of the contribution to the input series noise coming from the parallel noise of the DA is:

$$\overline{e_{iPar}^2} = \frac{1}{g_m^2}\left\{\overline{i_+^2} + \frac{1}{R_{Eq}^2}\left(\frac{R_C R_D}{(R_A + R_C + R_D)}\right)^2 \overline{i_-^2}\right\} \approx \frac{\overline{i_+^2}}{(g_m R_{Eq})^2}\left\{R_{Eq}^2 + \left(\frac{R_C R_D}{(R_A + R_C + R_D)}\right)^2\right\} = R_{NoPa}^2 \overline{i_+^2} \quad (9)$$

The latter two approximations in (9) are valid if the two noise sources $\overline{i_+^2}$ and $\overline{i_-^2}$ have similar statistic. For the example at hand R_{NoPa} is bout 16 Ω, a very good figure.

A rather long calculation for the noise contribution to the input series noise from the 4 resistors R_A,.., R_D leads to the simple expression:

$$\overline{e_{i\,Res}^2} = \frac{4K_BT}{(g_m R_{Eq})^2}\left\{R_{Eq} + \frac{R_C R_D}{(R_A + R_C + R_D)}\right\}. \qquad (10)$$

In the above eq. K_B is the Boltzmann constant and T the absolute temperature. The equivalent resistance results 1.45 Ω for the considered example.

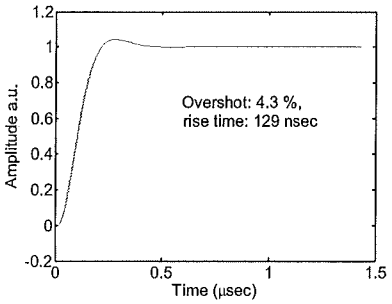

Fig. 6: Simulated impulse response of the CSP of Fig. 4. The feedback resistor R_F has been assumed to have a value ∞ for simplicity.

The input stage of Fig. 4 depends on the value of the supply voltage V_{CC}. It is possible to make the circuit able to increase the rejection to V_{CC} by substituting resistor R_A with the current generator I_{Gen} of Fig. 8. This kind of solution is more affordable in case a monolithic implementation is to be realized for the CSP.

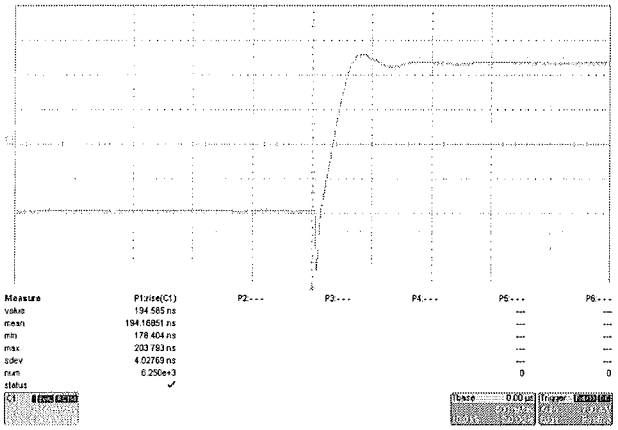

Fig. 7: Actual measured signal for the CSP of Fig. 4 when 2 SJN3600 JFETs are put in parallel with V_{DS}=3 V and I_{DS}=5 mA.

Eqs. (7) undergo to a modification for the arrangement of Fig. 8. Current generator I_{Gen} must supply the biasing current I_{DS} of the JFET and the current that flows in R_C and R_D:

$$I_{Gen} = \frac{(R_{Miller} - R_{Eq})I_{DS} + V_{DS}}{R_{Miller} - R_{Eq}}$$

$$R_B = \frac{R_{Eq}V_{DS}}{(R_{Miller} - R_{Eq})I_{DS} + V_{DS}} \qquad (11)$$

$$R_C = \frac{(R_{Miller} - R_{Eq})I_{DS}R_{Eq}}{\left[(R_{Miller} - R_{Eq})I_{DS} + V_{DS}\right]}$$

$$R_D = R_{Miller} - R_{Eq}\,.$$

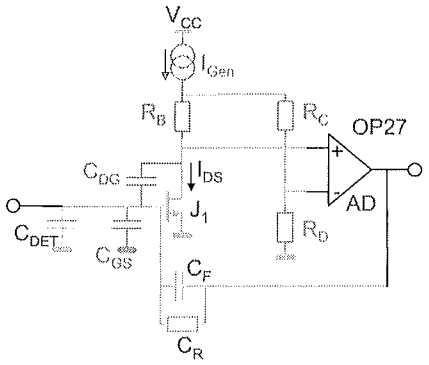

Fig. 8: The circuit solution of Fig. 4 with the current generator I_{Gen} in substitution of resistor R_A, to reject the supply voltage noise.

CONCLUSIONS

A 2-stages Charge Sensitive Preamplifier has been proposed with a novel frequency compensation technique. The circuit solution exploits both inputs of the differential amplifier in the second stage. This way the signal current from the input transistor can be made partially common mode, allowing to obtain a flat frequency response. A control of the value of the gain can be exploited, so minimizing the contribution to the input of the second stage noise. A complete mathematical analysis of the frequency response and the noise performances has been carried out and was confirmed by experimental results.

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