Chapter 13
Process Integration

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Objectives

- List three isolation methods
- Describe sidewall spacer process and application
- Explain the V_T adjustment implantation
- Name three conductors used for MOSFET gate
- List three metals used for interconnection process
- List basic steps for copper metallization process
- Identify the material most commonly used as final passivation layer for an IC chip

Introduction

- It takes up to 30 masks and several hundreds process steps to finish an IC chip fabrication.
- Every step is related to other steps.
- CMOS processes
  - Front-end:
    - well formation, isolation, and transistor making
  - Back-end
    - Interconnection and passivation

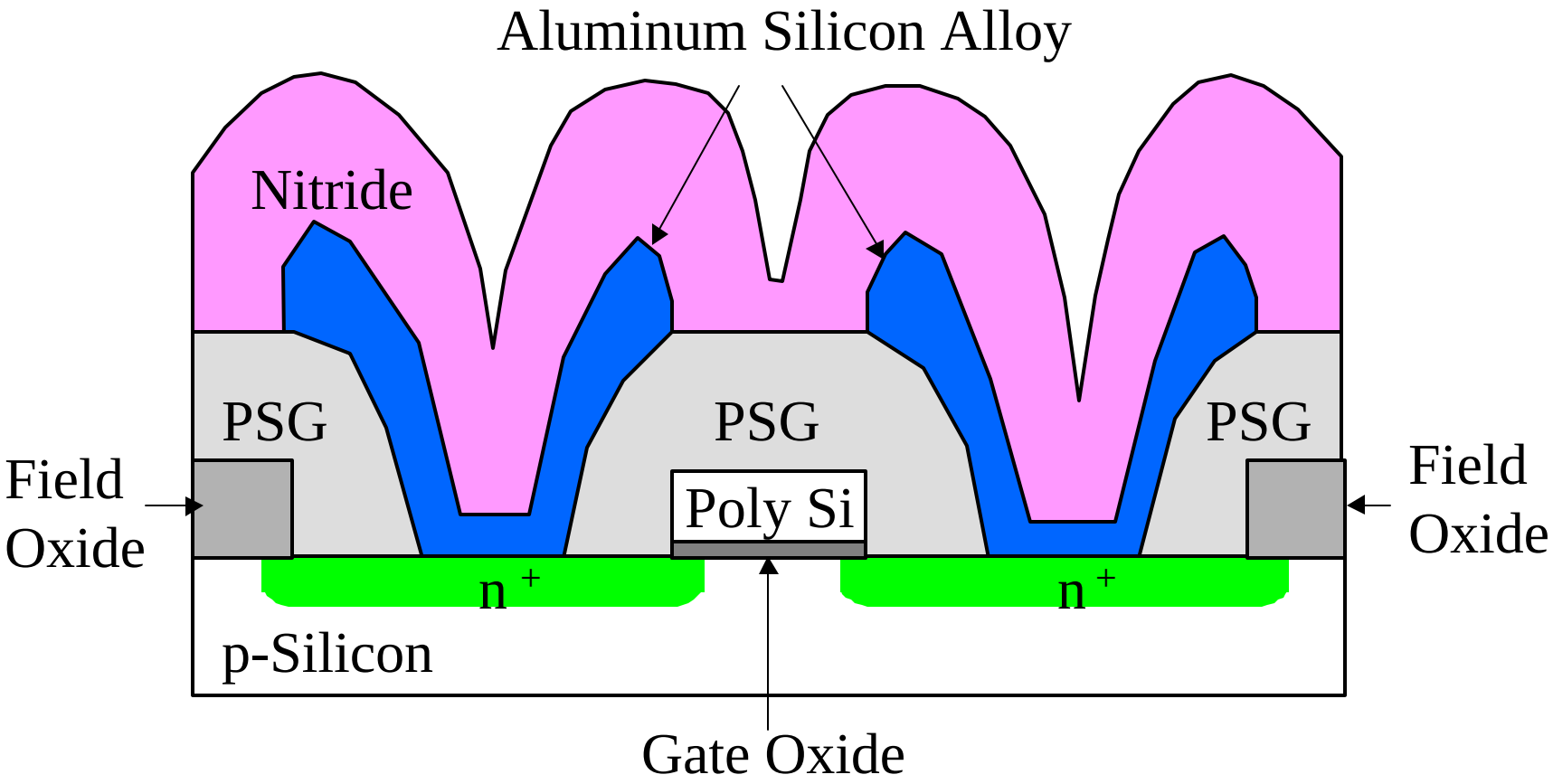
Wafer Preparation

- CMOS IC chips commonly used <100> wafer
- Bipolar and BiCMOS chips usually use with <111> wafers orientation.
- 1960 to mid-1970s, mainly PMOS, n-type wafer
- After mid-1970s, mainly NMOS, p-type wafer
- CMOS developed from NMOS process, for historical reason more fabs use p-type wafer

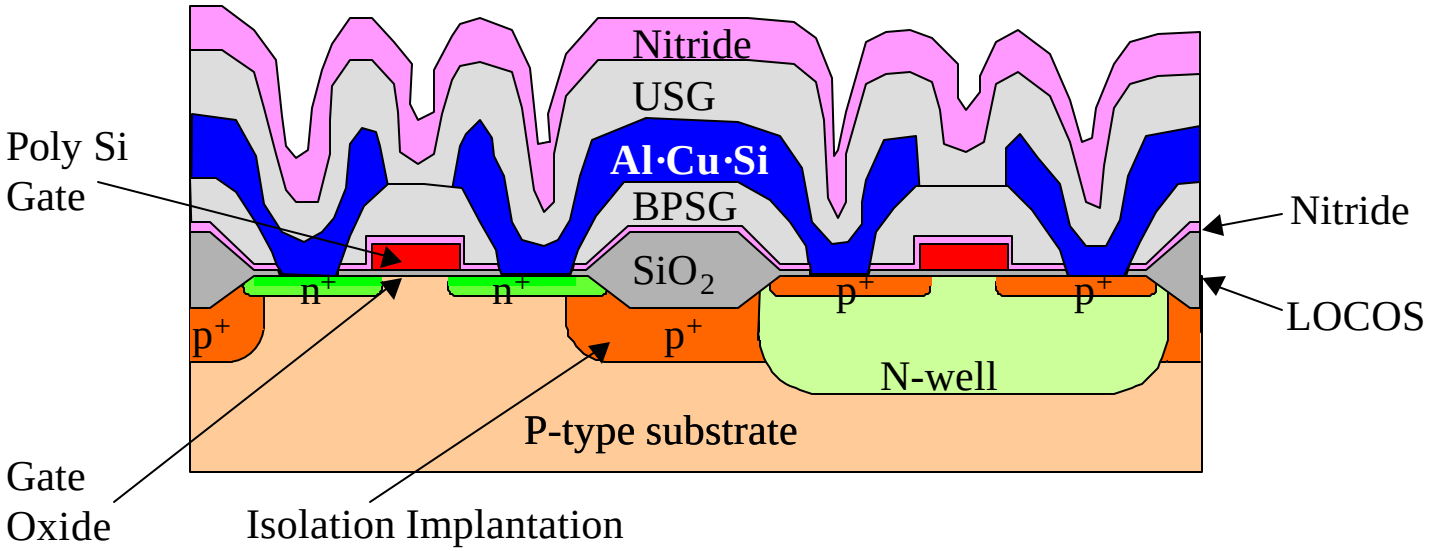
NMOS and CMOS Processes

- The simplest NMOS IC processing had five mask steps: activation, gate, contact, metal, and bonding pad
- The early CMOS IC processing added three more mask steps: n-well (for p-type substrate), activation, gate, n-source/drain, p-source/drain, contact, metal, and bonding pad
- Both processes used p-type wafers

NMOS


Aluminum Silicon Alloy
Nitride
PSG
PSG
PSG
Field
Oxide
Poly Si
Field
Oxide
n +
n +
p-Silicon
Gate Oxide

CMOS of the Early 1980s



Epitaxy Silicon Layer

- Bipolar transistors and BiCMOS chips require epitaxial silicon layer to form a buried layer
  - Some power devices even require wafers made by floating zone method
- When CMOS chip speed is not very high, it doesn’t need the epitaxy layer
- High-speed CMOS chips need epitaxy layer

Epitaxy Silicon Layer

- Silicon wafers made by the CZ method always have some oxygen because quartz crucible
- Oxygen can reduce carrier lifetime and slow down the device
- The epitaxy silicon layer creates an oxygen-free substrate and help to achieve high device speed

Epitaxy Silicon Layer

- RCA clean to remove contaminants
- Anhydrate HCl dry clean helps to remove mobile ions and the native oxide
- Epitaxy growth: high temperature CVD
  - silicon source: SiH_4 or SiH_2Cl_2, or $SiHCl_3$
  - H_2 as process, carrier, and purge gas
  - AsH_3 or PH_3 as n-type dopant gas,
  - B_2H_6 as p-type dopant gas

Wafers Used for IC fabrication

- Advanced CMOS IC chips normally use p-type <100> single crystal silicon wafers with p-type epitaxial layer
- Bipolar IC chips usually use <111> wafers

Well Formation

- Single well
- Self-aligned twin well
- Double photo twin well

Single Well

- Early CMOS IC processing
- N-well on p-type wafer
- P-well on n-type wafer
- High energy, low current ion implantation
- Thermal anneal and drive-in

N-well Formation

Wafer clean

Screen oxide grow

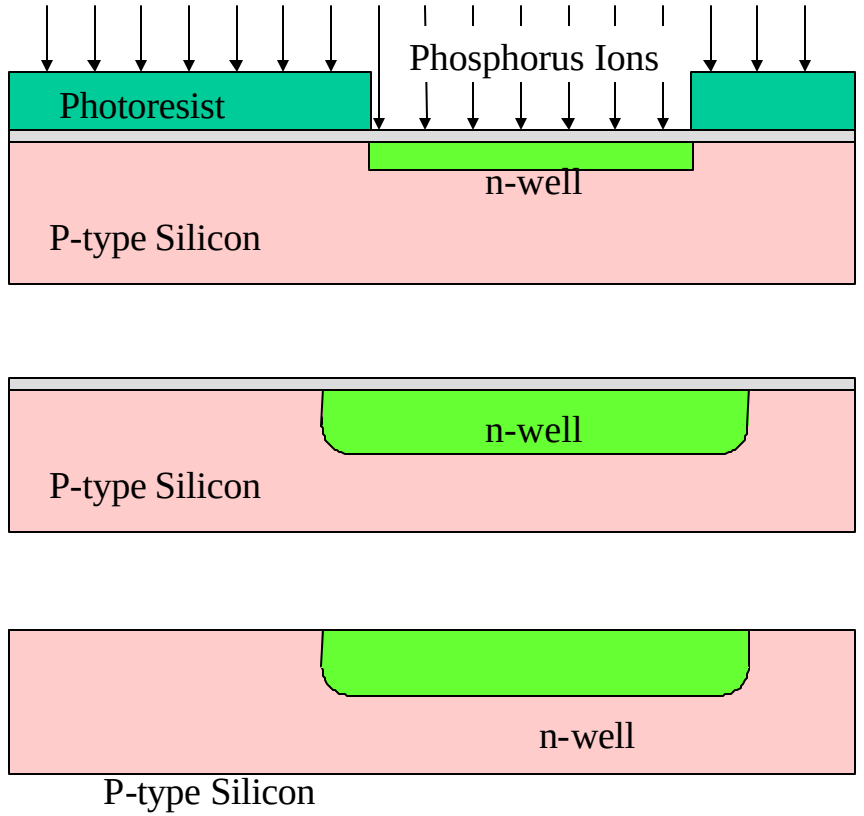
Well mask

Ion implantation (a)

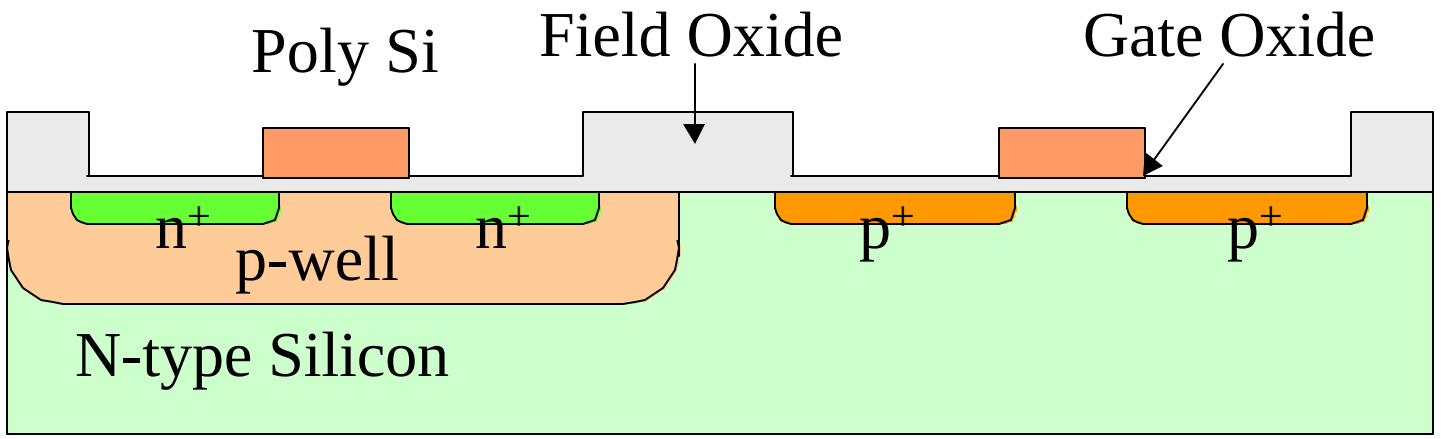
Photoresist strip

Anneal and drive-in (b)

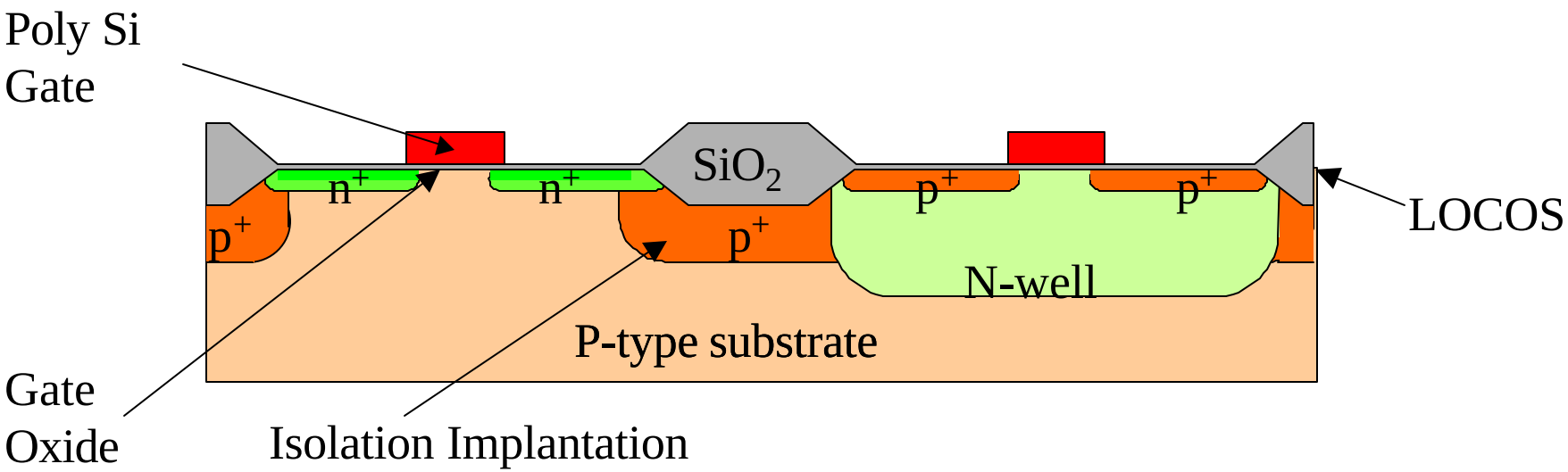
Screen oxide strip (c)



CMOS with P-well



CMOS with N-well

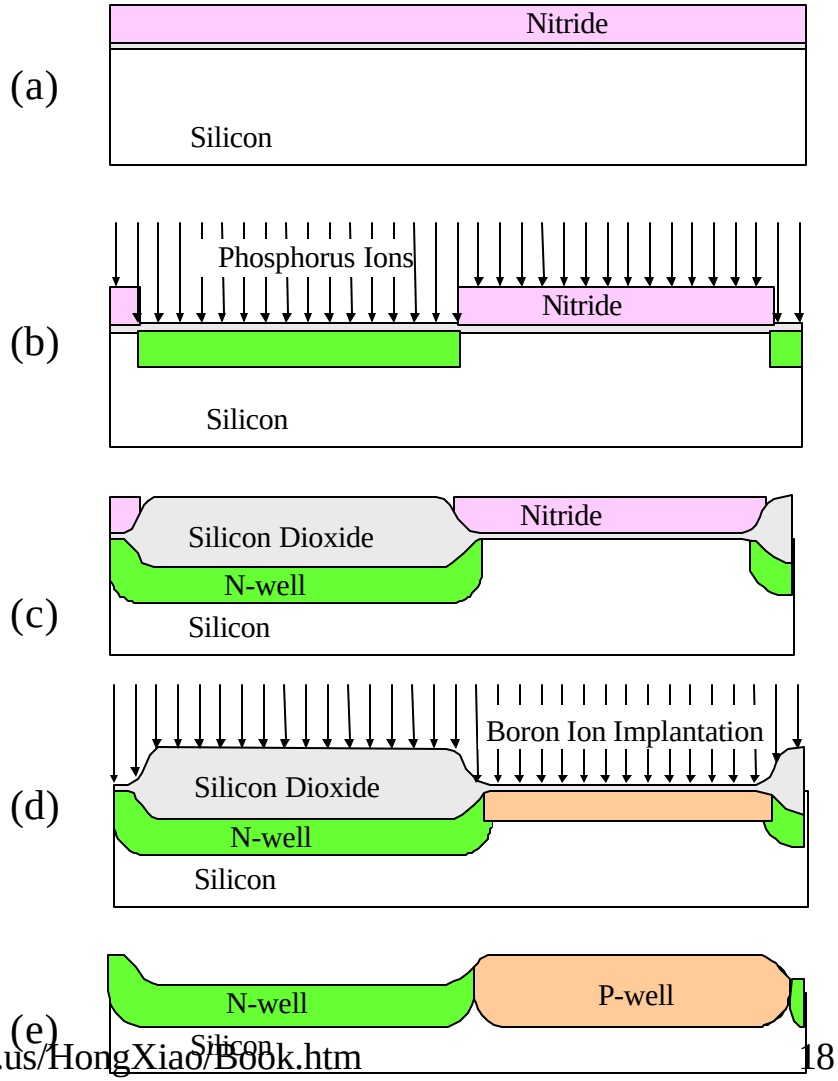


Self-aligned Twin Well

- More flexibility for the designers
- Self-aligned process save a mask step
- LPCVD Si_3N_4 is a very dense layer
- Block ion implantation on p-well
- Prevent oxidation on p-wee
- Oxide grown on n-well block p-well ion implantation

Self-aligned Twin Well

- Wafer clean
- Grow pad oxide
- Deposit nitride (a)
- N-well mask
- Etch nitride
- Strip photoresist
- N-well implantation (b)
- Anneal/drive-in and oxidation (c)
- Strip nitride
- P-well implantation (d)
- Anneal and drive
- Strip pad oxide (e)



Self-aligned Twin Well

- Advantage: reduce a photo mask step
  - Reduce cost
  - Improve IC chip yield.
- Disadvantage: wafer surface is not flat
  - n-well always has lower level than p-well
  - Affect photolithography resolution
  - Affect thin film deposition

Self-aligned Twin Well

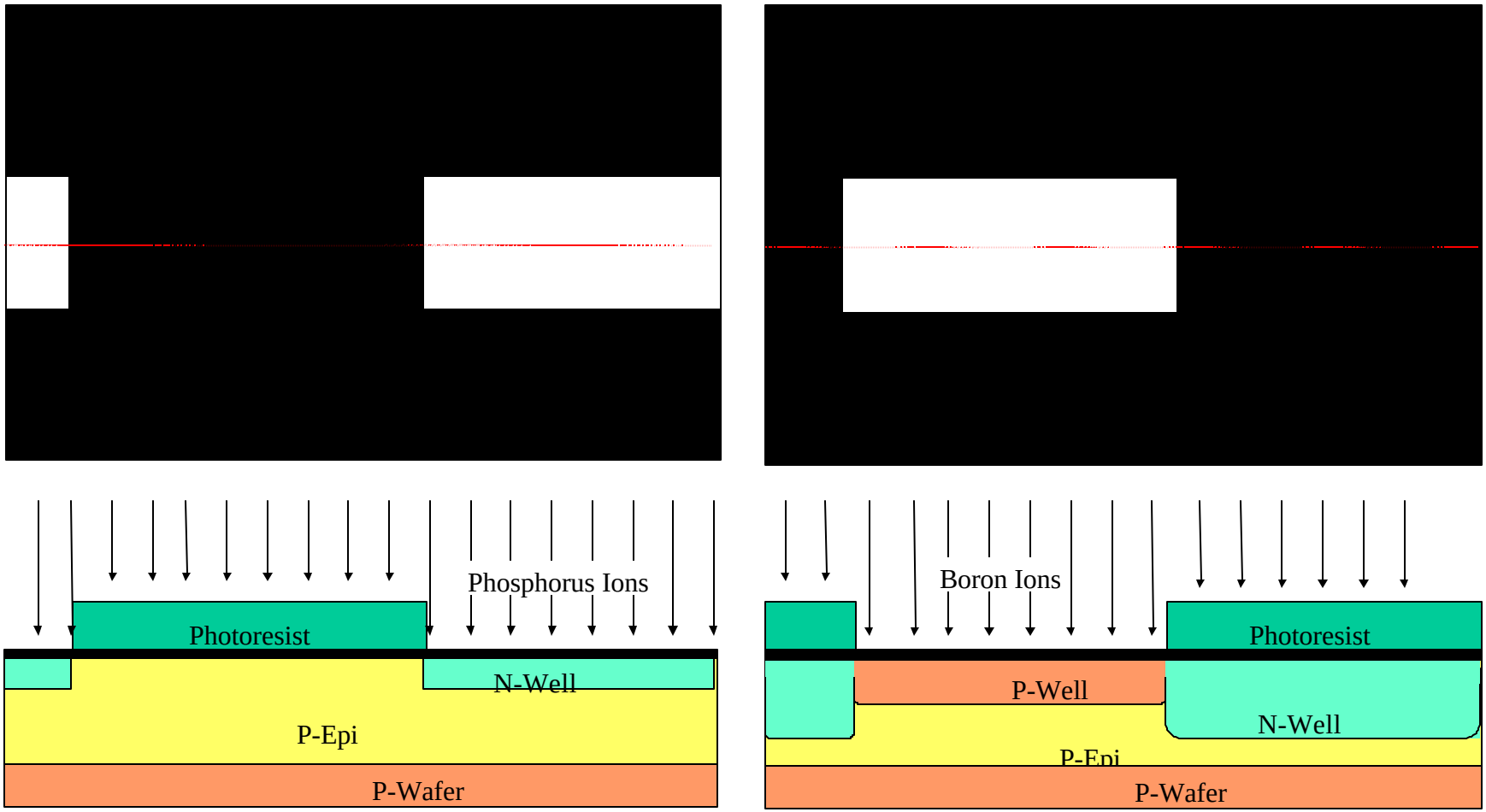
- N-well implant first
- Phosphorus diffuses slower than boron in single silicon
- If p-well implant first, boron in p-well could diffuse out of control during n-well anneal and drive-in

Twin Well

- Two mask steps
- Flat surface
- Common used in advanced CMOS IC chip

- High energy, low current implanters
- Furnaces annealing and driving-in

Twin Well


Phosphorus Ions
Photoresist
N-Well
P-Epi
P-Wafer
Boron Ions
Photoresist
P-Well
N-Well
P-Epi
P-Wafer

Isolations

- Blanket field oxide
- Local oxidation of silicon (LOCOS)
- Shallow trench isolation (STI)

Blanket Field Oxide

- Early years of IC industry
- Simple and strait forward
- Oxidation and etch
- Thickness is determined by V_{FT},
- $V_{FT} >> V$ to prevent cross-talking

LOCOS Formation

Wafer clean

Grow pad oxide

LPCVD nitride (a)

Mask 1, LOCOS

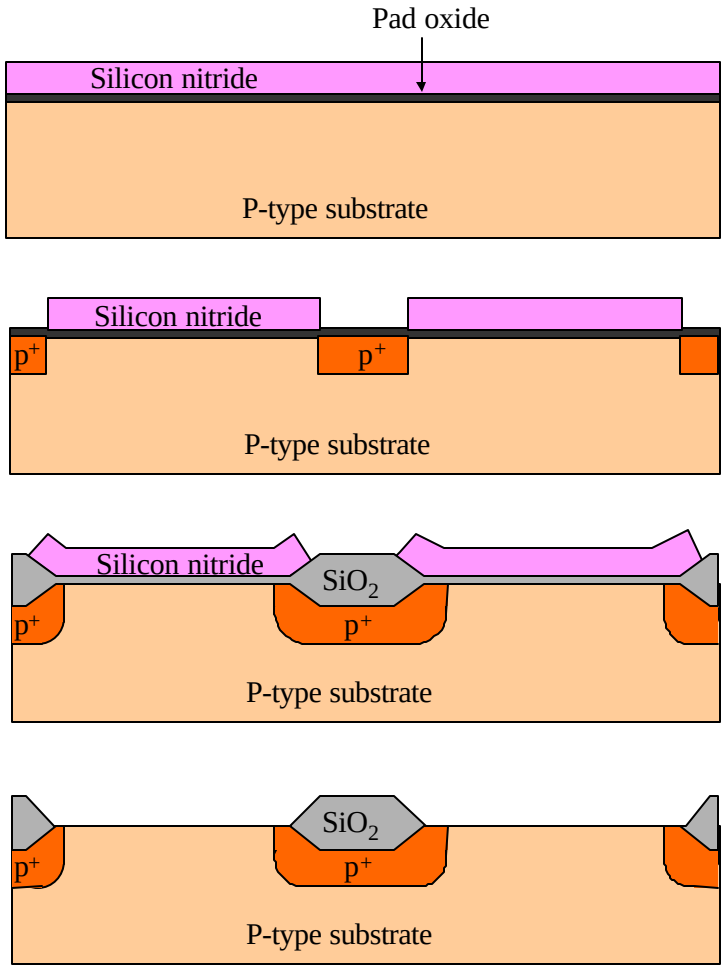
Etch nitride

Strip photoresist

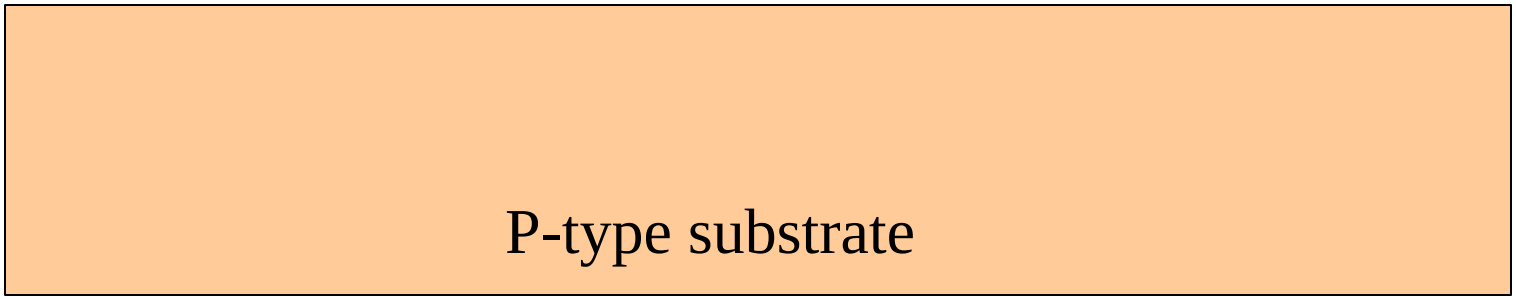
Isolation implantation, boron (b)

Wet oxidation, LOCOS formation (c)

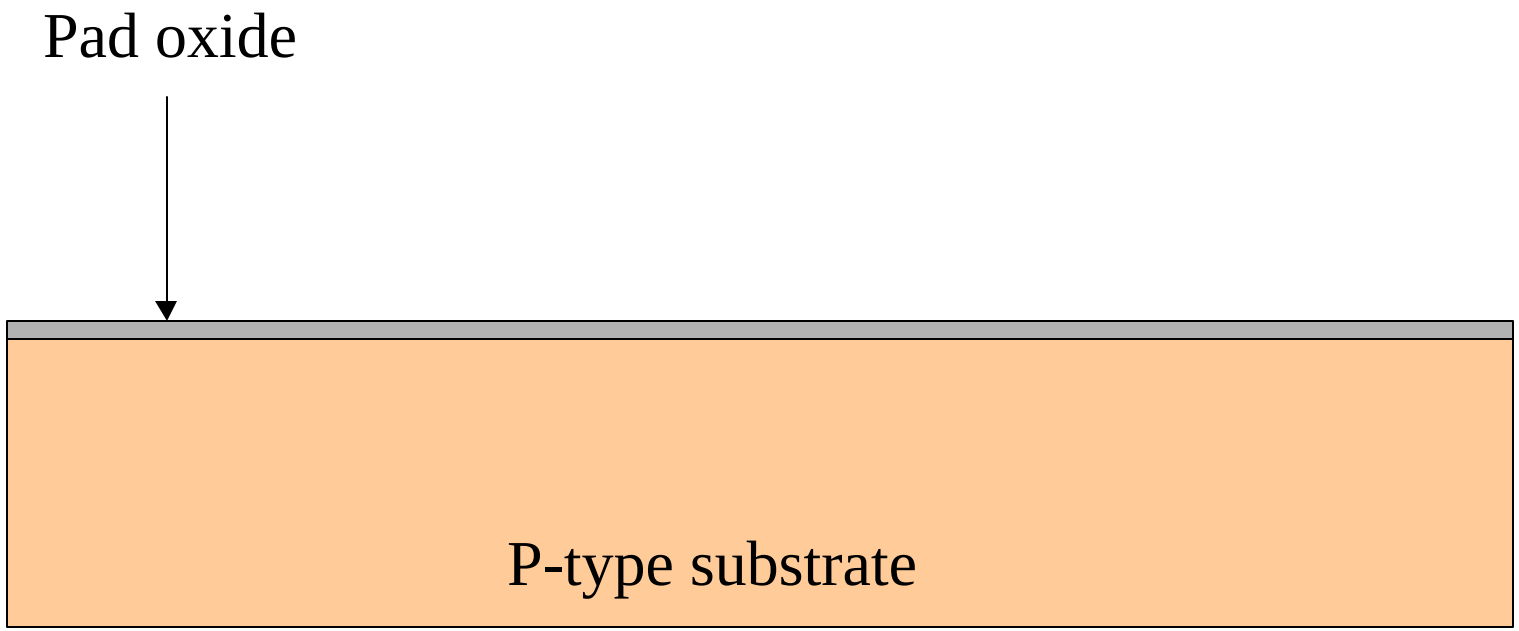
Strip nitride and pad oxide (d)



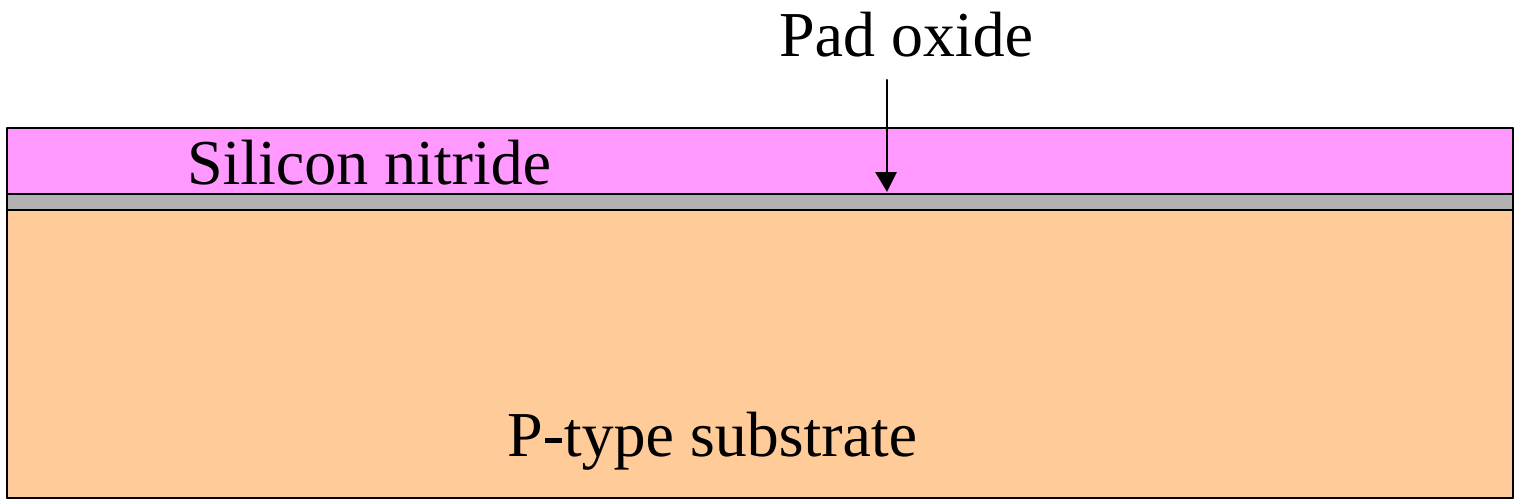
Wafer Clean



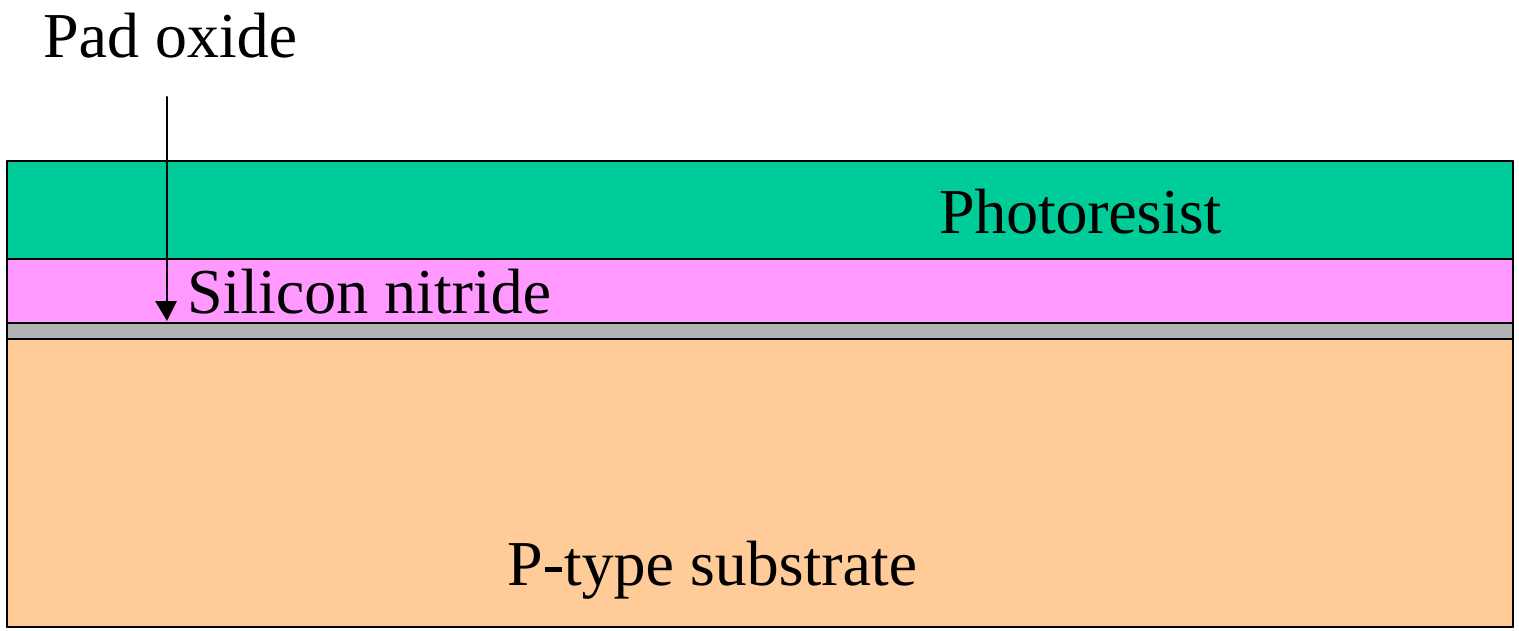
Pad Oxidation



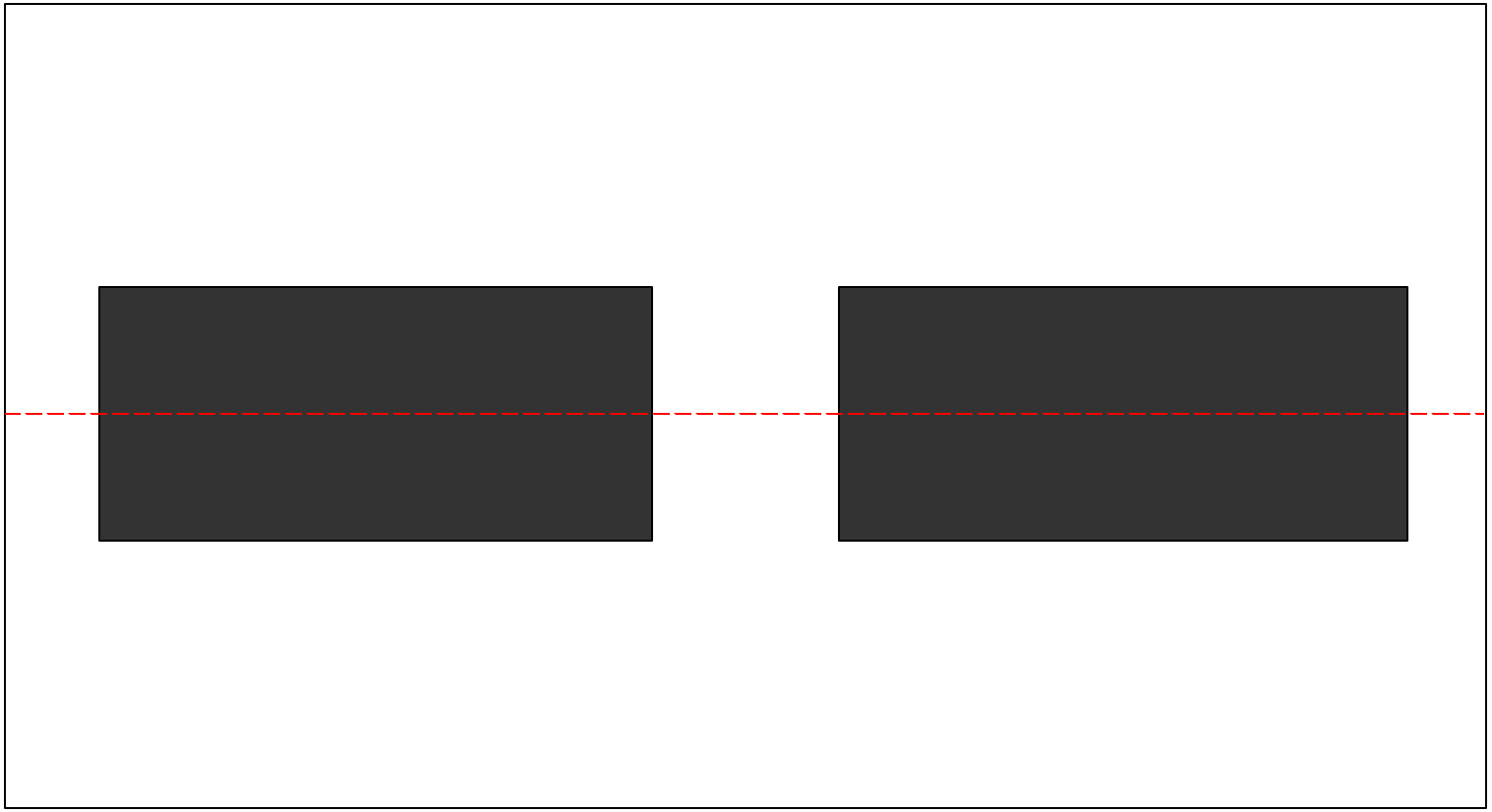
LPCVD Nitride



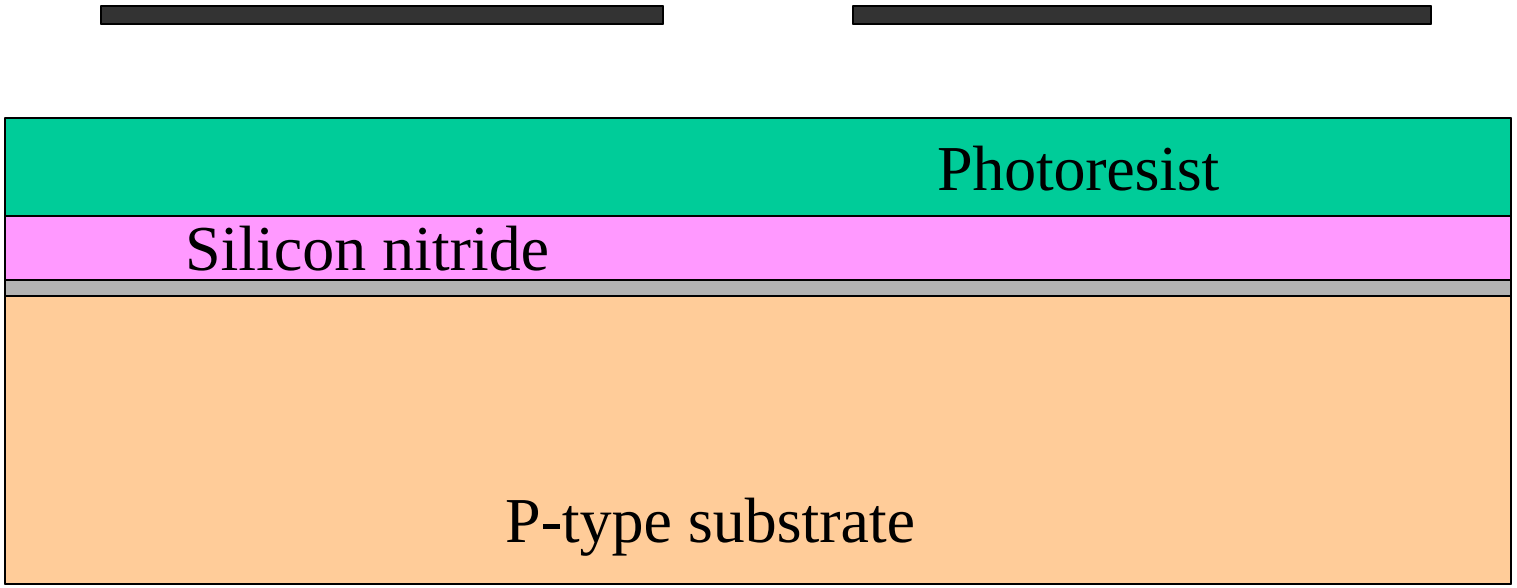
Photoresist Coating



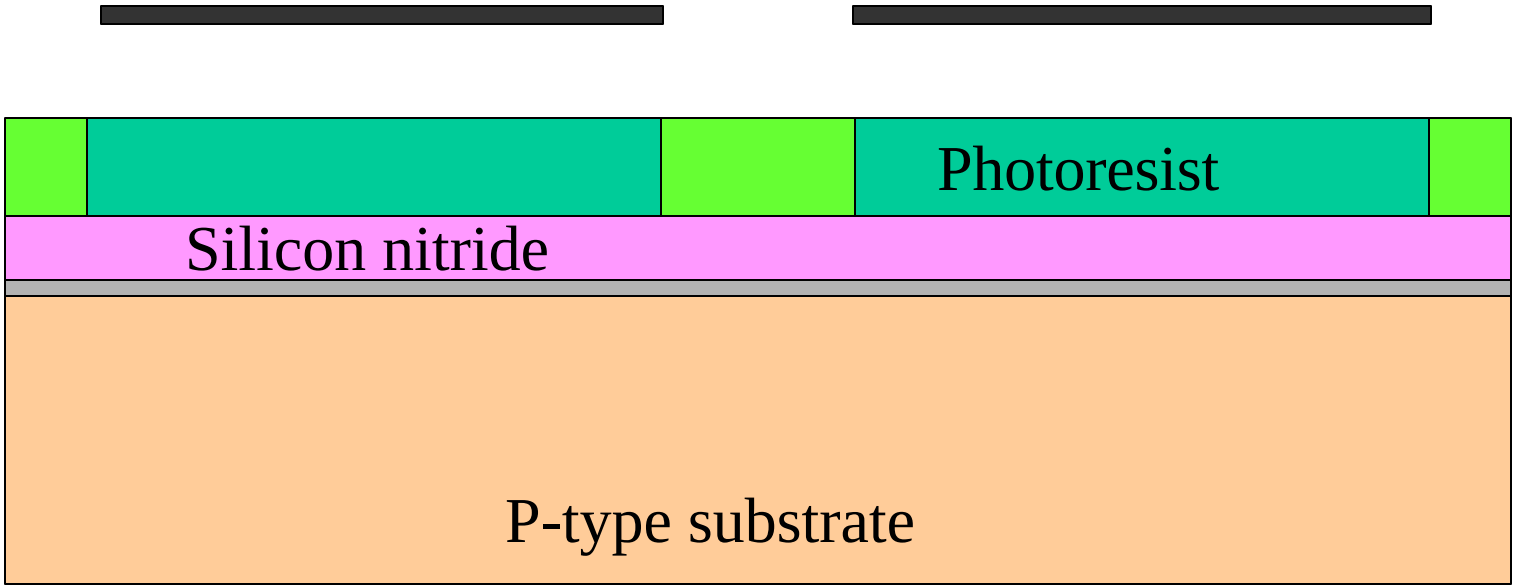
LOCOS Mask



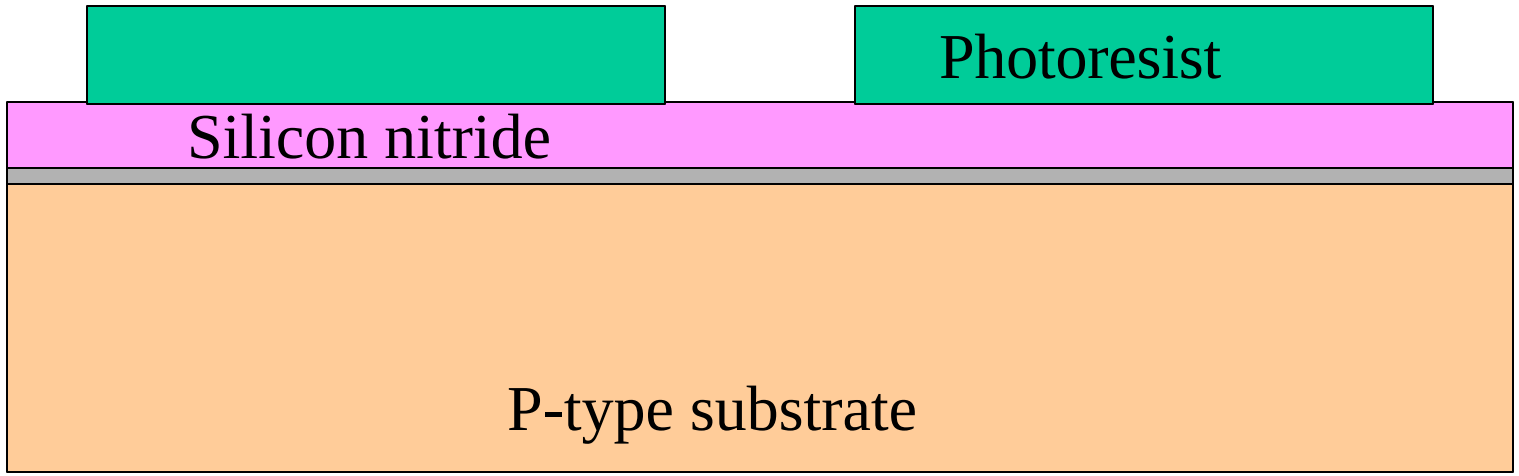
LOCOS Mask



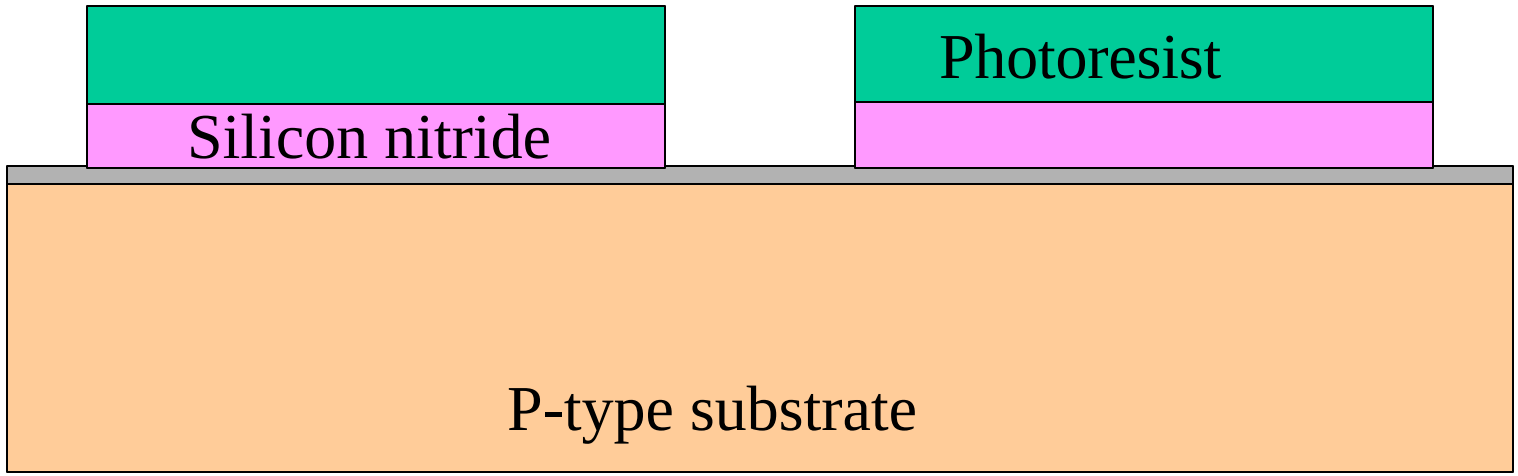
LOCOS Mask Exposure



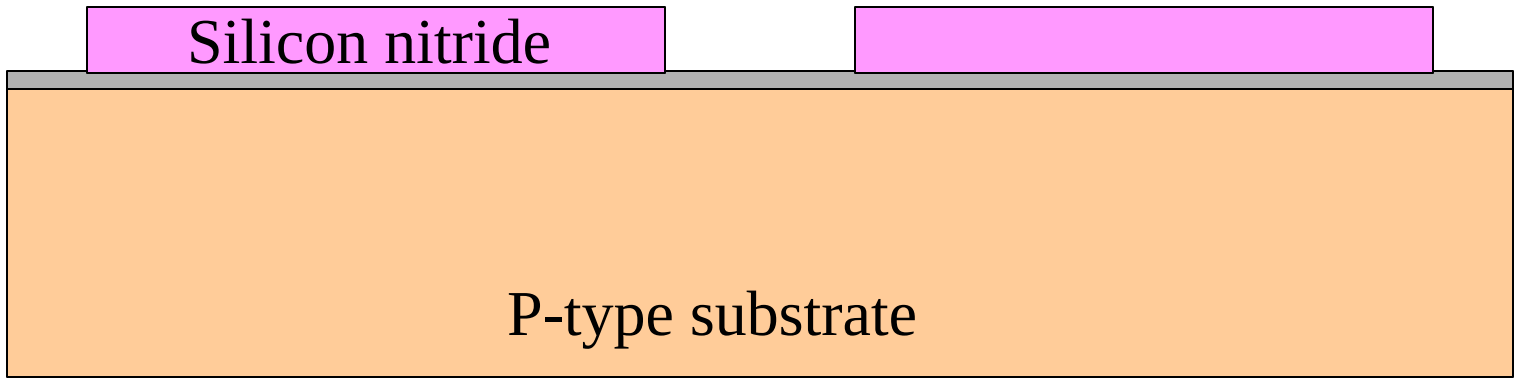
Development



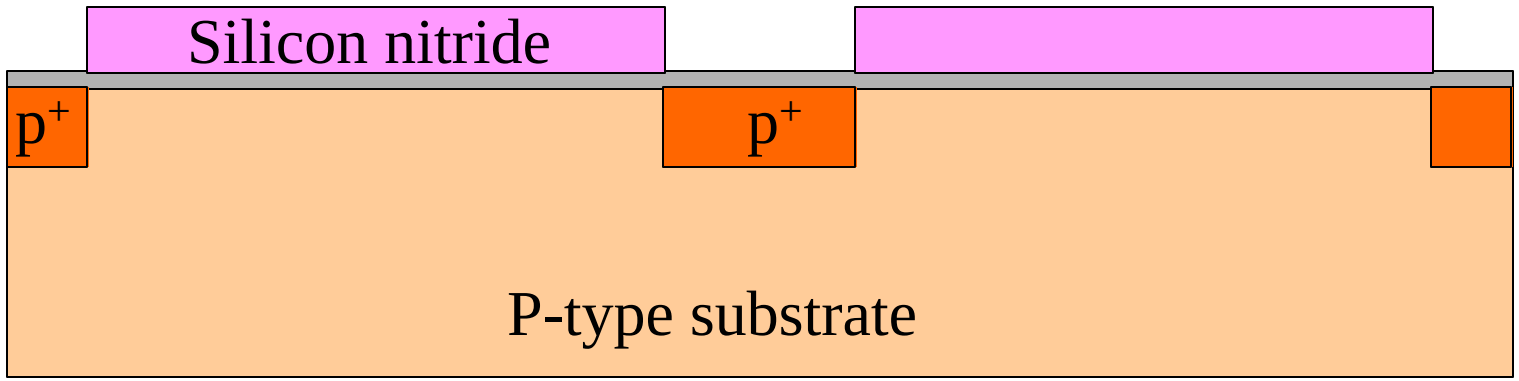
Etch Nitride



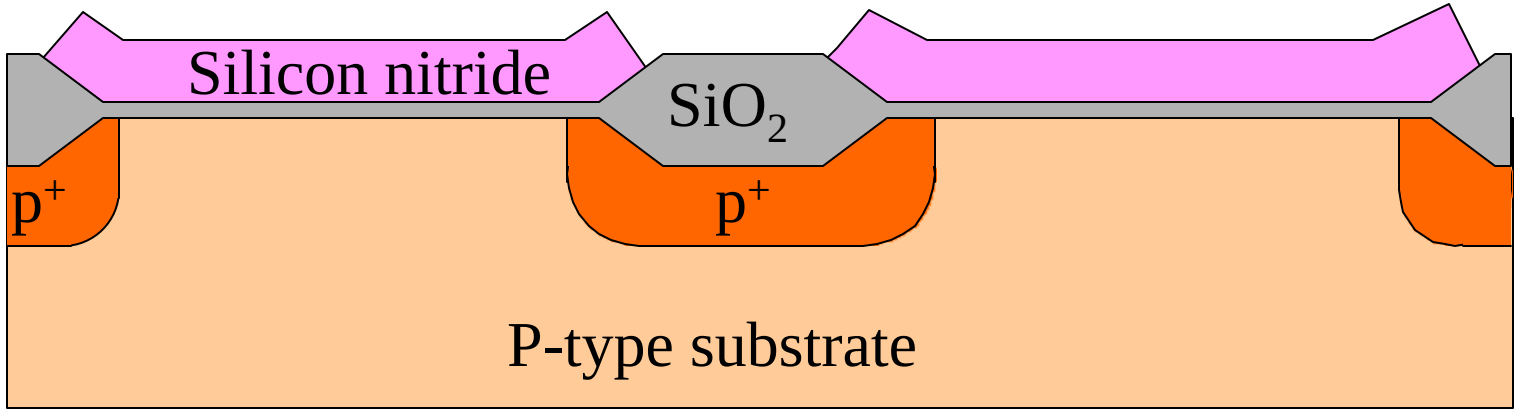
Strip Photoresist



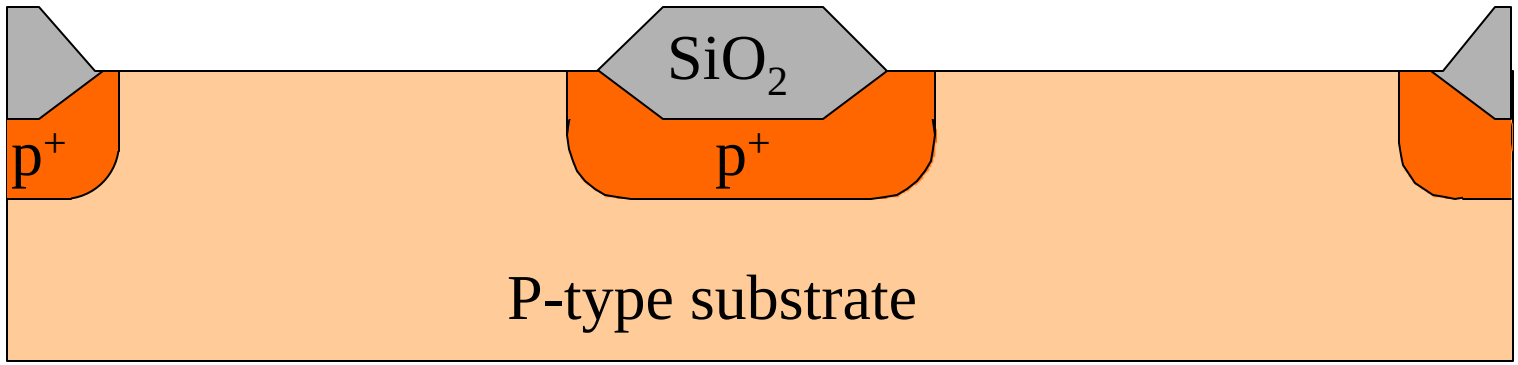
Isolation Implantation



Thermal Oxidation



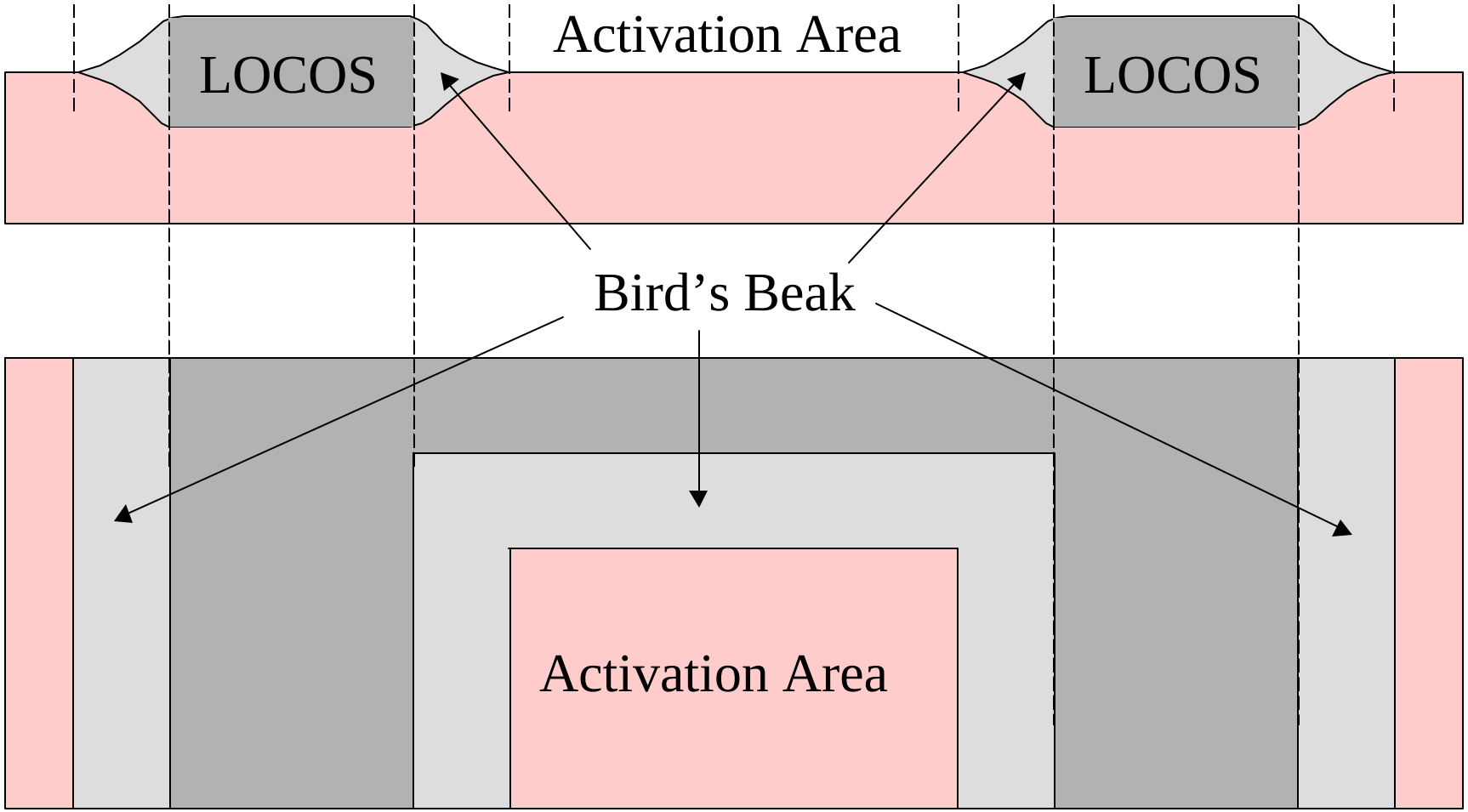
Strip Nitride



Problem of LOCOS

- Bird's beak
  - Oxygen diffuse isotropically in silicon dioxide
  - Oxide grow underneath nitride
  - Waste surface area
- Uneven surface
  - Oxide grow above the silicon surface
  - Affect photolithography and thin film deposition

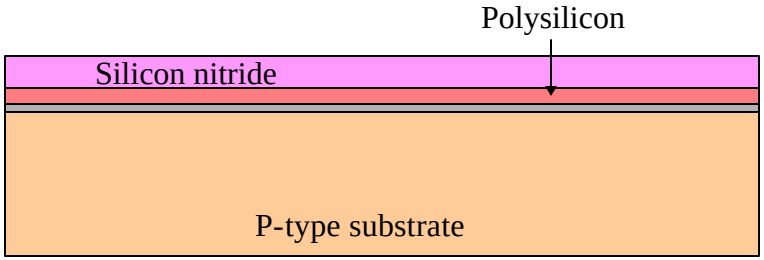
Bird's Beak of LOCOS



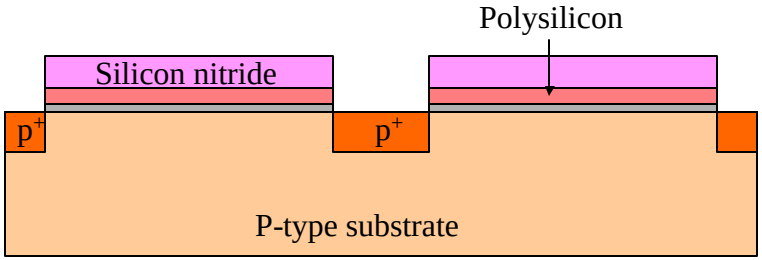
Poly Buffered LOCOS (PBL)

- Reducing “bird’s beak”
- Deposit polysilicon before LPCVD nitride
- Poly-Si consumes lateral diffusing oxygen
- Reduce “bird’s beak” to 0.1 to 0.2 μm.

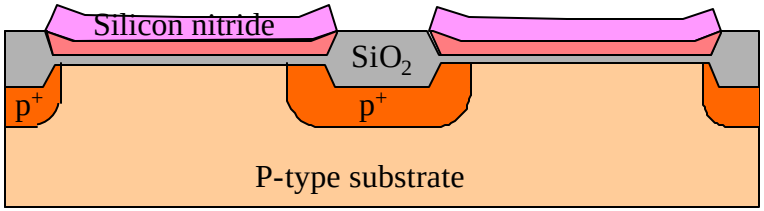
Poly Buffered LOCOS



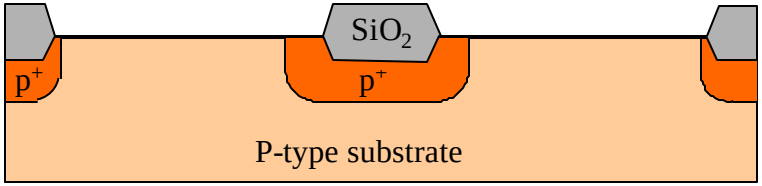
Pad oxidation, poly and nitride LPCVD



Nitride, poly, and oxide etch, B implantation



Oxidation



Strip pad oxidation, poly and nitride

Shallow Trench Isolation (STI)

- LOCOS and PBL work fine when feature size > 0.5 μm
- Intolerable when feature < 0.35 μm
- Silicon etch and oxidation of trench was researched to reduce oxide encroachment
- Process was then developed with CVD oxide trench fill

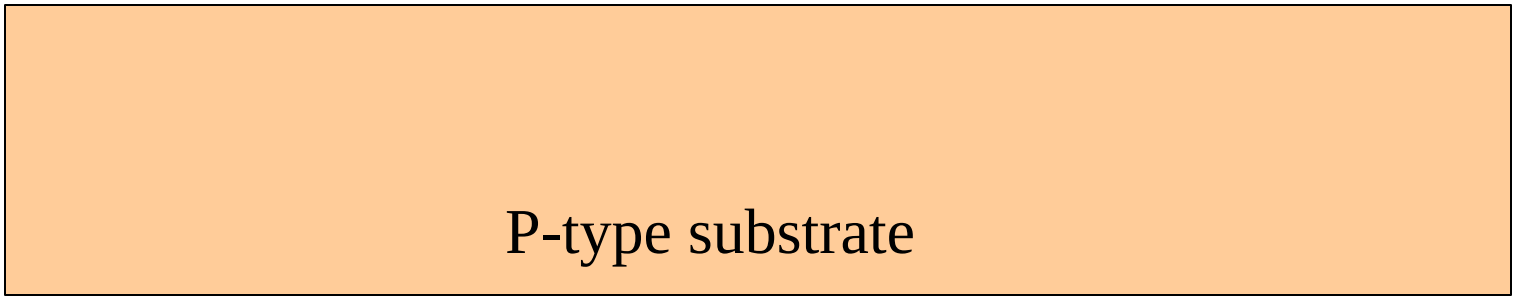
STI and LOCOS

- STI
  - No bird's beak
  - Smoother surface
  - More process steps
- LOCOS
  - Simpler, cheaper, and production proven
  - Used in IC fabrication until feature < 0.35 μm

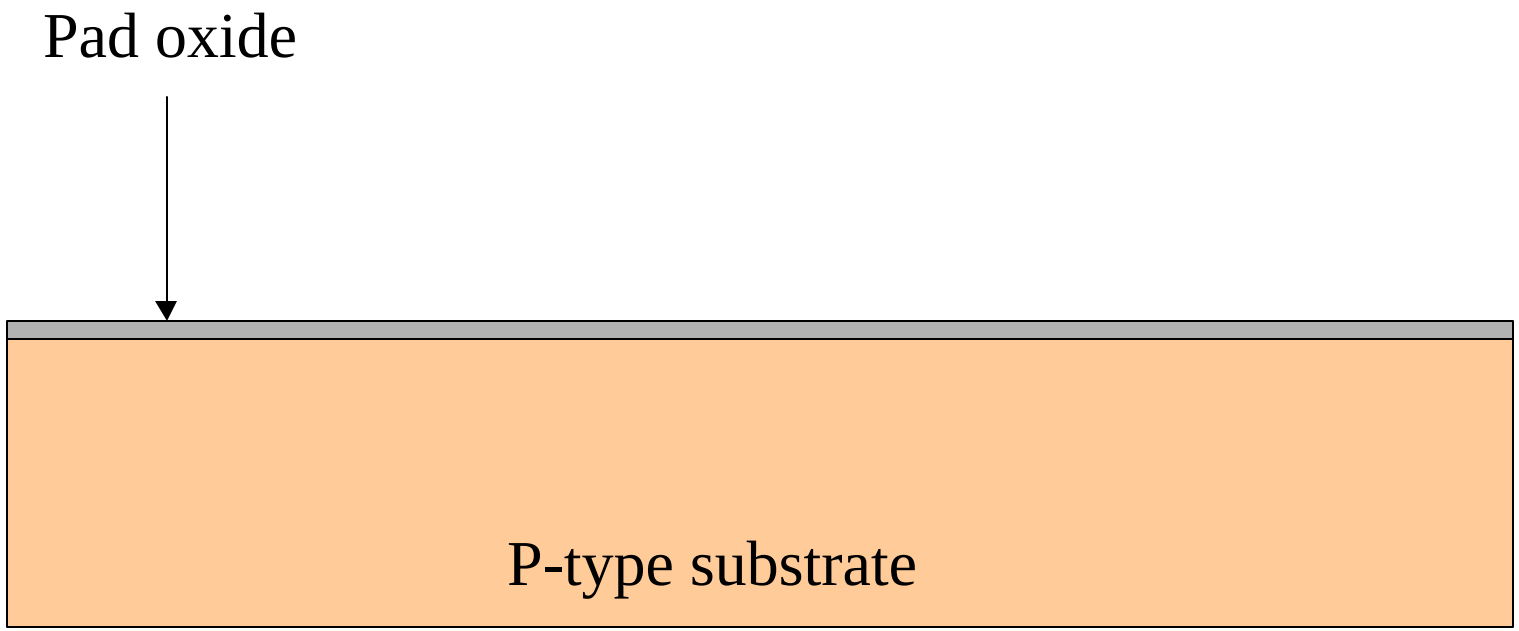
STI and LOCOS

- Early STI process
  - Oxide etch back
  - CF_4/O_2 chemistry
  - Endpoint by C-N line
- Advanced STI process: oxide CMP
  - Better process control
  - Higher yield

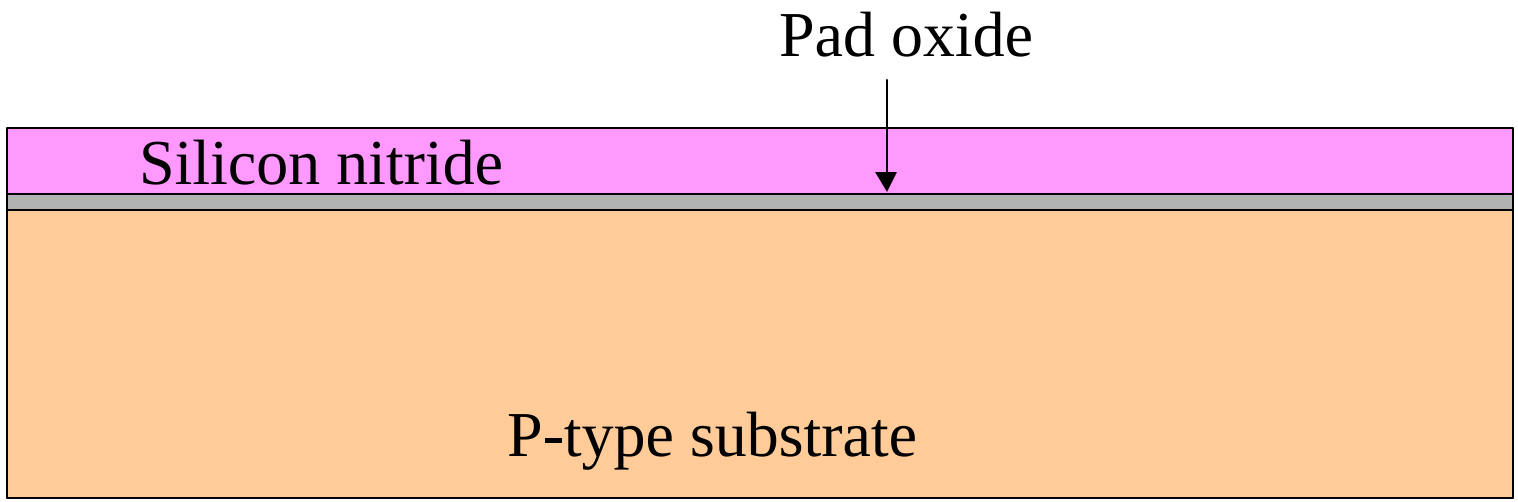
Early STI: Wafer Clean



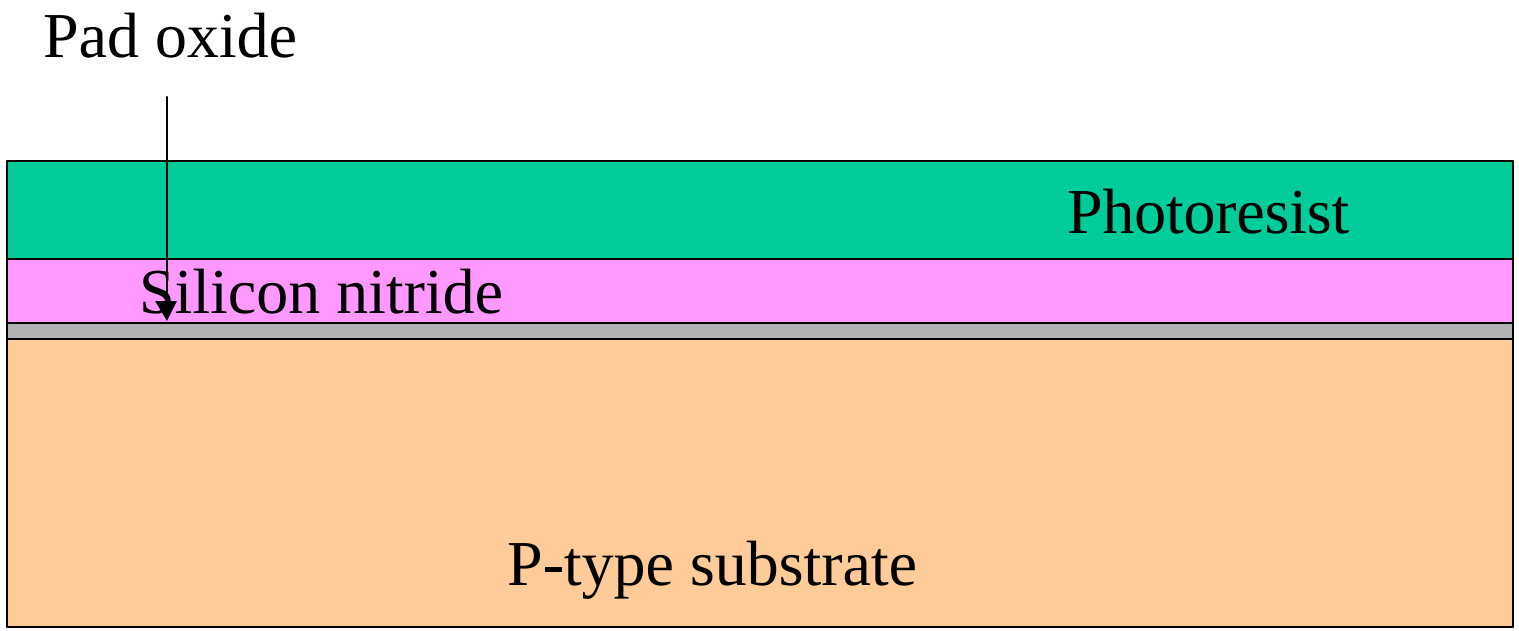
Early STI: Grow Pad Oxide



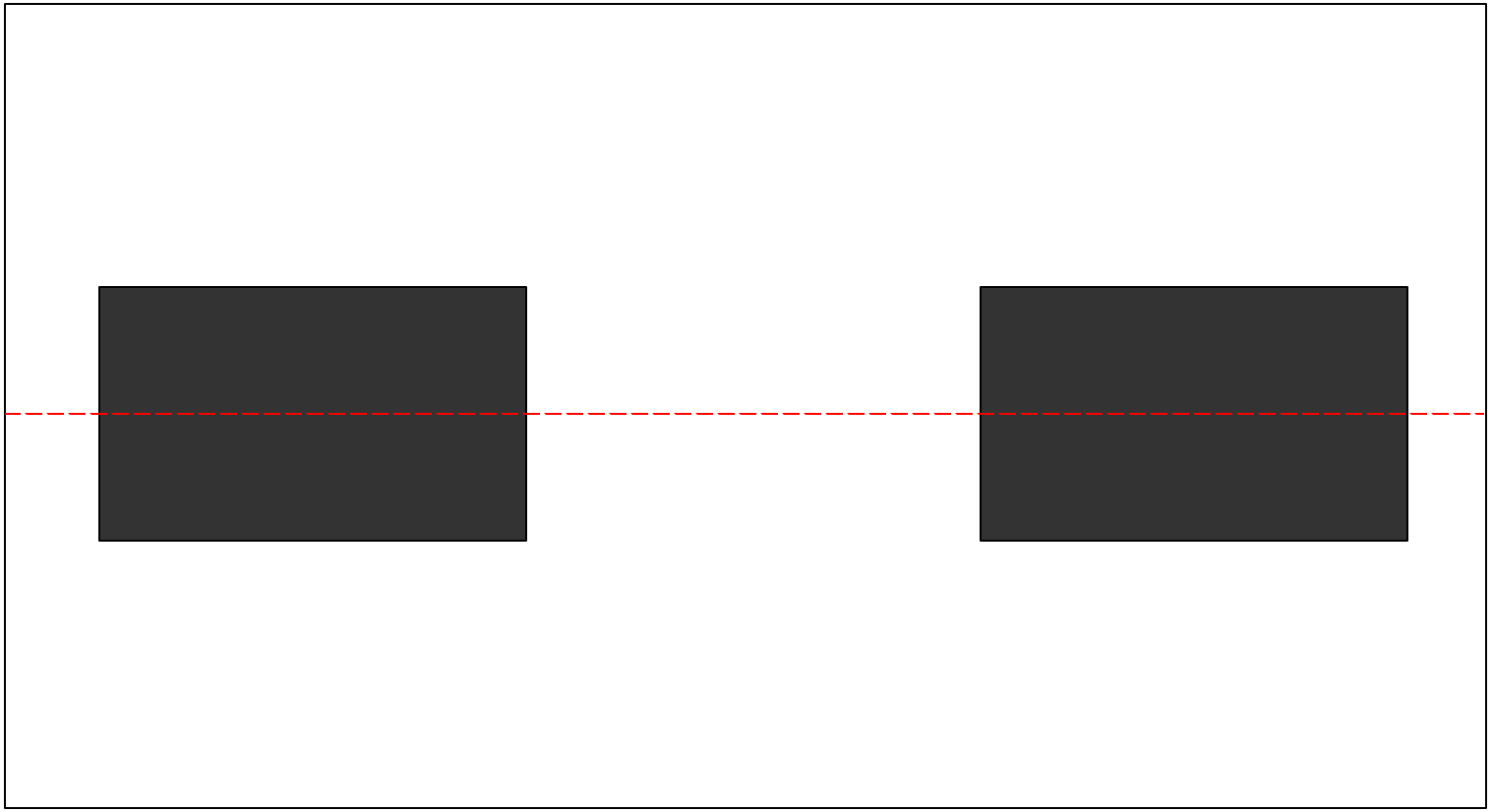
Early STI: LPCVD Silicon Nitride



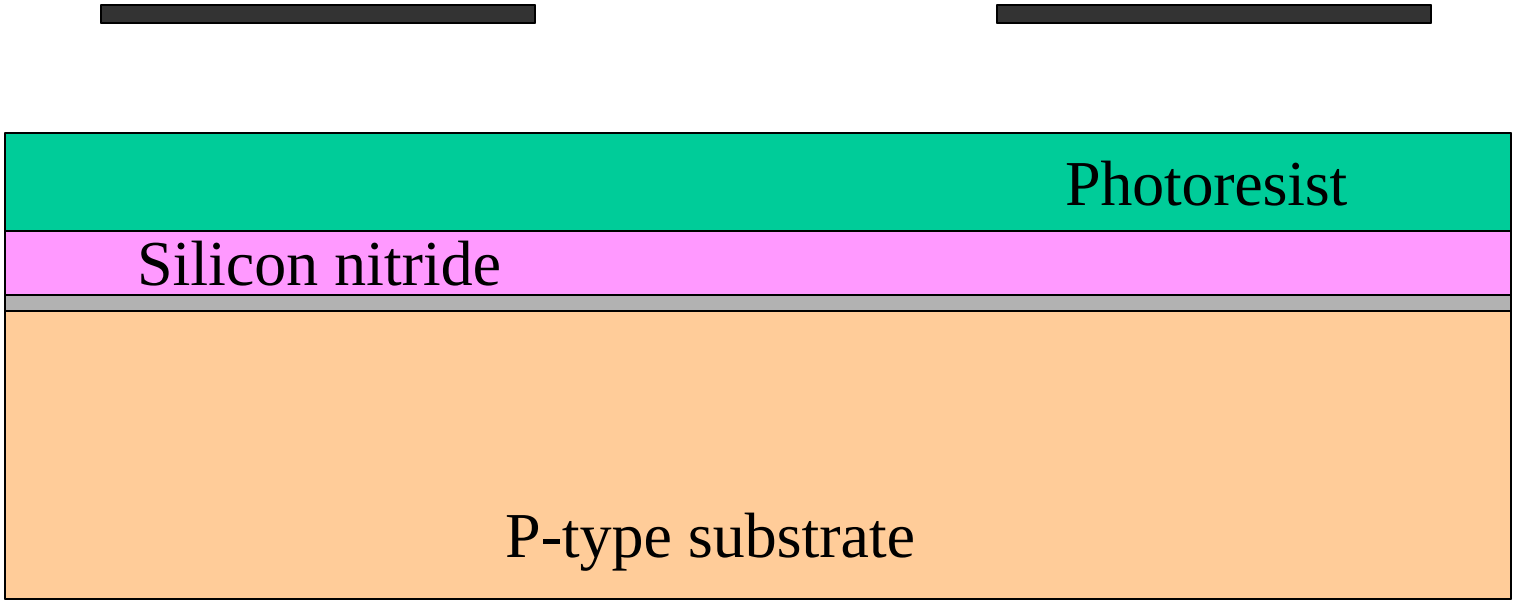
Early STI: Photoresist Coating



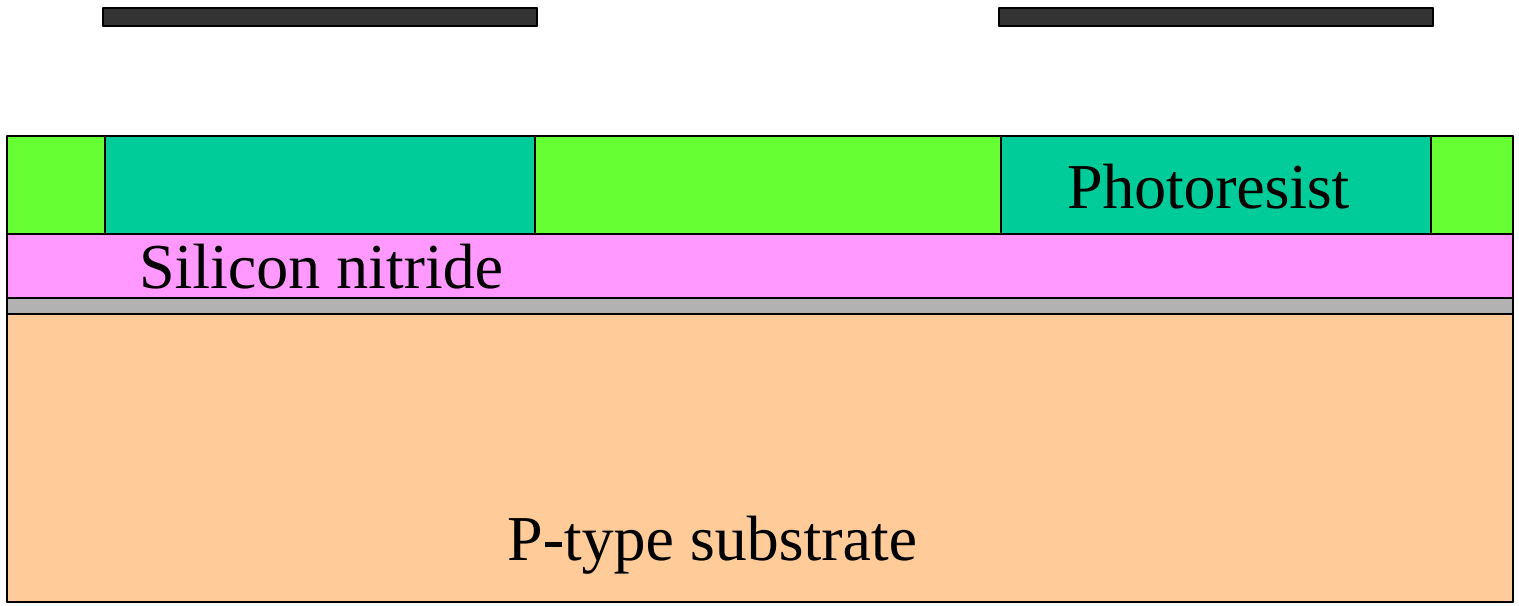
Early STI: STI Mask



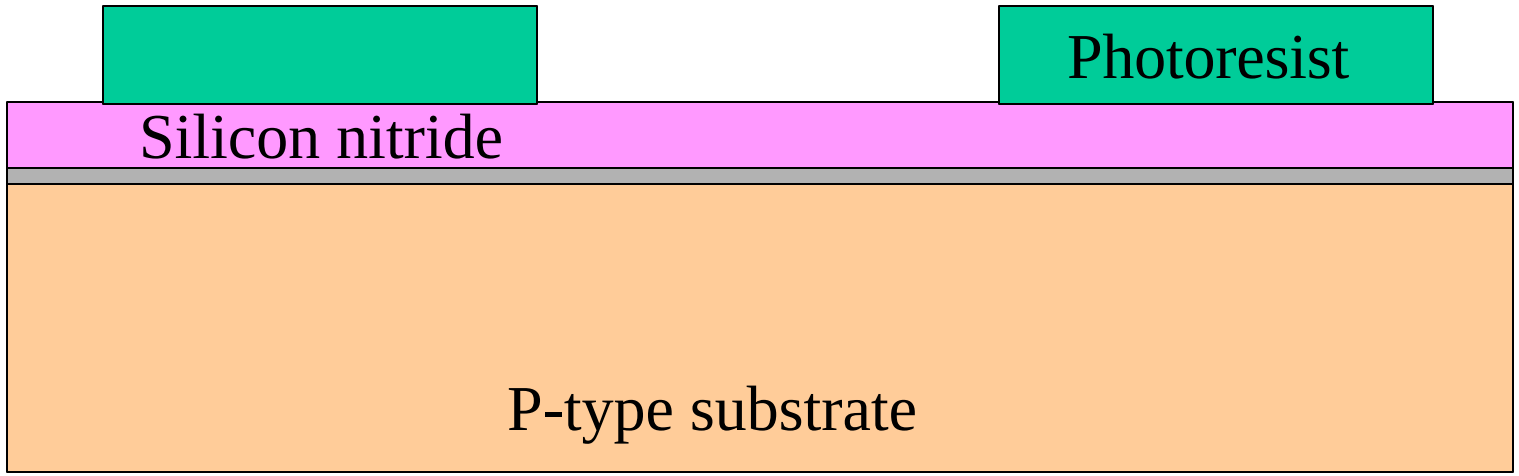
Early STI: STI Mask Alignment



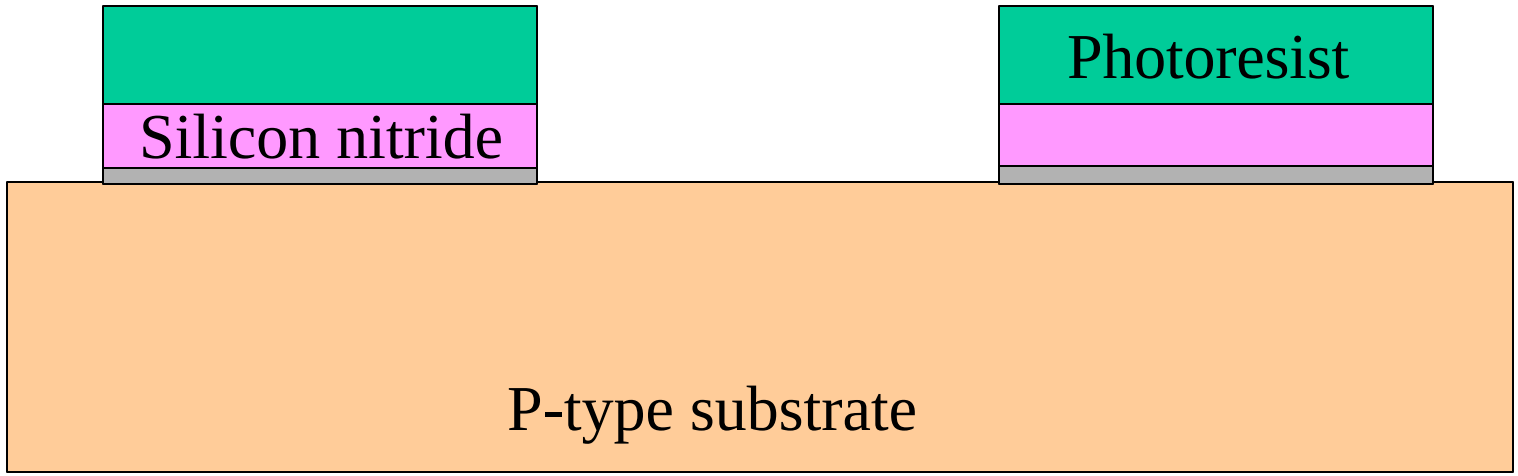
Early STI: STI Mask Exposure



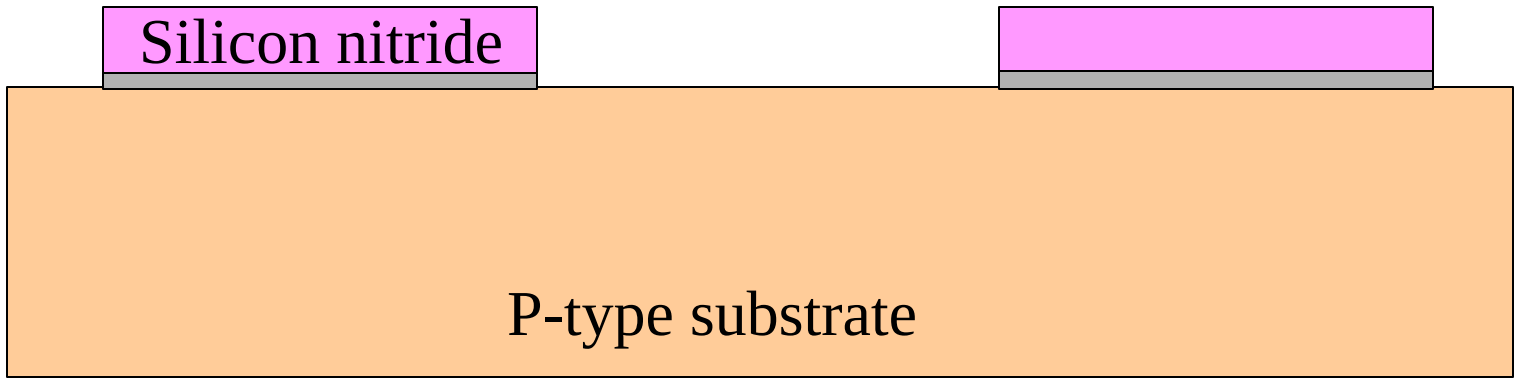
Early STI: Development



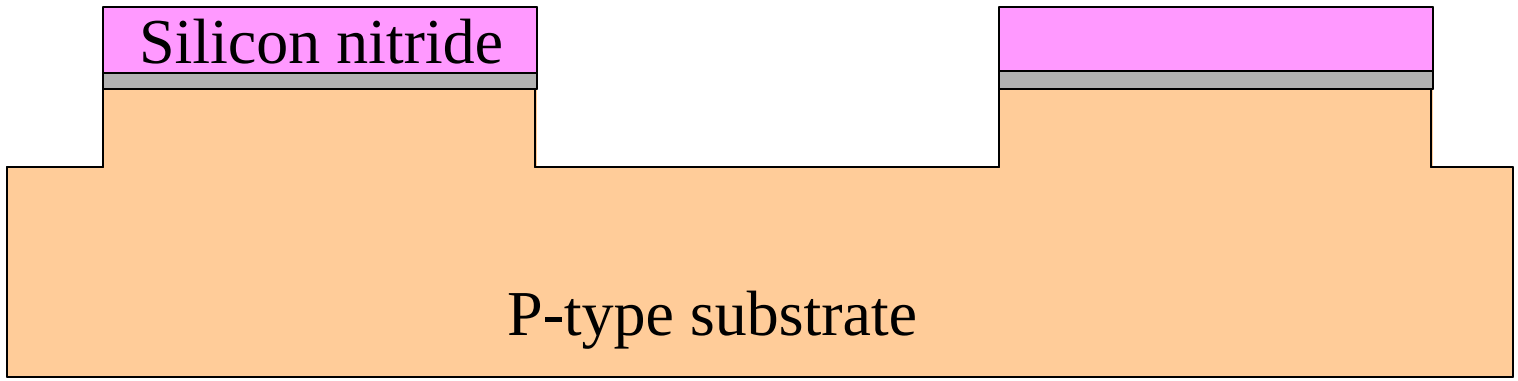
Early STI: Etch Nitride and Pad Oxide



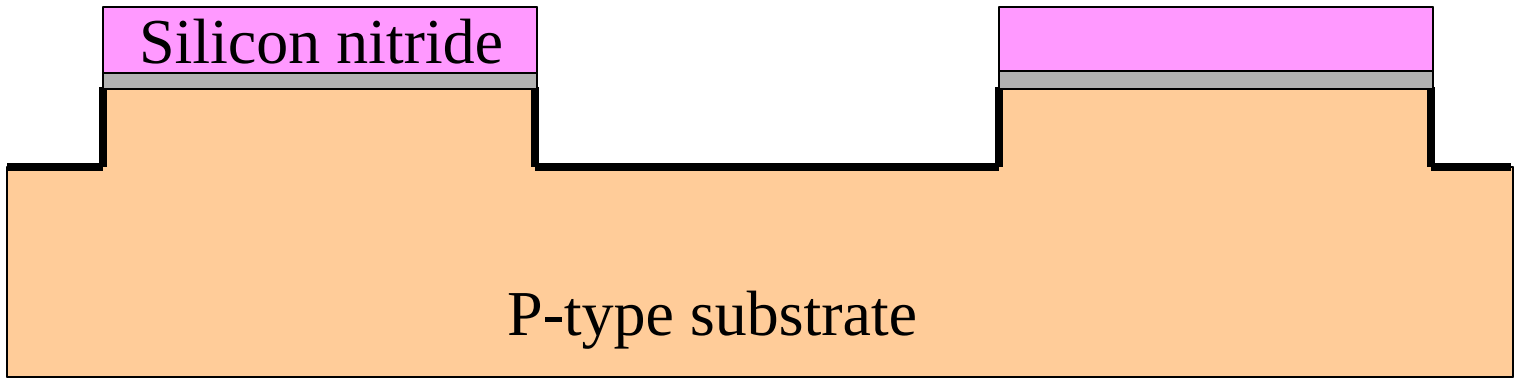
Early STI: Strip Photoresist



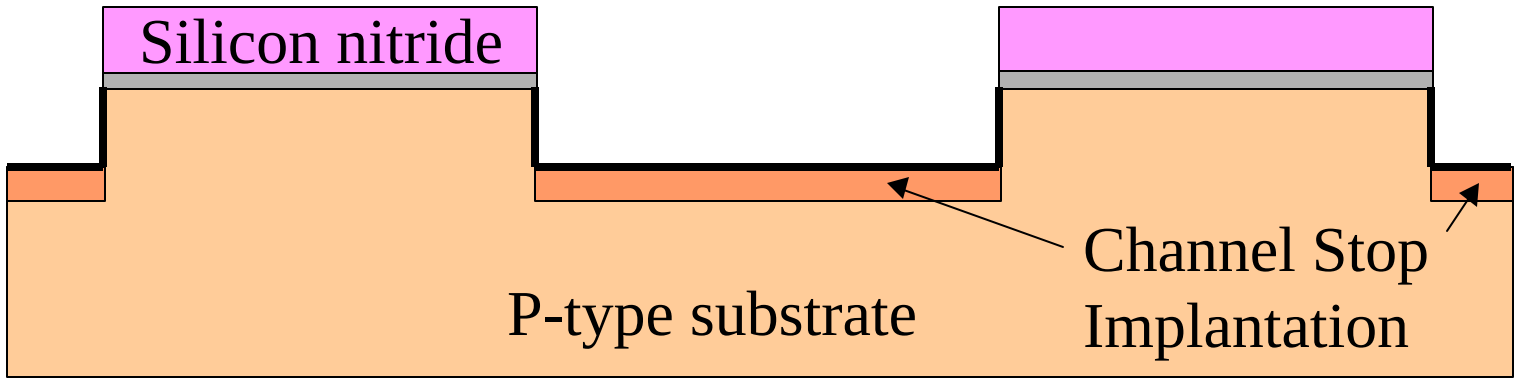
Early STI: Etch Silicon



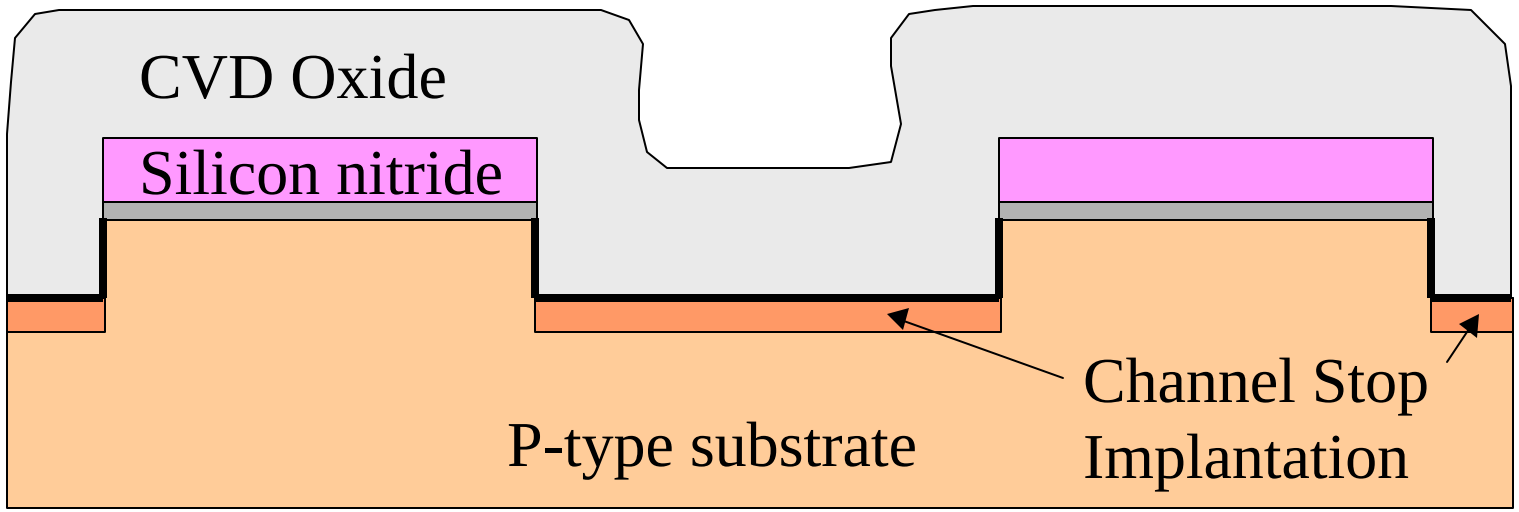
Early STI: Grow Barrier Oxide



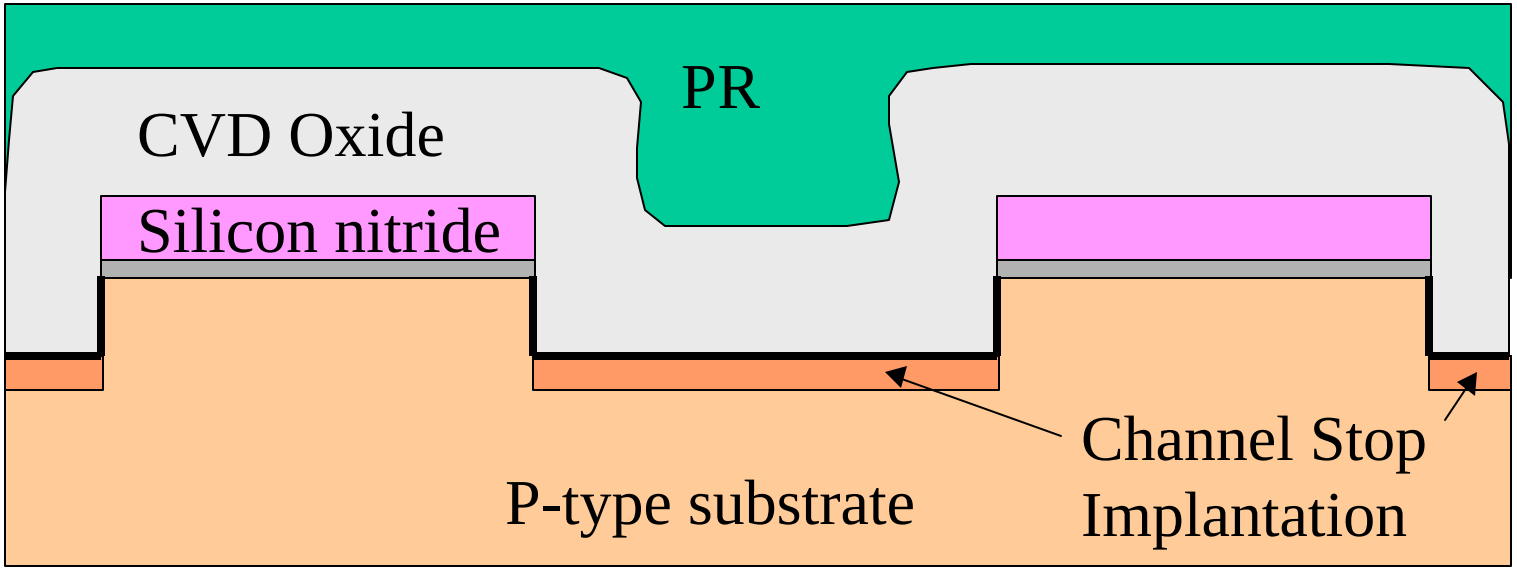
Early STI: Channel Stop Implantation, Boron



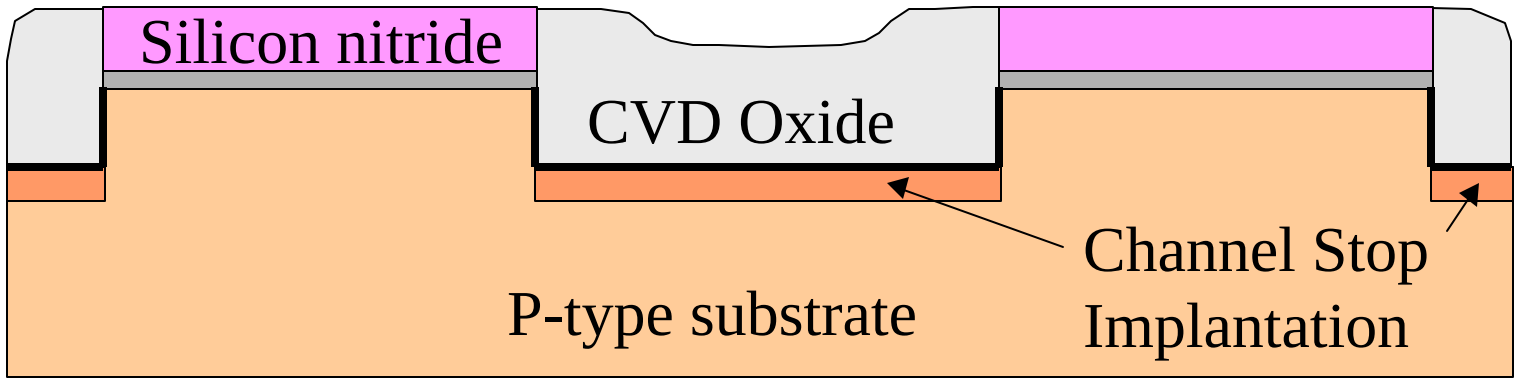
Early STI: CVD Oxide



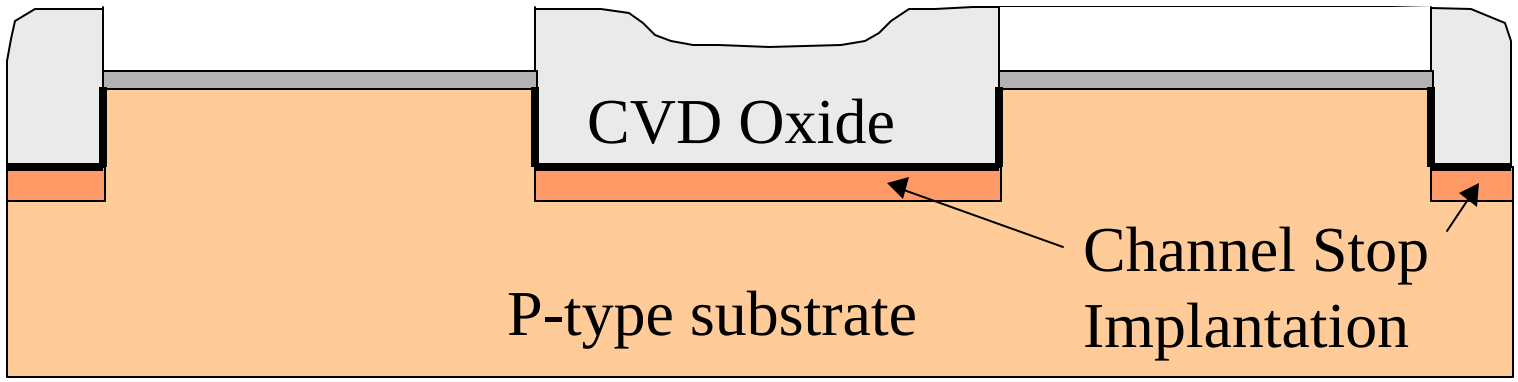
Early STI: Photoresist Coating



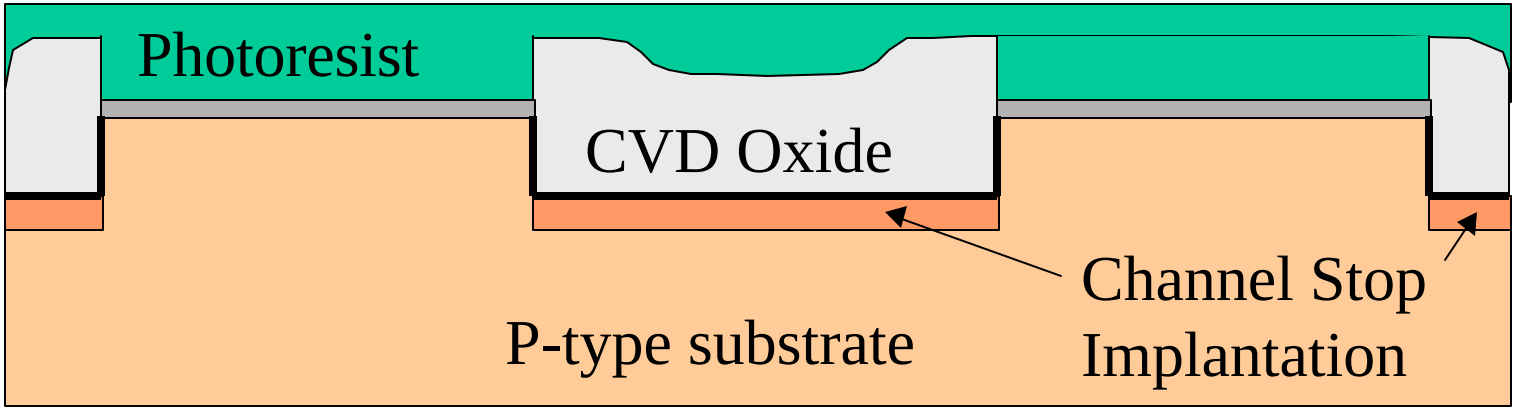
Early STI: Oxide Etch Back, Stop on Nitride



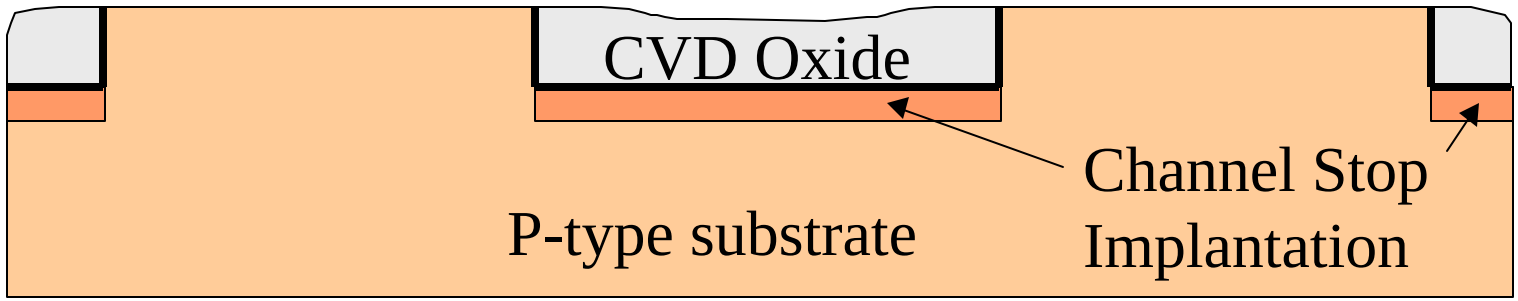
Early STI: Strip Nitride



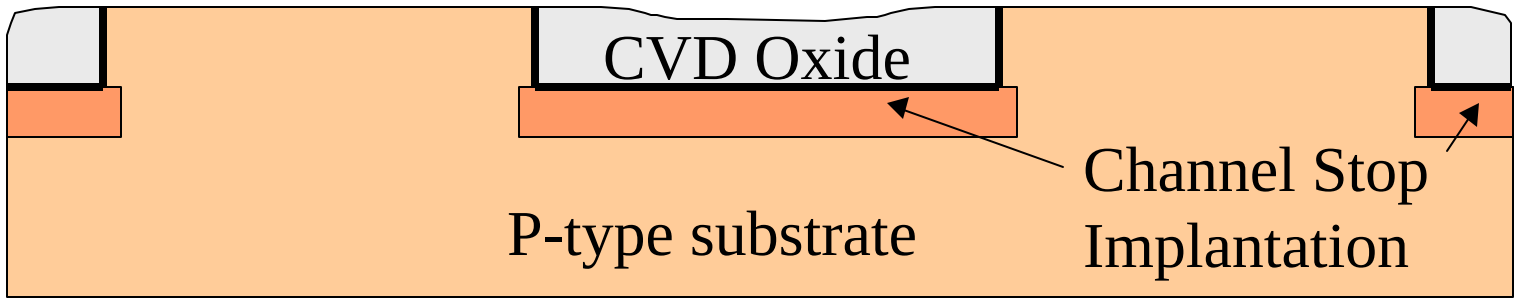
Early STI: Photoresist Coating



Early STI: Oxide Etch Back



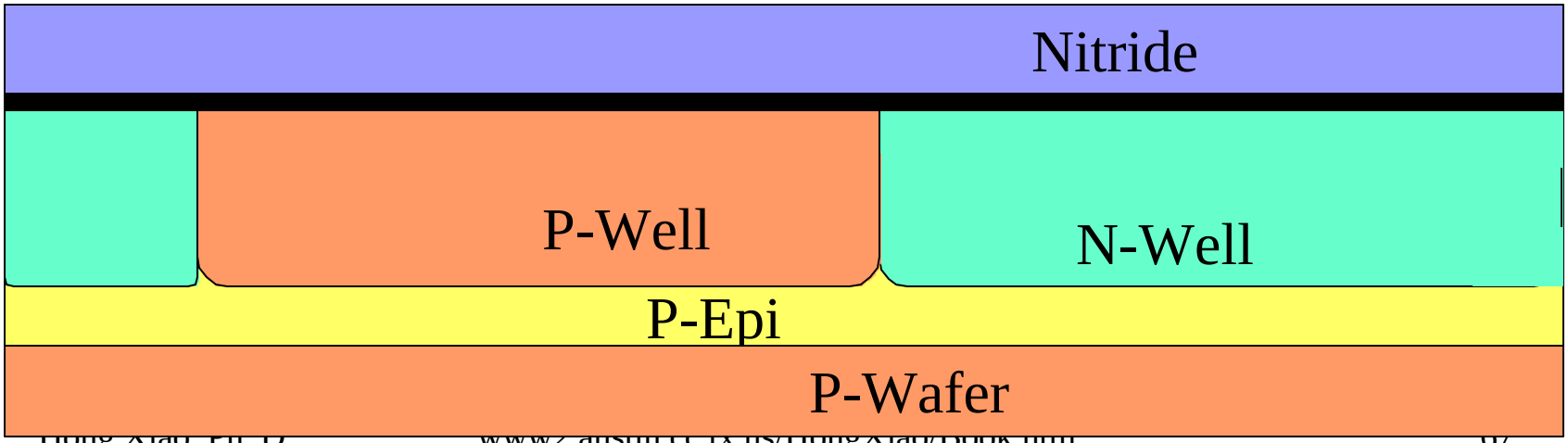
Early STI: Oxide Annealing



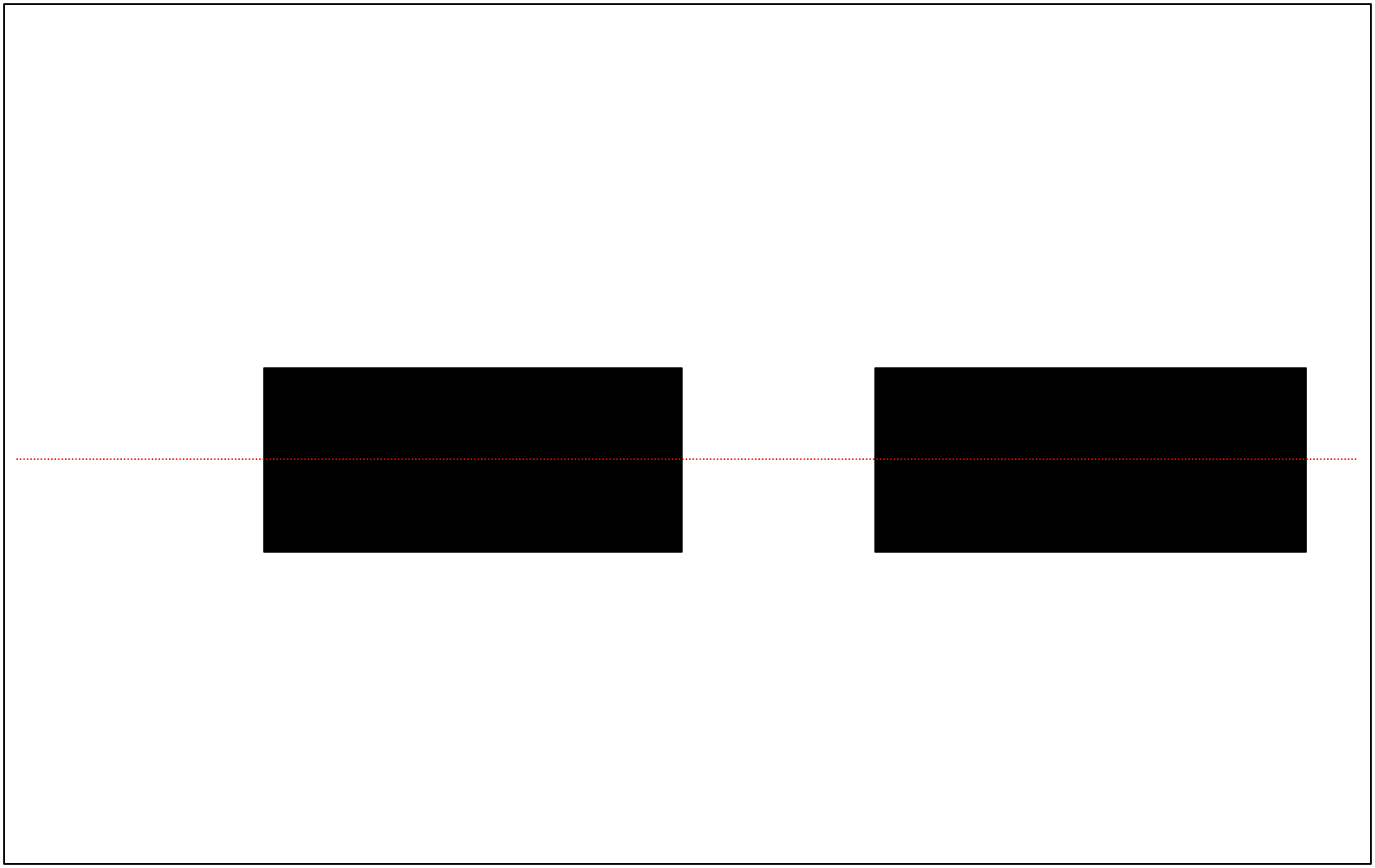
Advanced STI

- No need for channel stop ion implantation to raise the field threshold voltage.
- Trench fill can also be achieved with O_3-TEOS process
  - Need anneal at > 1000 °C to densify the film
- HDP oxide does not require thermal anneal

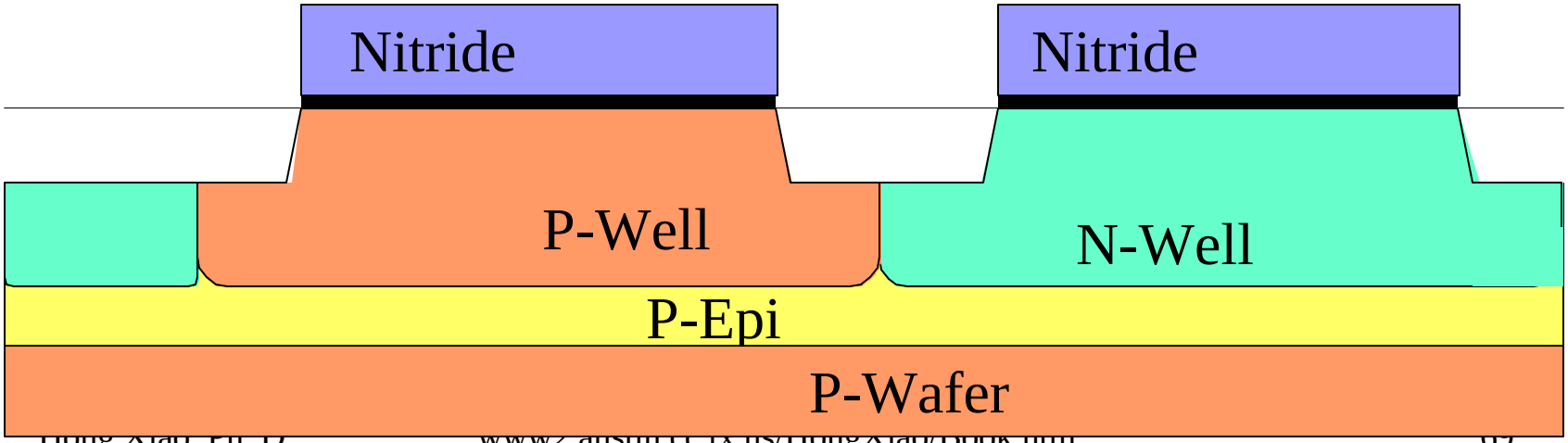
Advanced STI: Pad Oxidation and LPCVD Nitride



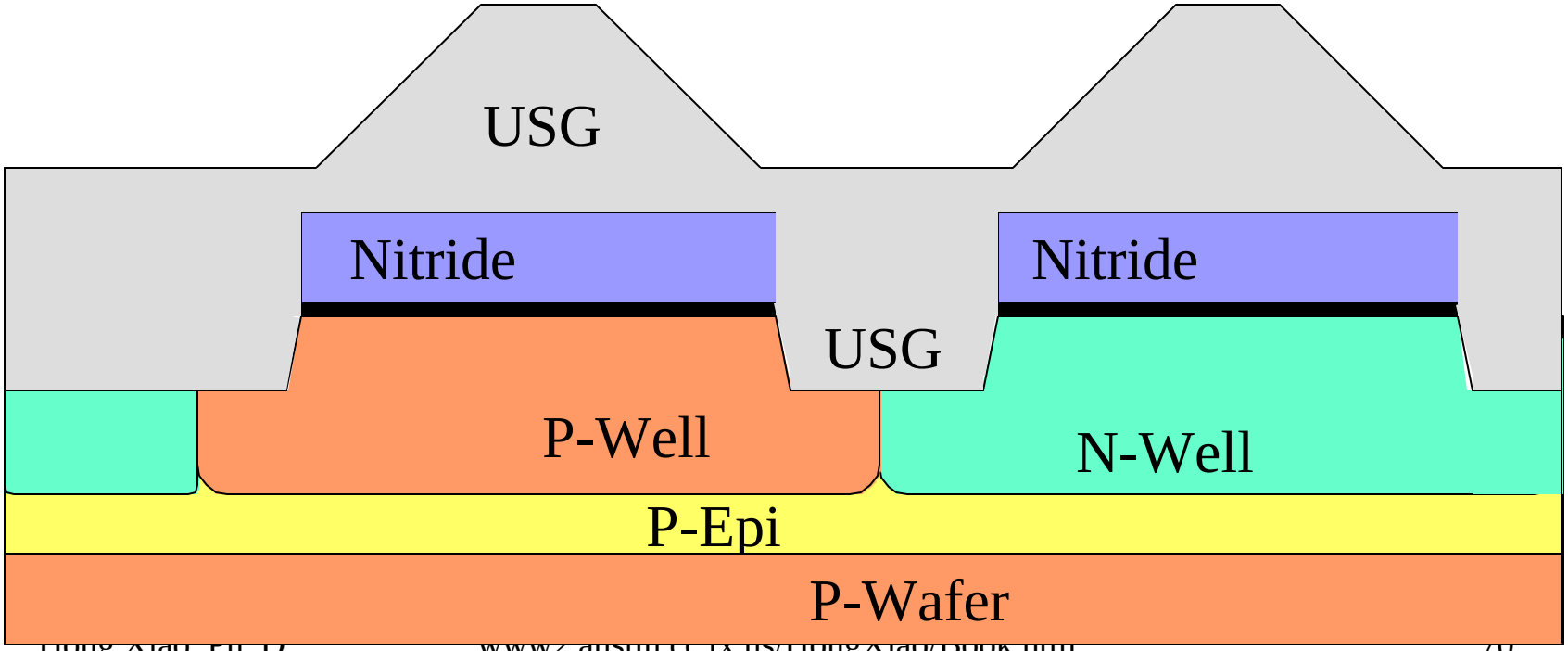
Advanced STI: STI Mask



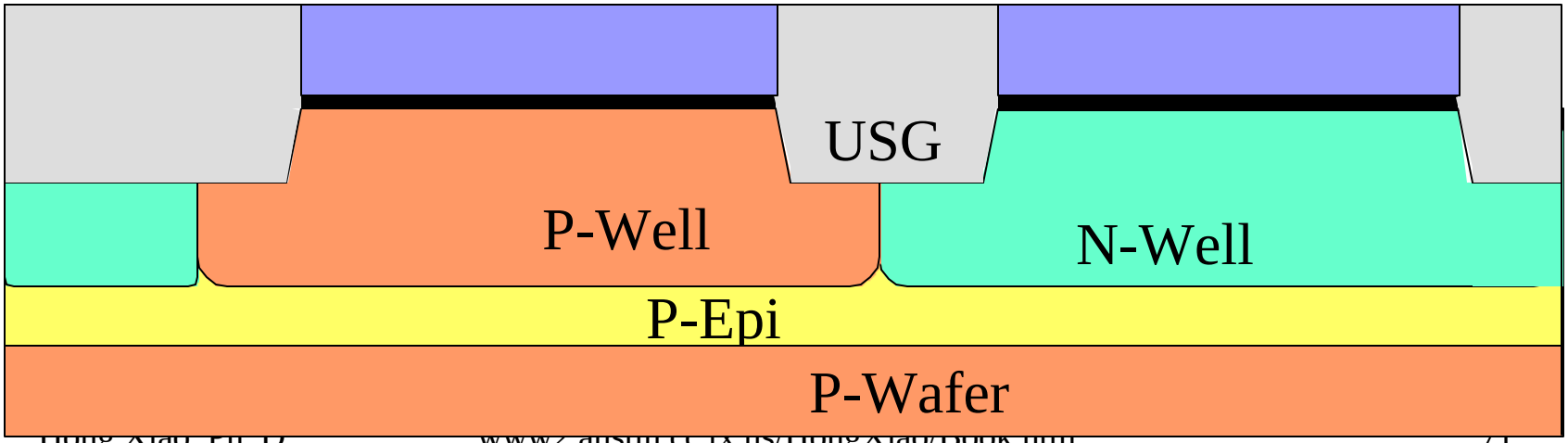
Advanced STI: Etch Nitride, Oxide, and Silicon, Strip Photoresist



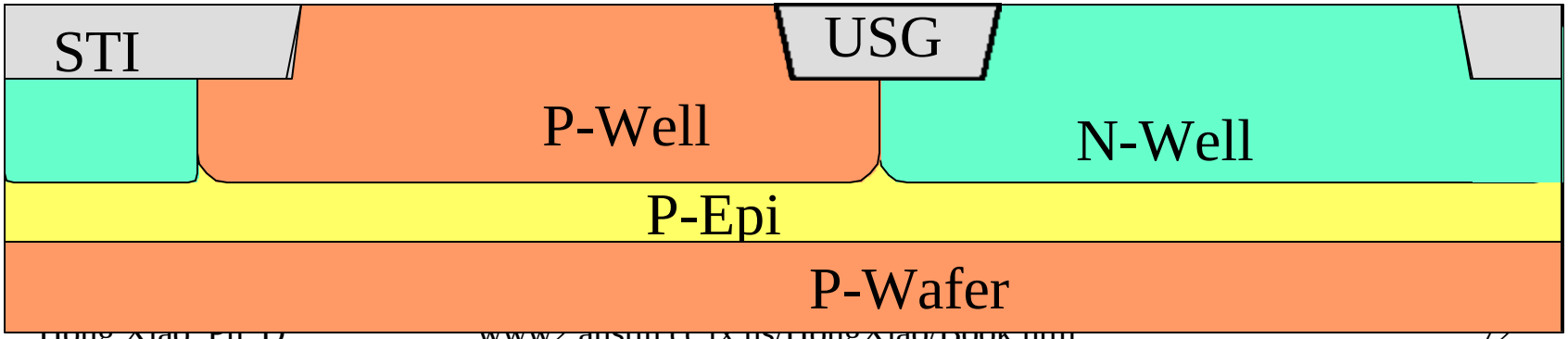
Advanced STI: HDP CVD Oxide



Advanced STI: CMP Oxide, Stop on Nitride



Advanced STI: Nitride Strip



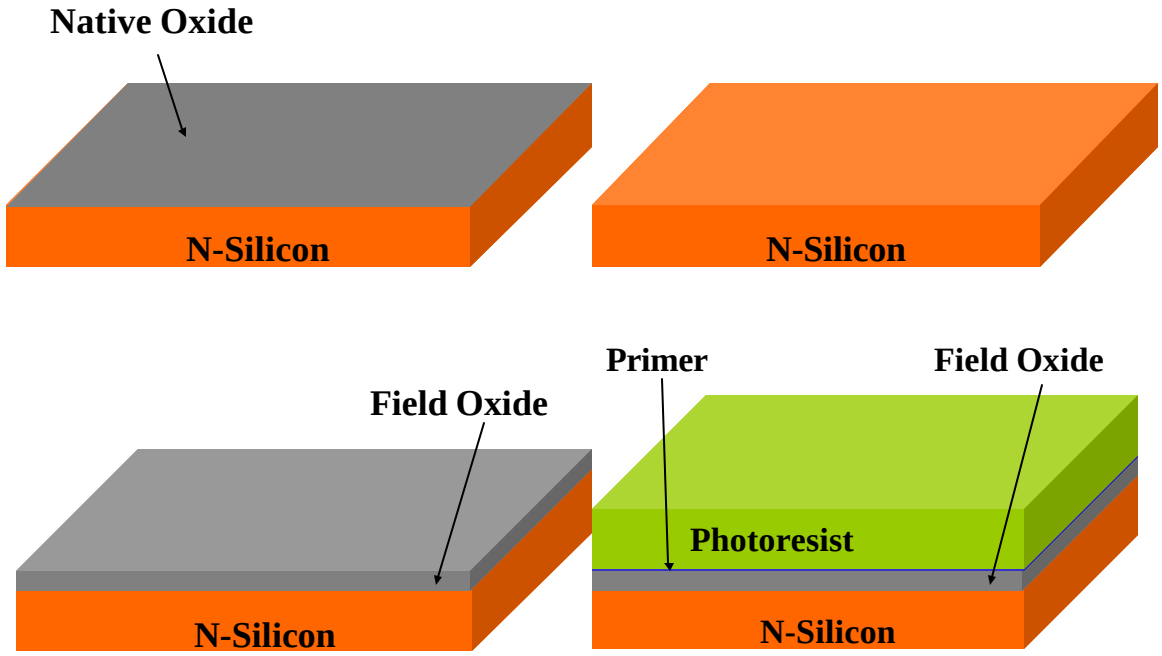
Transistor Making

- Metal gate
- Self-aligned gate
- Lightly doped drain (LDD)
- Threshold adjustment
- Anti punch-through
- Metal and high-κ gate MOS

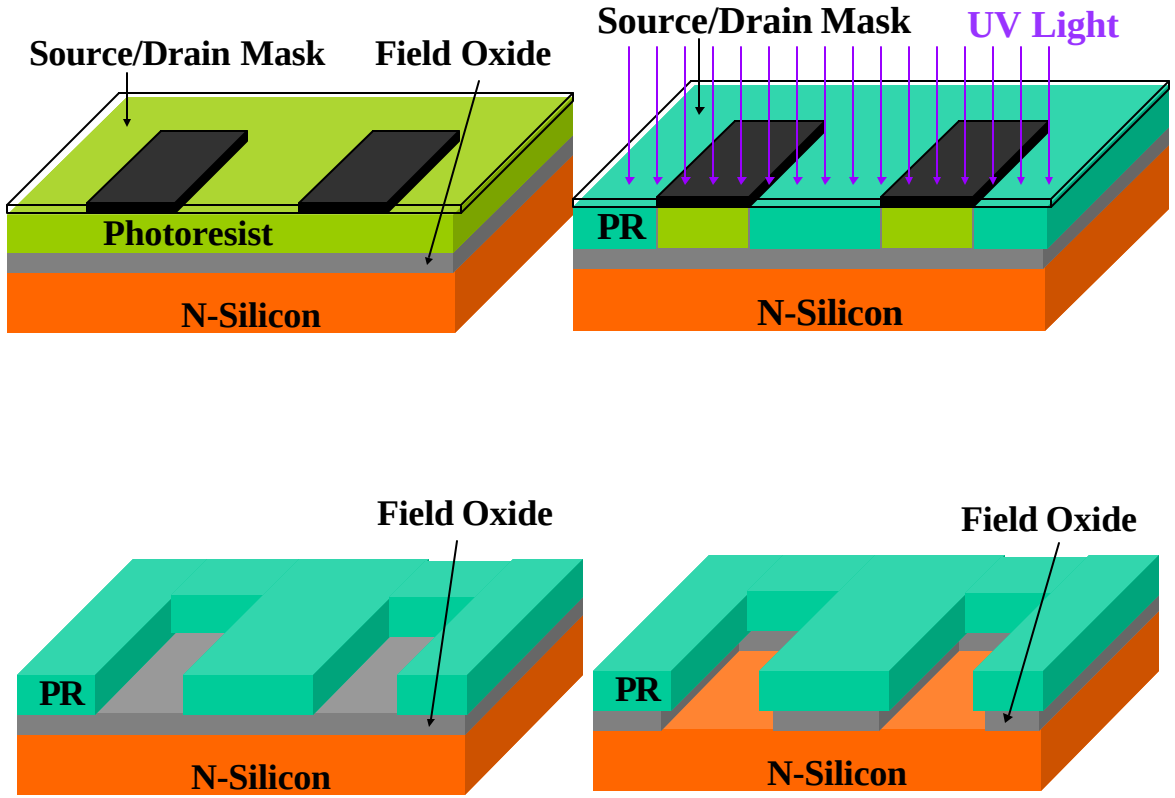
Transistor Making: Metal Gate

- Form source/drain first
  - Diffusion doping with silicon dioxide mask
- Align gates with source/drain, then gate area was etched and gate oxide is grown
- The third mask define the contact holes
- The fourth mask form metal gates and interconnections.
- Last mask defined the bonding pad

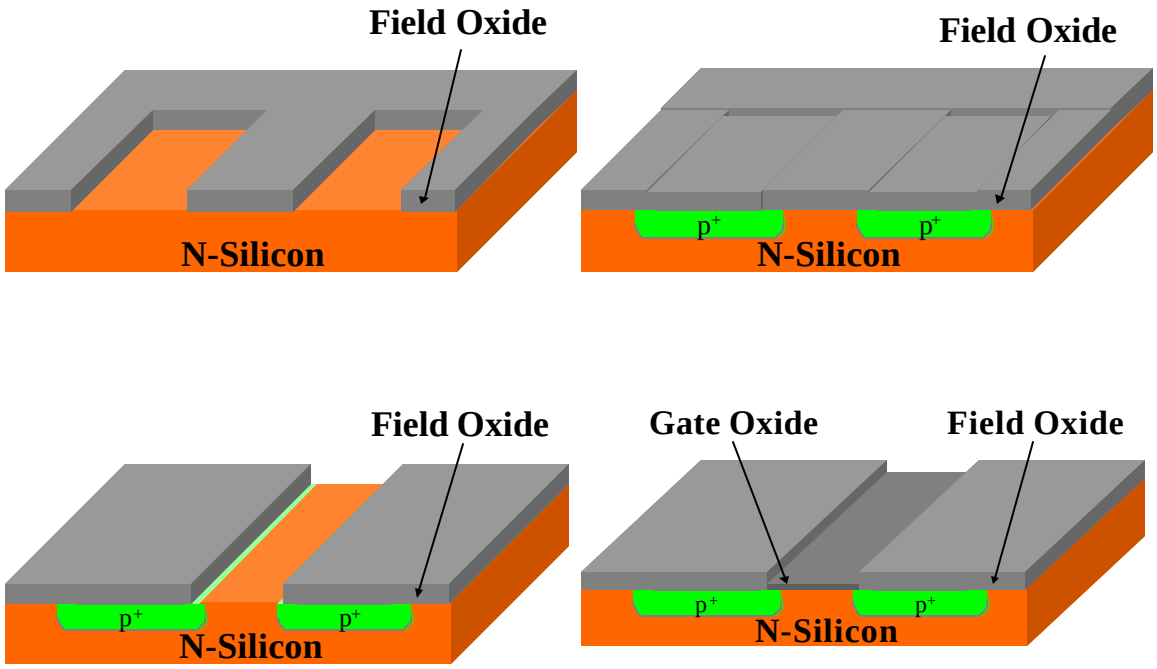
Wafer Clean, Field Oxidation, and Photoresist Coating



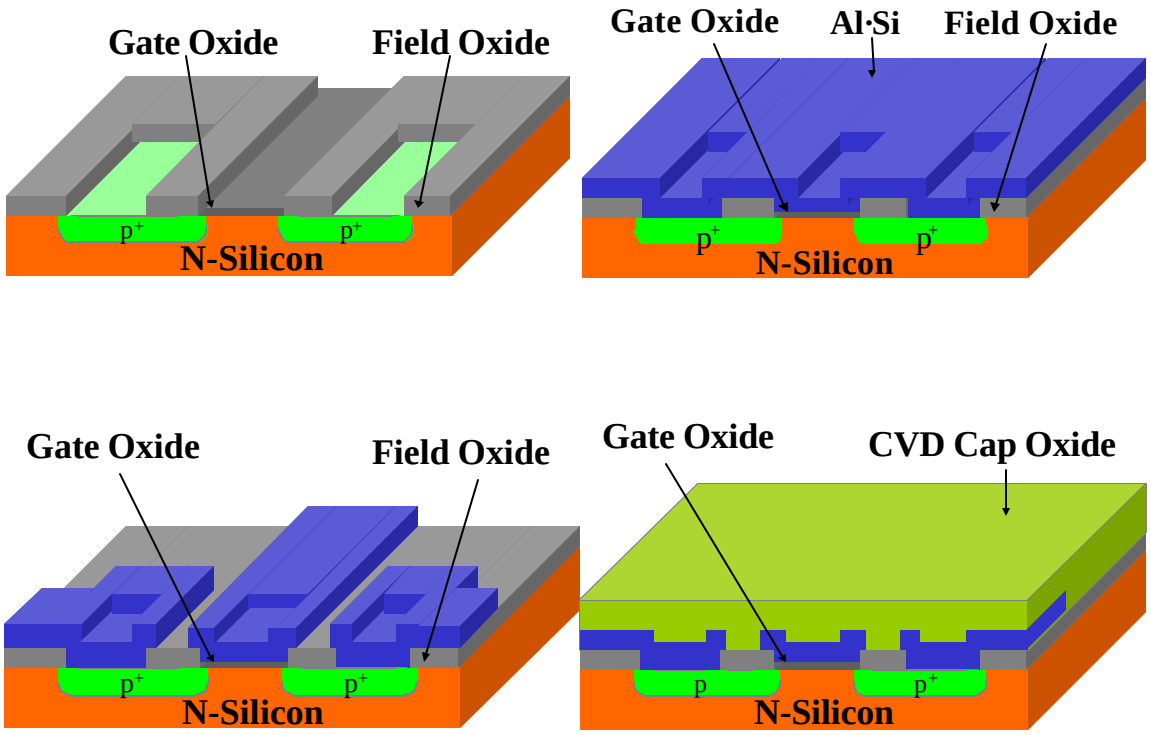
Photolithography and Oxide Etch



Source/drain Doping and Gate Oxidation



Contact, Metallization, and Passivation



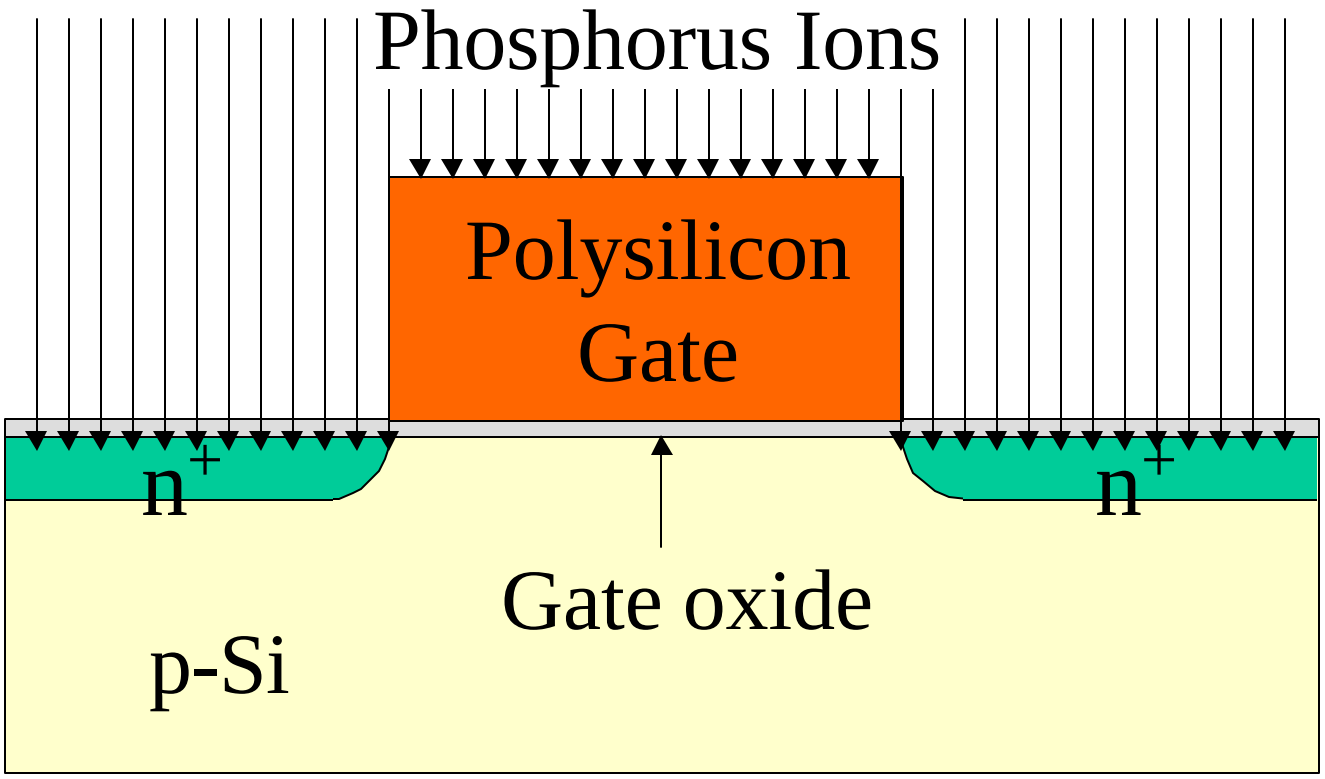
Self-aligned Gate

- Introduction of ion implantation
- NMOS instead of PMOS
- Polysilicon replaced aluminum for gate
  - Al alloy can’t sustain the high temperature post-implantation anneal

Self-aligned Gate

- Activation area for transistors making
- Gate oxidation and polysilicon deposition
- Gate mask defines the gate and local interconnection.
- Transistors are made after ion implantation and thermal annealing
- Advanced MOSFET are made in this way

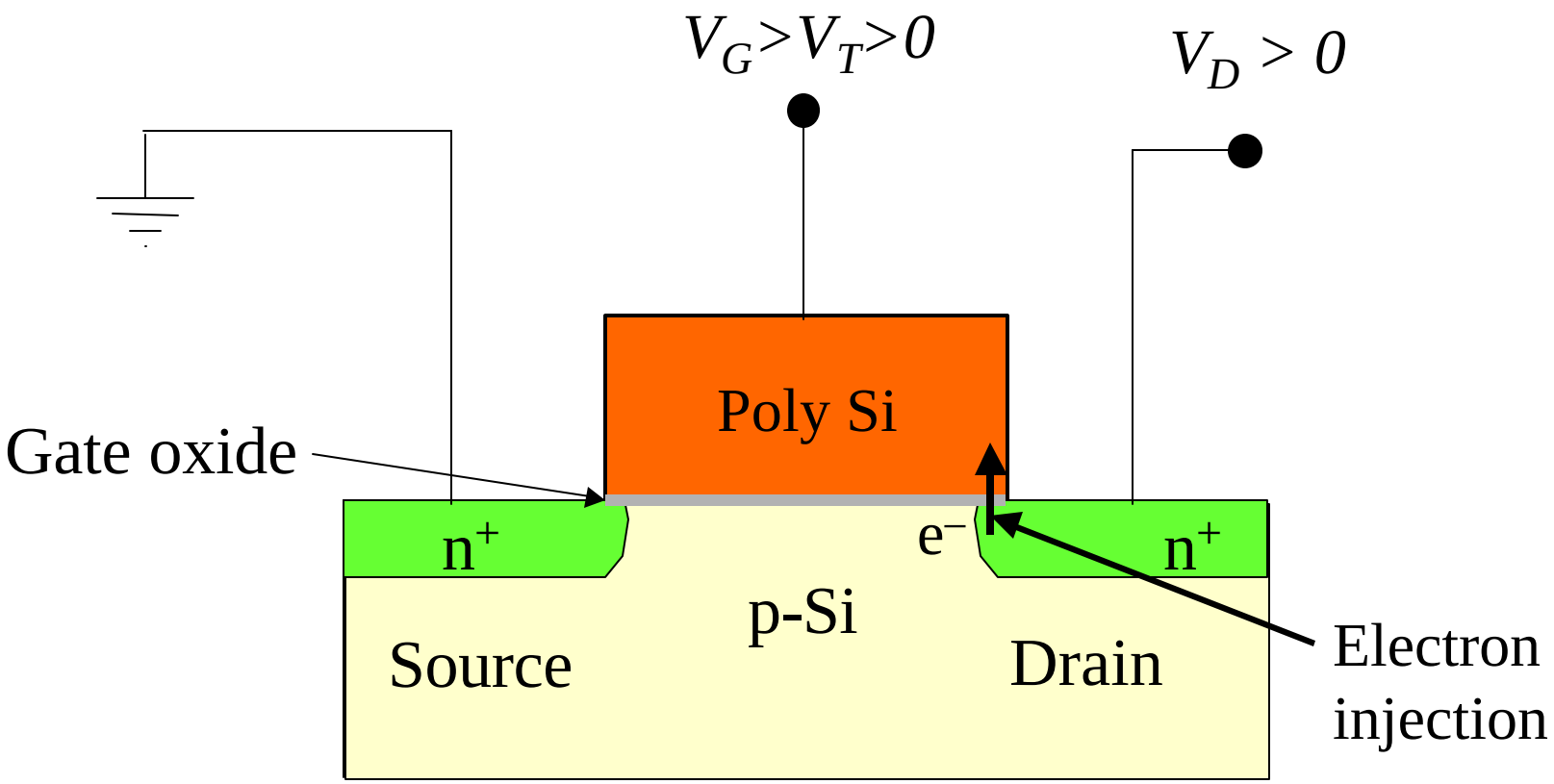
Transistor Making: Self-aligned Gate



Hot Electron Effect

- Gate width is < 2 microns,
- Vertical electric field accelerates electrons tunneling through the thin gate oxide layer
- Hot electron effect
  - gate leakage affect transistor performance
  - trapping of electrons in the gate oxide cause reliability problems for the IC chips
- LDD is used to prevent hot electron effect

Hot Electron Effect



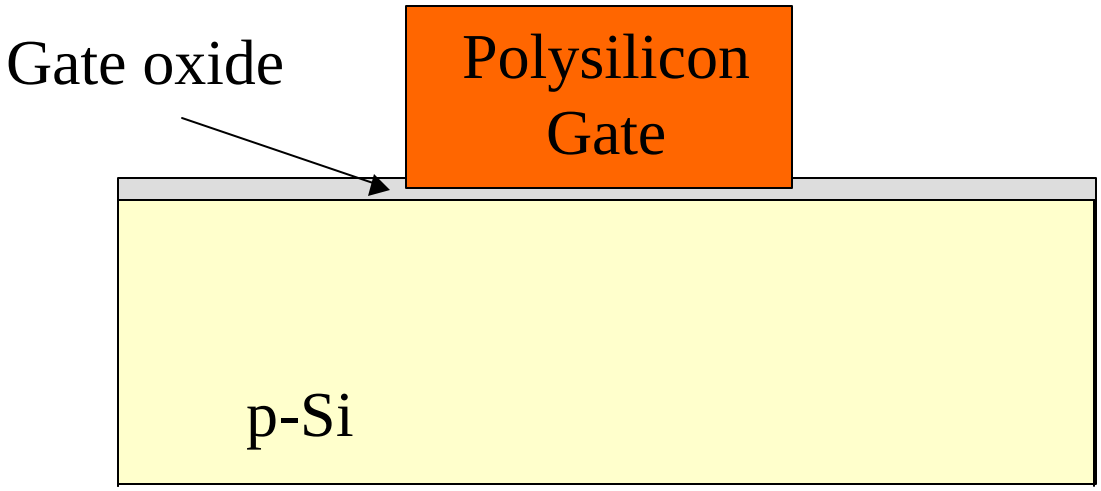
LDD Formation

- Low energy, low current ion implantation
  - very low dopant concentration and shallow junction just extended underneath the gate
- Sidewall spacers can be formed by depositing and etching back dielectric layers
- High current, low energy ion implantation forms the heavily doped source/drain
  - Source/drain are kept apart from the gate

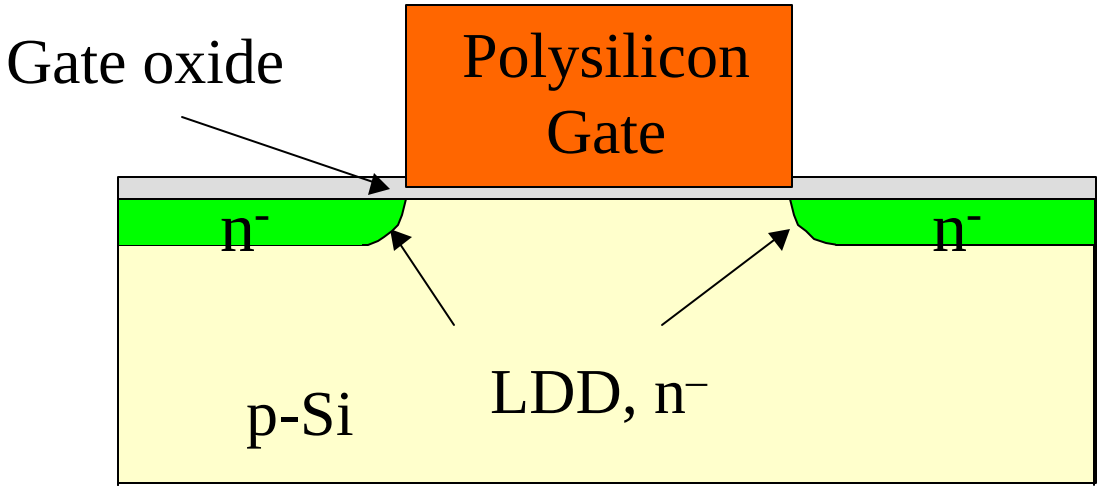
LDD Formation

- Reduce the vertical electric field of the source/drain bias
- Reduce the available electrons for tunneling
- Suppress the hot electron effect

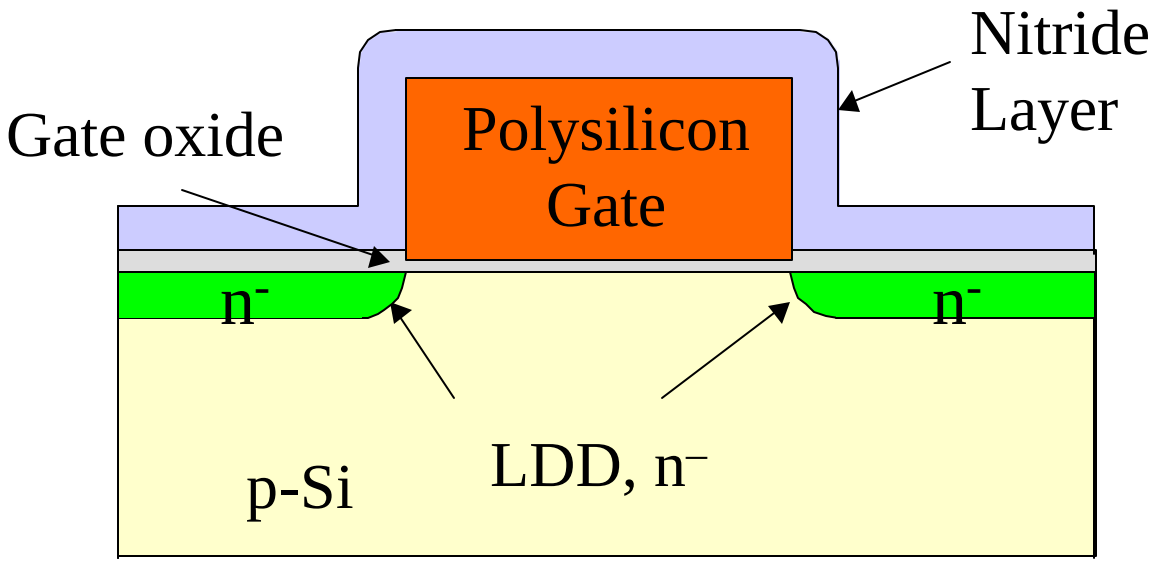
Poly Etch, PR Strip and Poly Anneal



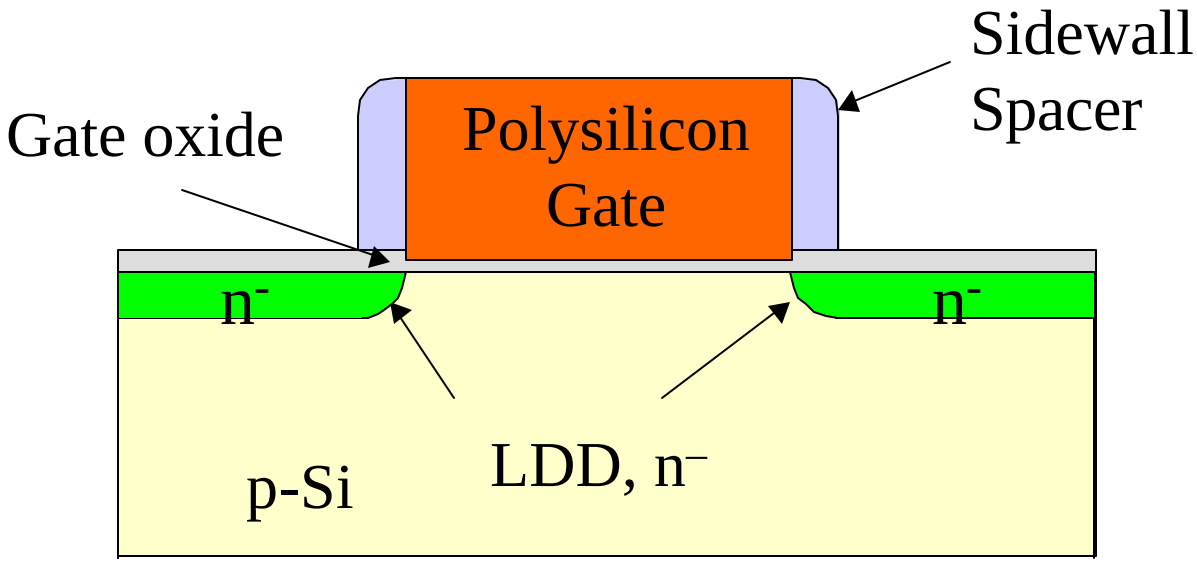
LDD implantation



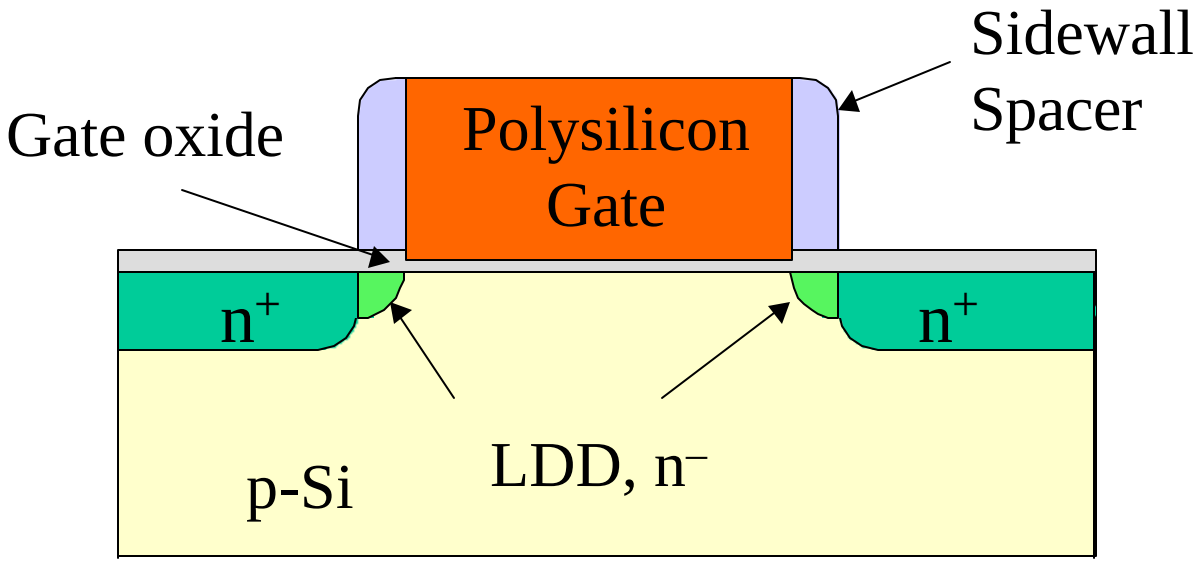
Nitride Deposition



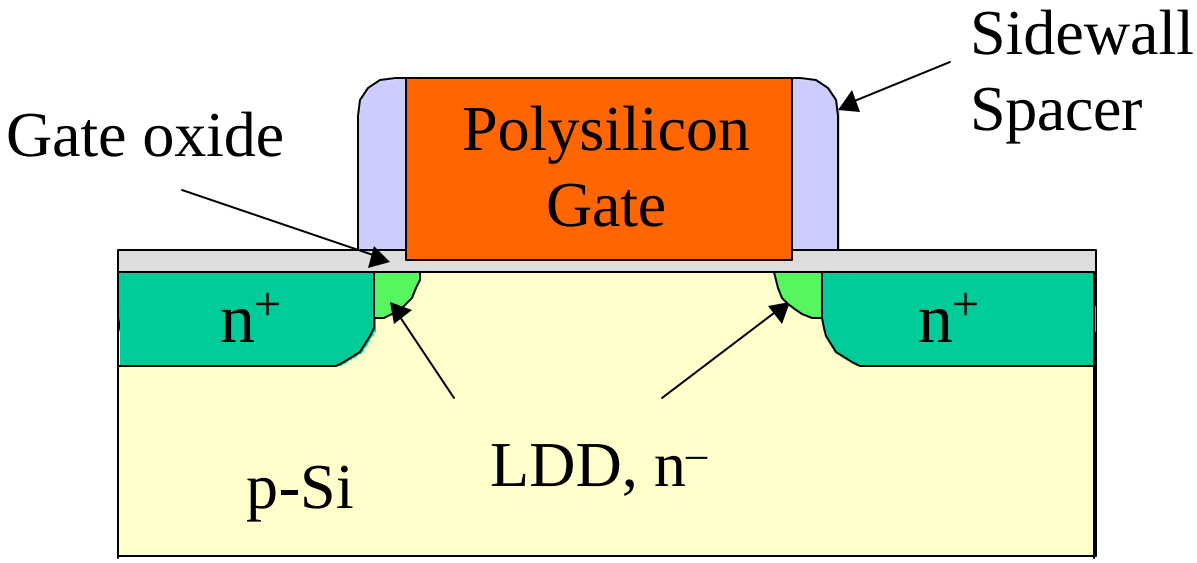
Nitride Etch Back



Source Drain Implantation



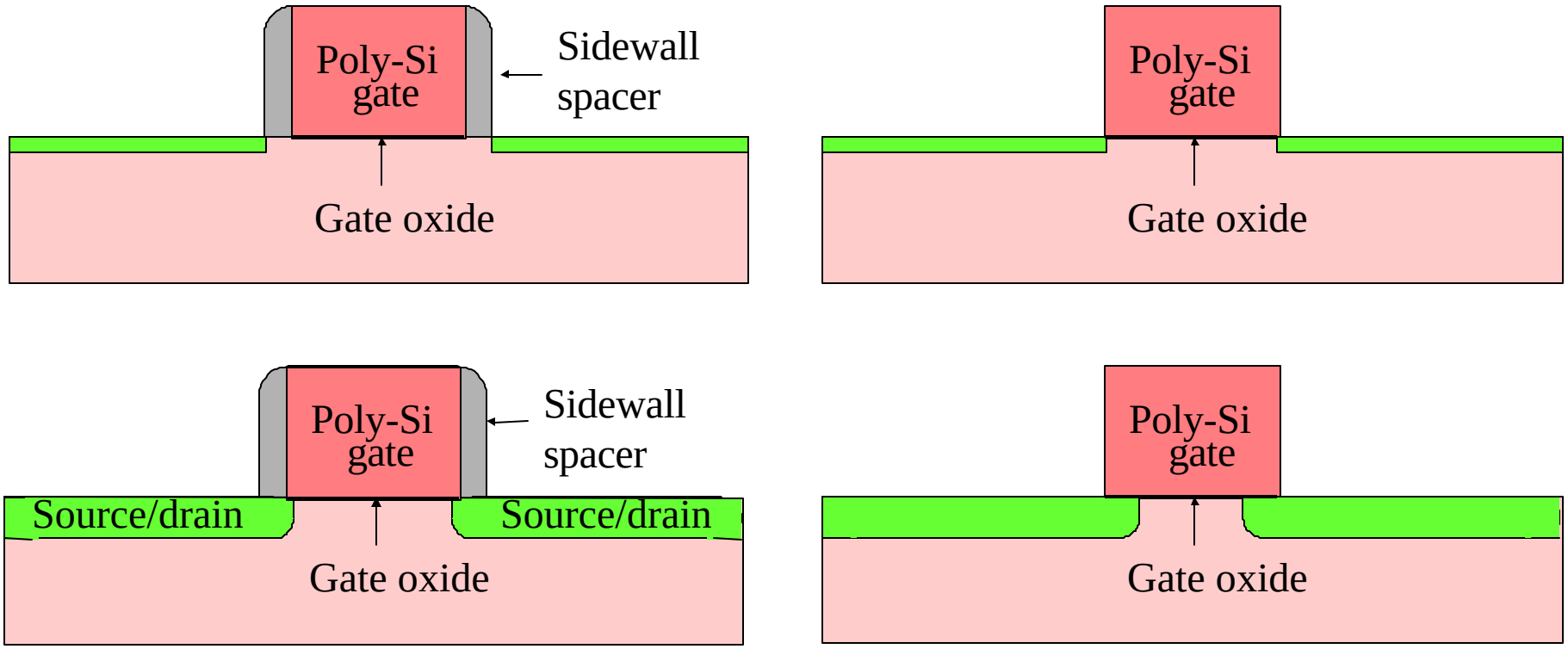
Implantation Anneal



Dopant Diffusion Buffer

- Sub-0.18 μm, and <1.5 V, hot electron effect may not be so important anymore
- The LDD implantation process probably is no longer needed.
- Sidewall spacers are still needed to provide a diffusion buffer for the dopant in the source/drain junction.

Dopant Diffusion Buffer



(a)

After anneal, source/drain are just right

(b)

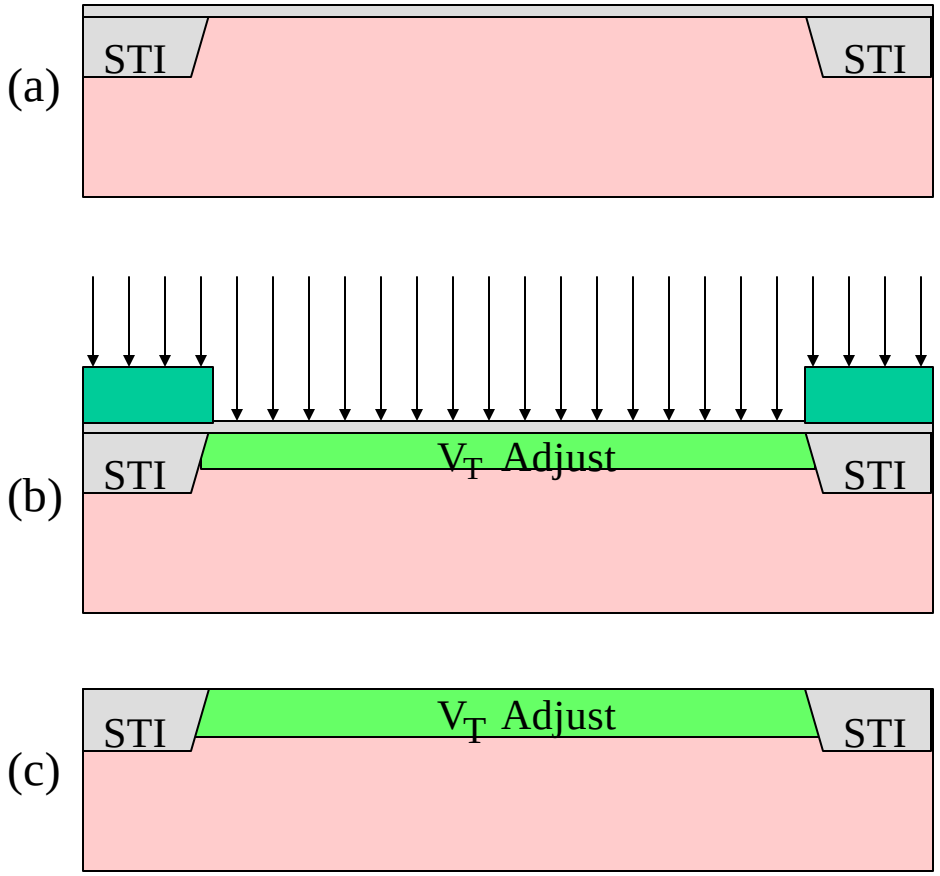
After anneal, source/drain are too close

V_T Adjustment Implantation

- Controls threshold voltage of MOSFET
  - Ensure supply voltage can turn-on or turn-off the MOSFET in IC chip
- Low energy, low current implantation
- Usually before the gate oxide growth
- Two implantations: a p-type and an n-type

V_T Adjust Implantation

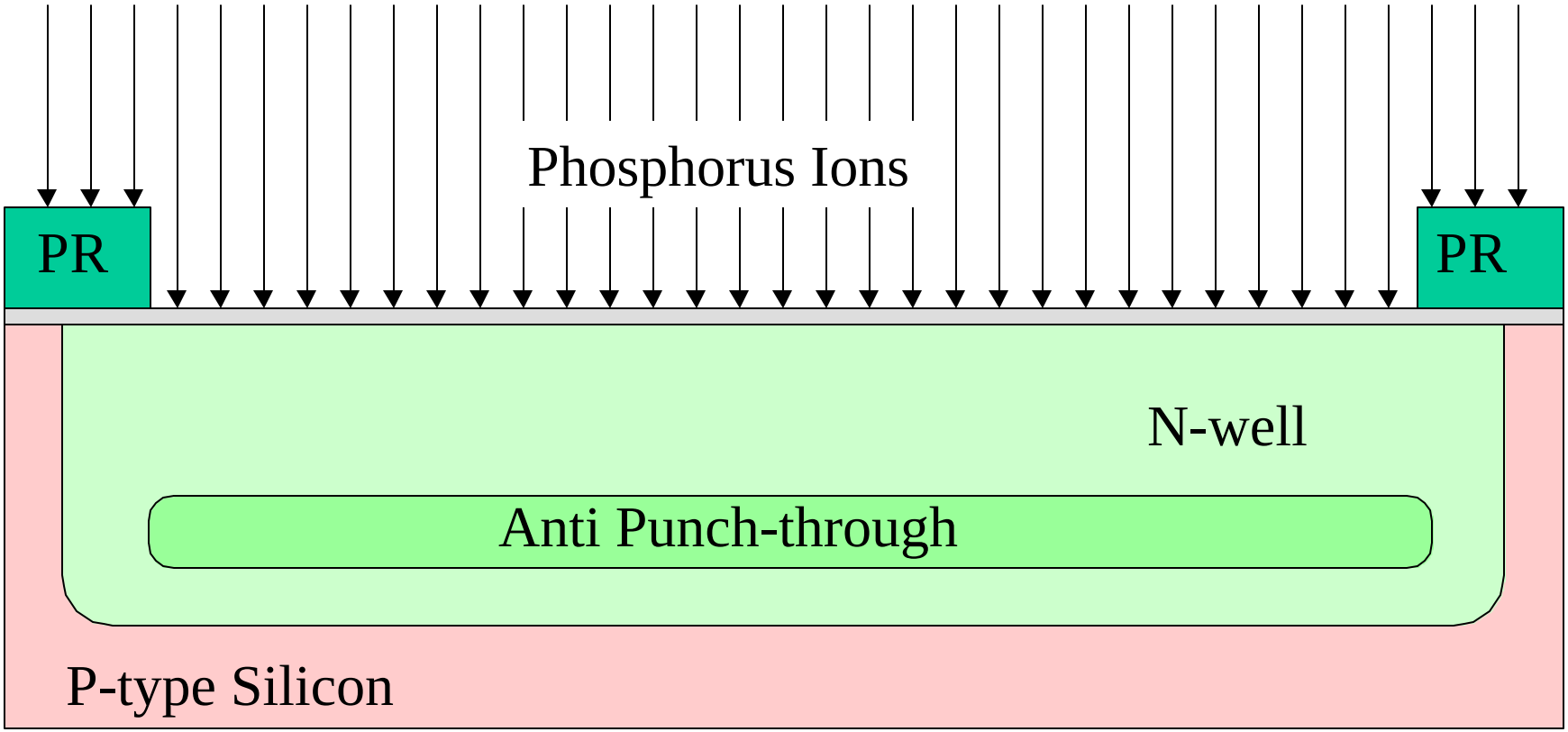
- Wafer clean
- Grow sacrificial oxide (a)
- Activation mask
- Threshold adjustment implantation (b)
- Strip photoresist
- Anneal
- Strip sacrificial oxide (c)



Anti-punch-through Implantation

- Punch-through effect
  - The depletion regions of the source and drain short each other under the influence of both gate-substrate bias and source-drain bias
- Anti punch-through implantation
  - Medium energy, low current
  - Protects transistors against punch-through
  - Normally performed with well implantation

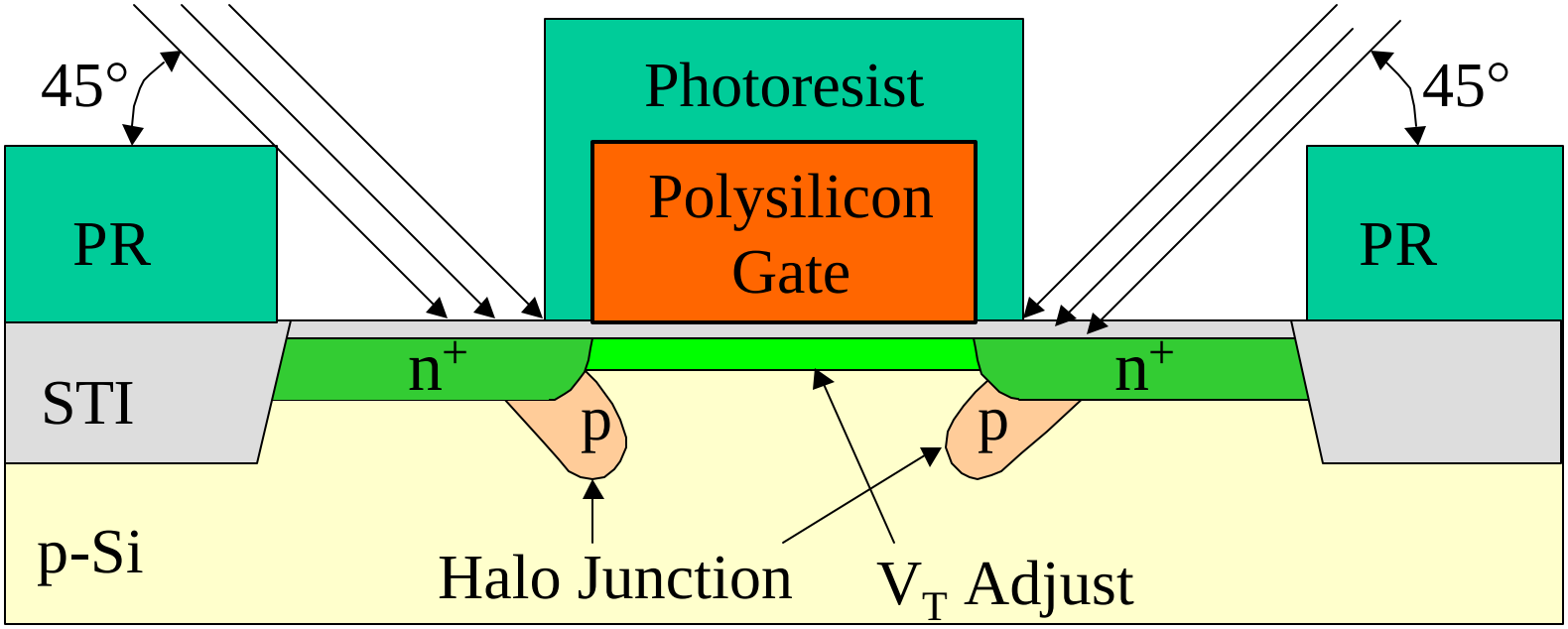
Anti Punch-through Implantation



Halo Implantation

- Another implantation process commonly used to suppress punch through effect
- Low energy and low current
- Large incident angle, 45°

Halo Implantation



High-κ Gate Dielectric

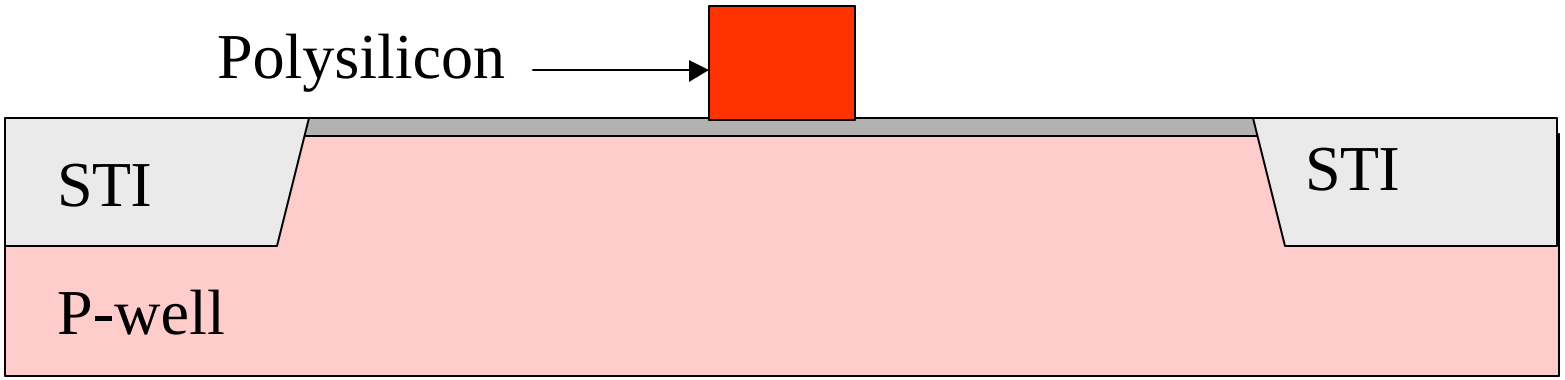
- Device sizes shrinking, t_{ox} is too thin for MOSFET to operate reliably even at 1 V
- Need high-κ dielectric to replace SiO_2 as gate dielectric material for < 0.1 μm device
  - High-κ, thicker gate dielectric, better prevention of tunneling and breakdown
  - Large enough gate capacitance to hold enough charges to turn-on the MOSFET

Metal Gate

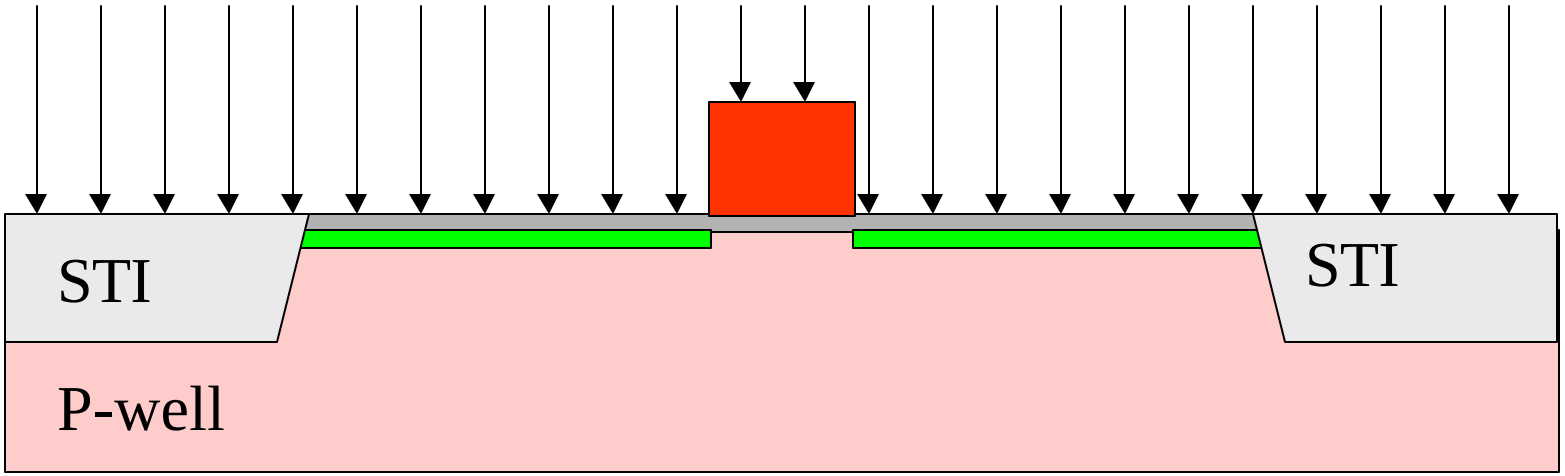
- Lower resistivity
- Help to improve device speed

- A possible future transistor making process
- Metal and high-κ dielectric gate

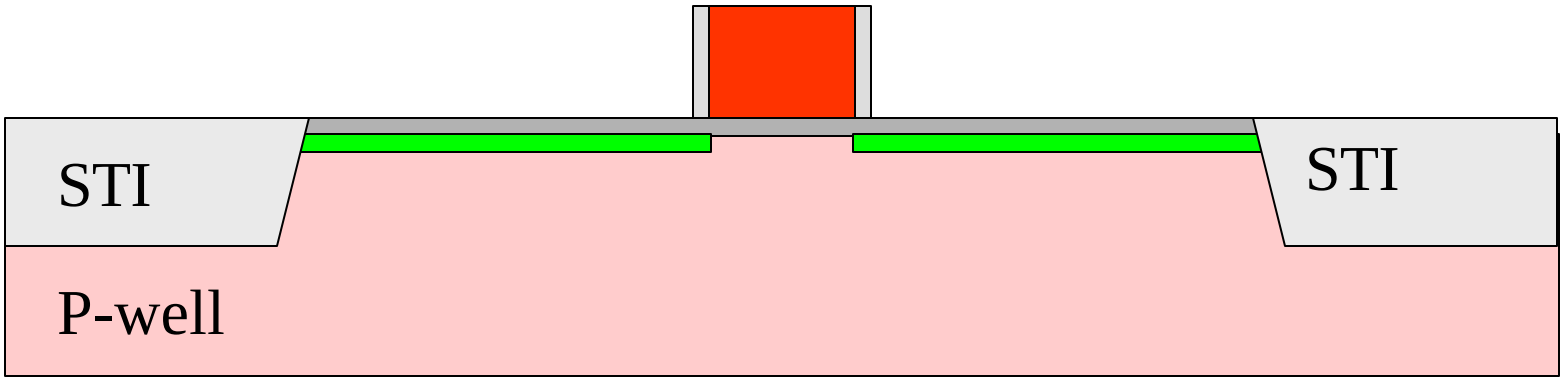
Strip Photoresist



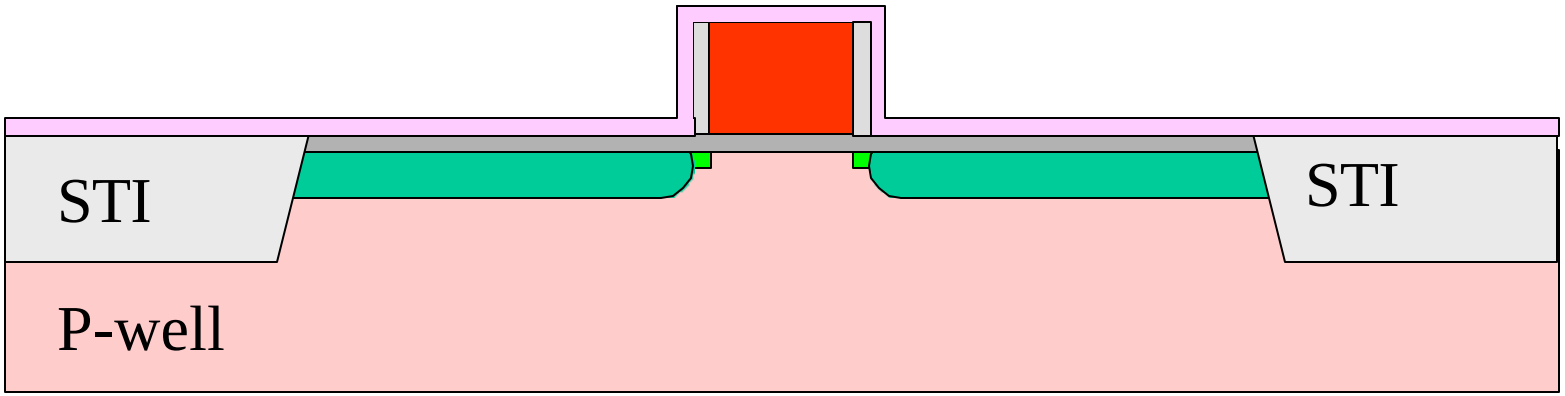
Extension Ion Implantation



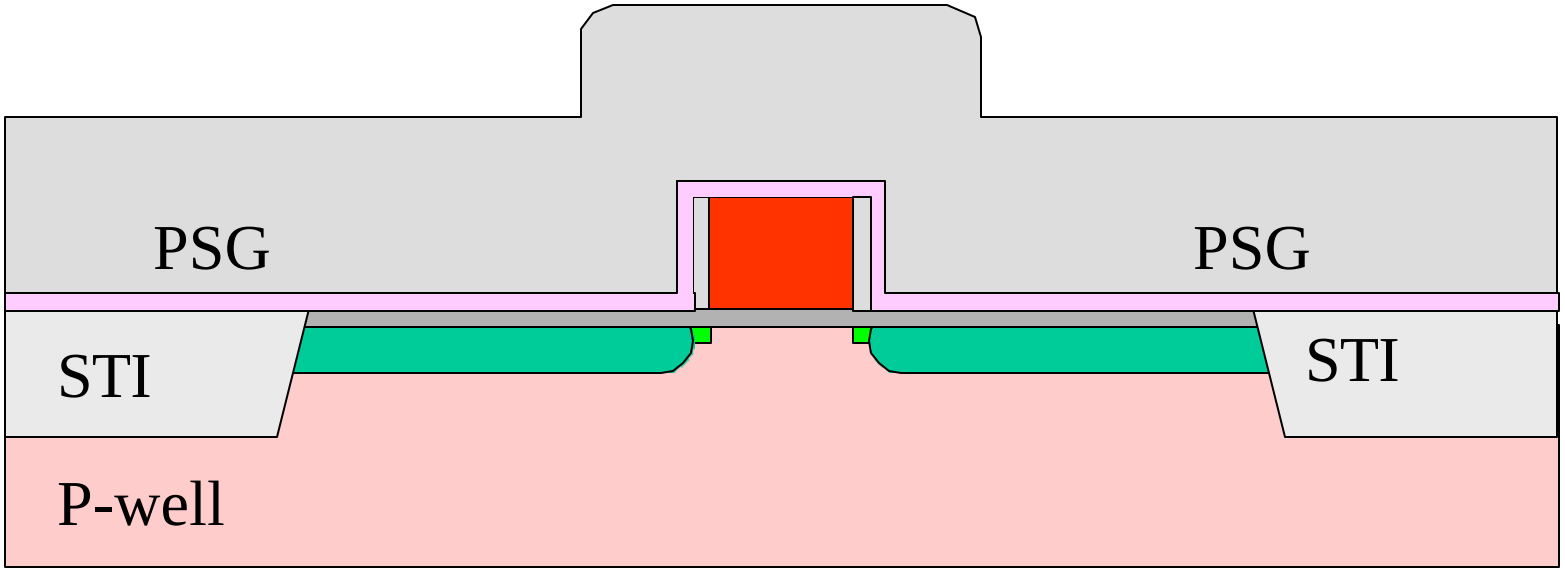
Oxide/Nitride Etch Back,



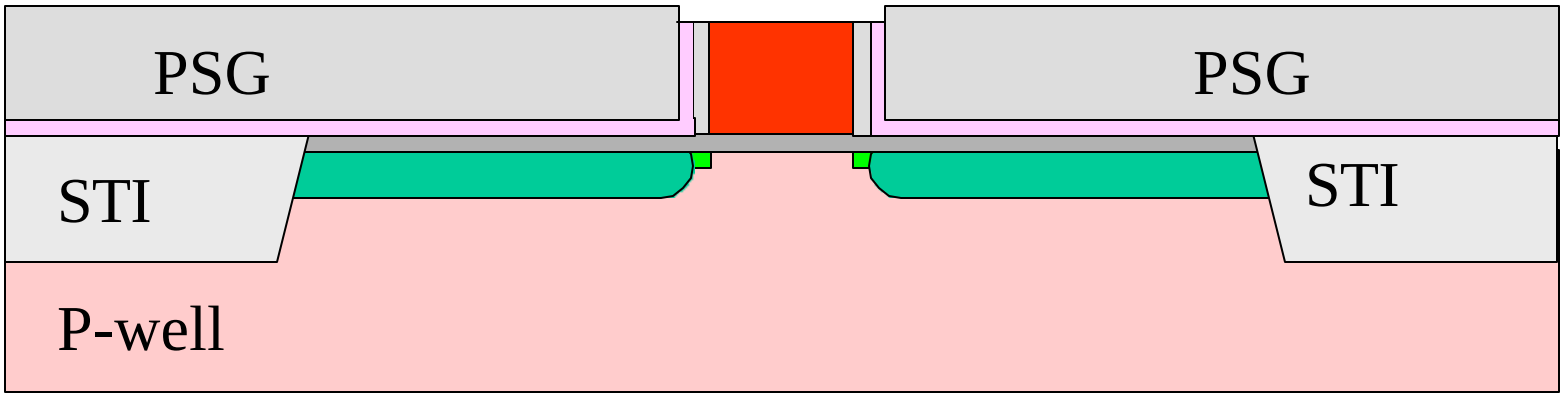
RPCVD Nitride



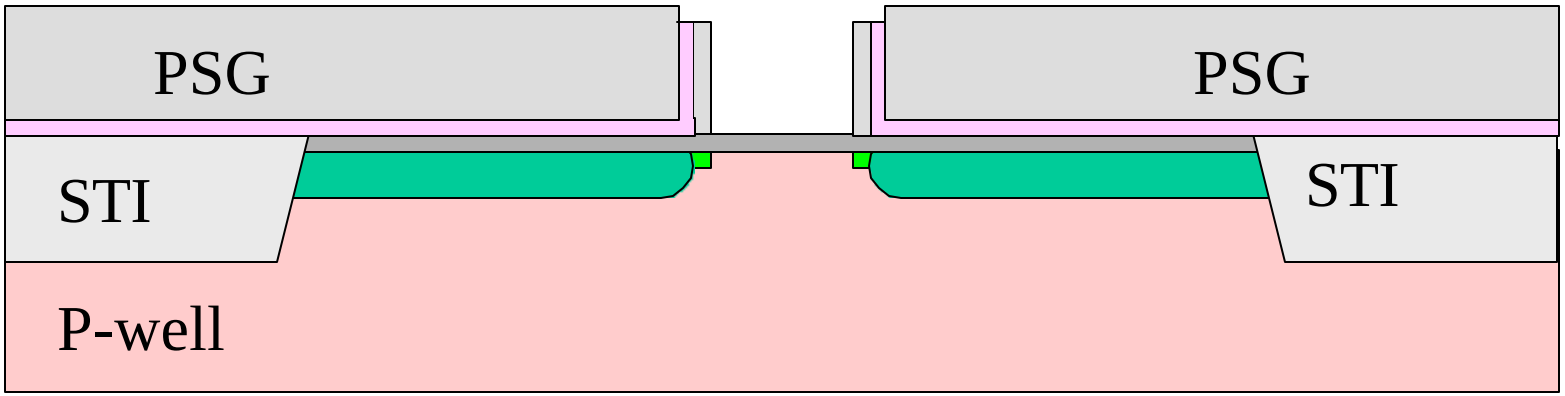
CVD PSG



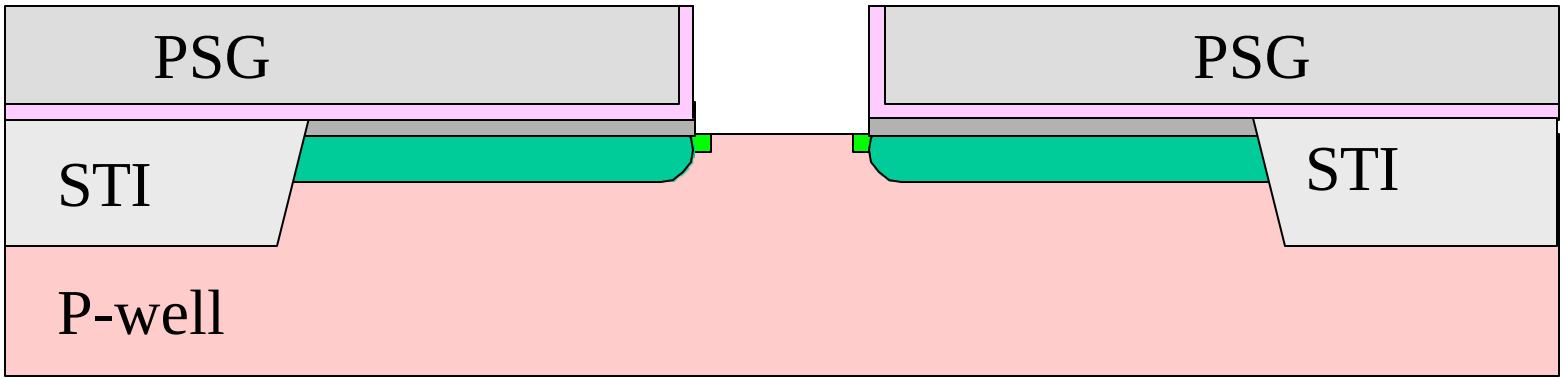
Strip Nitride



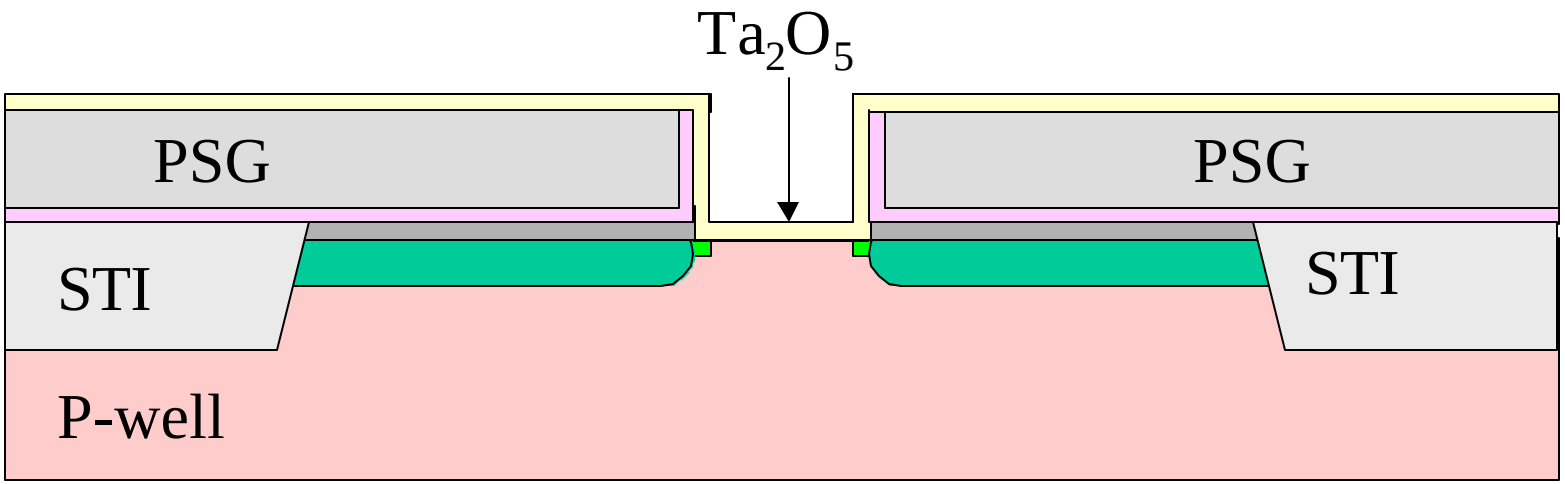
Strip Polysilicon



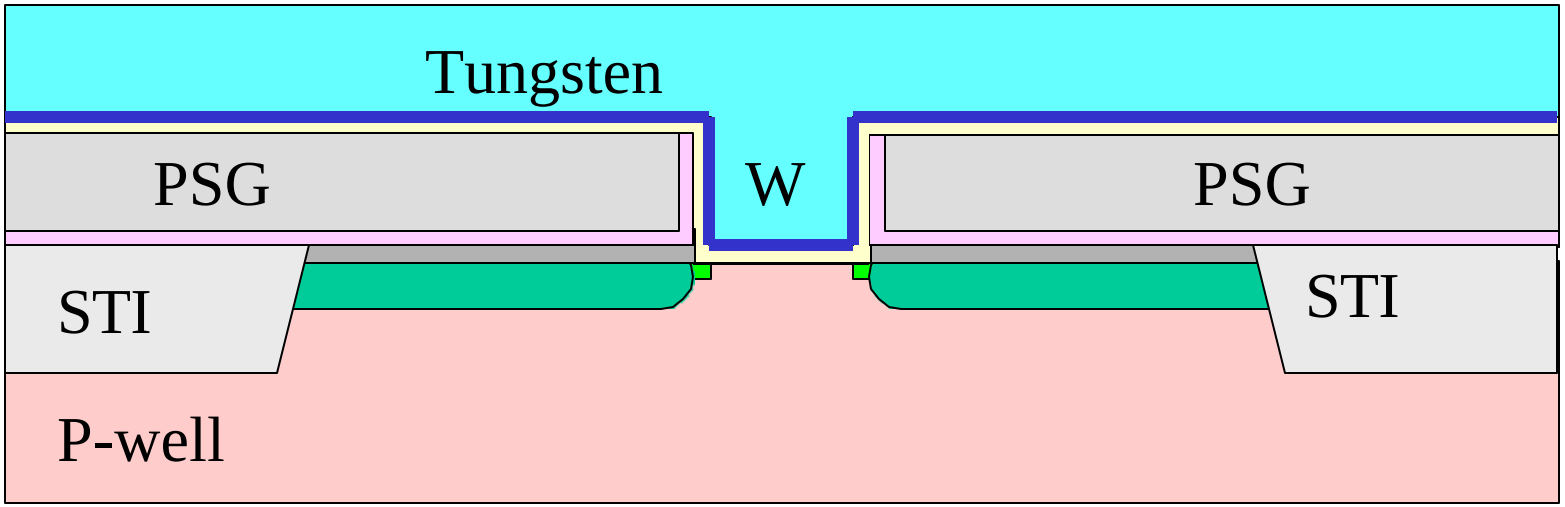
Strip Oxide



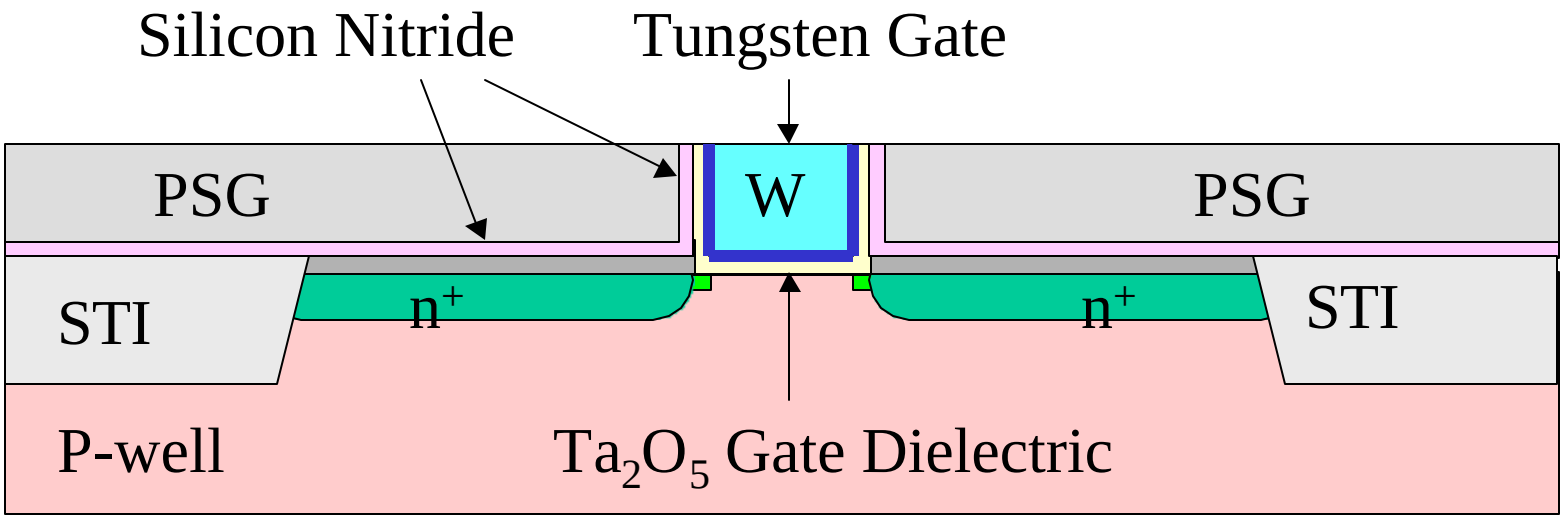
Deposit (Ta_2O_5) and RTA



CVD Tungsten



CMP Tantalum Pentaoxide



Metal and High-κ Gate MOSFET Dummy Gate Process

- For < 0.1 μm IC device
- PSG CMP, polysilicon and oxide stripping, and high-κ dielectric deposition.
- Ta_2O_5, κ ~ 25, TiO_2 κ up to 80, and HfO_2
- CVD plus RTA process
- It may never be used due to complexity
- Advantage: can used Ta_2O_5 hard hard to etch.

Metal and High-κ Gate MOSFET Traditional Process

- Traditional MOSFET making process in R&D
  - Dielectric deposition and annealing
  - Metal deposition
  - Photolithography
  - Metal etch
  - Ion implantation
  - Rapid thermal annealing.
- Too early to predict which method will win

Interconnection

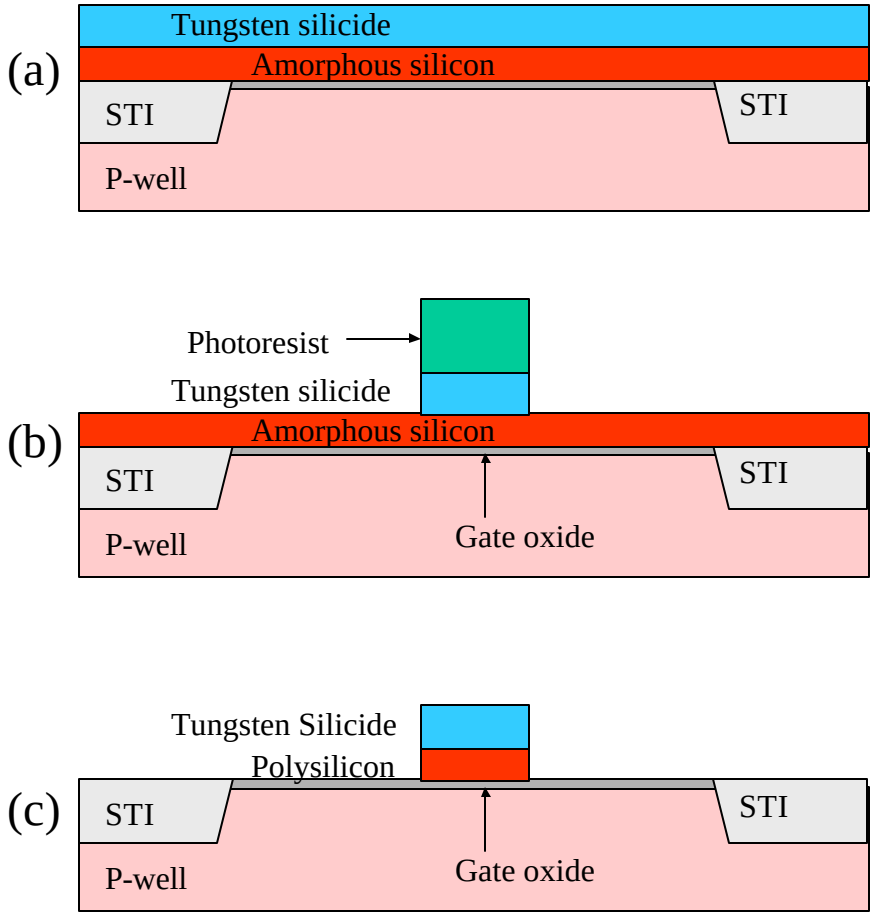
- Making transistor: front-end
- Interconnection: back-end
  - Multi metal layers with dielectric in between
  - Local interconnection: silicide
  - PMD: doped oxide, PSG or BPSG
  - W and Al alloy metallization
  - IMD: USG and FSG
  - Transition to copper and low-κ interconnection

Local Interconnection

- Connection between neighboring transistors
- Usually polysilicon or polycide stack
- WSi_2, $TiSi_2$, and $CoSi_2$ are commonly used
  - WSi_x: CVD process with WF_6 and SiH_4
- $TiSi_2$: PVD Ti on Si then thermal anneal

Tungsten Silicide Process

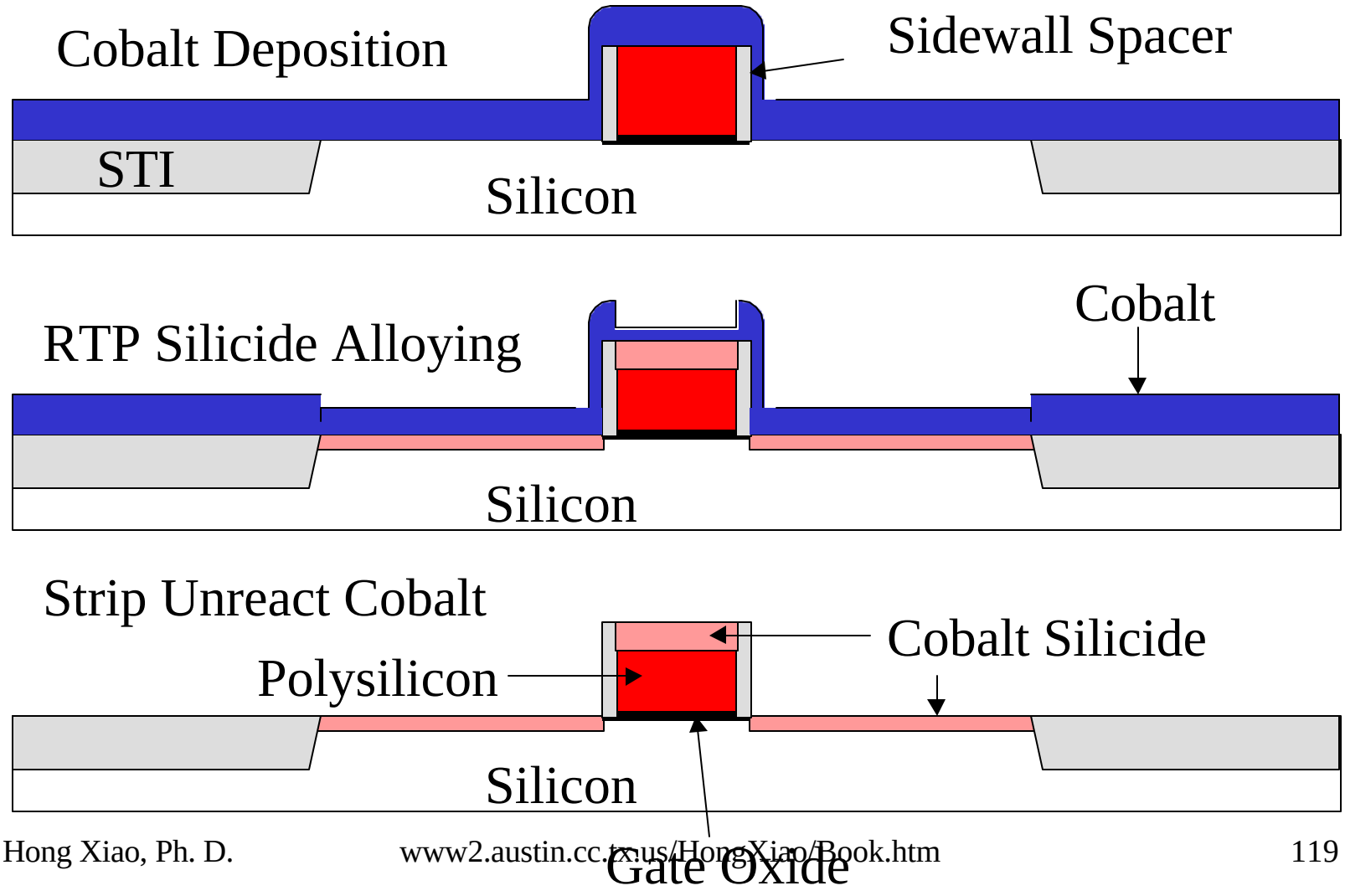
- Wafer clean
- Grow gate oxide
- Deposited amorphous silicon
- Deposited tungsten silicide (a)
- Gate and local interconnection mask
- Etch tungsten silicide (fluorine chemistry) (b)
- Etch amorphous silicon (chlorine chemistry)
- Strip photoresist
- Polysilicon and silicide annealing (c)



Self-aligned Silicide (Salicide)

- $TiSi_2$ and $CoSi_2$
- Lower resistivity than WSi_2
- $TiSi_2$ when gate size > 0.2 μm
- $CoSi_2$ when gate size < 0.2 μm
- Metal (Ti or Co) PVD
- Thermal anneal to form silicide
- Strip unreacted metal

Cobalt Self-aligned Silicide Process



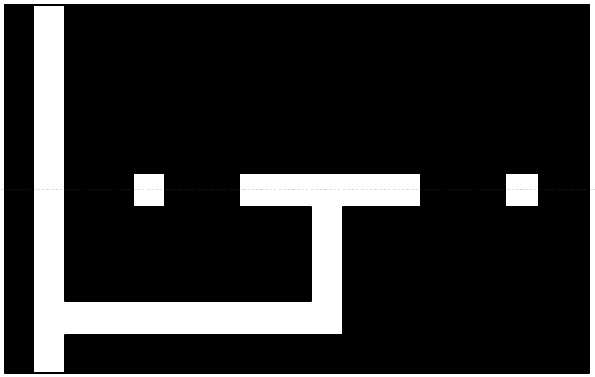
Tungsten Local Interconnection

- Lower resistance, higher speed, less power
- Damascene: similar to W plug formation
  - Etched trenches are in silicate glass layer
  - Deposit Ti and TiN barrier/adhesion layers
  - CVD W fill trenches
  - CMP to remove bulk W from wafer surface
  - W left in trenches to form local interconnection

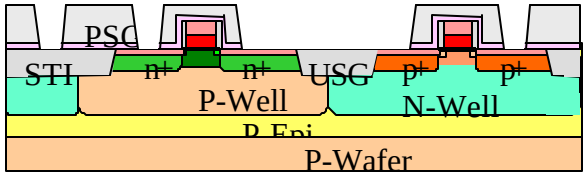
Tungsten Local Interconnection

- CMP PSG
- Wafer clean
- Local interconnection mask (a)
- Etch PSG
- Strip photoresist
- Wafer clean (b)
- Argon sputtering clean
- Sputtering Ti
- Sputtering TiN
- CVD TiN
- TiN treatment
- CVD Tungsten (c)
- CMP Tungsten
- CMP titanium and titanium nitride (d)
- Wafer clean

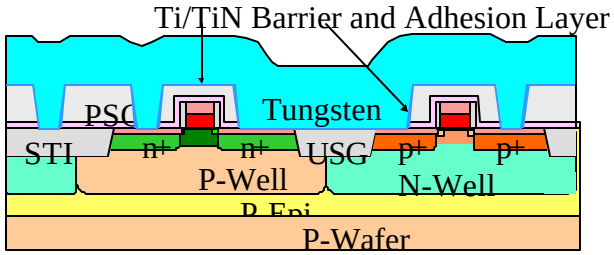
(a)



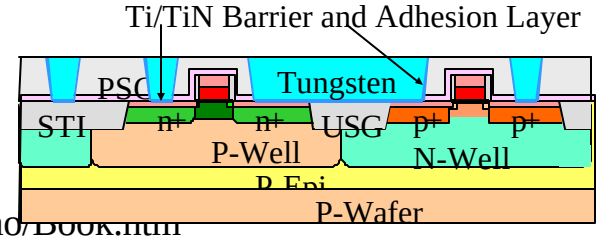
(b)



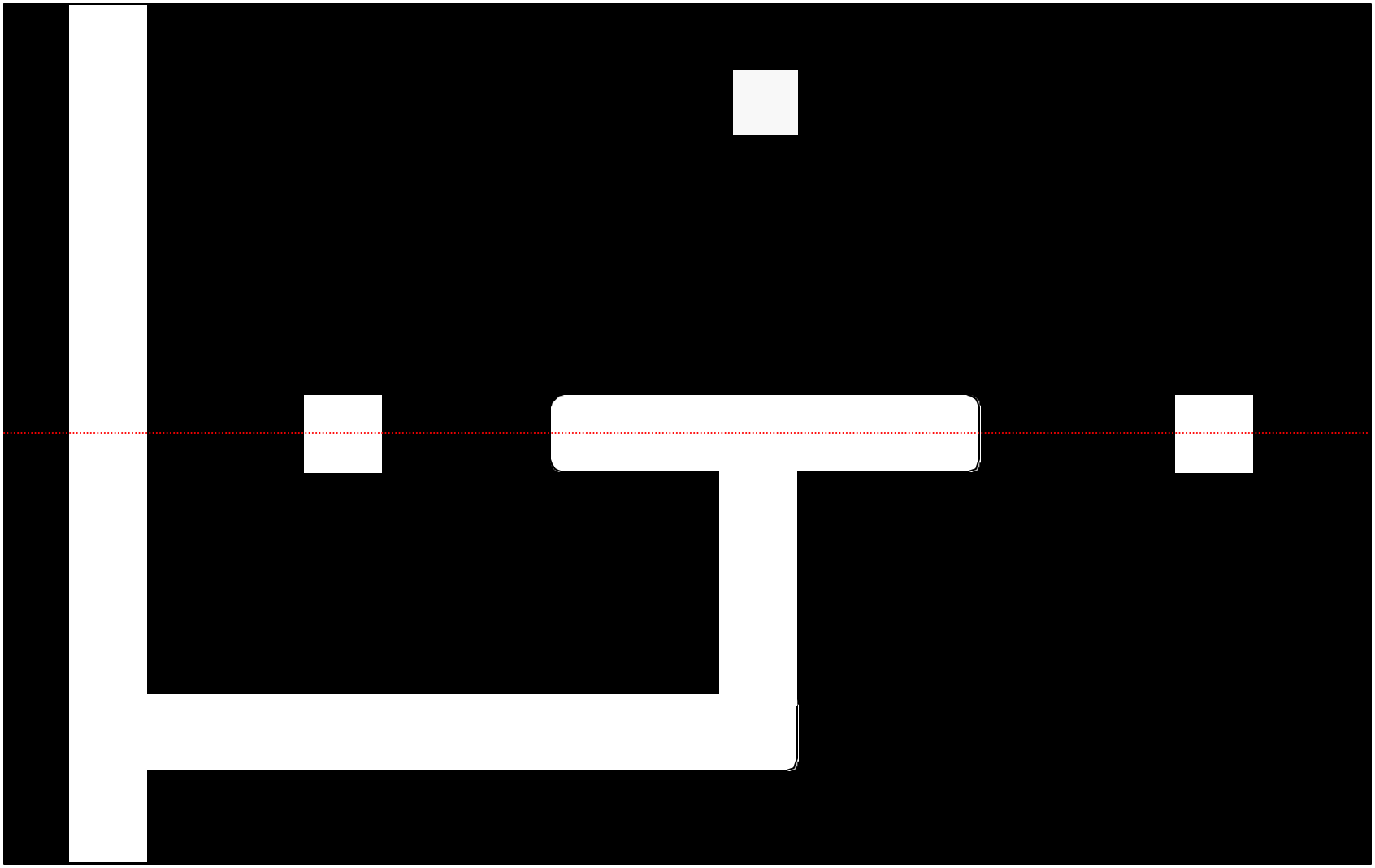
(c)



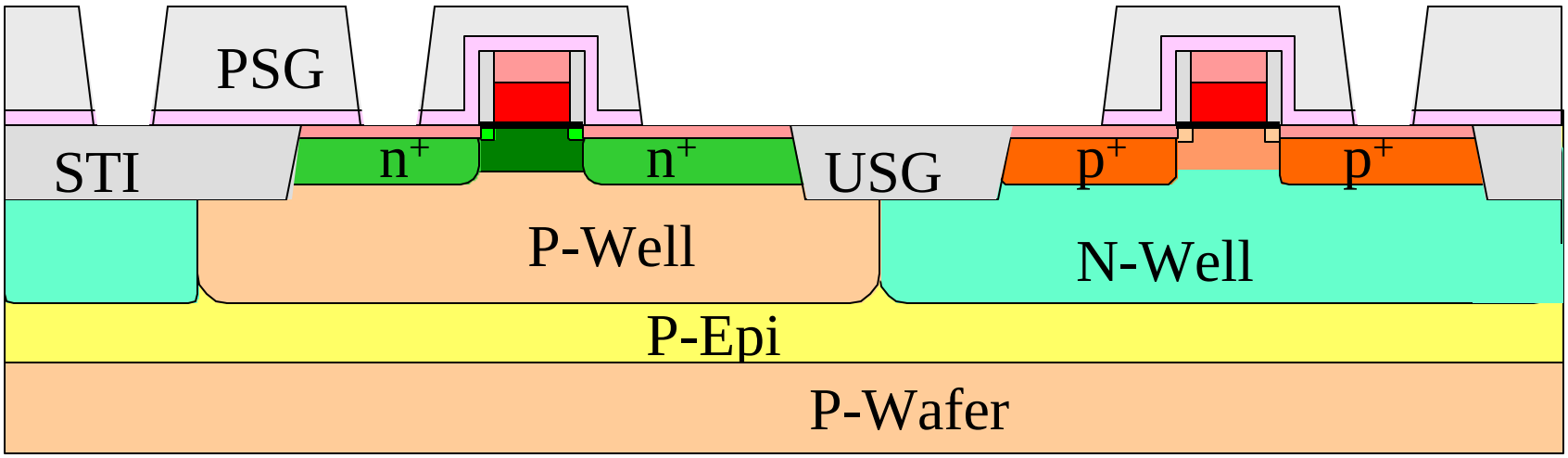
(d)



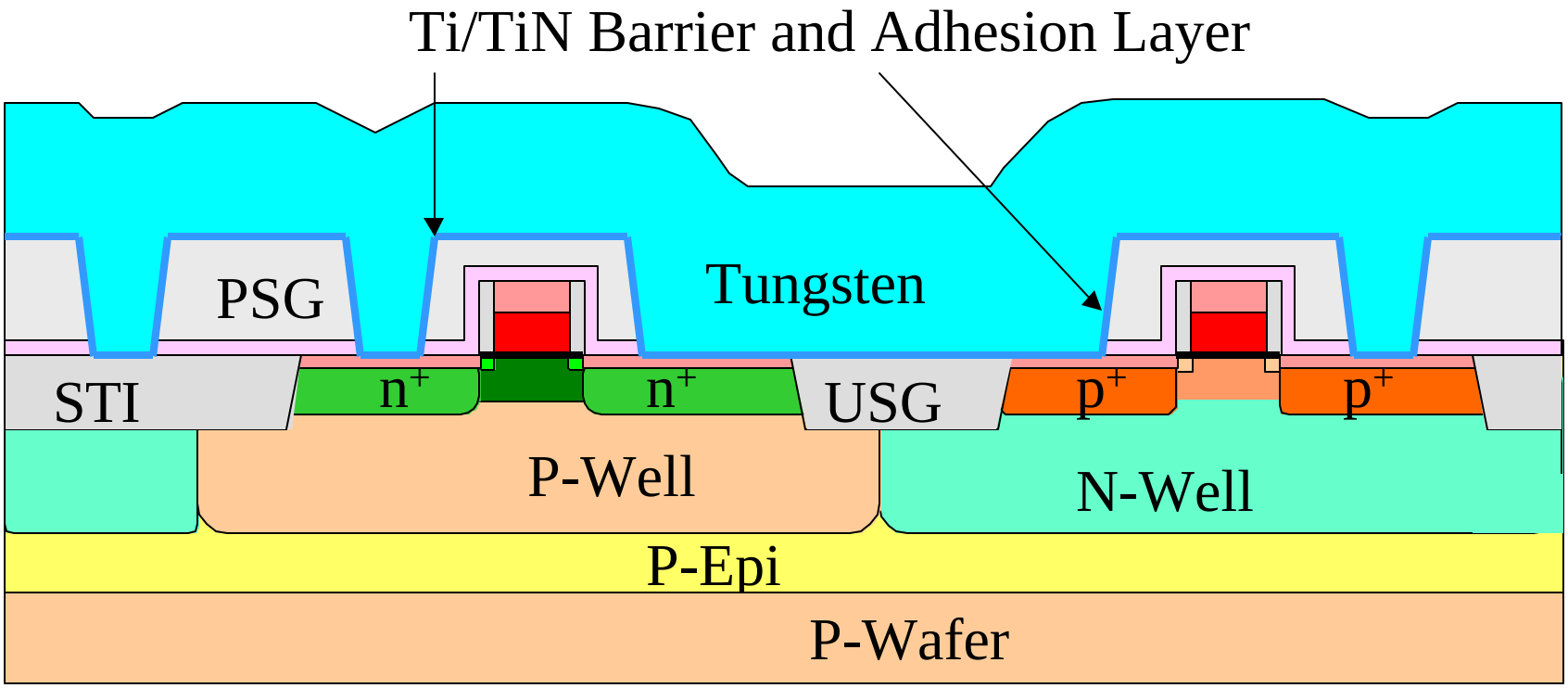
Mask 10: Local Interconnection



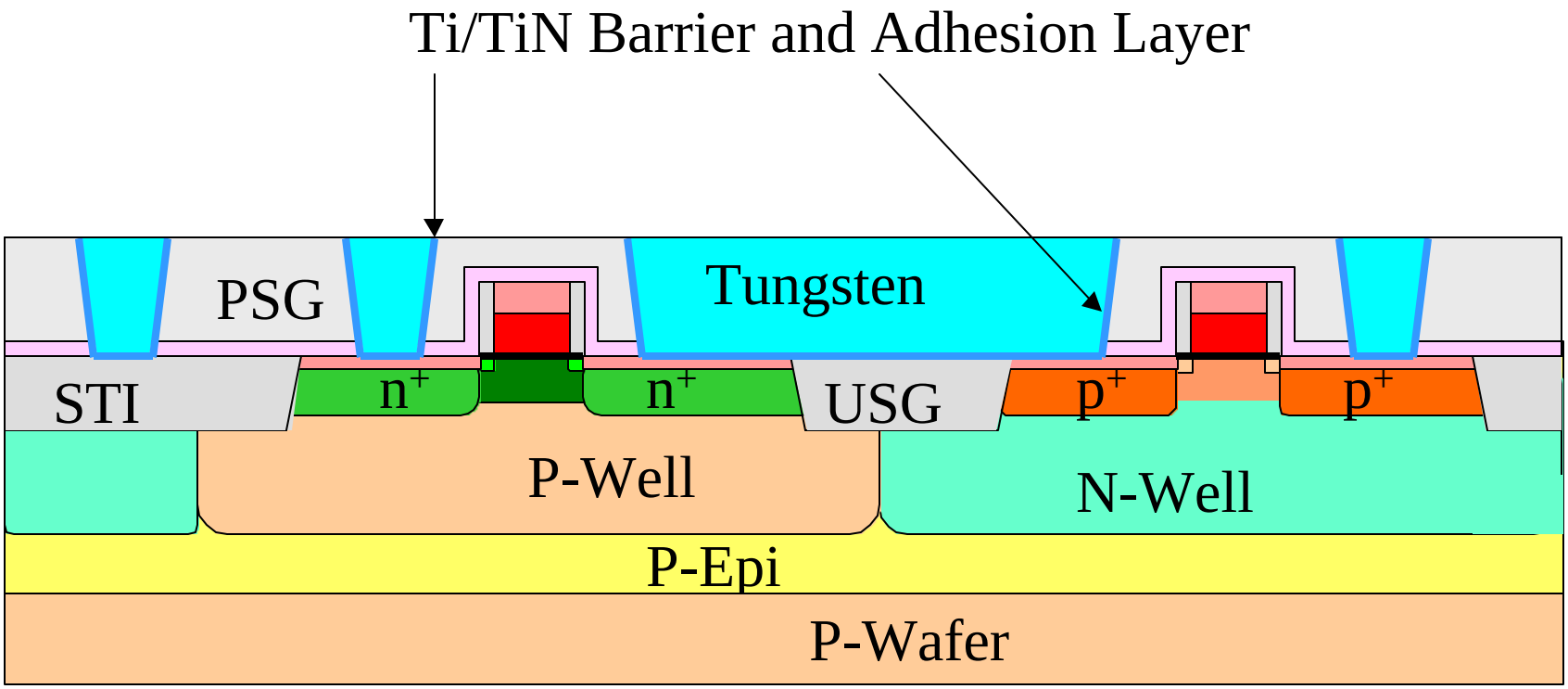
Strip Photoresist/Clean



PVD Ti/TiN and CVD TiN/W



CMP W/TiN/Ti, Clean



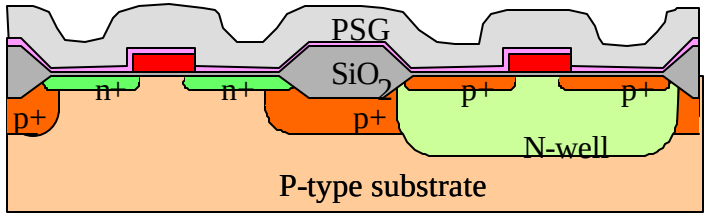
Early Global Interconnection

- Oxide CVD
- Photolithography, oxide etch, and PR strip
- Metal PVD
- Photolithography, metal etch, and PR strip
  - Oxide etch forms contact or via holes
  - metal etch forms interconnection lines

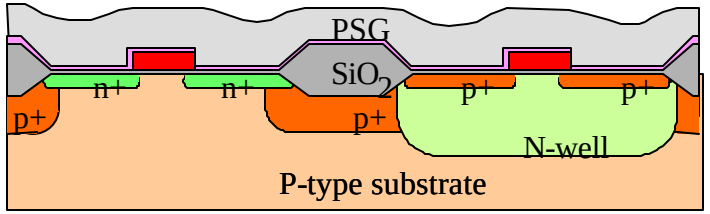
Early Aluminum Interconnection

- CVD PSG (a)
- PSG reflow (b)
- Wafer clean
- Contact hole mask
- Etch PSG
- Strip photoresist (c)
- Wafer clean
- Deposit Al alloy (d)
- Metal interconnection mask
- Etch metal
- Strip photoresist (e)
- Metal anneal

(a)



(b)



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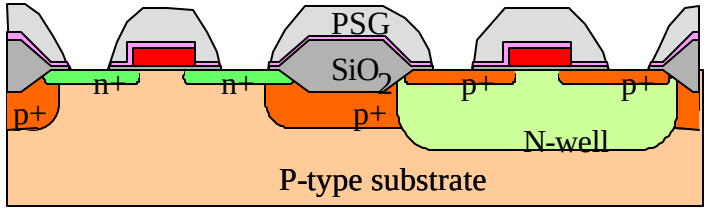

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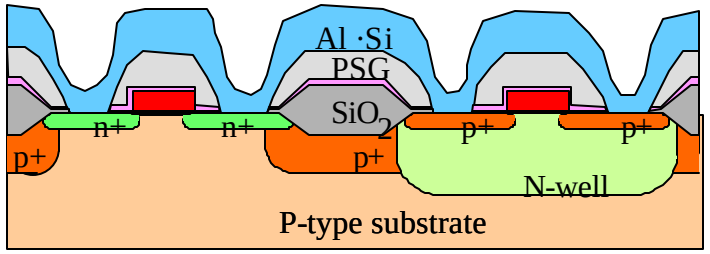

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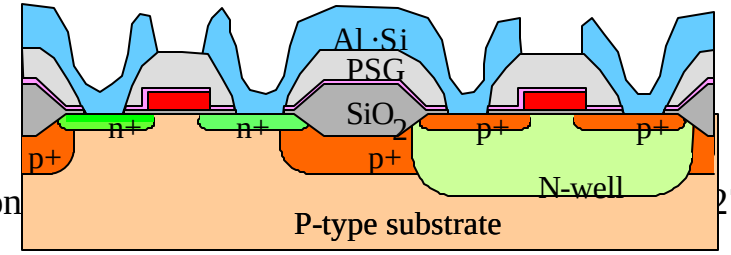


Multi-level Interconnection

- Earlier interconnection has rough surface
- problems in photolithography and metal PVD
- Tungsten to fill narrow contact and via holes

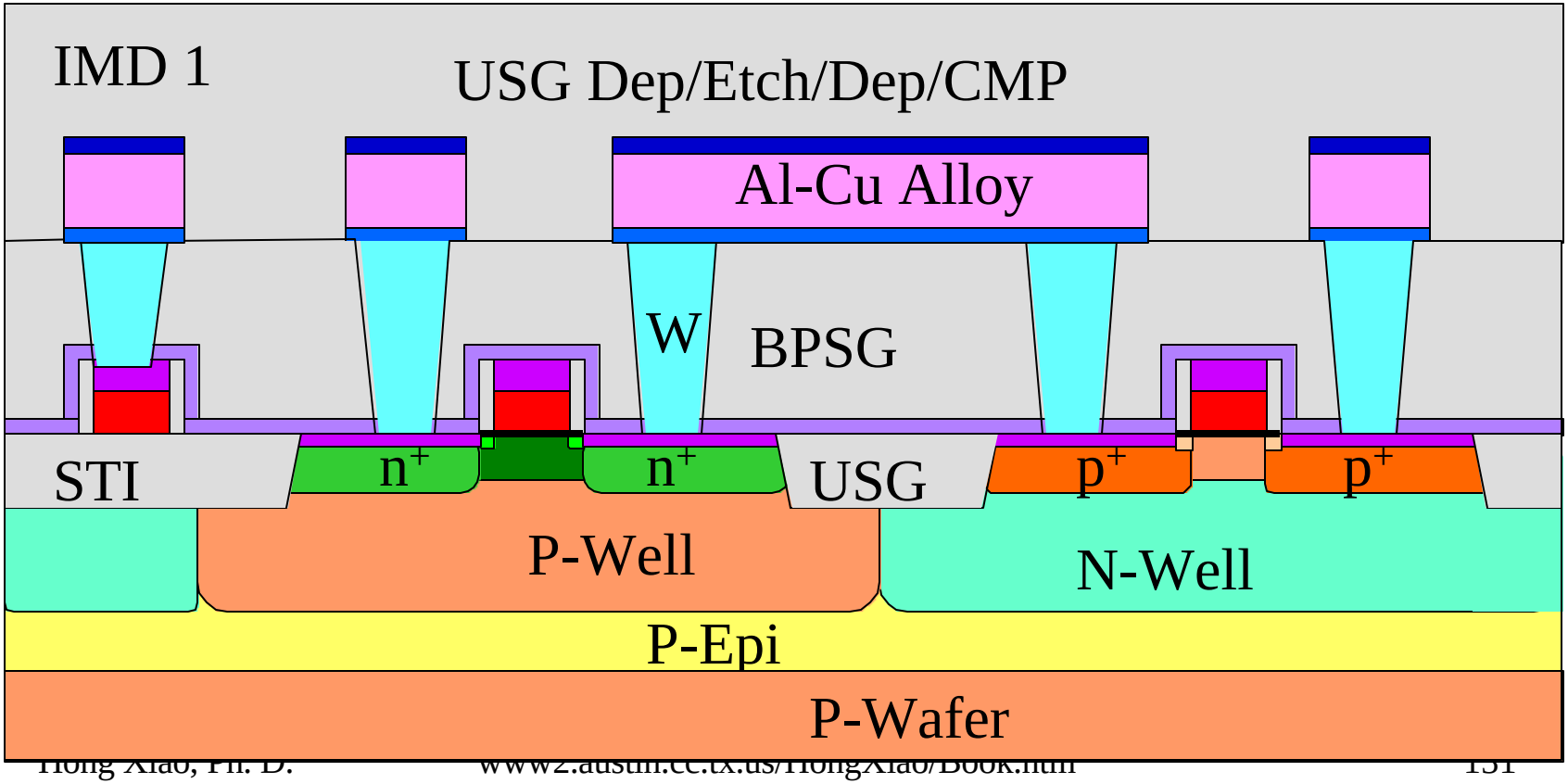
Multi-level Interconnection

- The basics interconnection process steps:
  - Dielectric CVD and planarization
  - Photolithography, oxide etch, and PR strip
  - W CVD, bulk W removal
  - Metal stack PVD,
  - Photolithography, oxide etch, and PR strip
- PSG or BPSG for PMD and USG for IMD

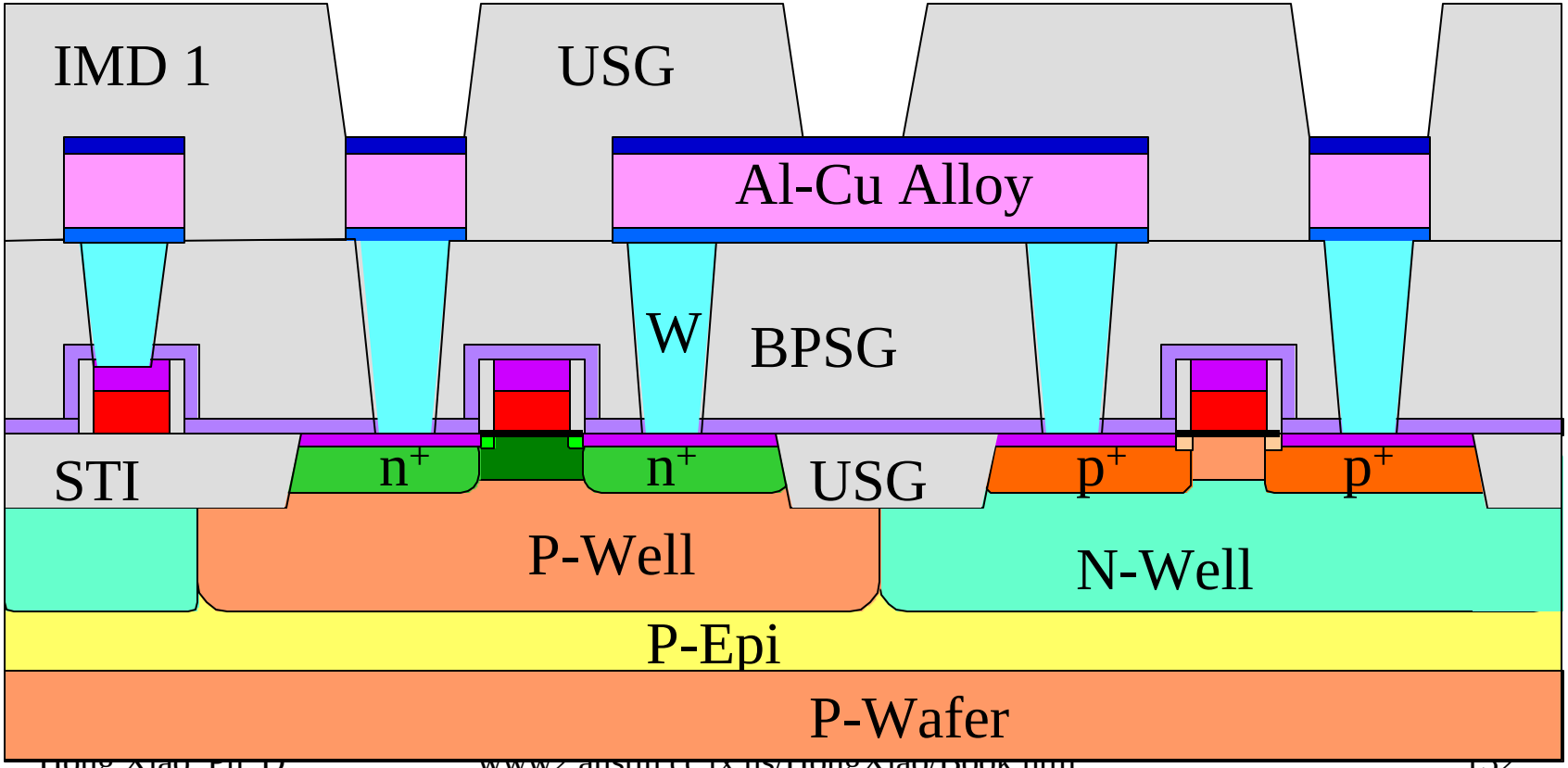
Multi-level Interconnection

- Dielectric CMP for planarization
- W CMP to removal bulk tungsten
- Metal stack: Ti welding layer, Al·Cu alloy, and TiN ARC
- Metal etch defines metal interconnection lines

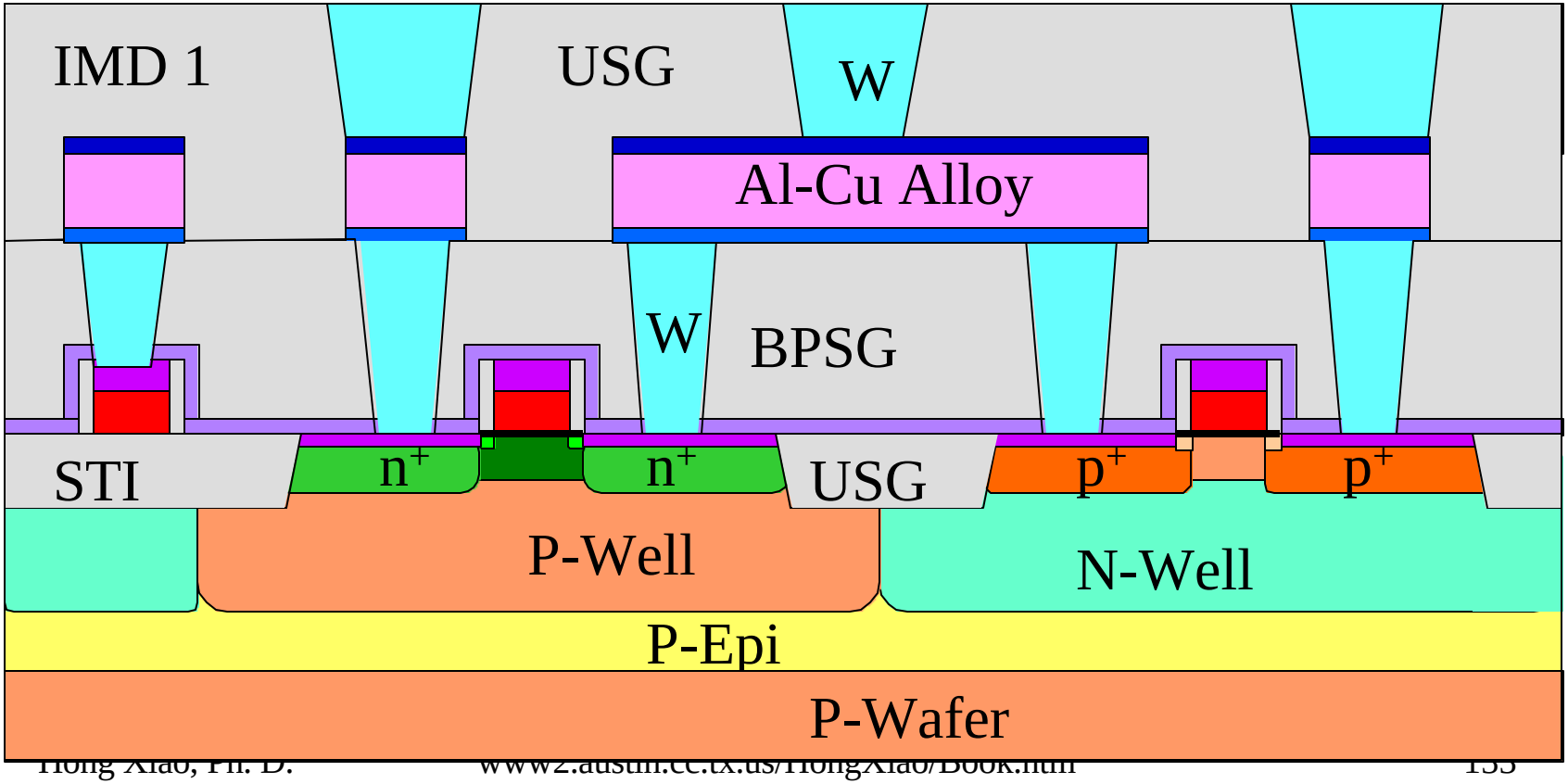
PE-TEOS USG Dep/Etch/Dep/CMP



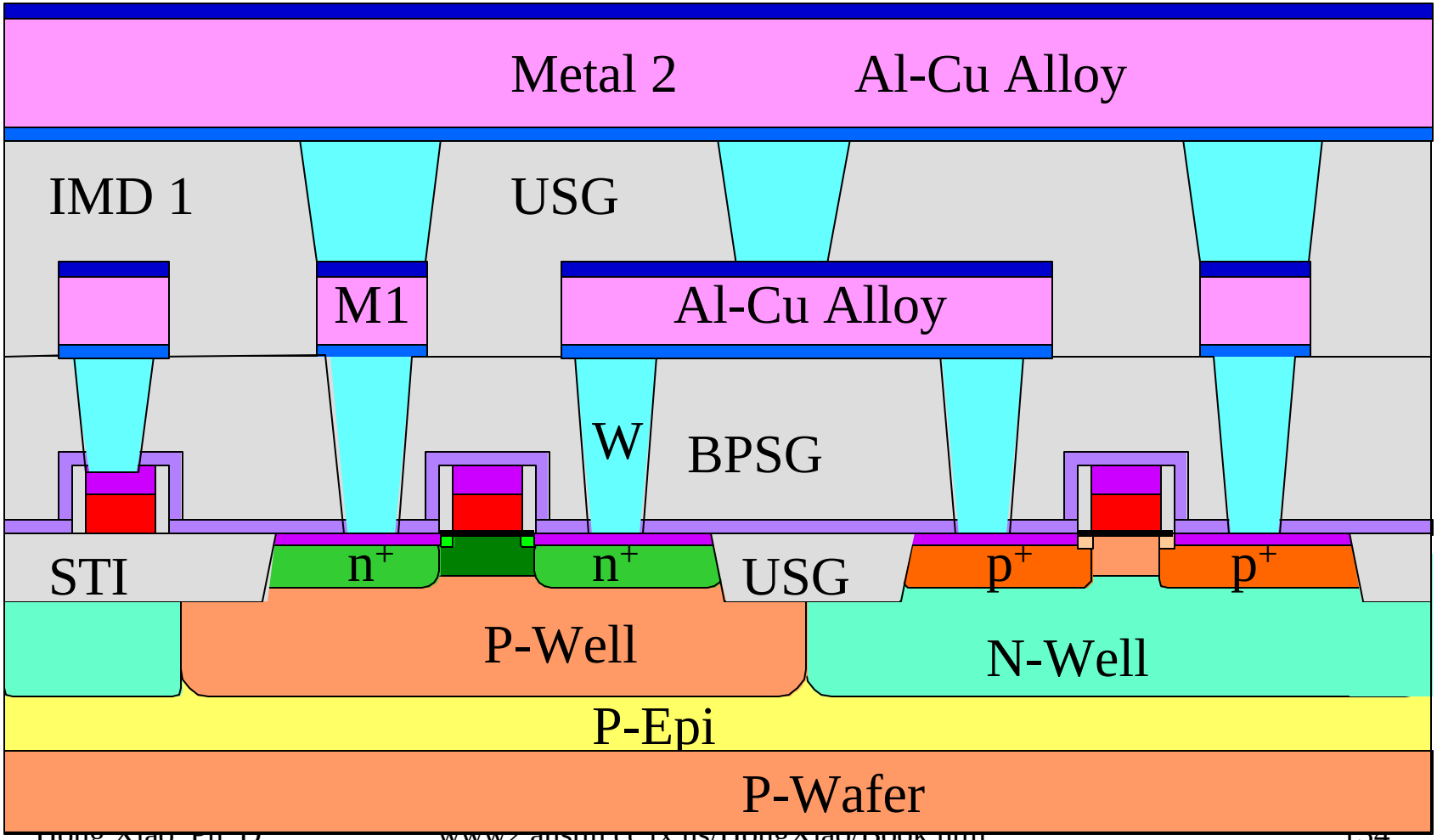
Via Etch, Etch USG



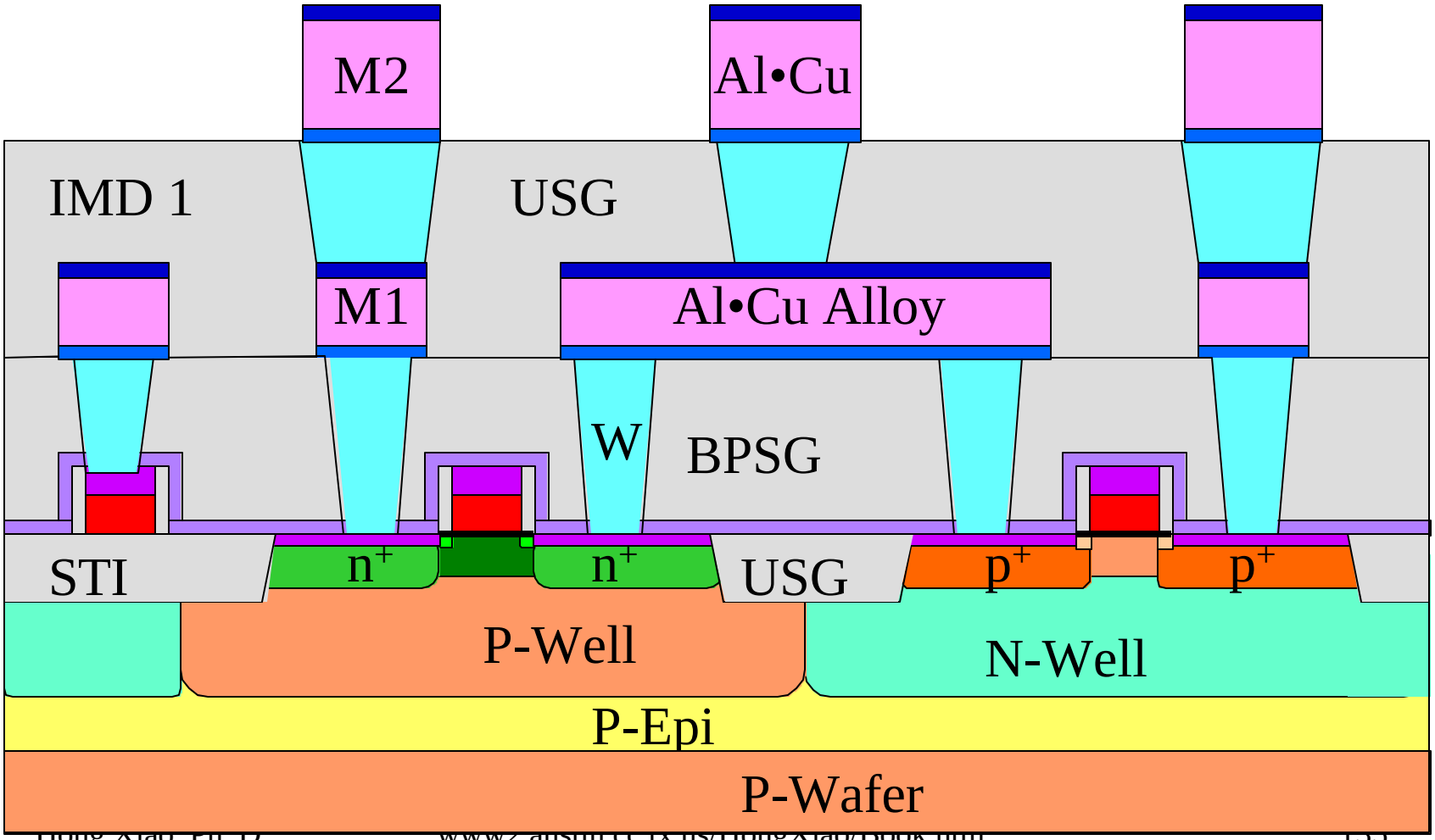
Tungsten CVD and CMP



Via Etch, Etch USG



Etch Metal 2


M2
Al•Cu
IMD 1
USG
M1
Al•Cu Alloy
W
BPSG
STI
n+
n+
USG
p+
p+
P-Well
N-Well
P-Epi
P-Wafer

Copper Interconnection

- Lower resistivity and higher resistance toelectromigration than aluminum alloy
- Faster and reliable interconnection
- Hard to dry etch delayed copper application
- CMP developed and matured in the 1990s
- Used in bulk W removal for plug formation
- Copper process is similar to W plug process

Copper Interconnection

- Trenches are etched on dielectric surface
- Copper is deposited into the trenches
- CMP removes bulk copper layer on surface
- Copper lines embedded in dielectric layer
- No need for metal etch

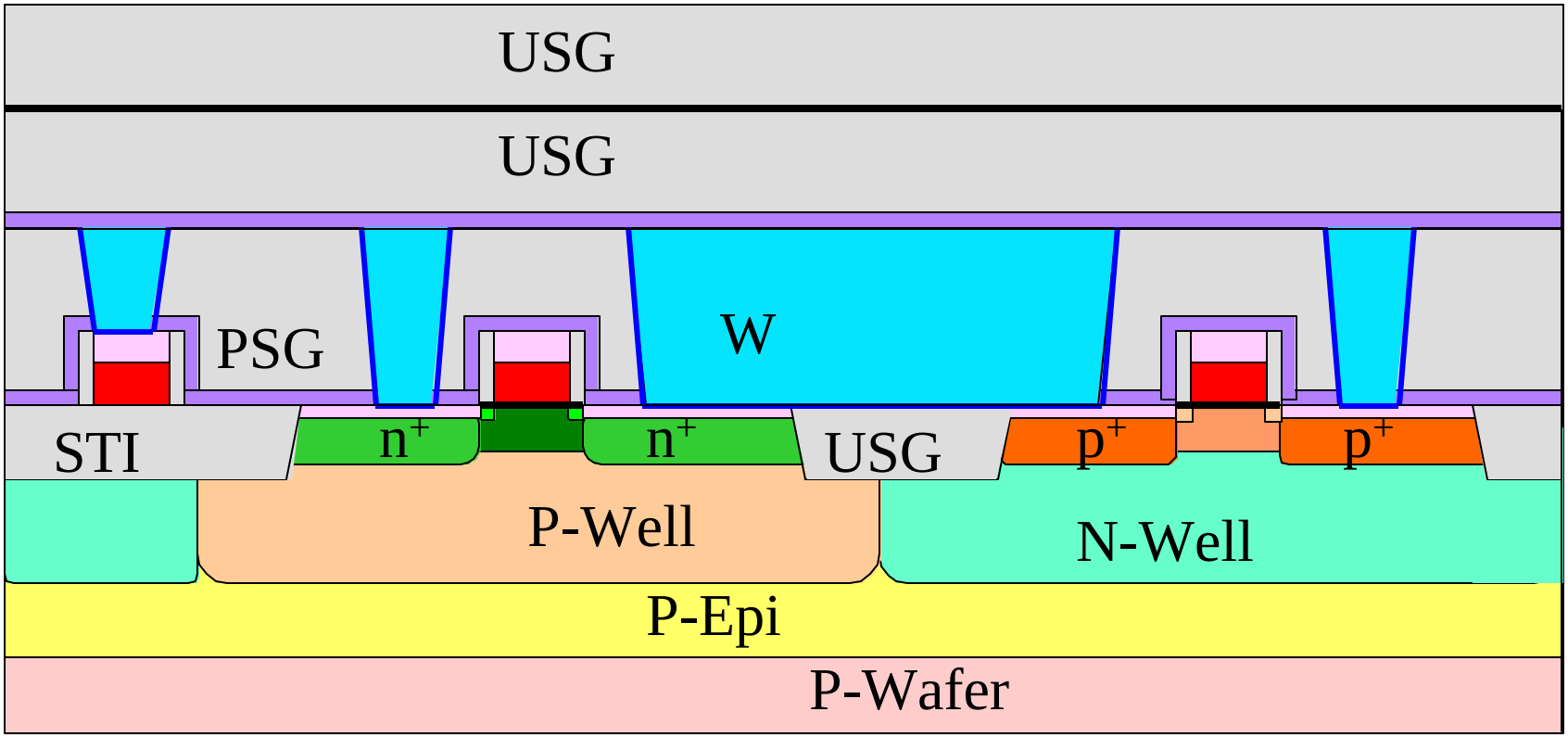
Copper Interconnection

- Dual damascene process
- Most commonly used method for the copper metallization
  - Photolithography, etch via, and PR strip
  - Photolithography, etch trench, and PR strip
  - Metal depositions and anneal
  - Metal CMP

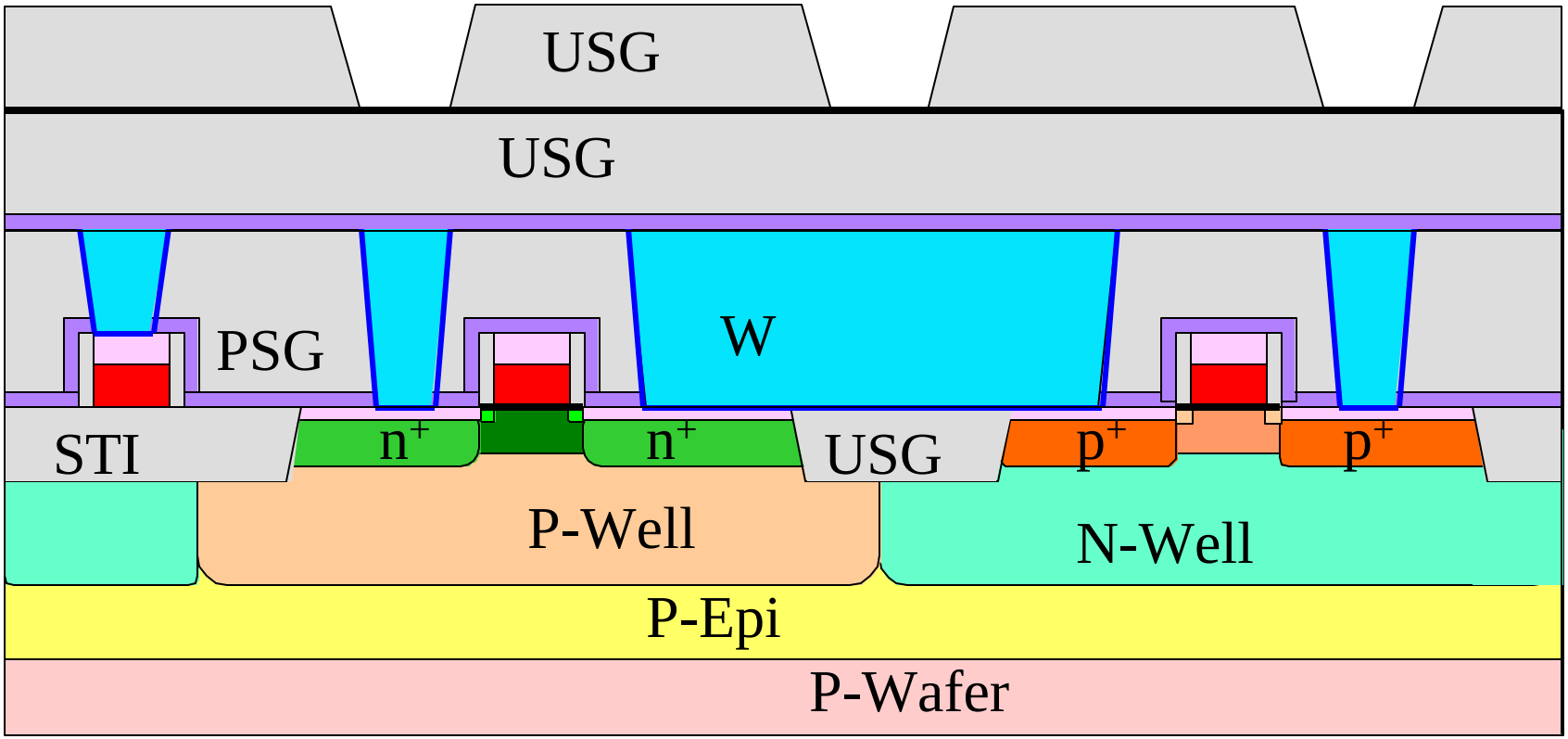
Basic Differences

- Traditional process: one dielectric etch and one metal etch
- Dual damascene copper process: two dielectric etches, no metal etch
- The main challenges of the dual damascene copper process are dielectric etch, metal deposition and metal CMP

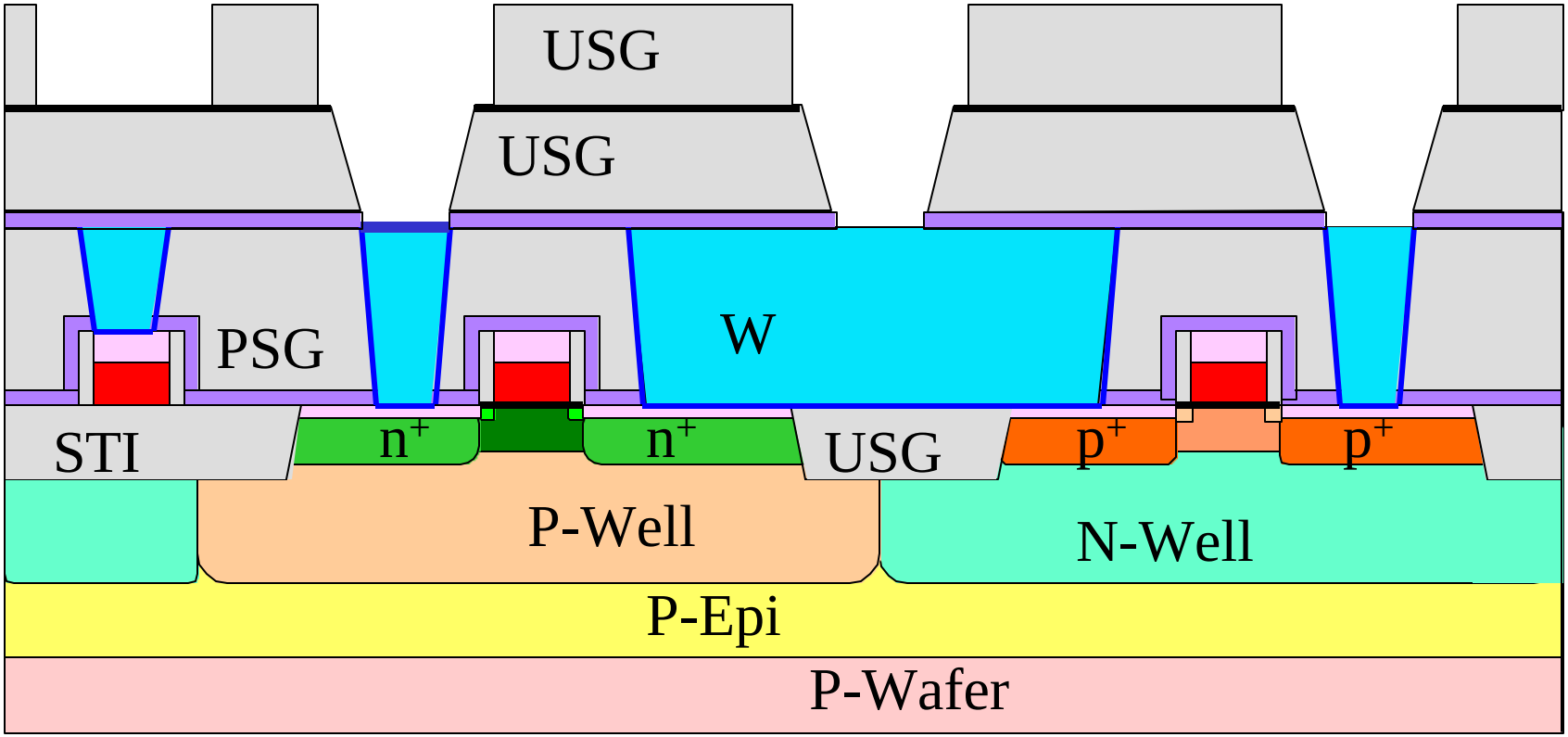
PECVD Nitride/USG/nitride/USG



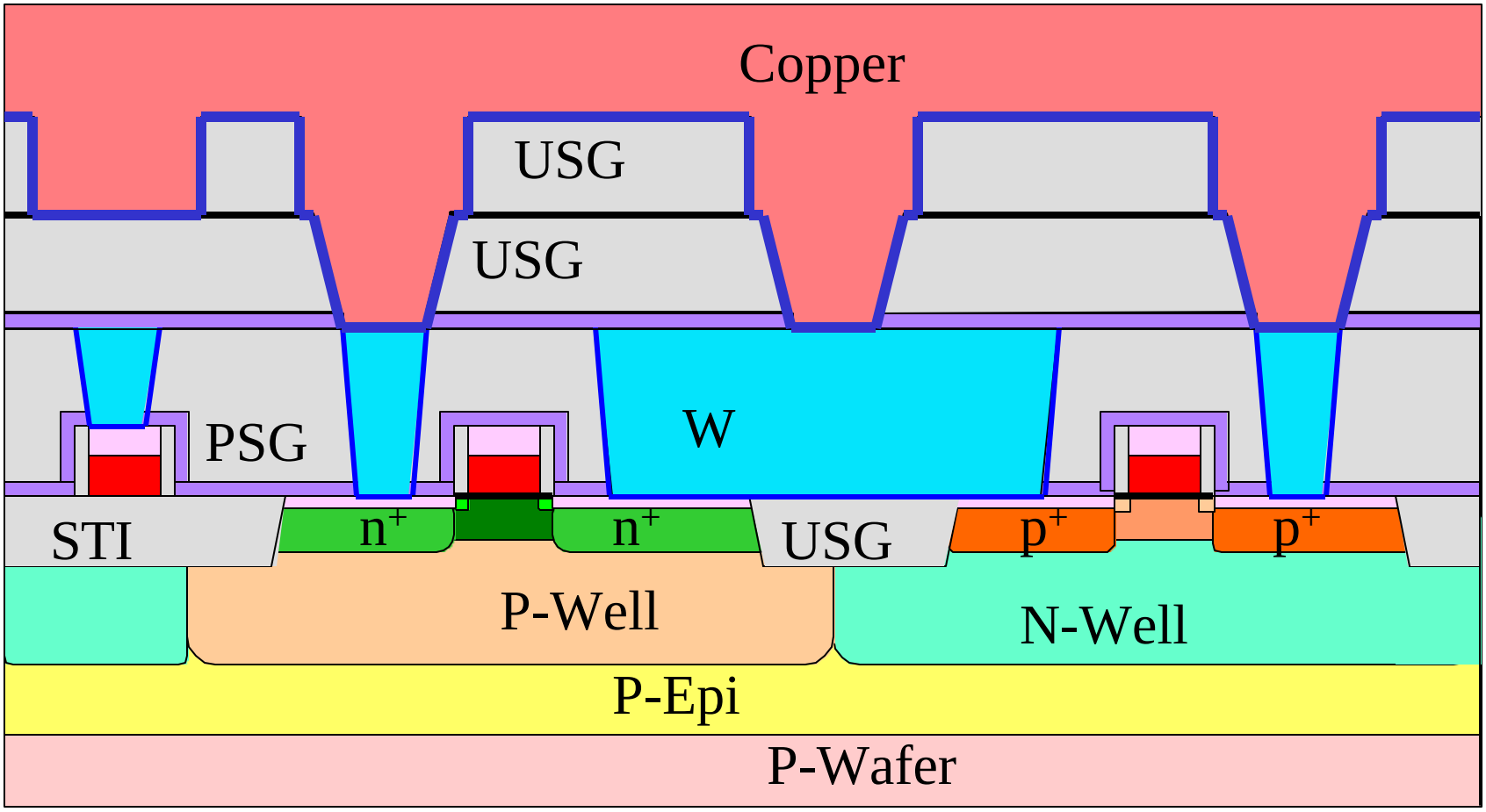
Via Mask, Etch Via, and Strip PR



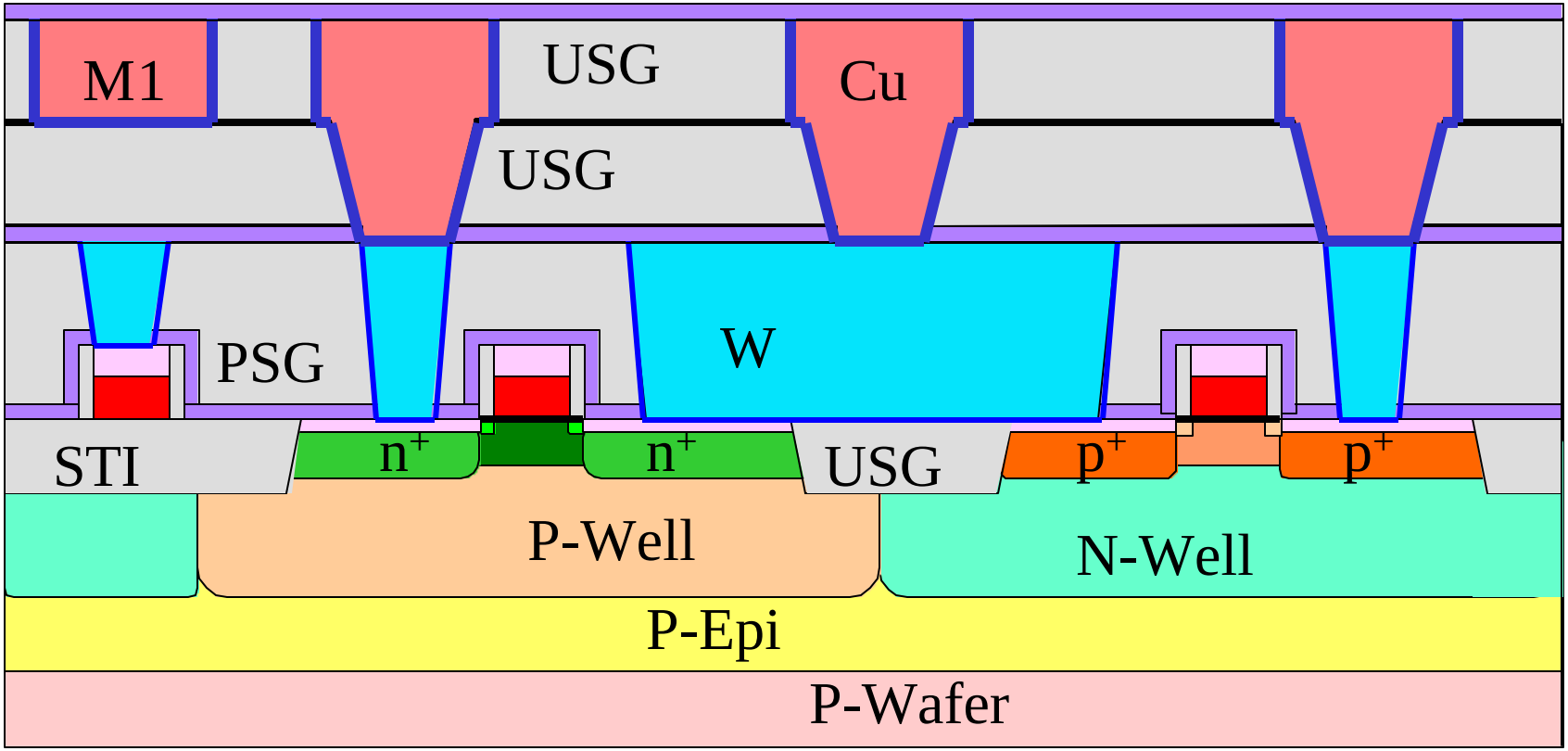
Trench Mask, Etch Trench, Strip PR



PVD Ta and Cu, ECP Bulk Cu, Anneal



CMP Cu and Ta, PECVD Nitride



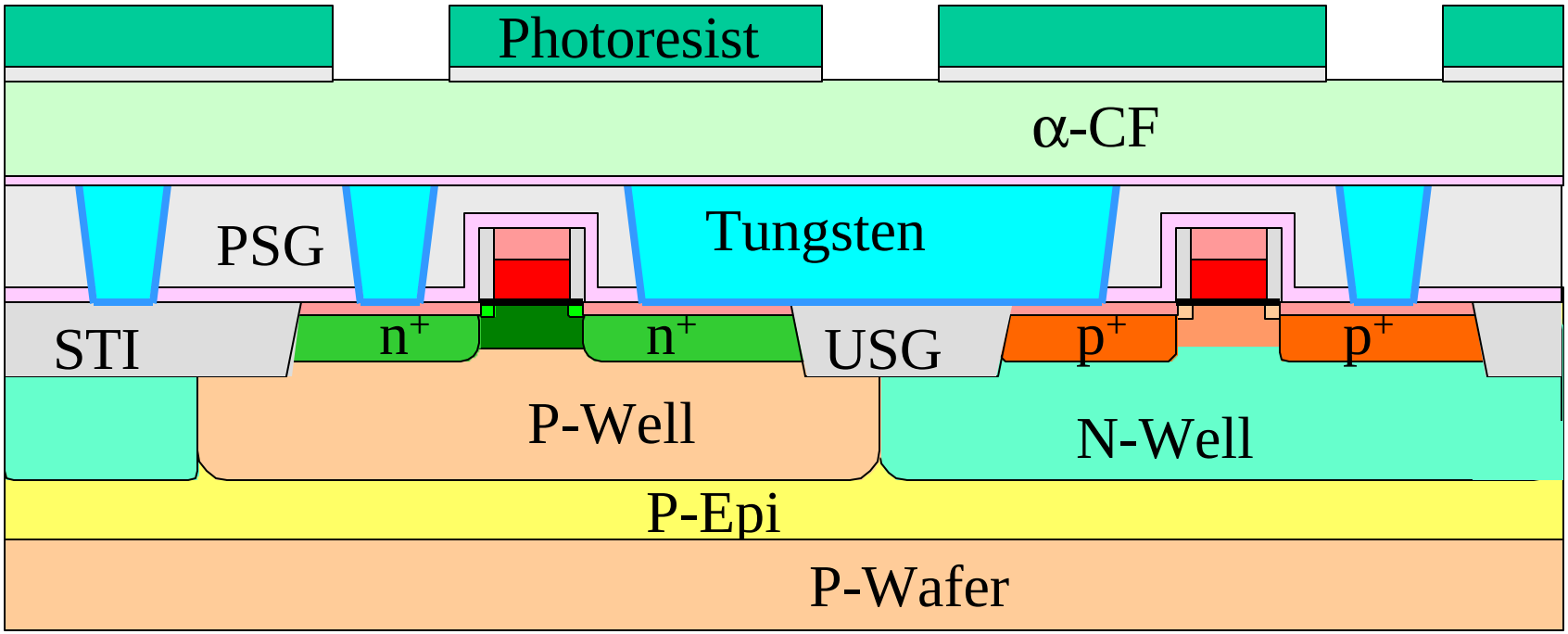
Copper Metallization

- Nitride seal layer prevent copper diffusion and oxidation
- Etch stop nitride separate via and trench etch
- Tantalum used as copper barrier layer
- PVD copper seed layer
- ECP bulk copper

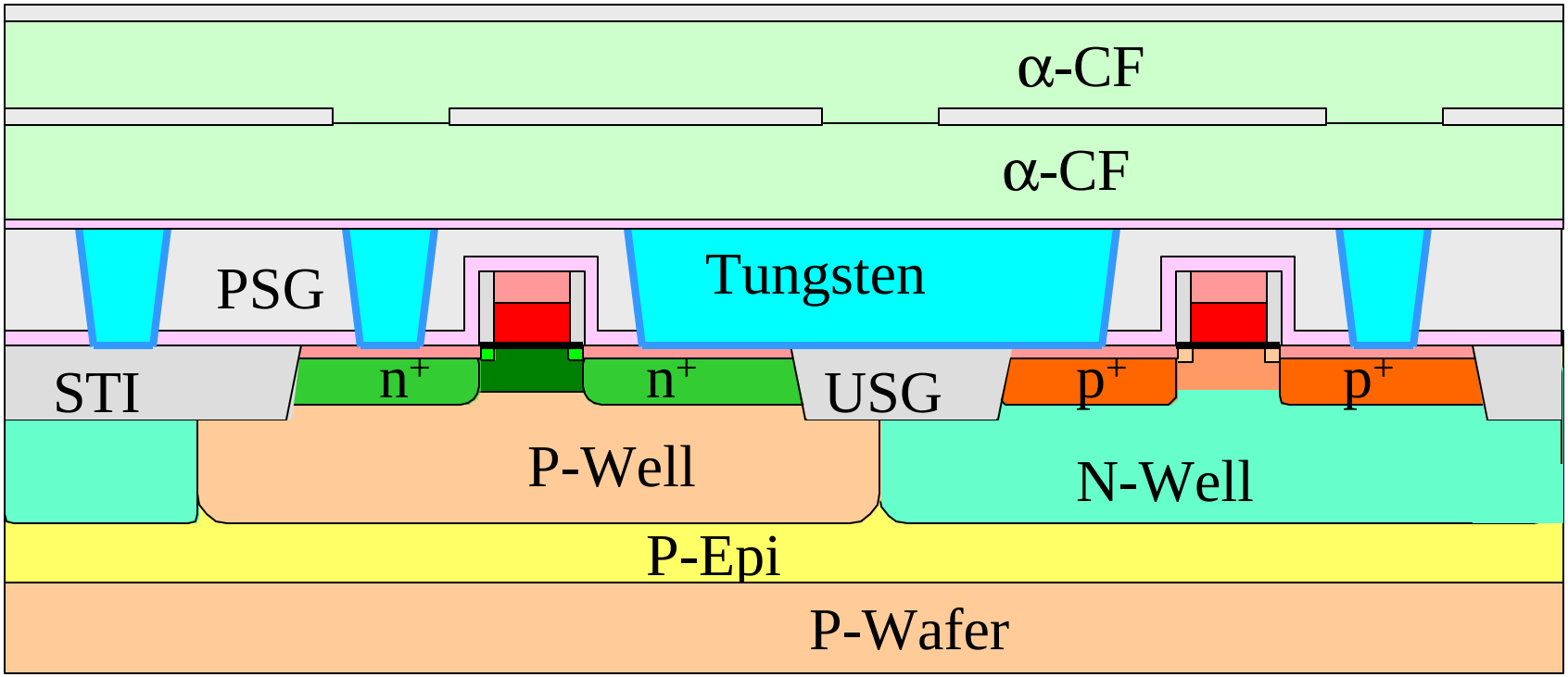
Copper and Low-κ

- Further increase IC chip speed
- low-κ dielectric still in R&D
- α-CF, κ = 2.5 to 2.7
- Can't be etched with fluorine chemistry
- It needs oxygen chemistry to etch
- New challenges for the process integration

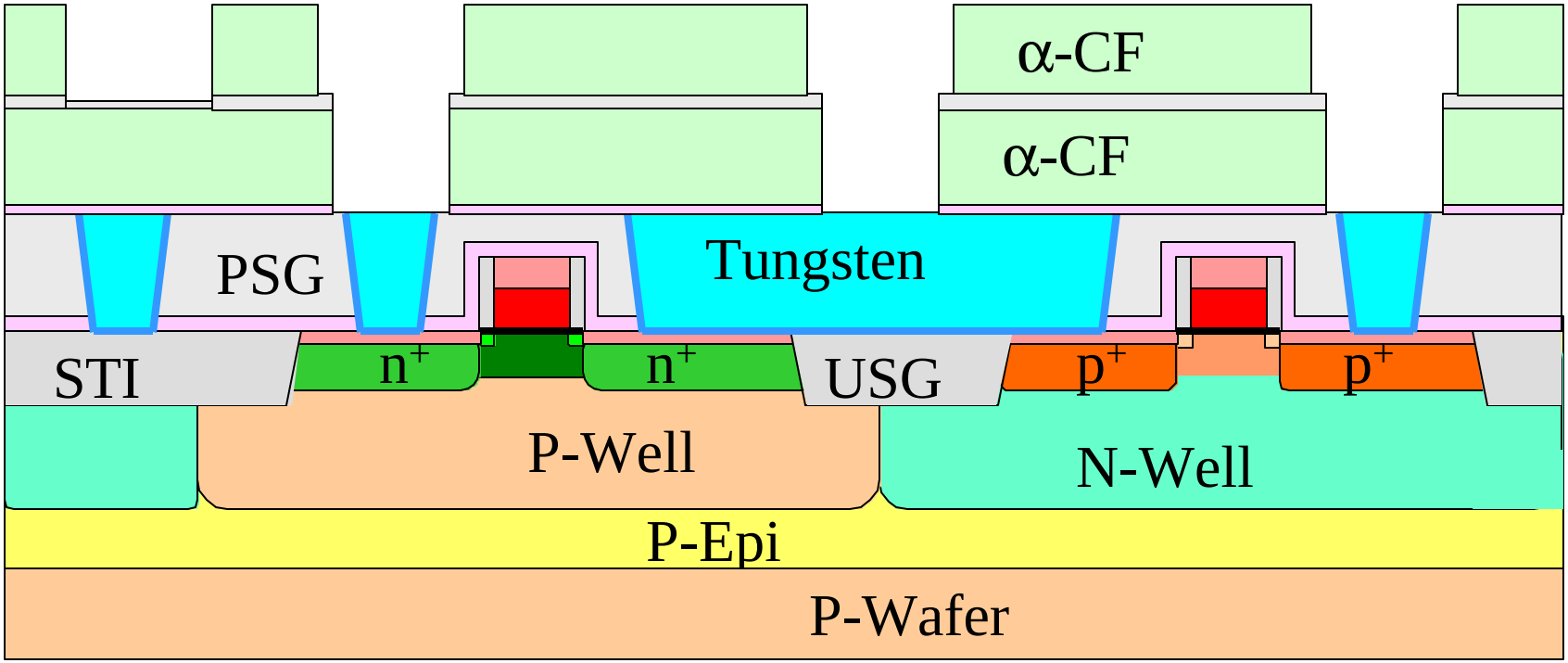
PECVD α-CF, USG, Via Mask, and Etch USG Hard Mask



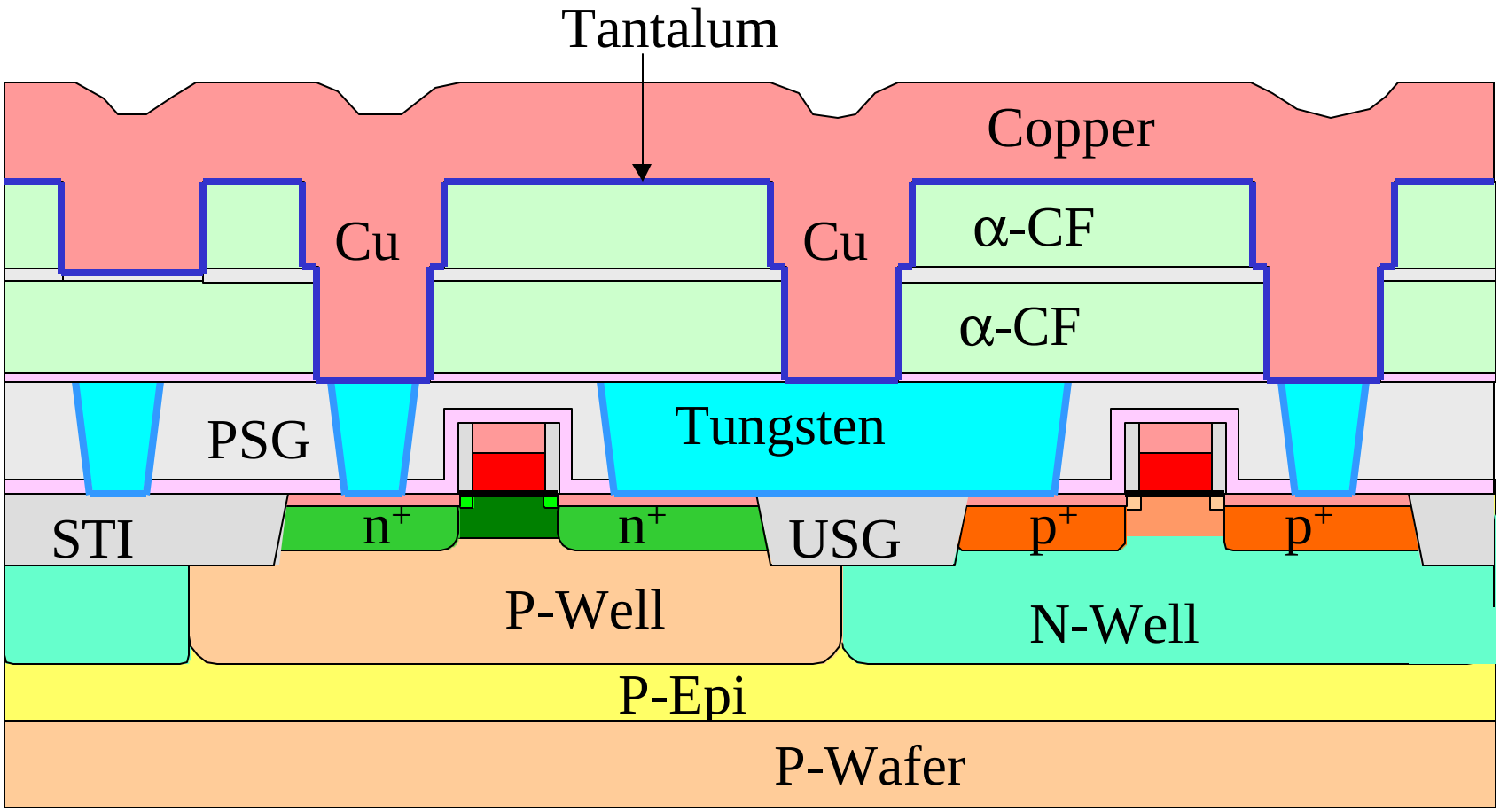
PECVD α-CF and USG



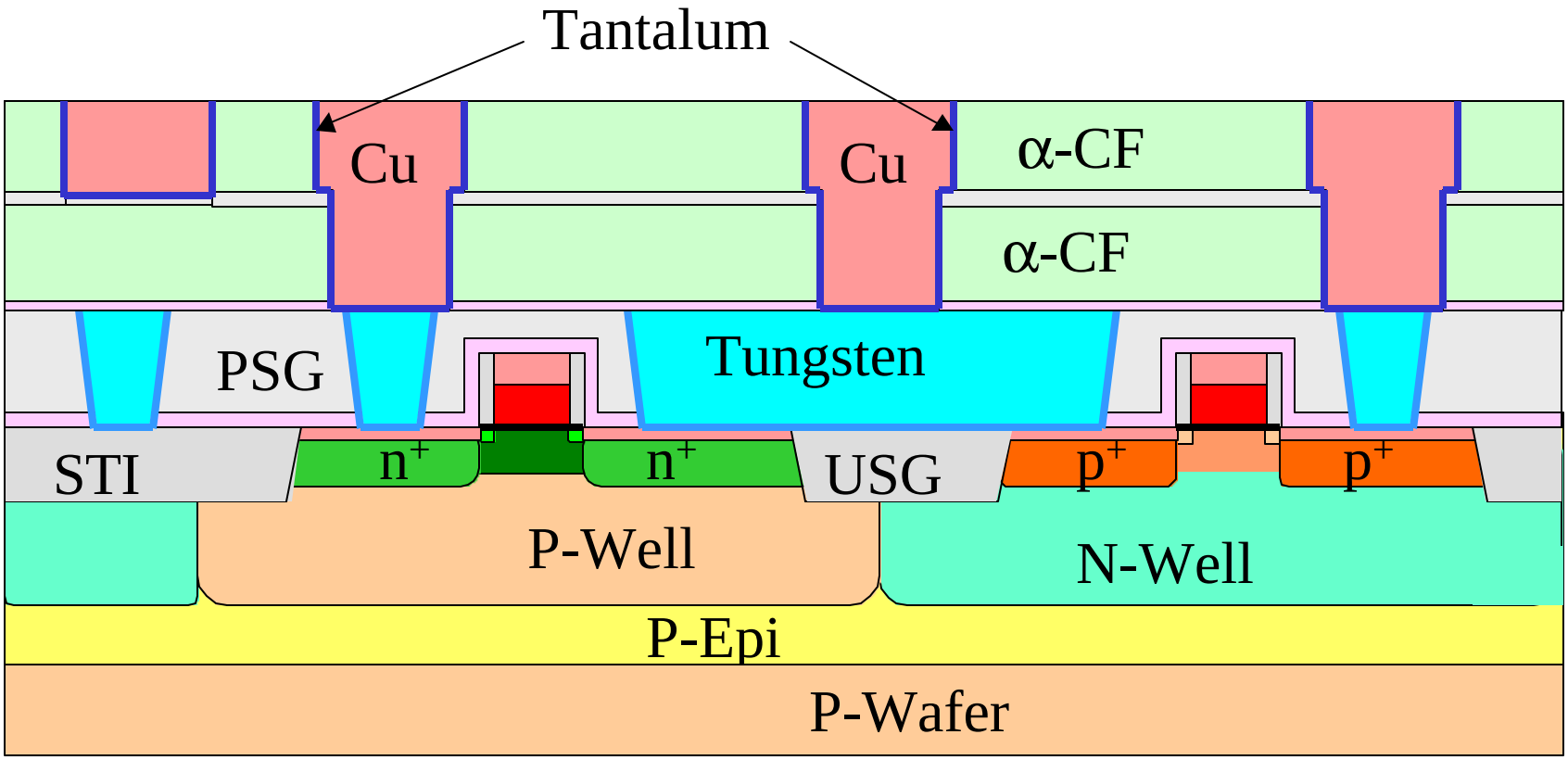
Etch α-CF and Seal Nitride



PVD Ta, Cu Seed, and ECP Cu



CMP Copper and Tantalum



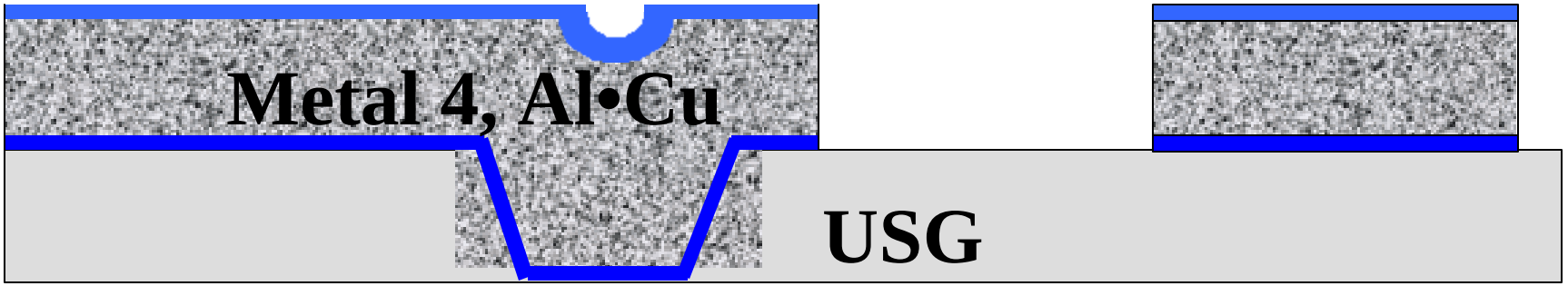
Copper and Low-κ

- Oxygen plasma is used to etch α-CF
- PR can't last long in oxygen plasma
- SiO_2 hard mask is needed
- Oxygen can't etch oxide and nitride
- Trench and via can be etched at the same time
  - High selectivity of α-CF to oxide and nitride
- PR is removed when oxygen plasma etch α-CF

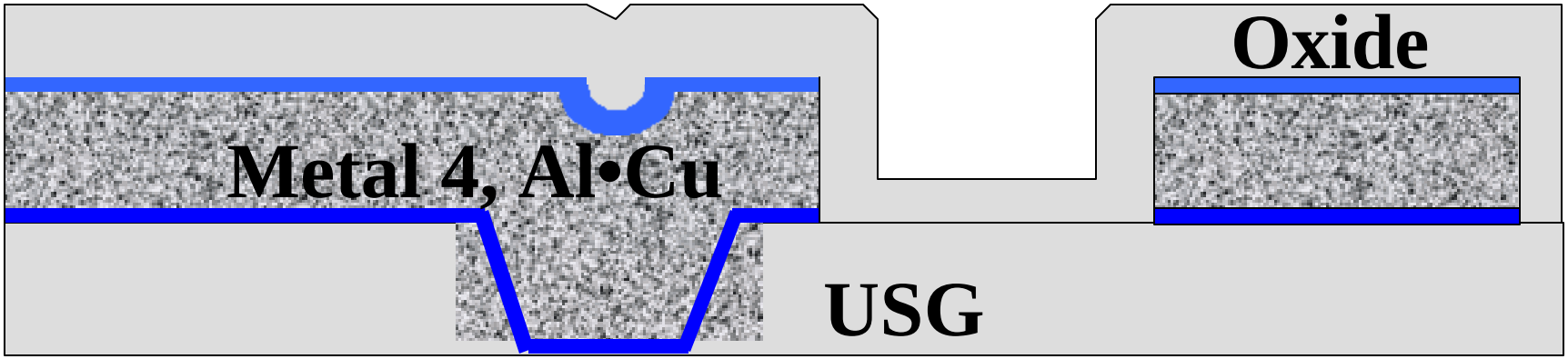
Passivation

- Protect IC chip from moisture and other contaminants such as sodium
- Silicon nitride is the most commonly used
- Usually oxide layer is used as a stress buffer
- SiH_4 based PECVD for both oxide and nitride
- Bonding pad mask or connecting bump mask
- Fluorine based nitride/oxide etch
- Strip PR to finish wafer processing

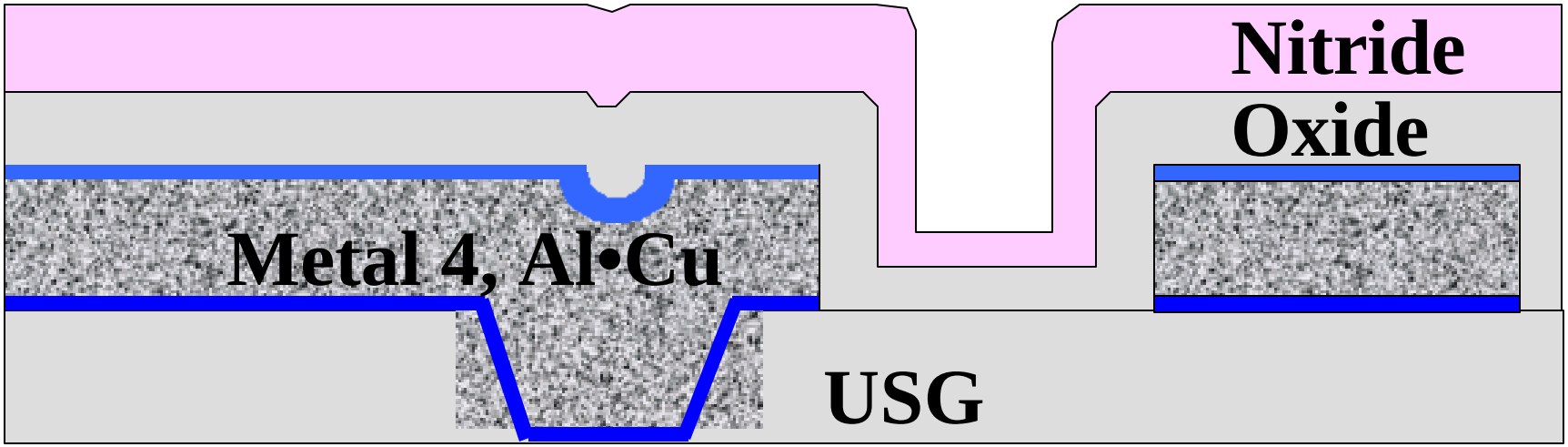
Metal Anneal



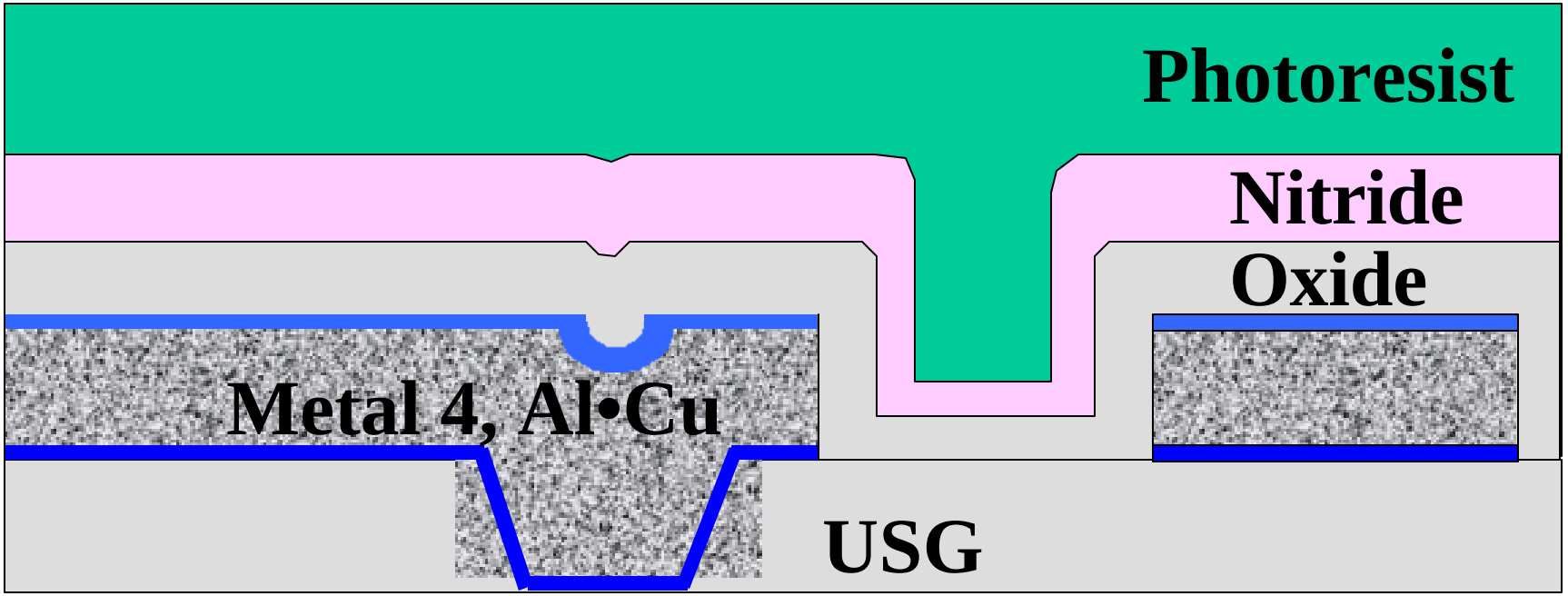
PECVD Oxide



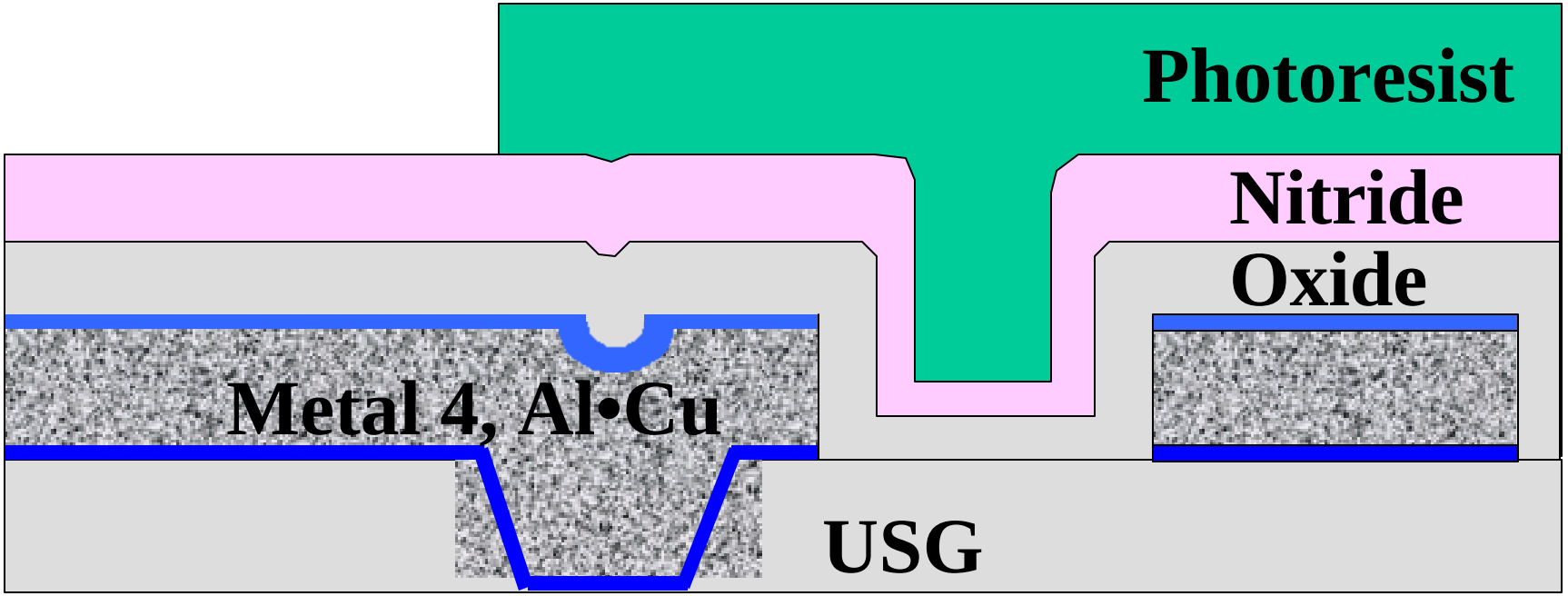
PECVD Nitride



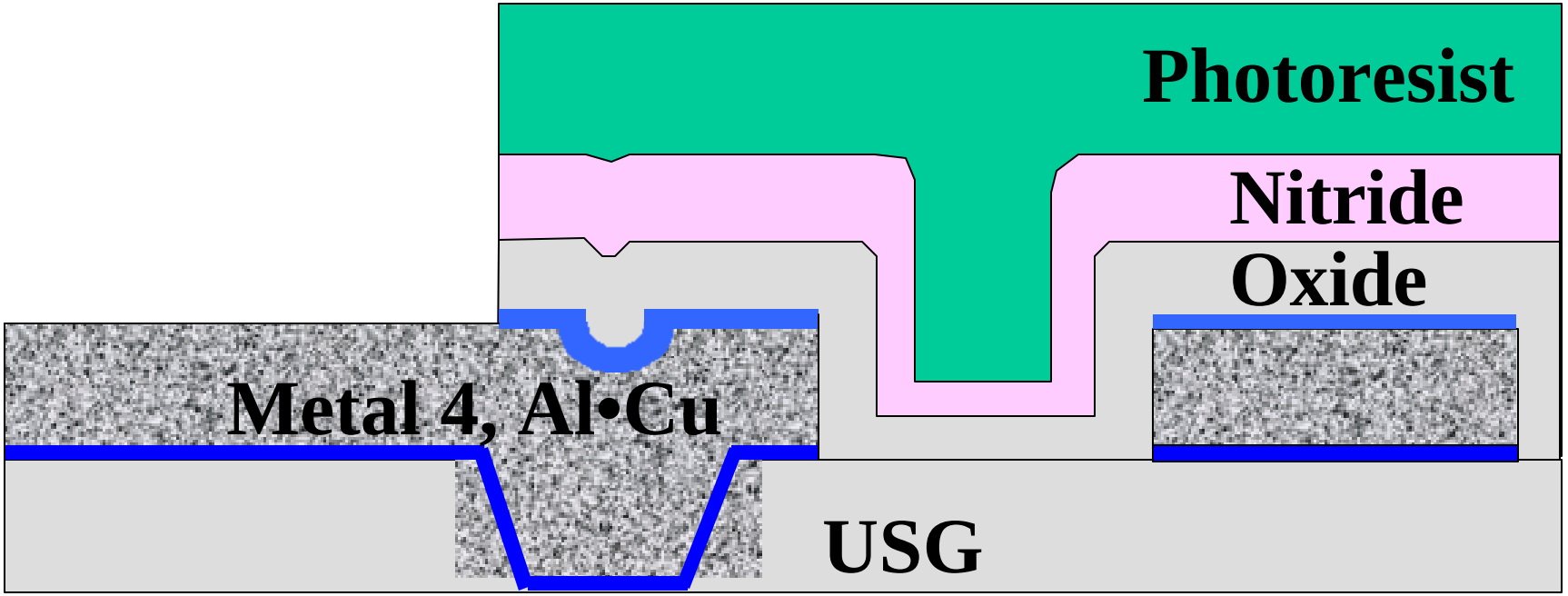
Photoresist Coating



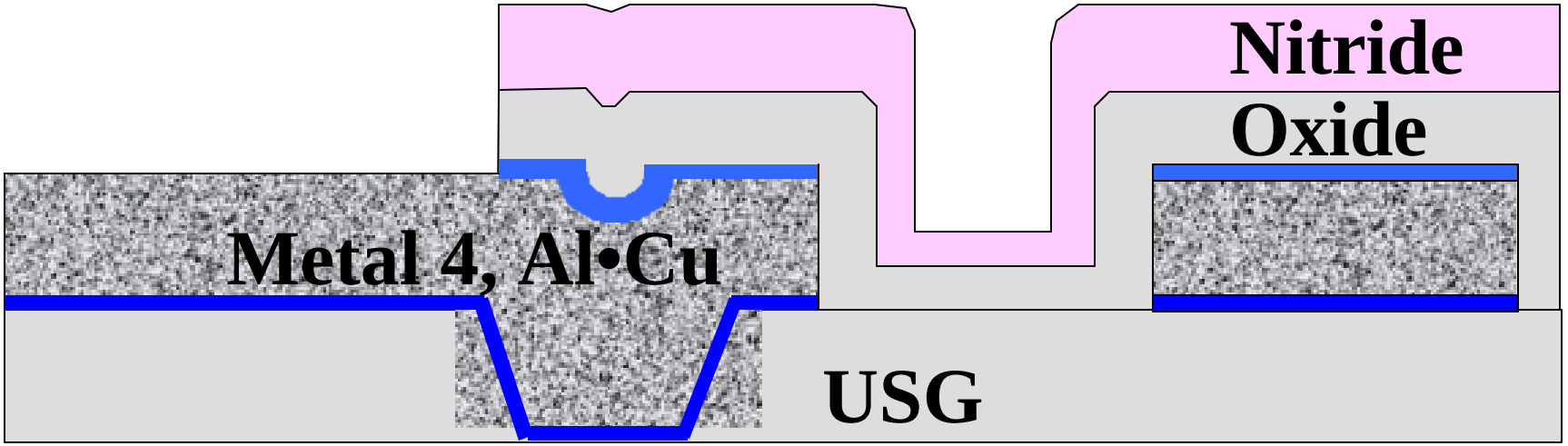
Bonding Pad Mask Exposure and Development



Etch Nitride and Oxide



Strip Photoresist



Summary

- Well formation process
- Isolations: field oxide, LOCOS, and STI
- Sidewall spacer for LDD and salicide
- Al, poly-Si and silicide for gate and local interconnections
- W, Ti and Al alloy are commonly used in traditional interconnection process.

Summary

- Basic process steps for copper metallization are dielectric deposition, dielectric etches, metal deposition, and metal polishing
- Silicon nitride is the most commonly used passivation materials in IC processing