Chapter 14
CMOS Processes

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Objectives

- List the major process technology changes from the 1980 to the 1990s
- Explain the differences between copper metallization and traditional metallization

From 1960s to 1970s

- 1960s
  - PMOS
  - Diffusion
  - Metal gate
- 1970s
  - NMOS
  - Ion implantation
  - Polysilicon gate

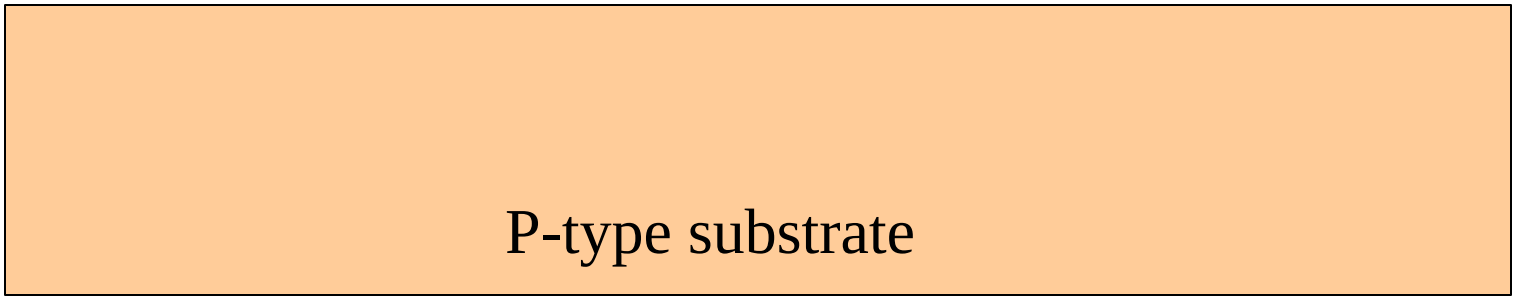
1980's Technology

- LCD replacing LED as indicators for electronic watches and calculators
- CMOS IC replacing NMOS IC for lower power consumption
- Minimum feature size: from 3 μm to 0.8 μm
- Wafer size: 100 mm (4 in) to 150 mm (6 in)

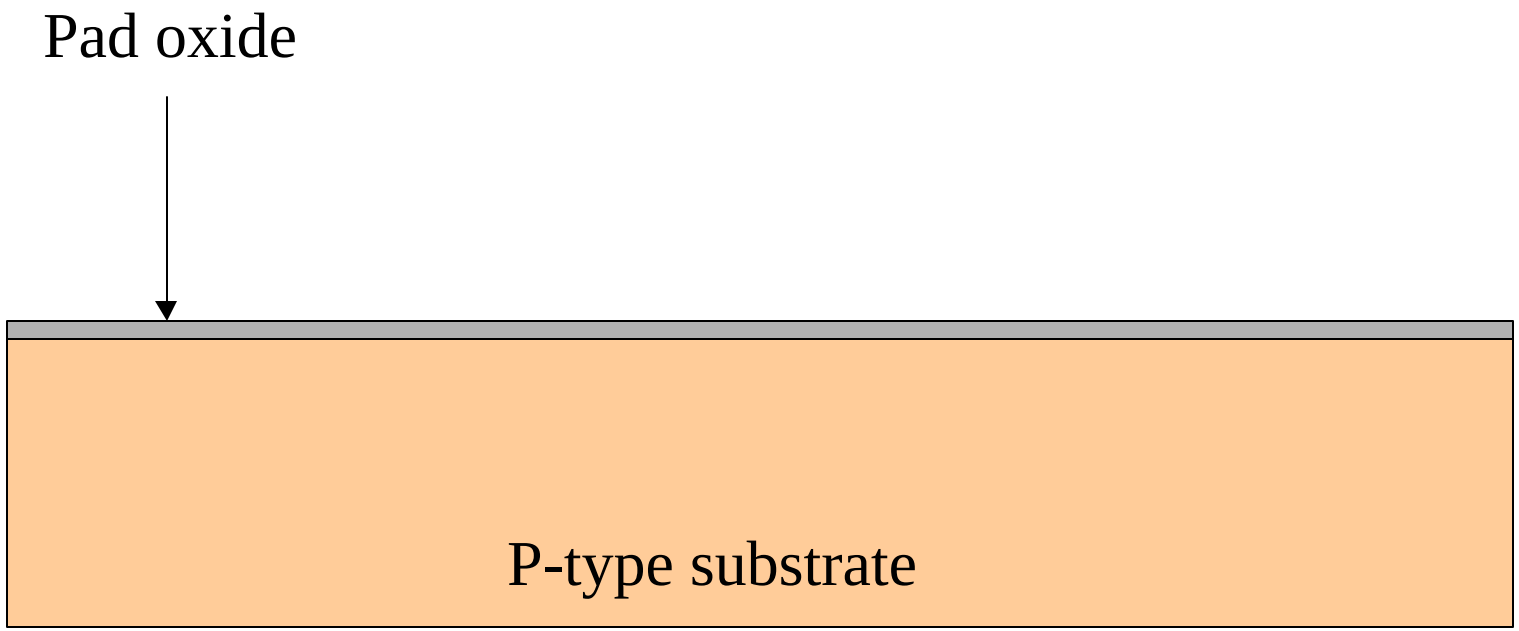
1980’s CMOS Technology

- LOCOS
- PSG and reflow
- Evaporator for metal deposition
- Positive photoresist
- Projection printer
- Plasma etch and wet etch

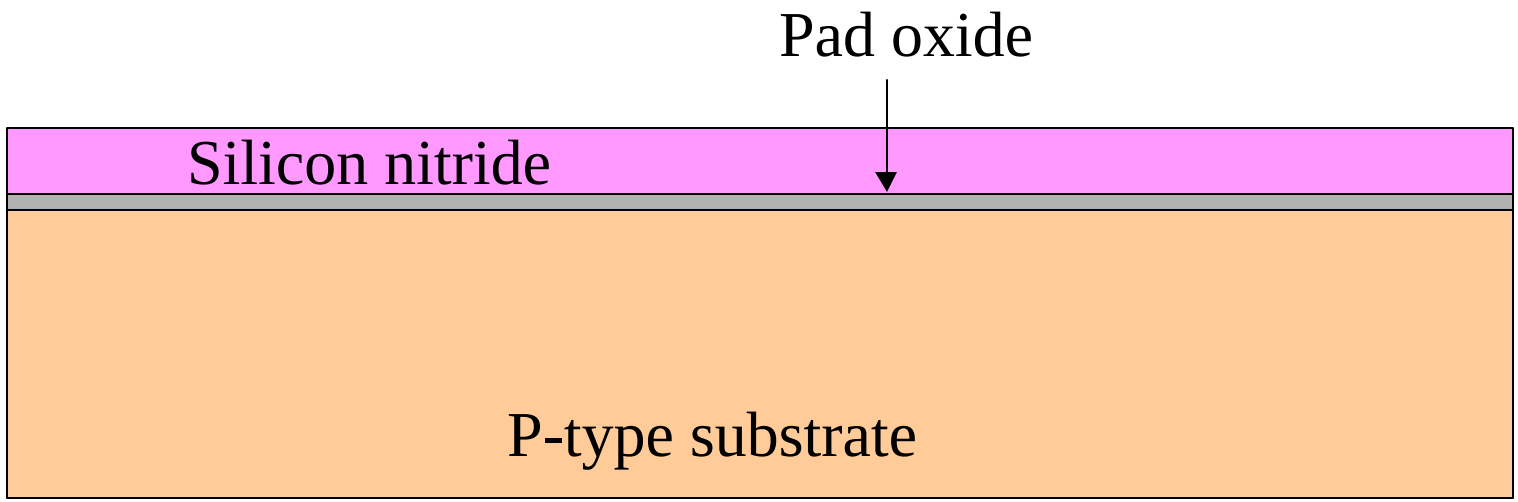
1980’s Technology, Wafer Clean



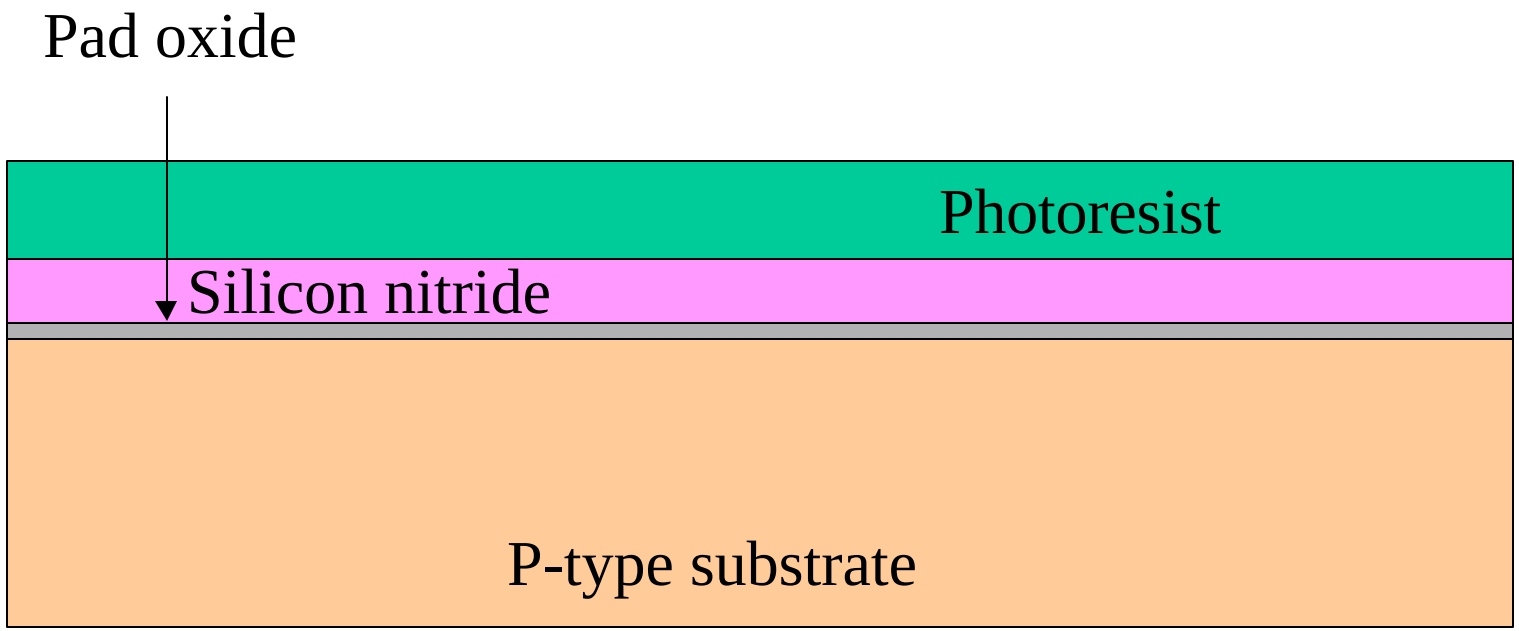
Pad Oxidation



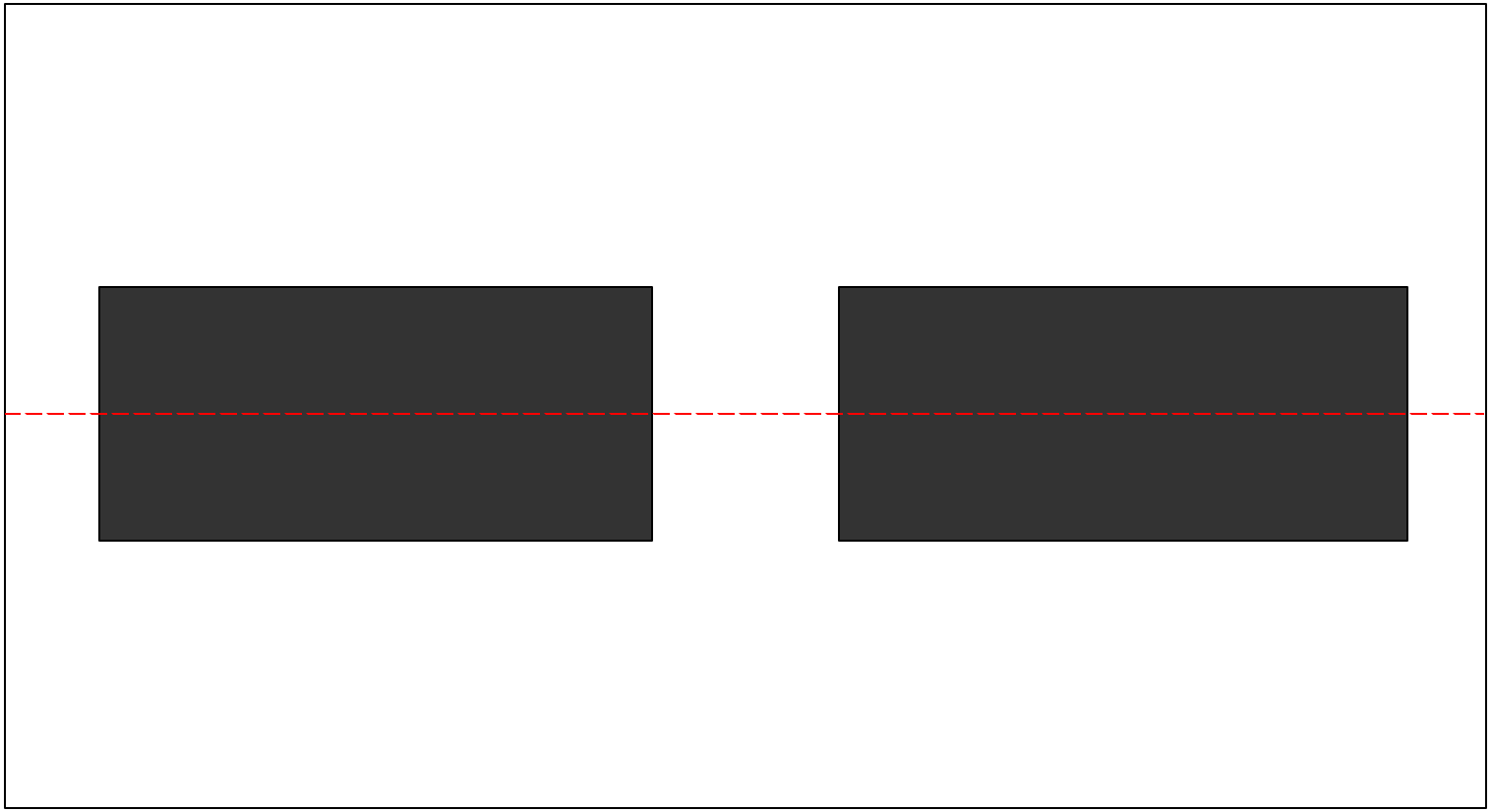
LPCVD Nitride



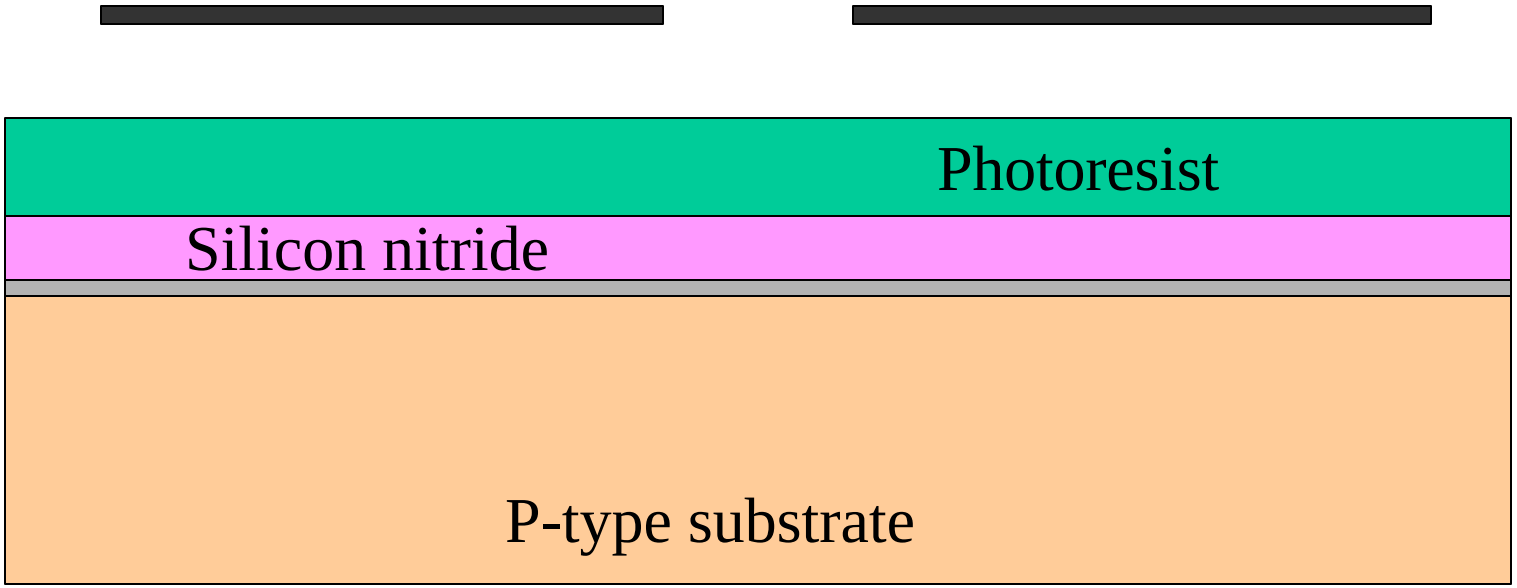
Photoresist Coating



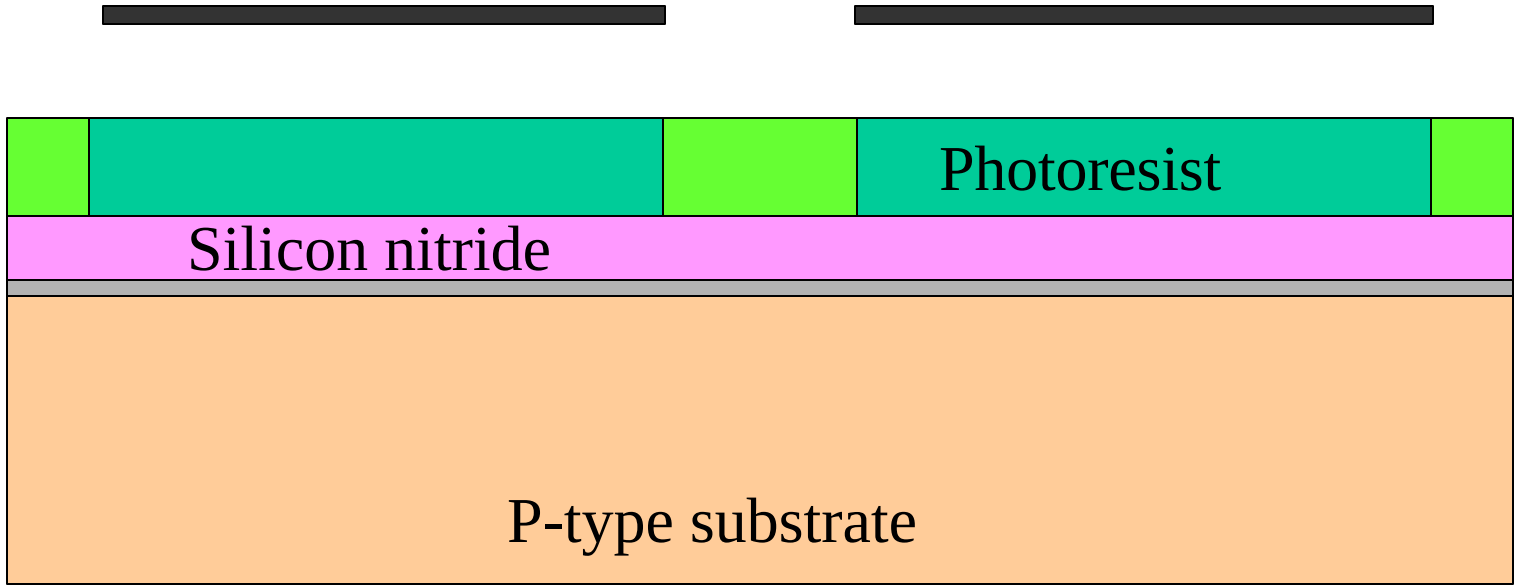
Mask 1, LOCOS



Mask 1, LOCOS



Alignment and Exposure



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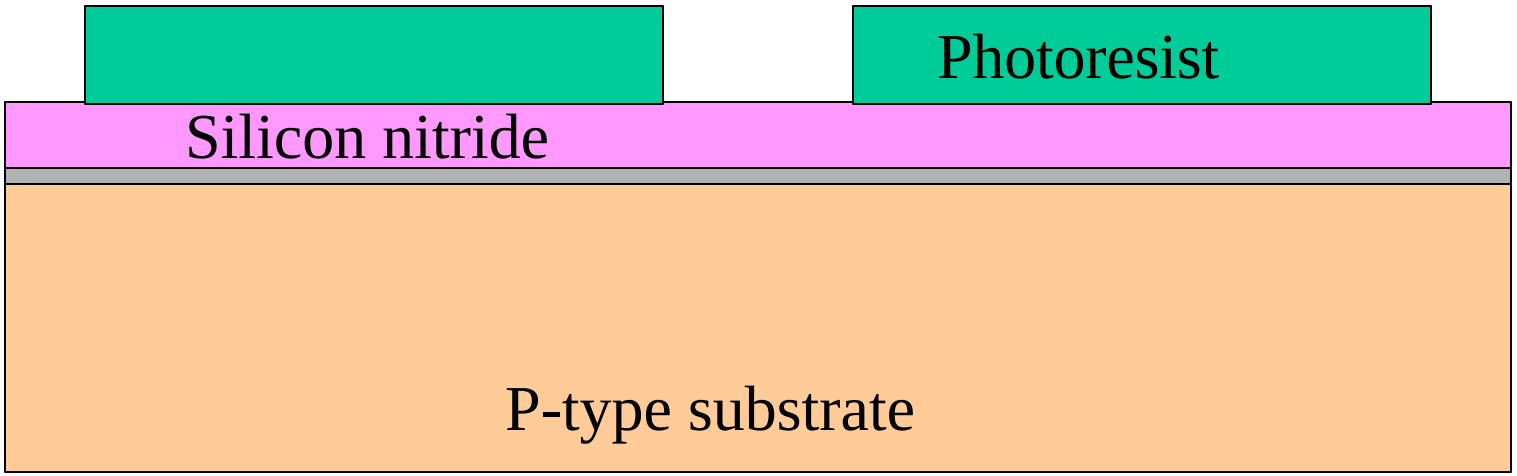
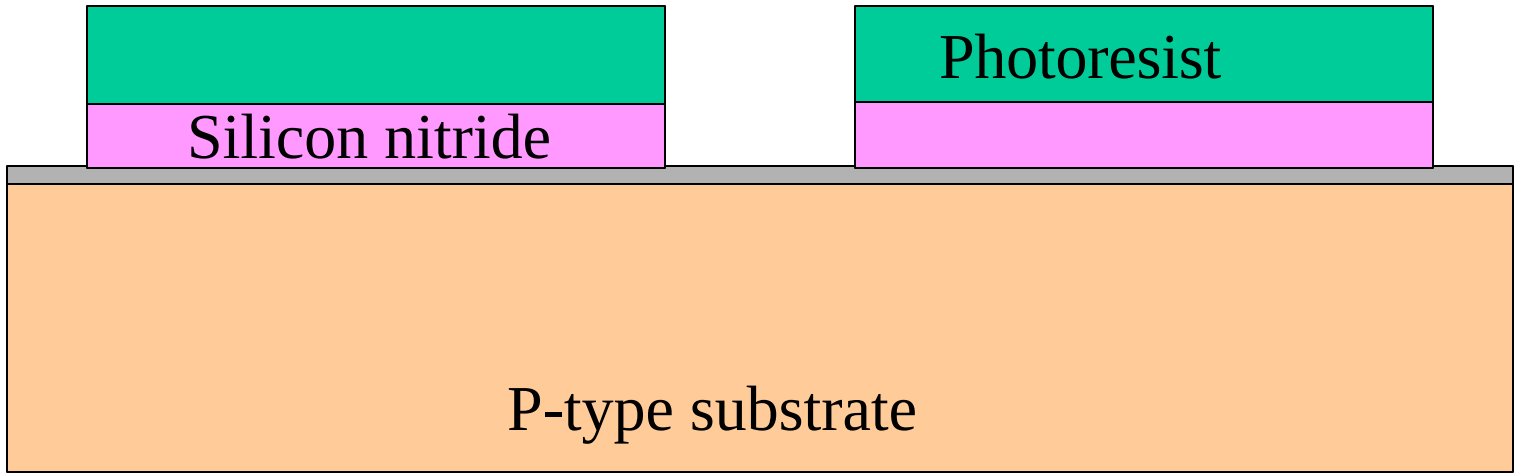
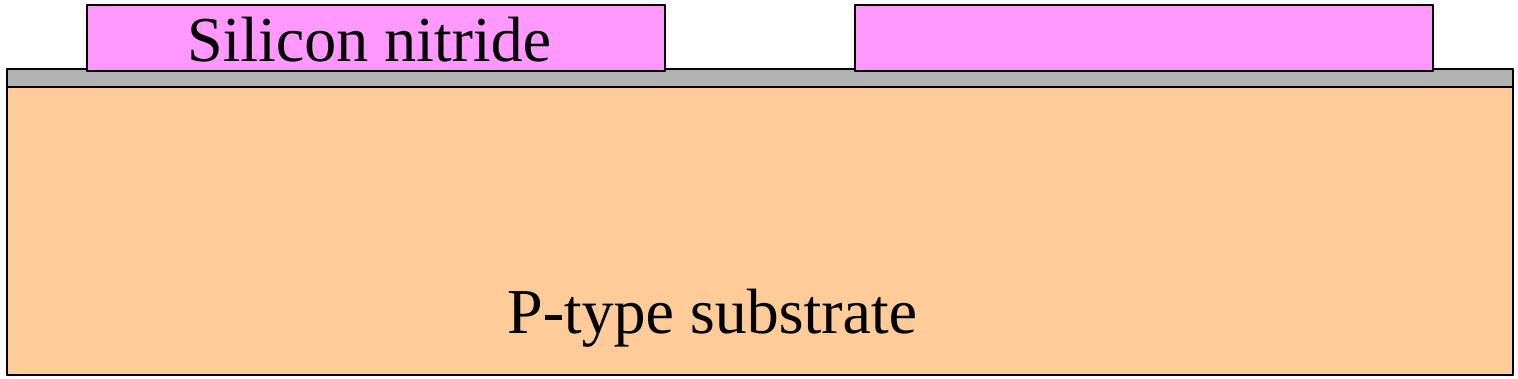


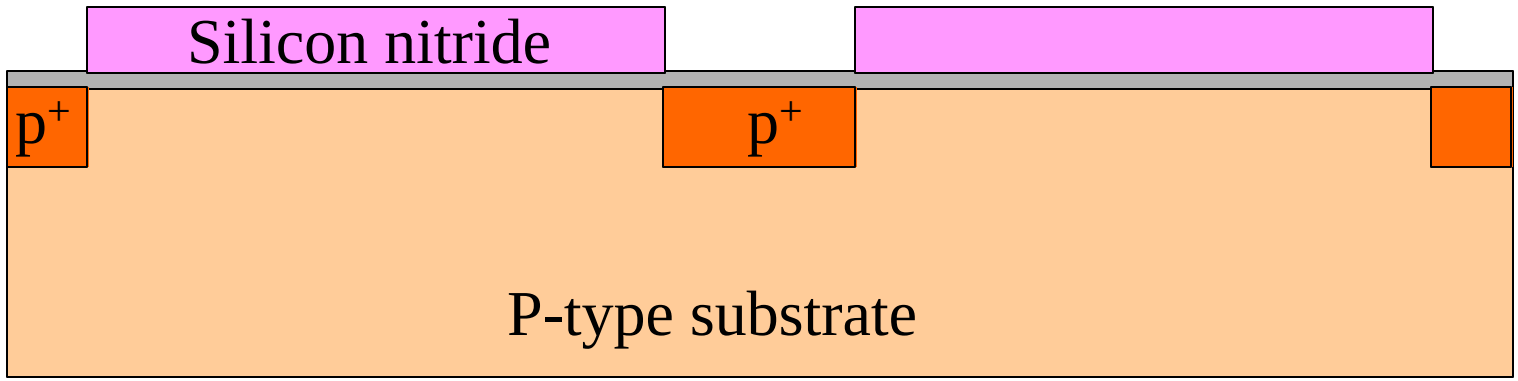
Etch Nitride



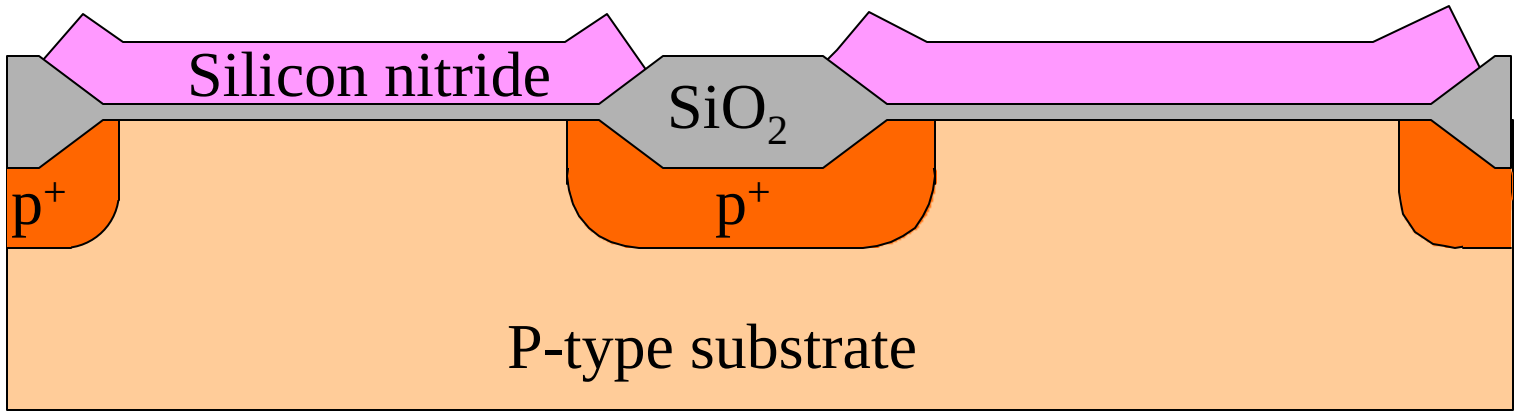
Strip Photoresist



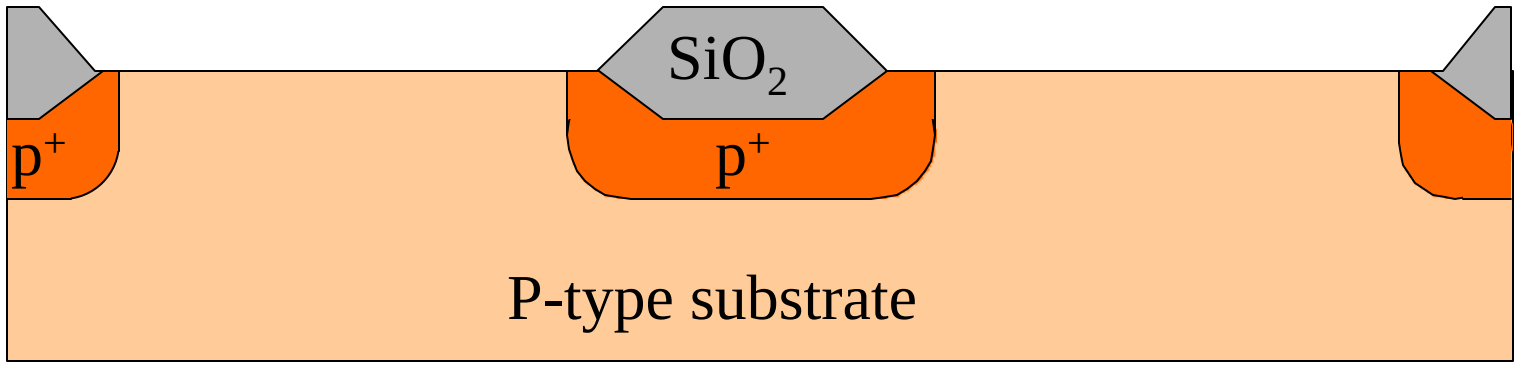
Isolation Implantation



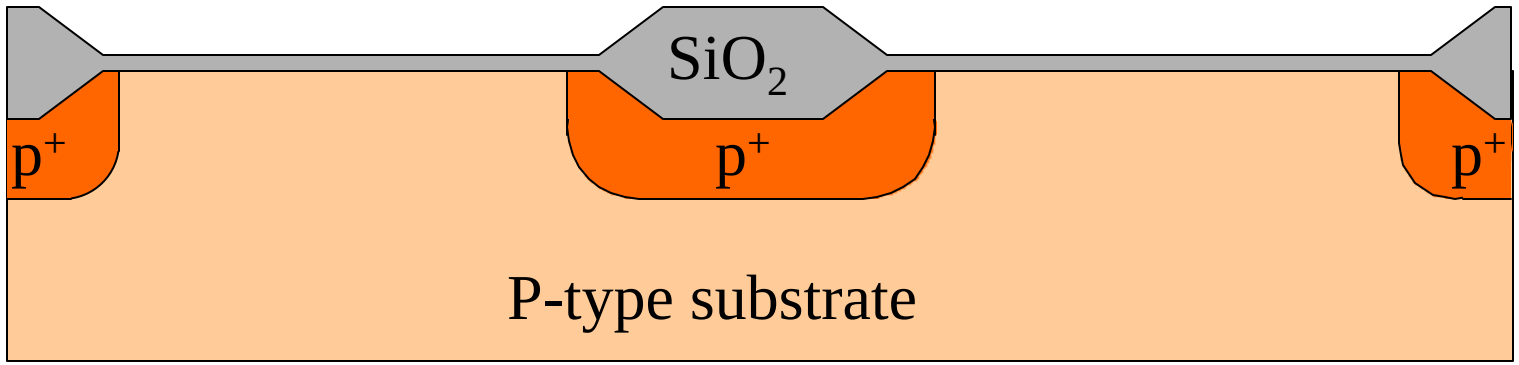
LOCOS Oxidation



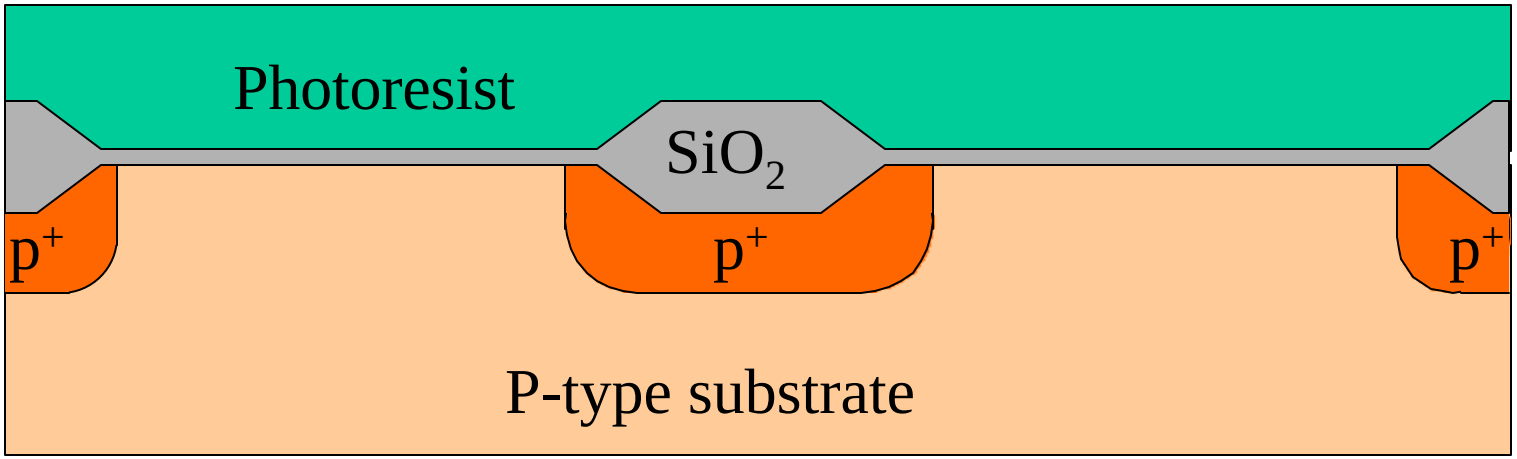
Strip Nitride and Pad Oxide, Clean



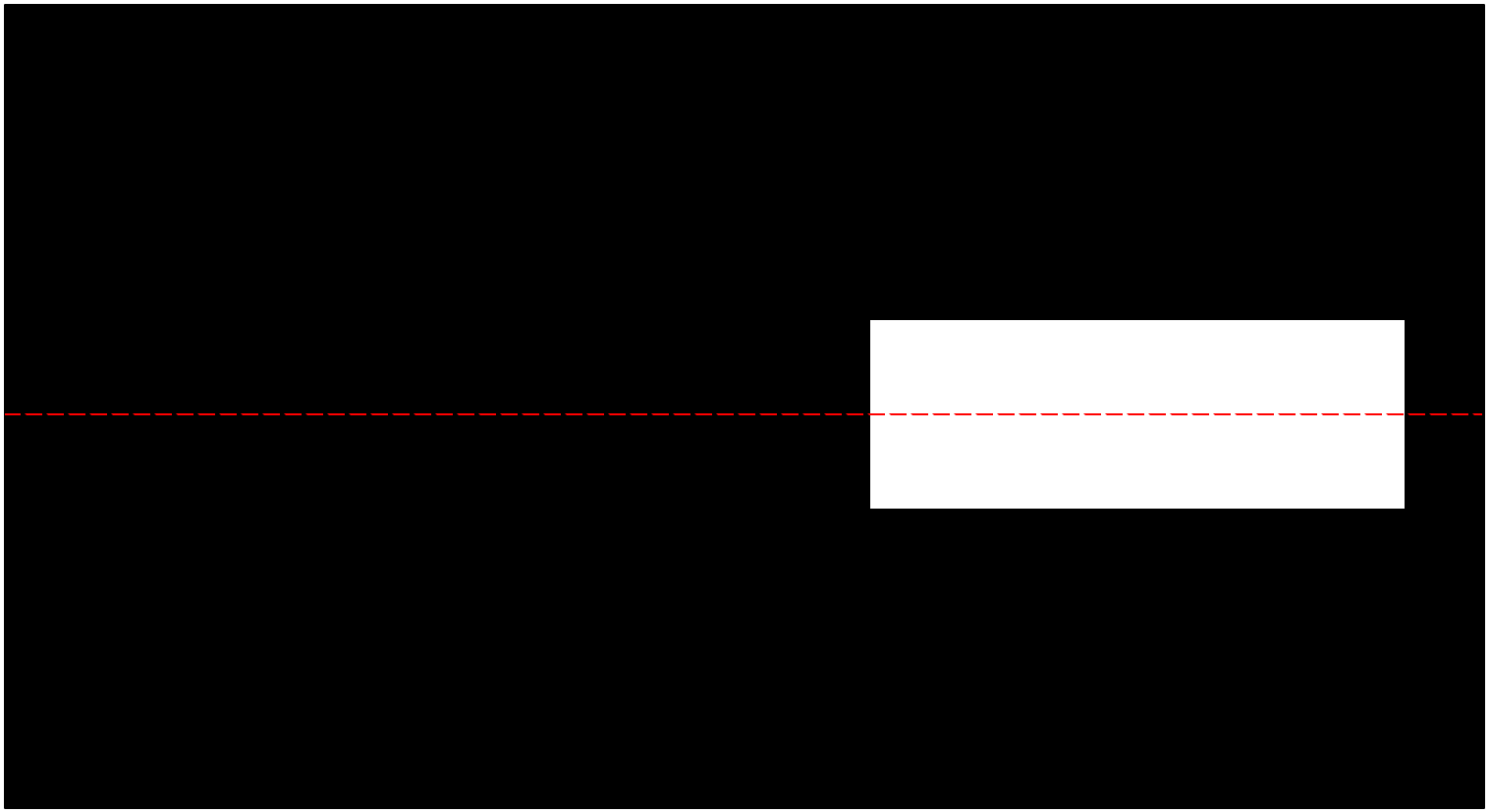
Screen Oxidation



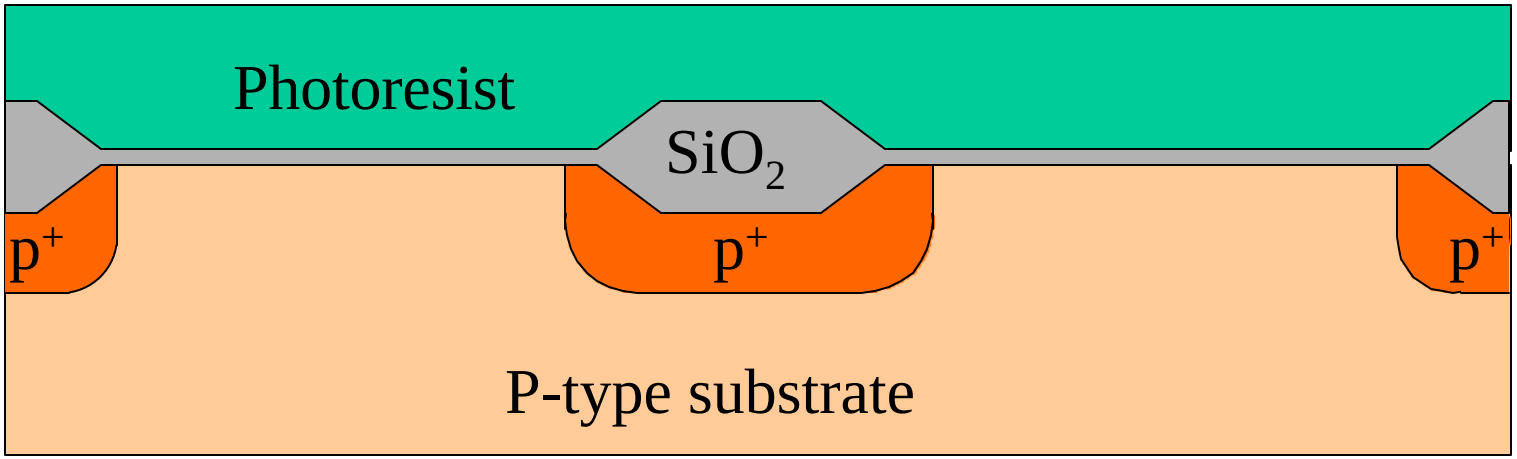
Photoresist Coating



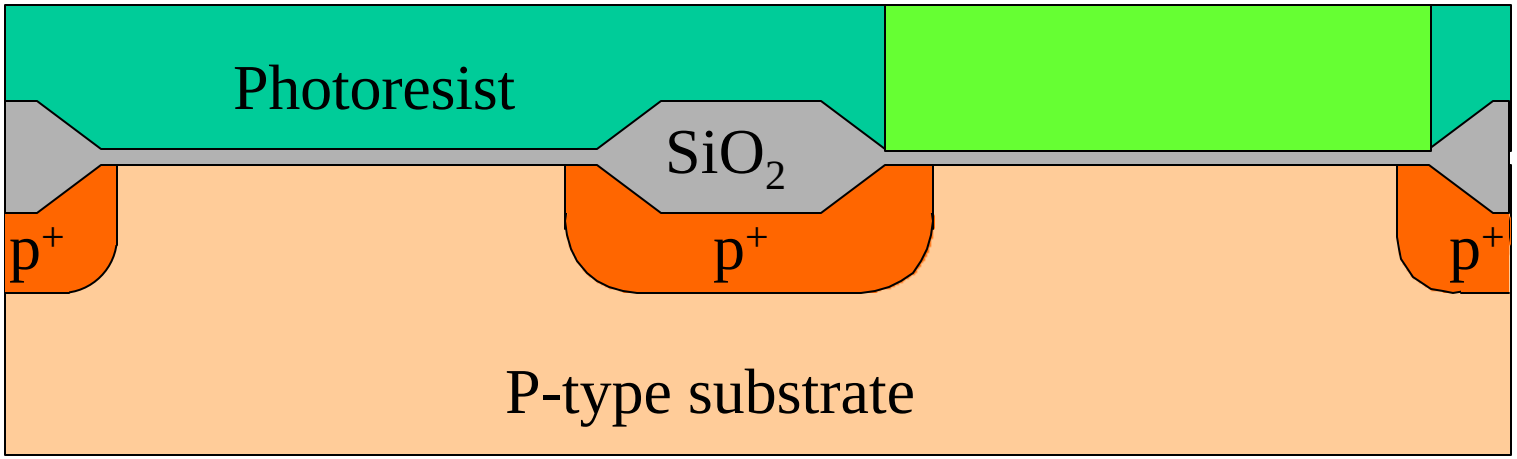
Mask 2, N-well



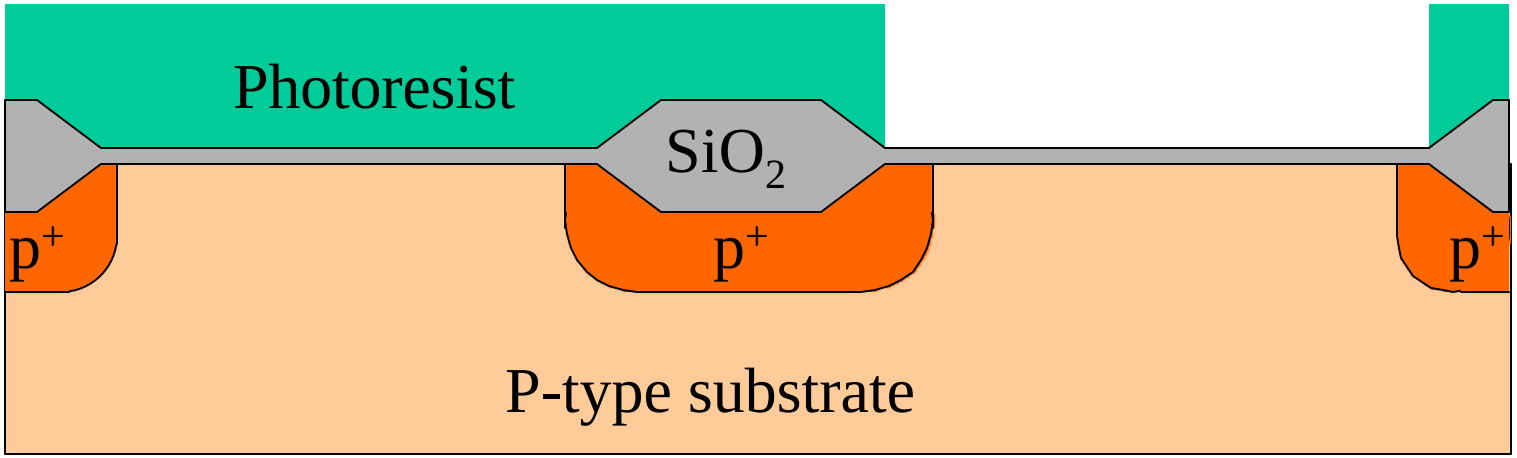
Mask 2, N-well



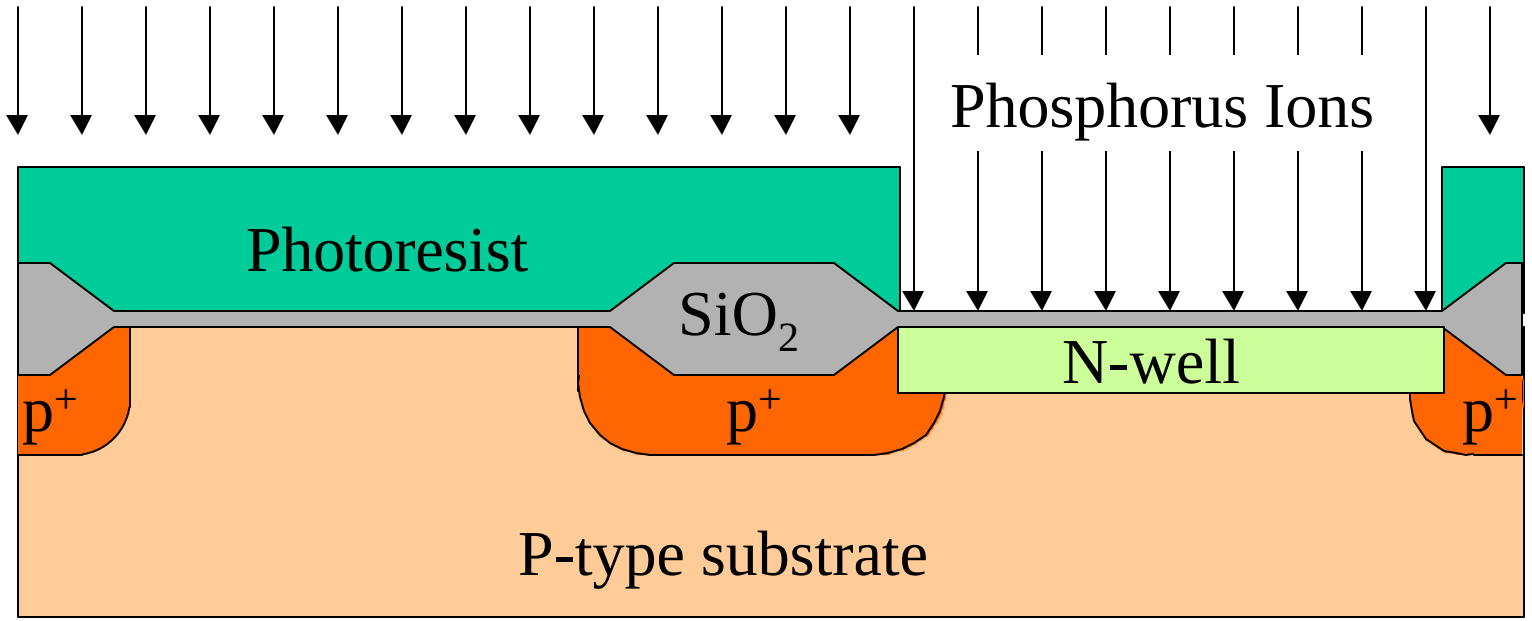
Exposure



Development



N-well Implantation



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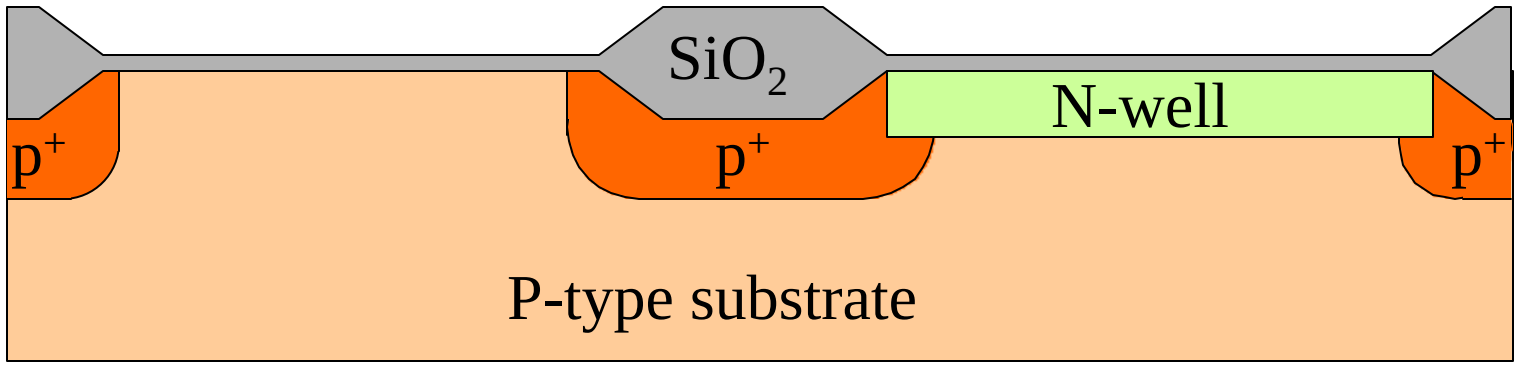
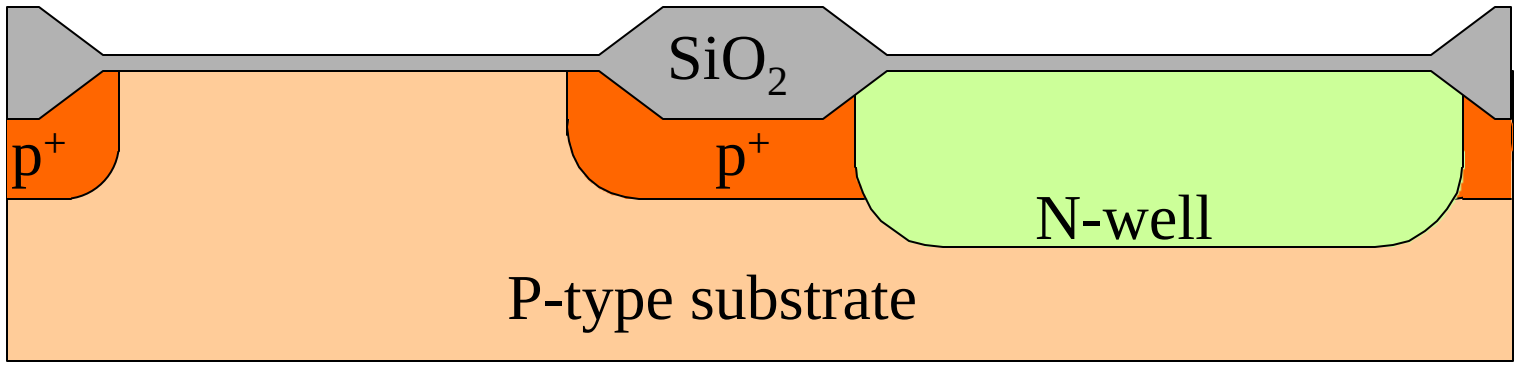
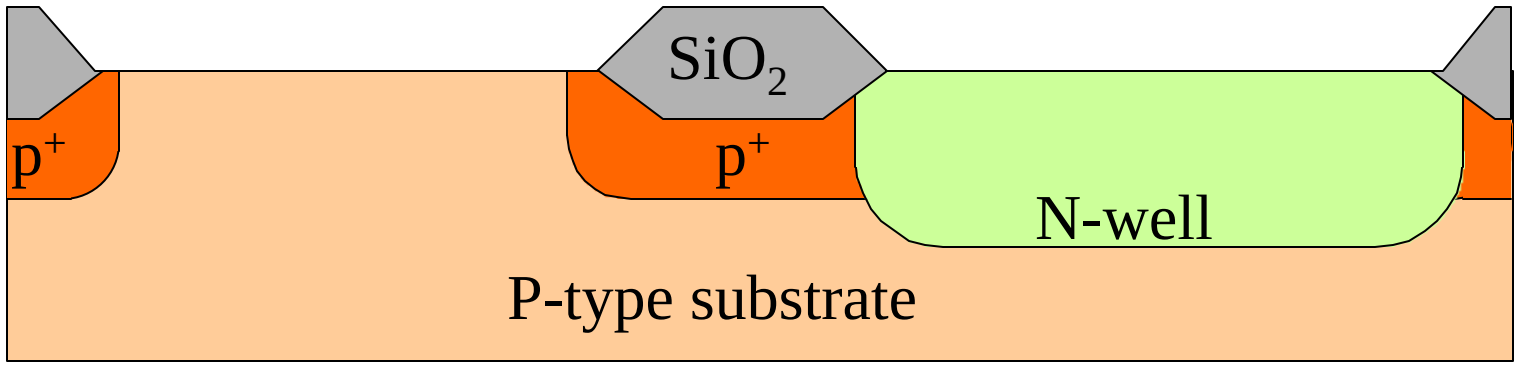


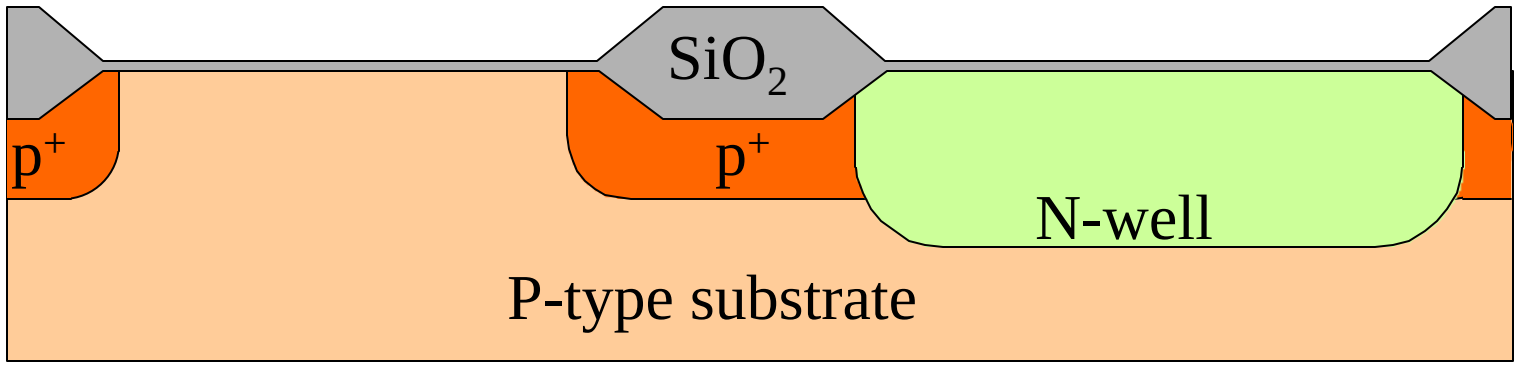
N-well Drive-in



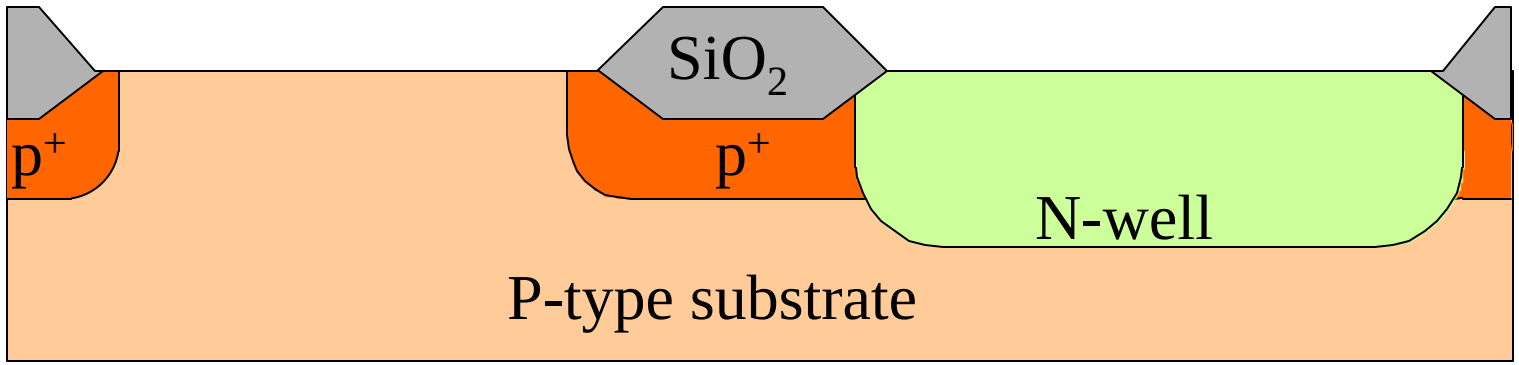
Strip Screen Oxide



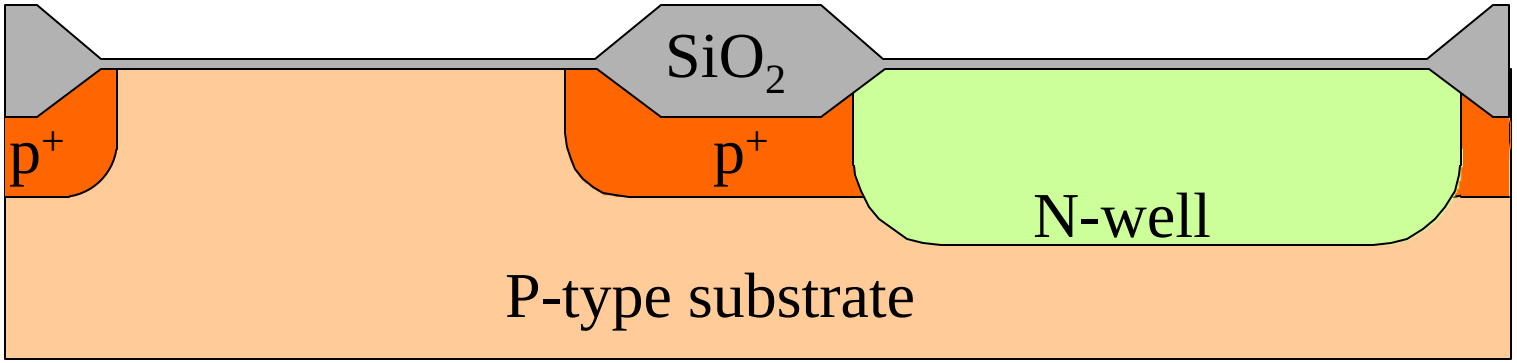
Grow Sacrificial Oxide



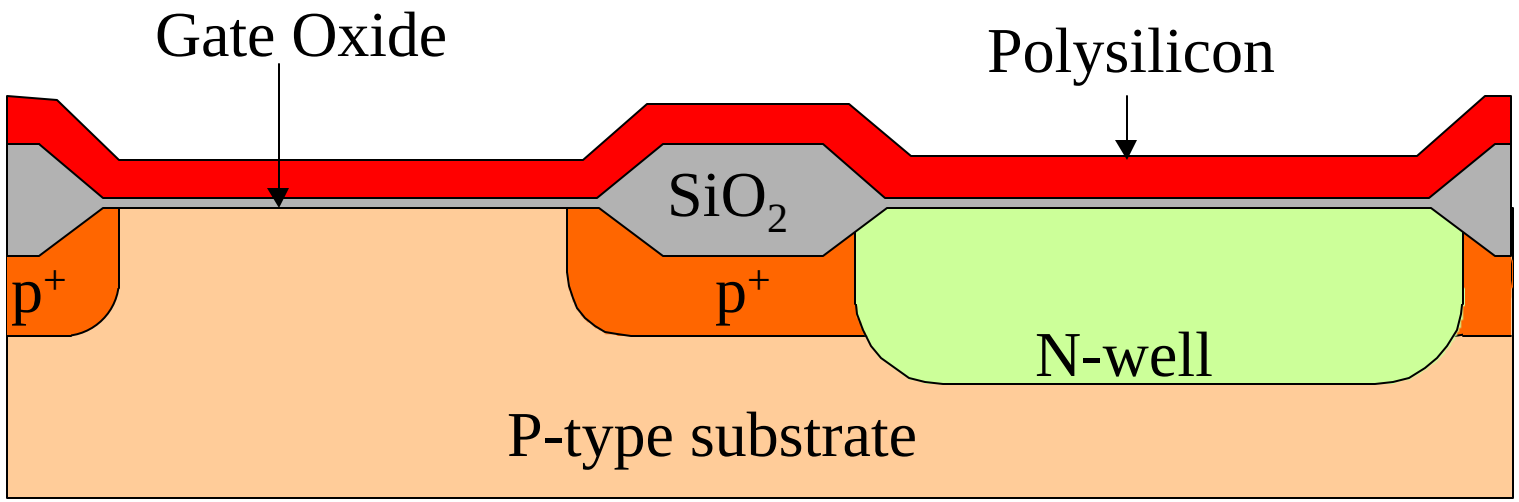
Strip Sacrificial Oxide



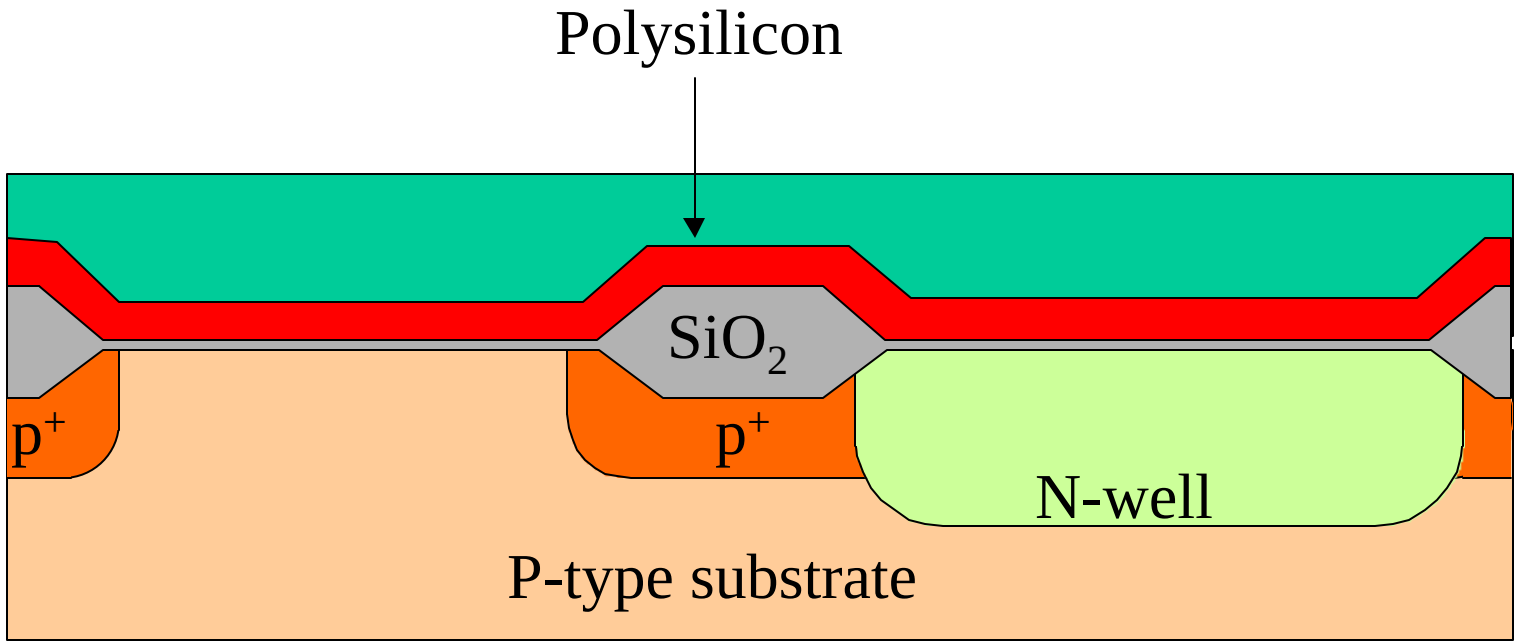
Grow Gate Oxide



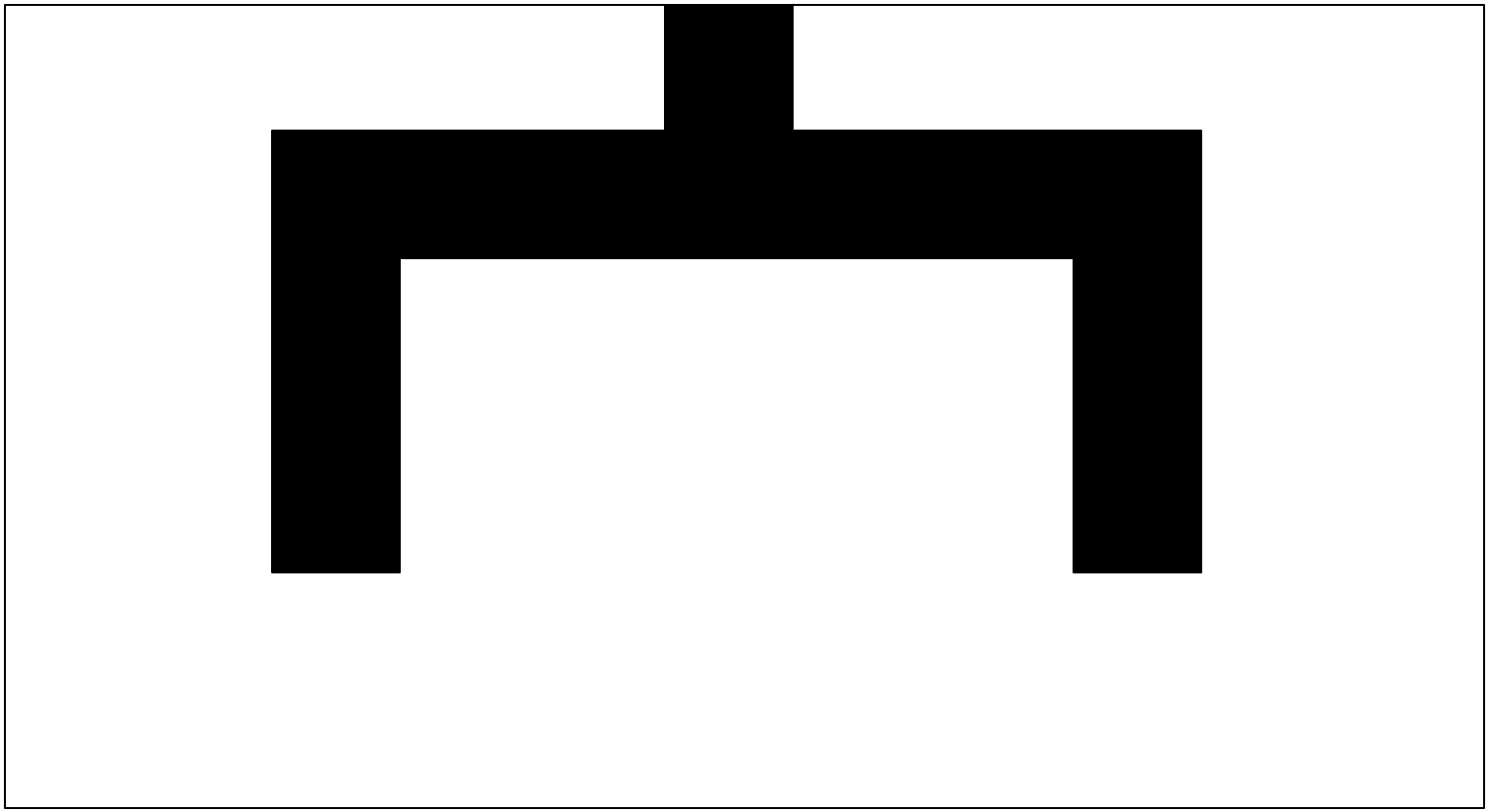
Deposit Polysilicon



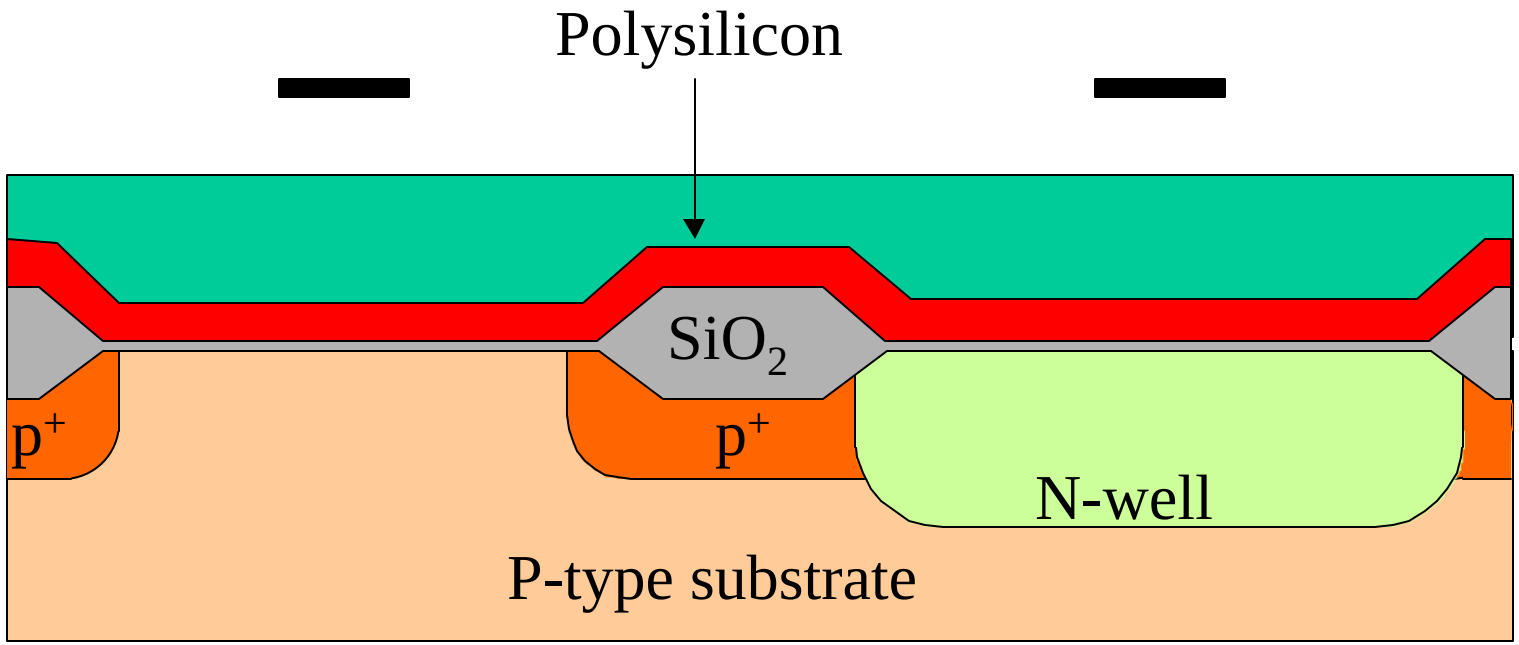
Photoresist Coating



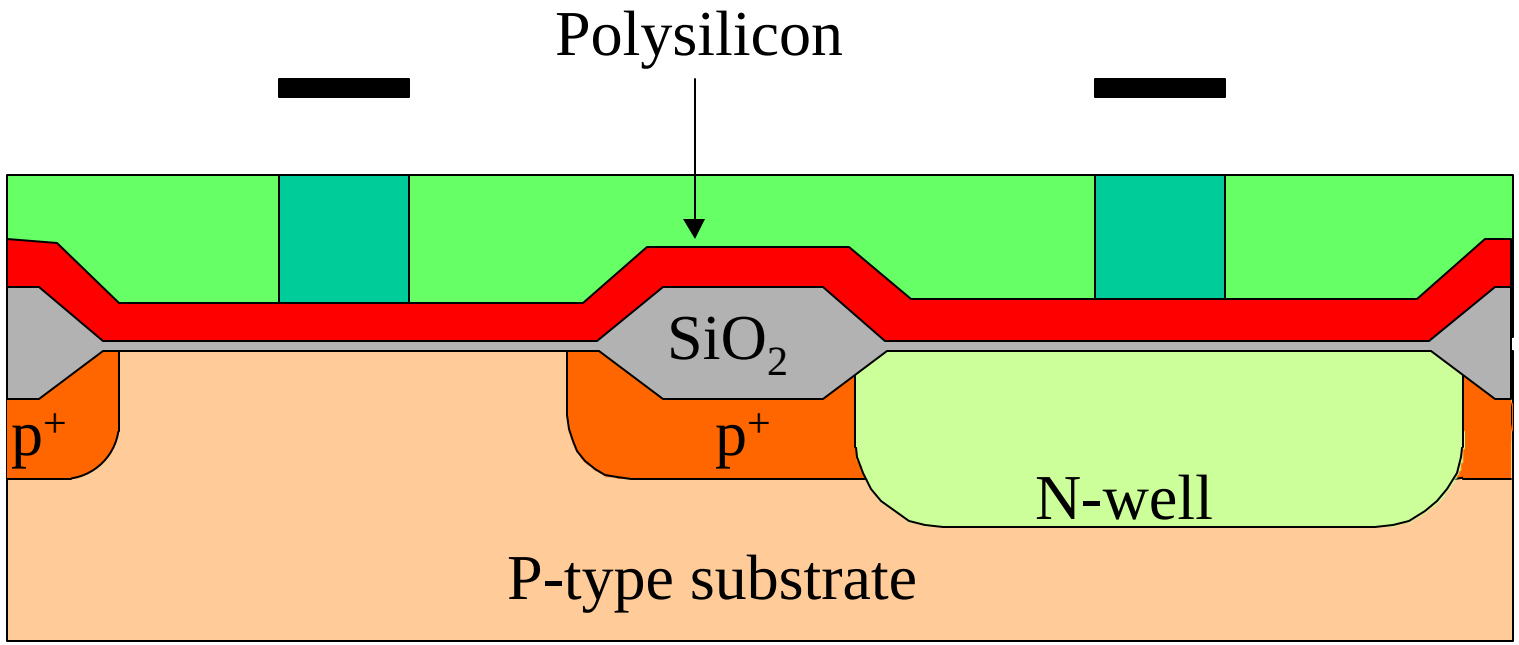
Mask 3, Gate and Local Interconnection



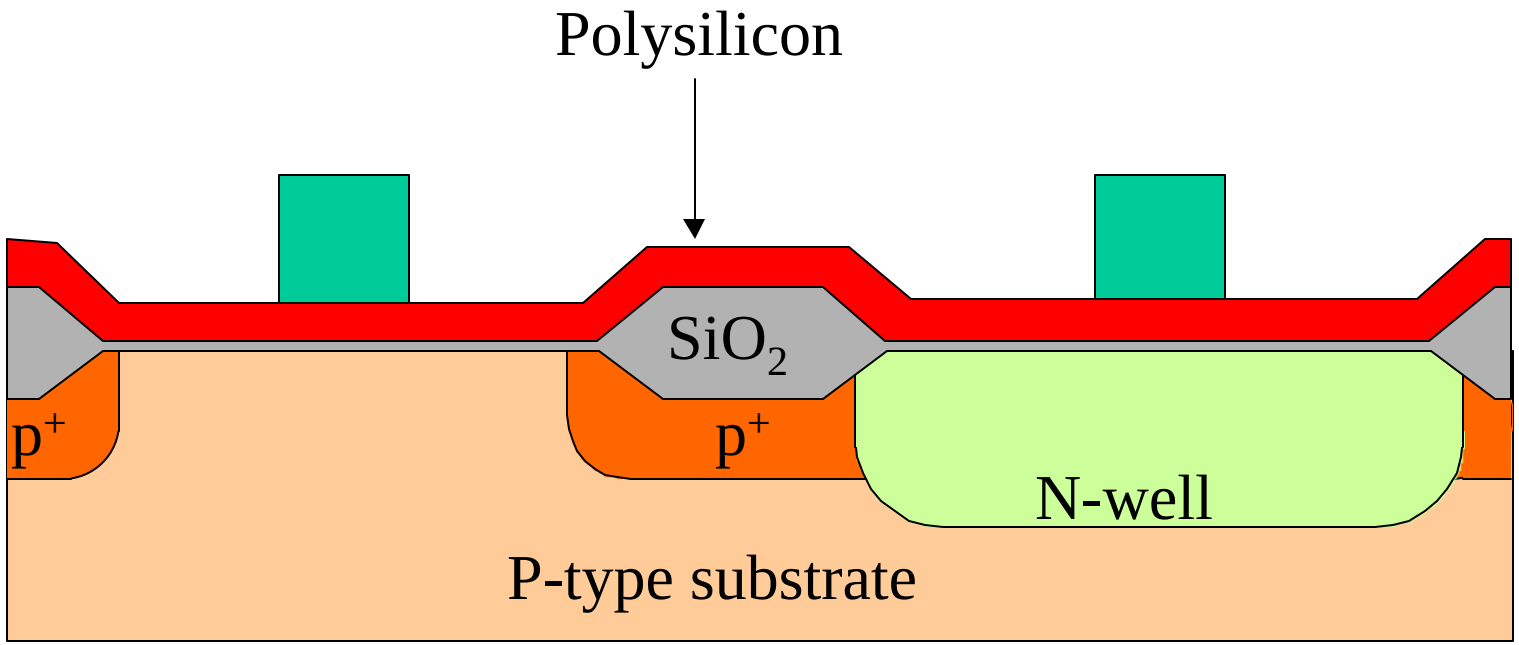
Mask 3, Gate and Local Interconnection



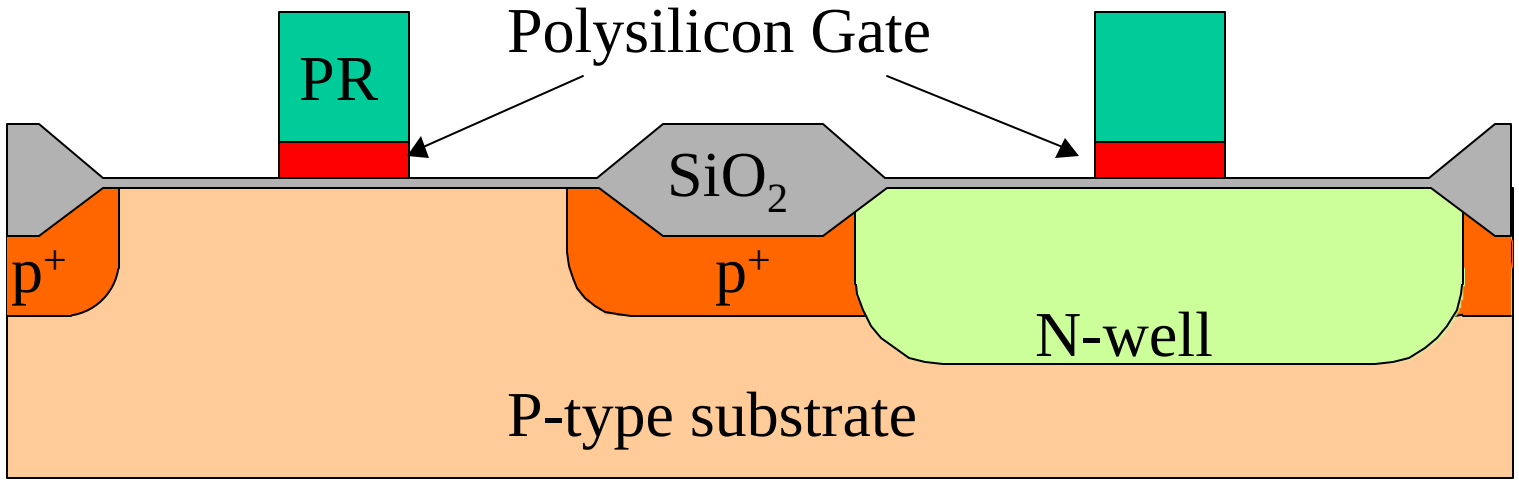
Exposure



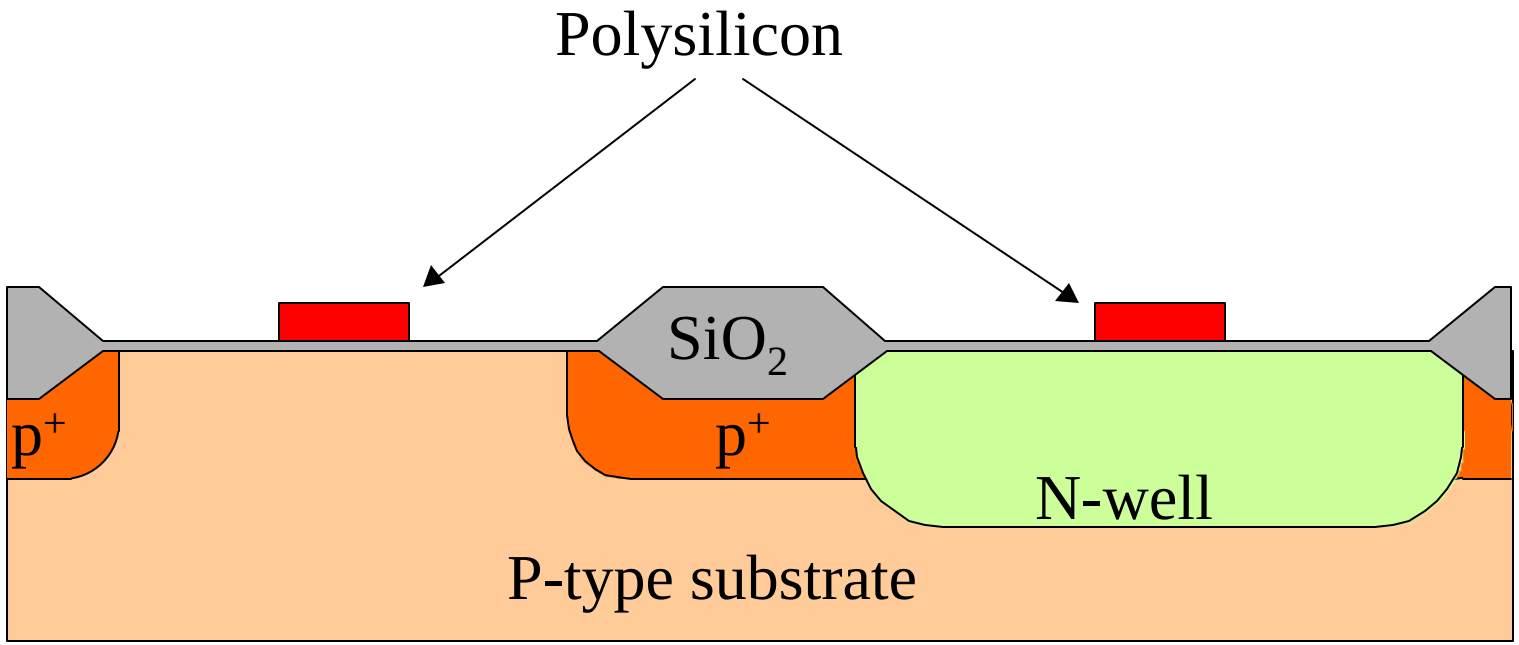
Development



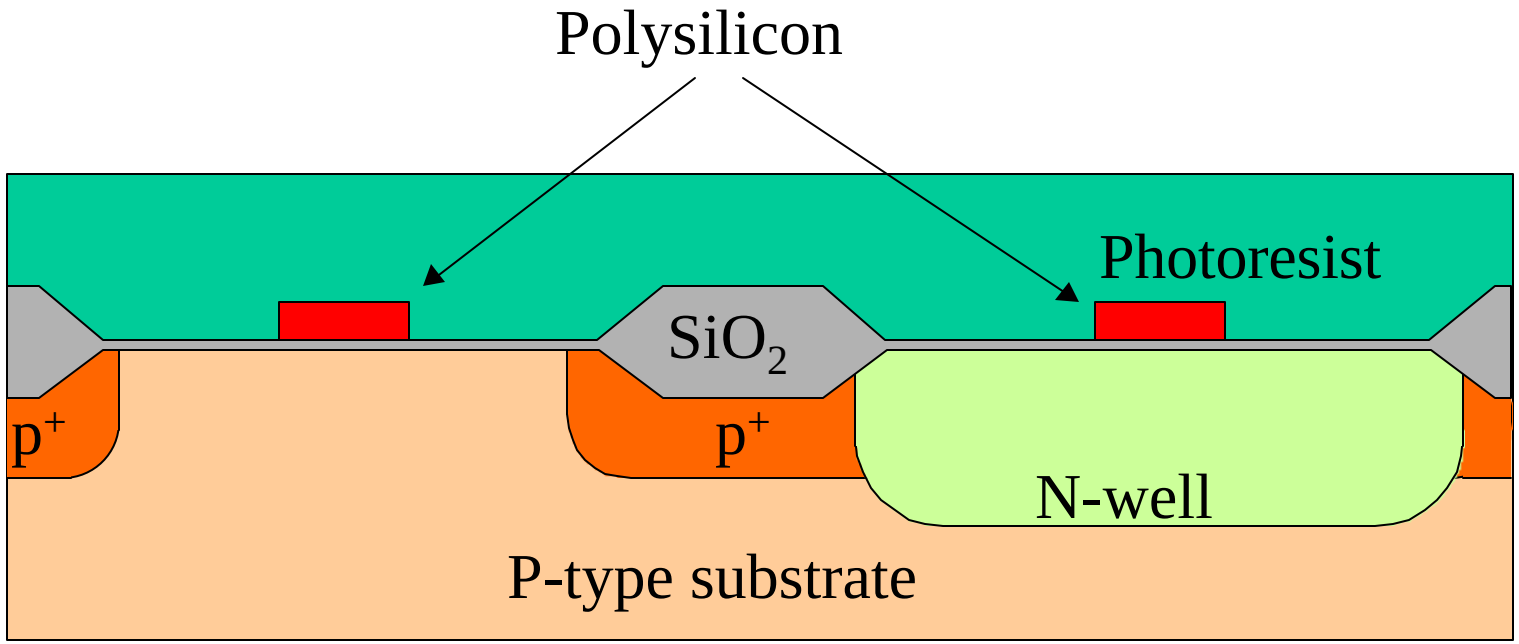
Etch Polysilicon



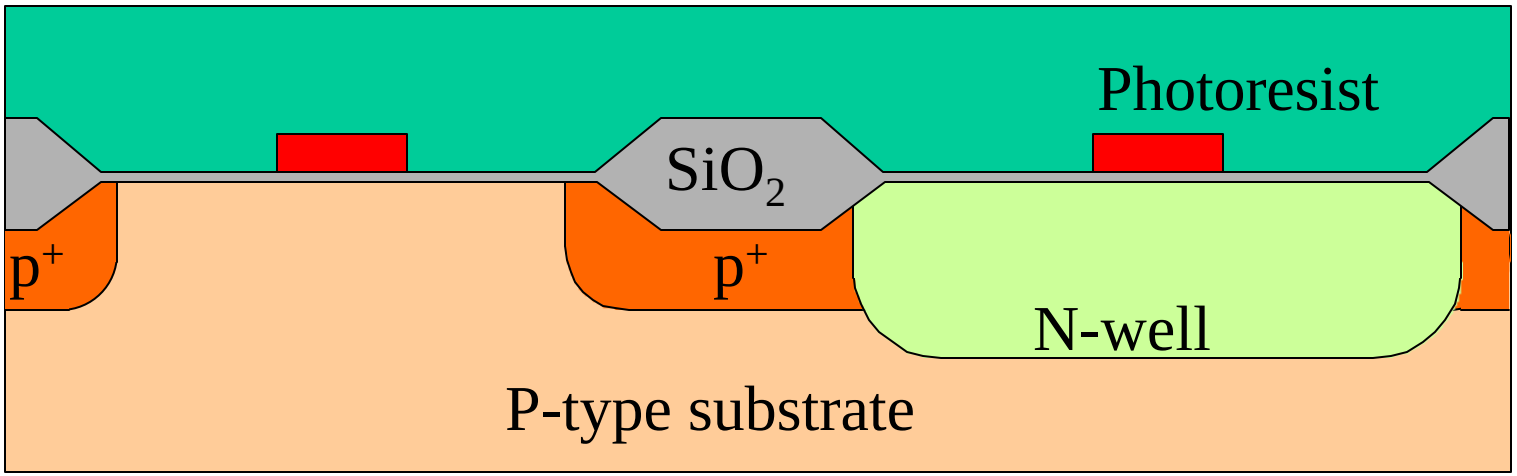
Strip Photoresist



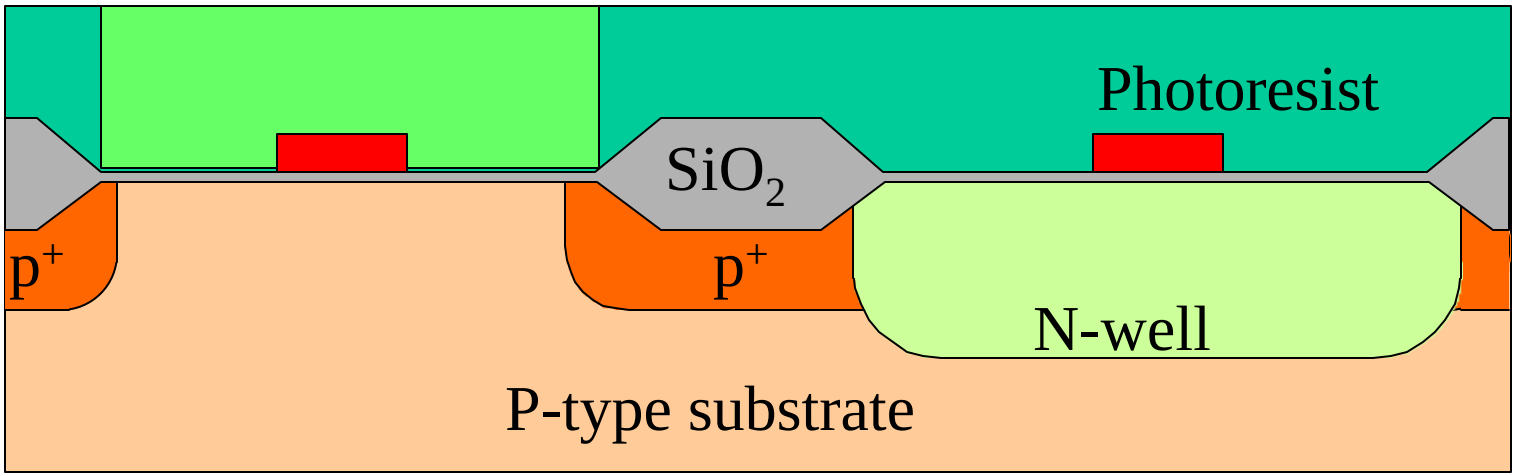
Photoresist Coating



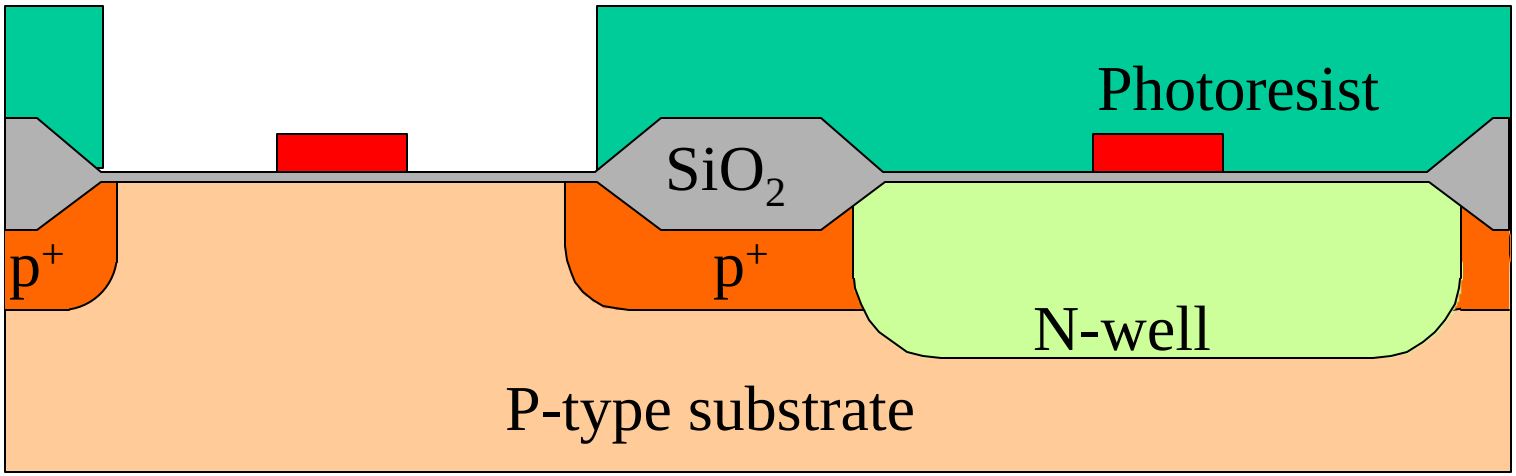
Mask 4, n-Source/Drain



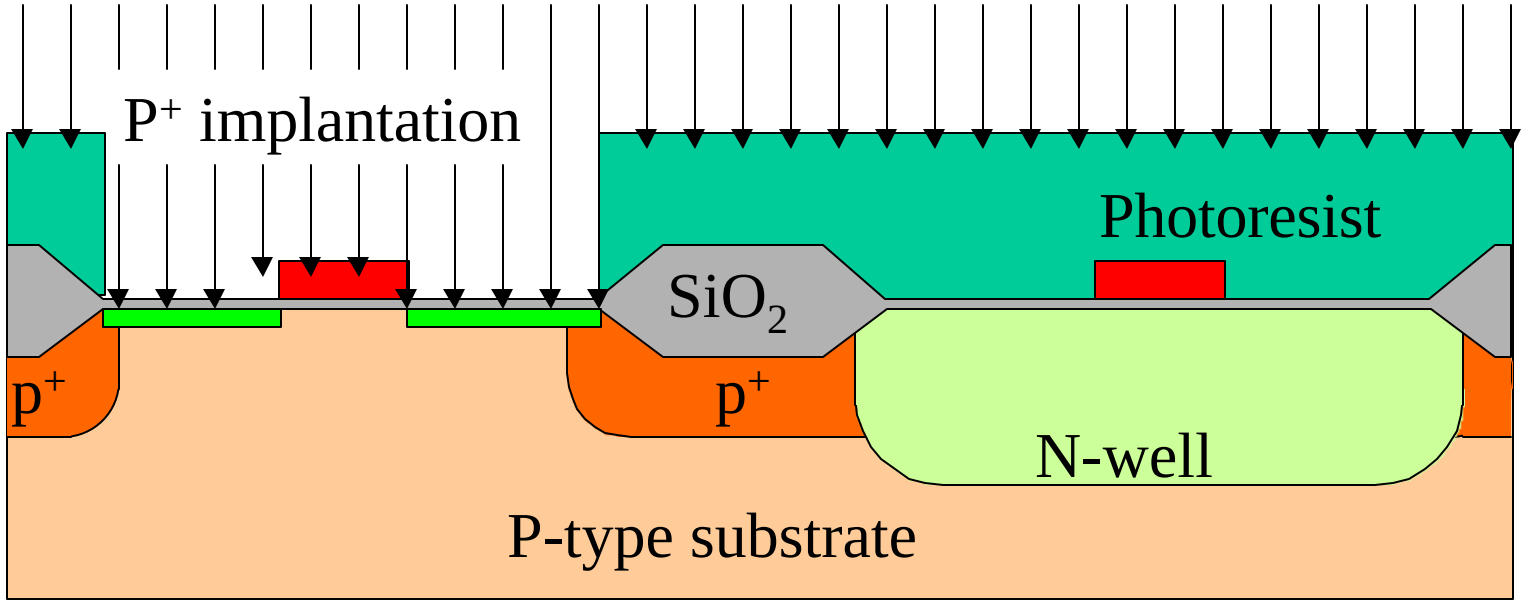
Exposure



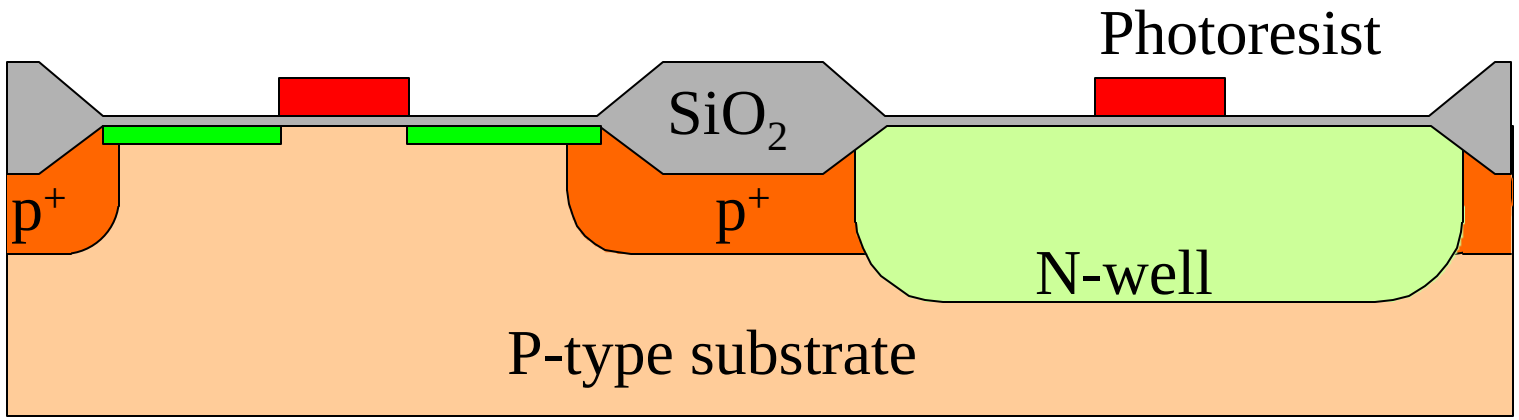
Development



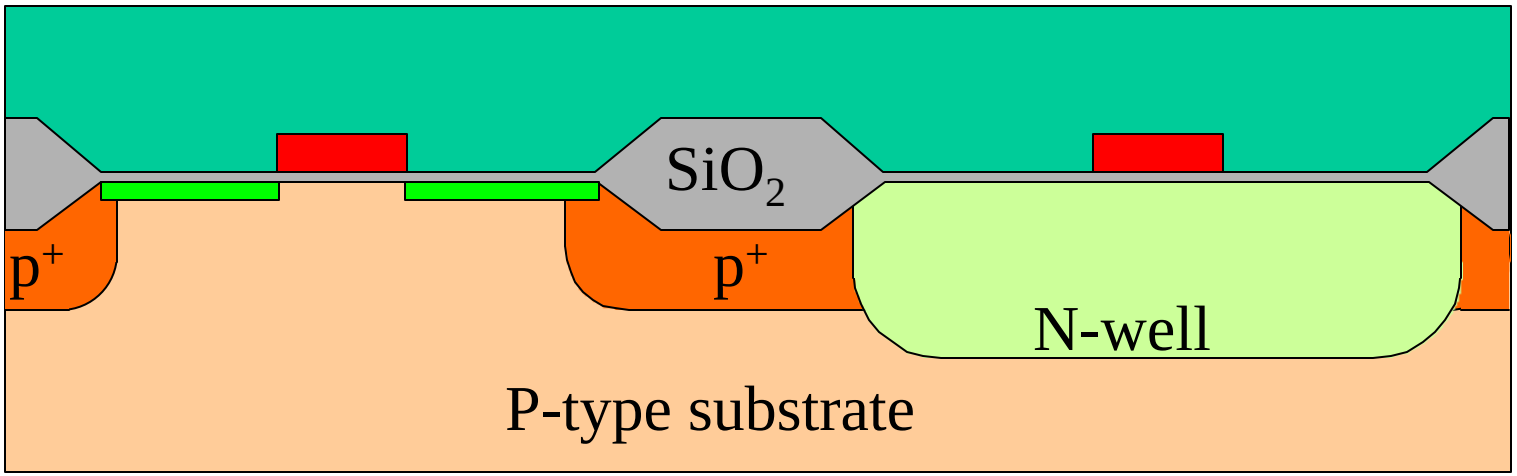
N-Source/Drain Ion Implantation



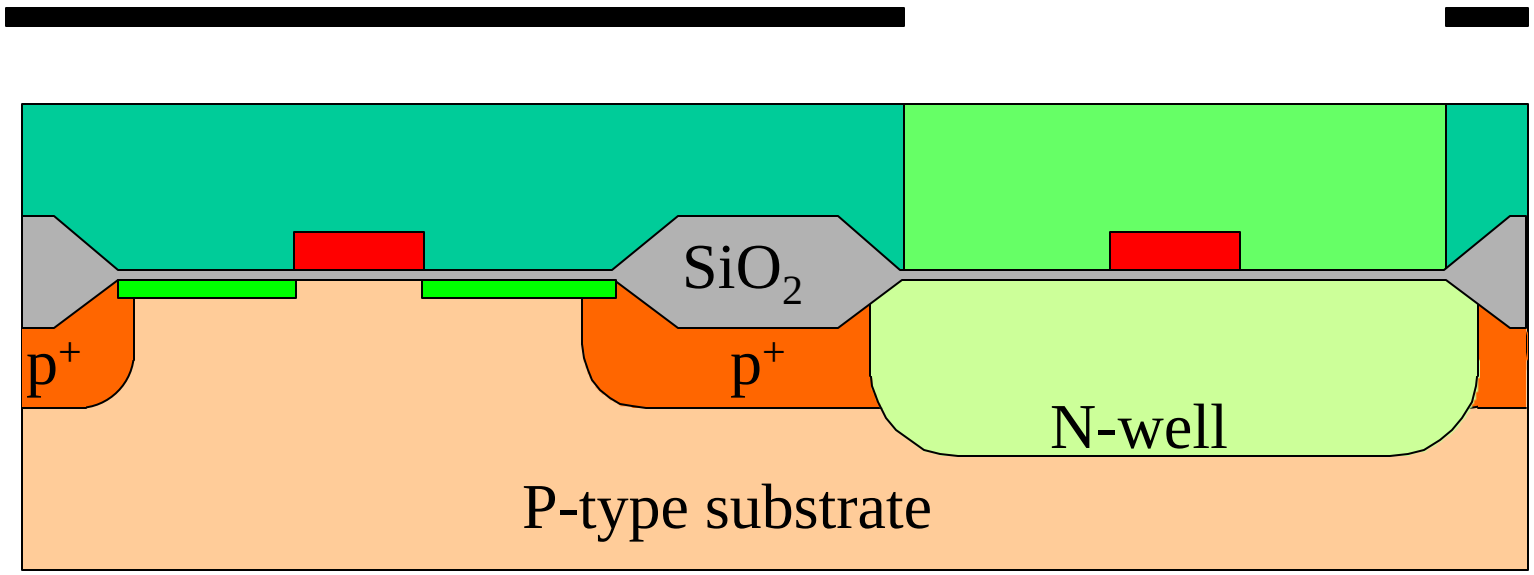
Strip Photoresist



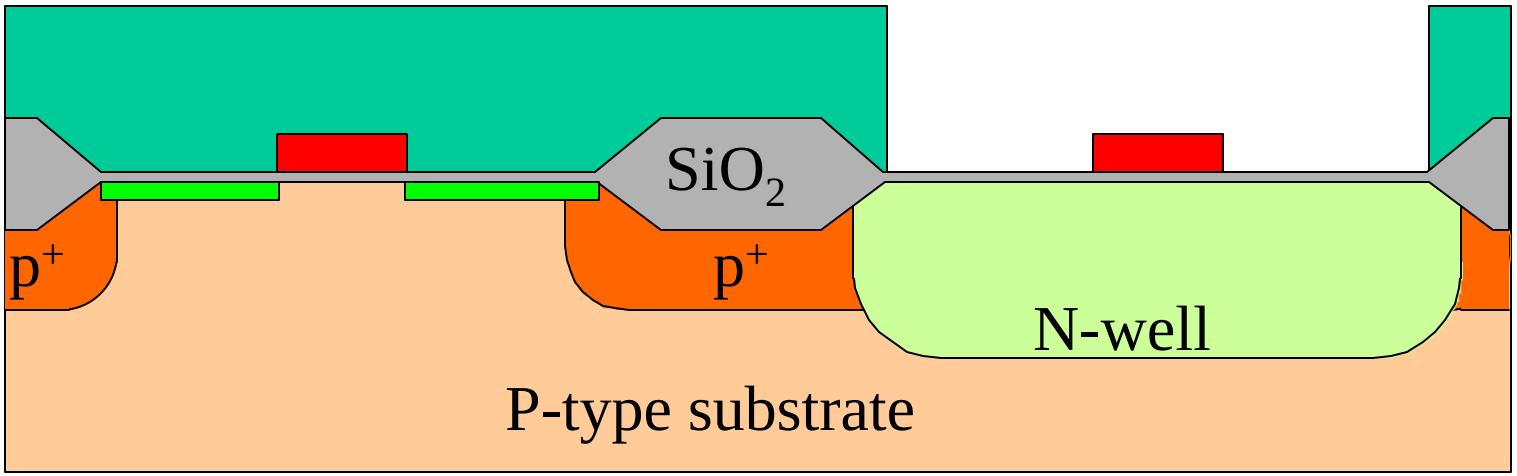
Photoresist Coating



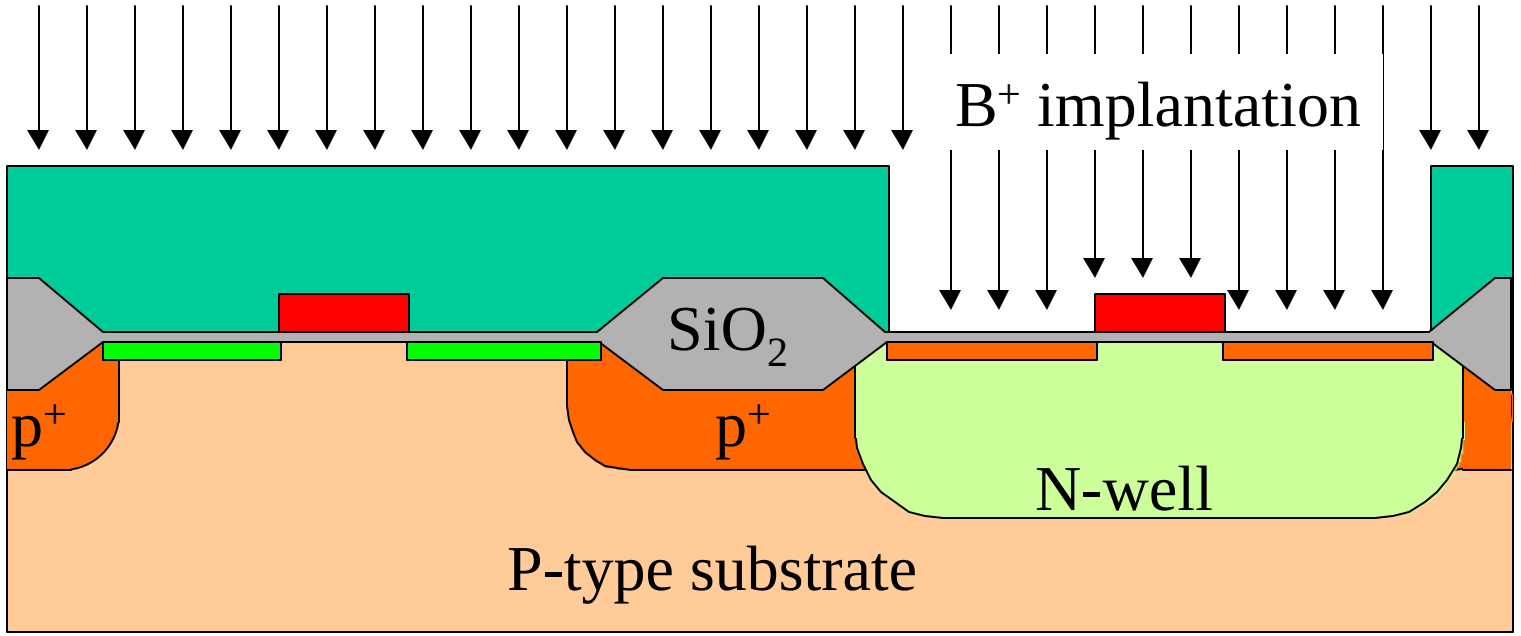
Mask 5, P-Source/Drain Exposure



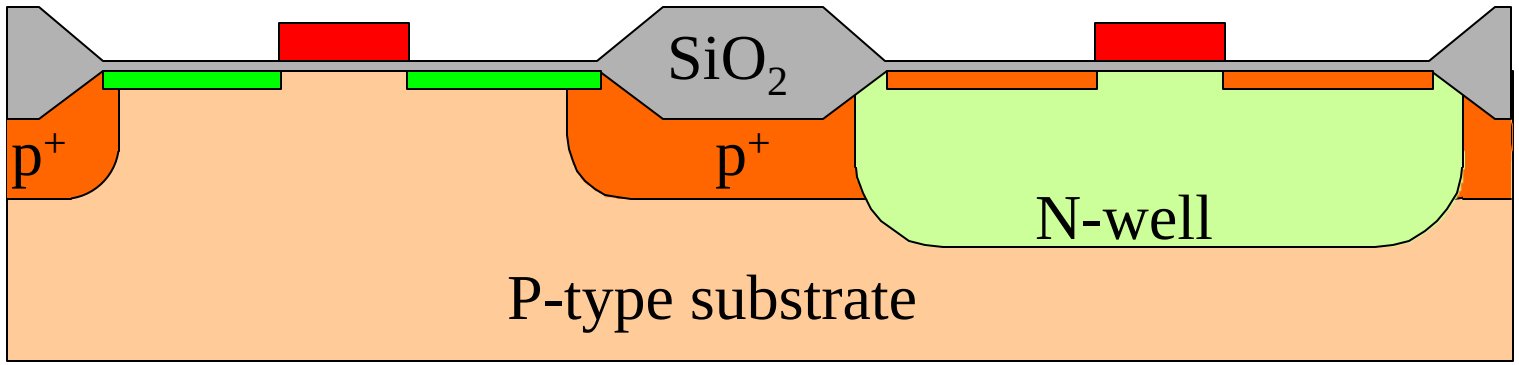
Development



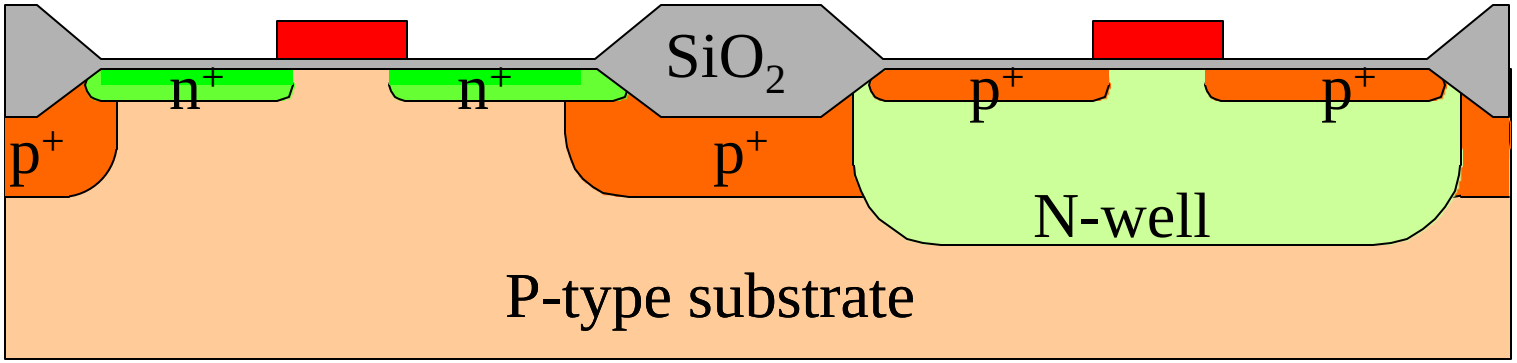
P-Source/Drain Implantation



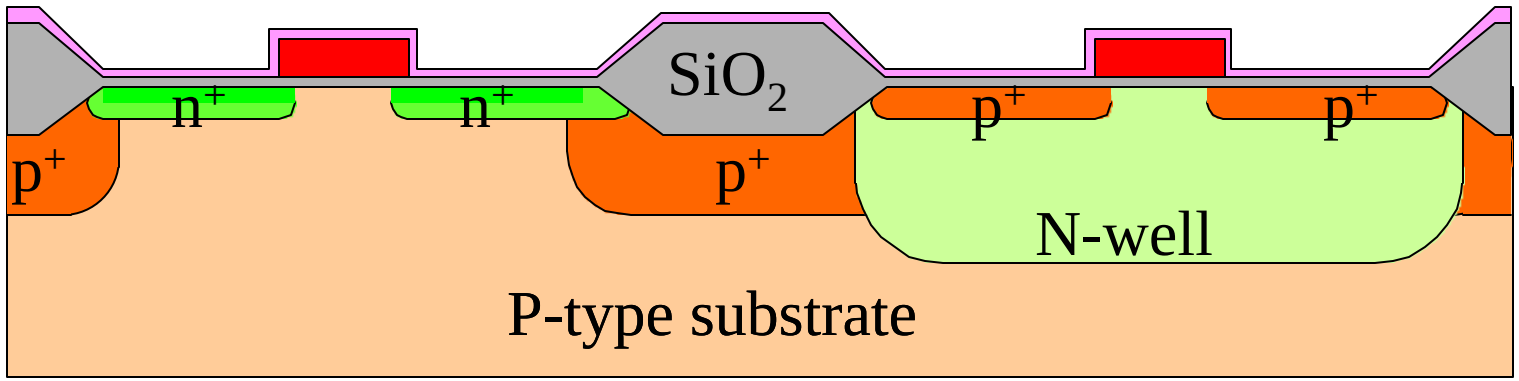
Strip Photoresist



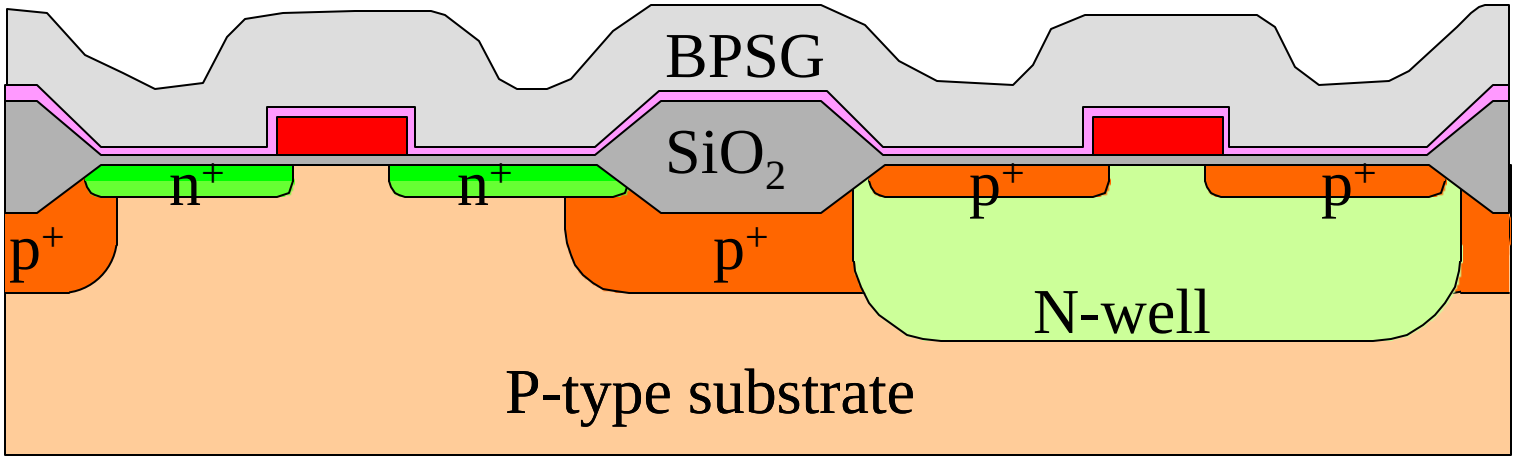
Anneal



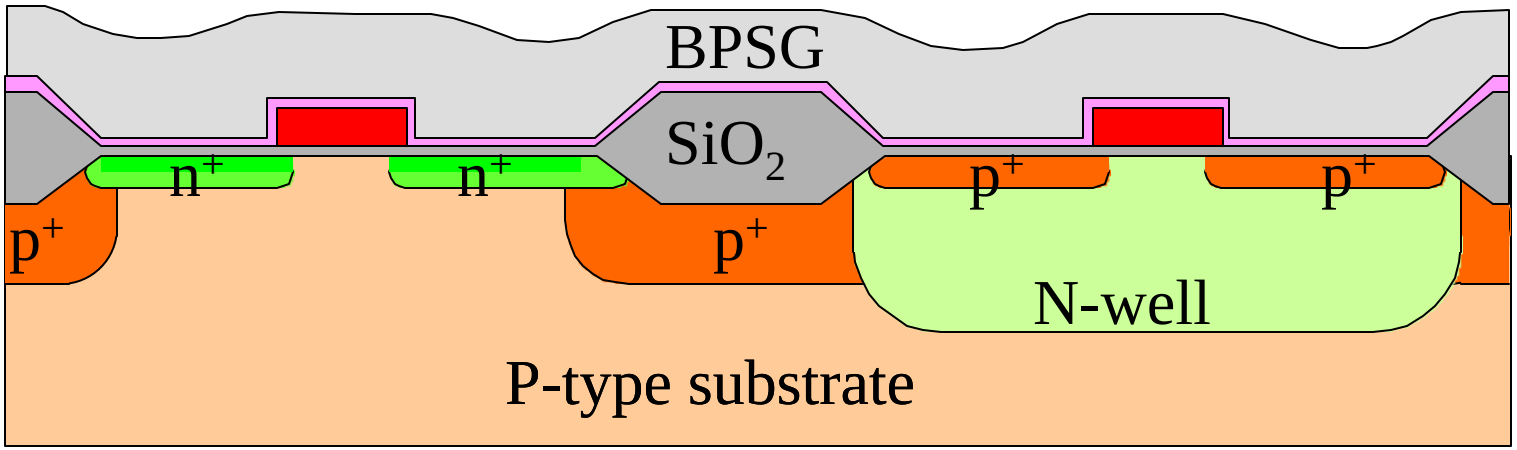
LPCVD Barrier Nitride



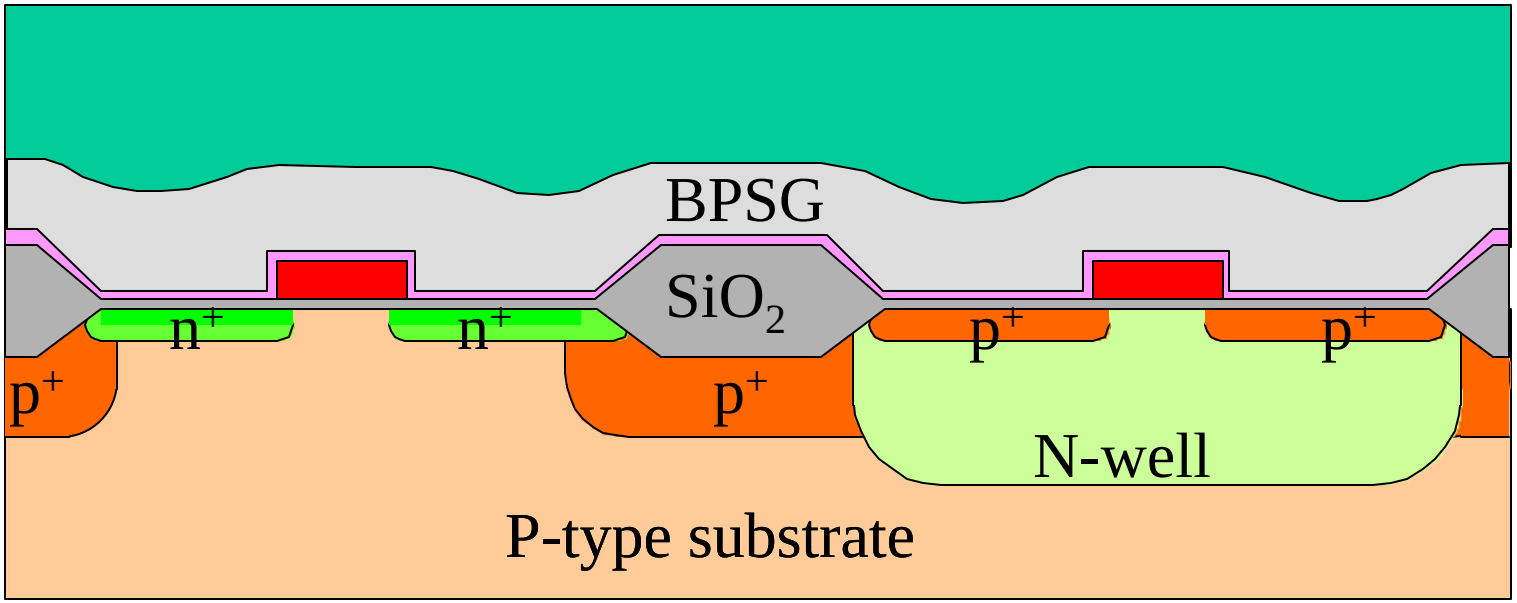
CVD BPSG



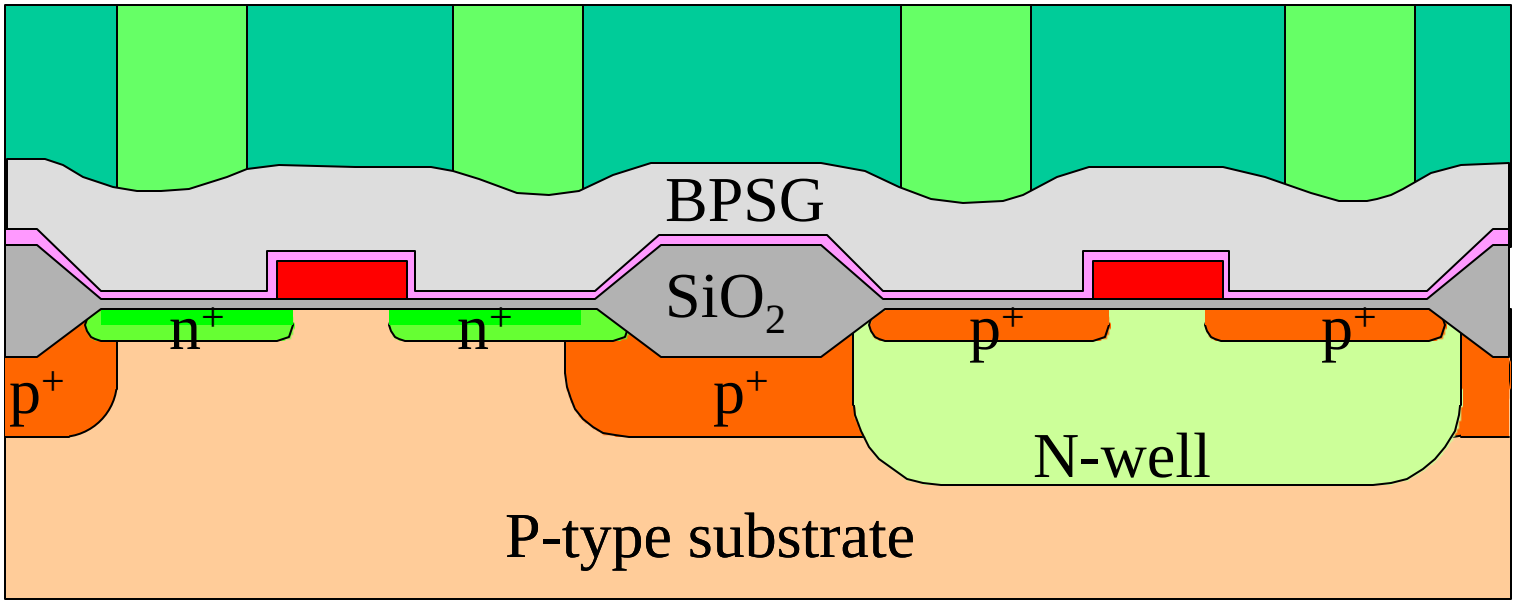
BPSG Reflow



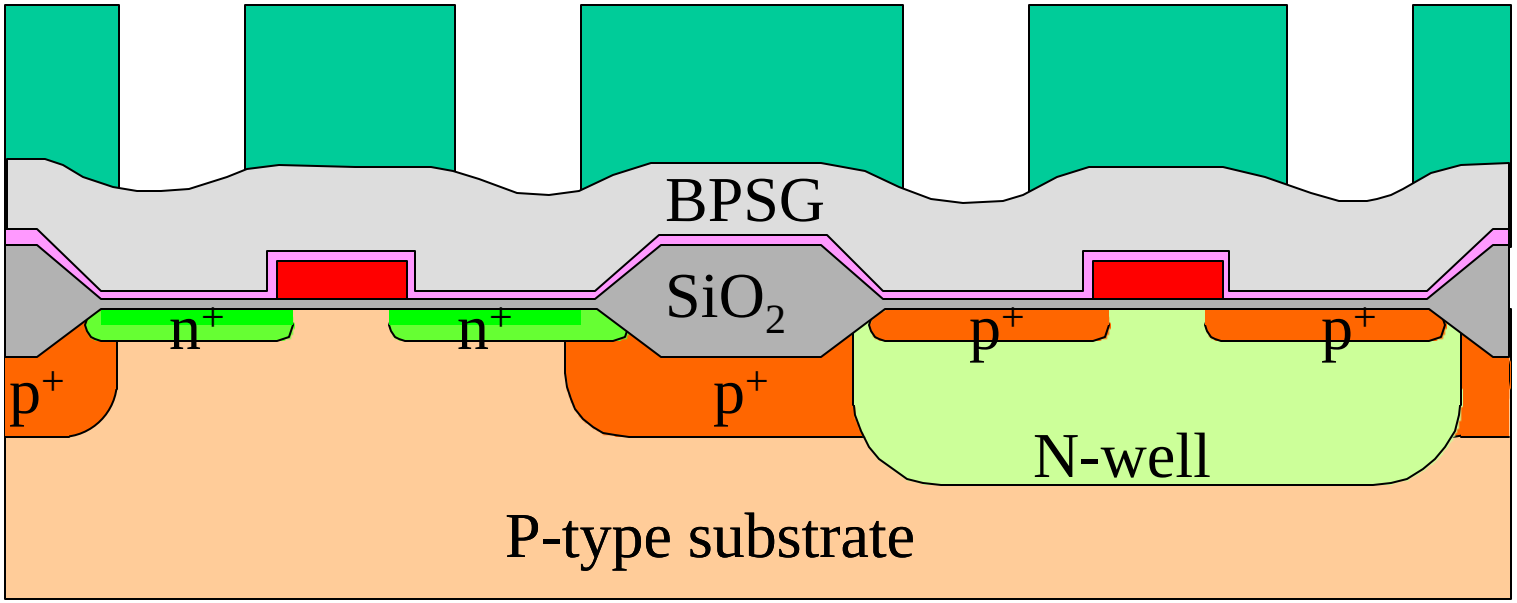
Photoresist Coating



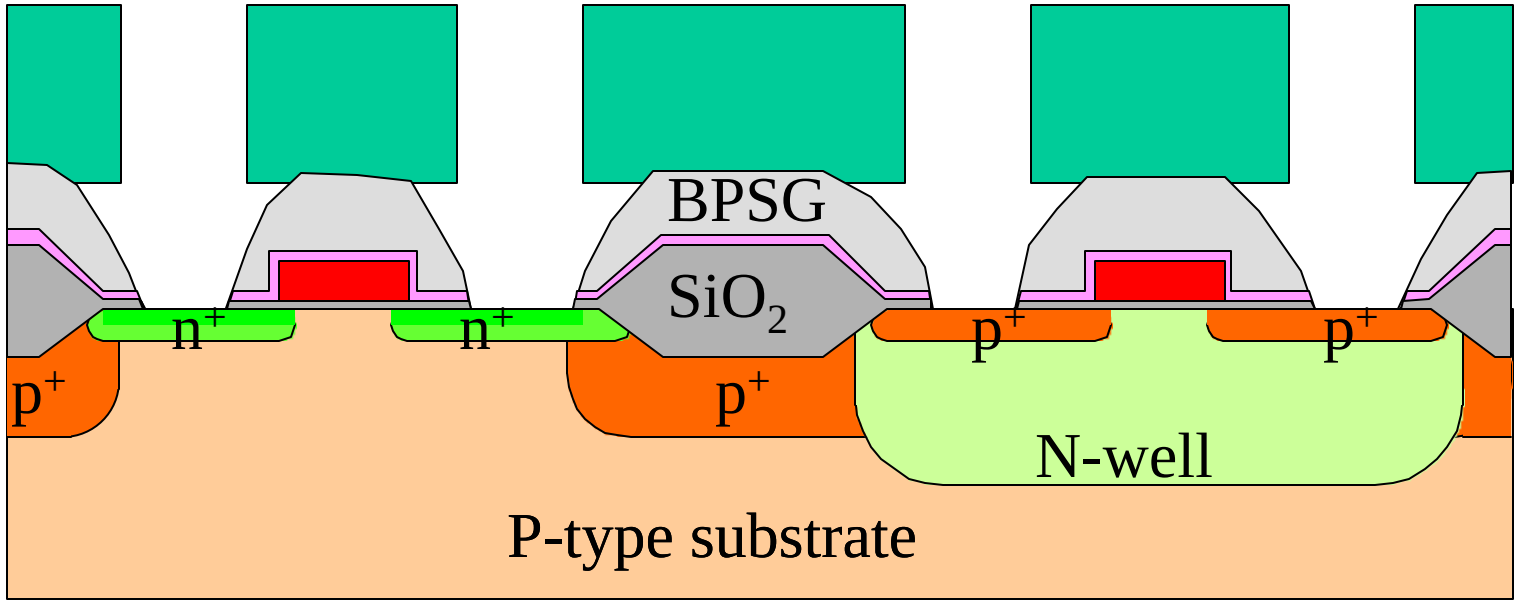
Mask 6, Contact Exposure



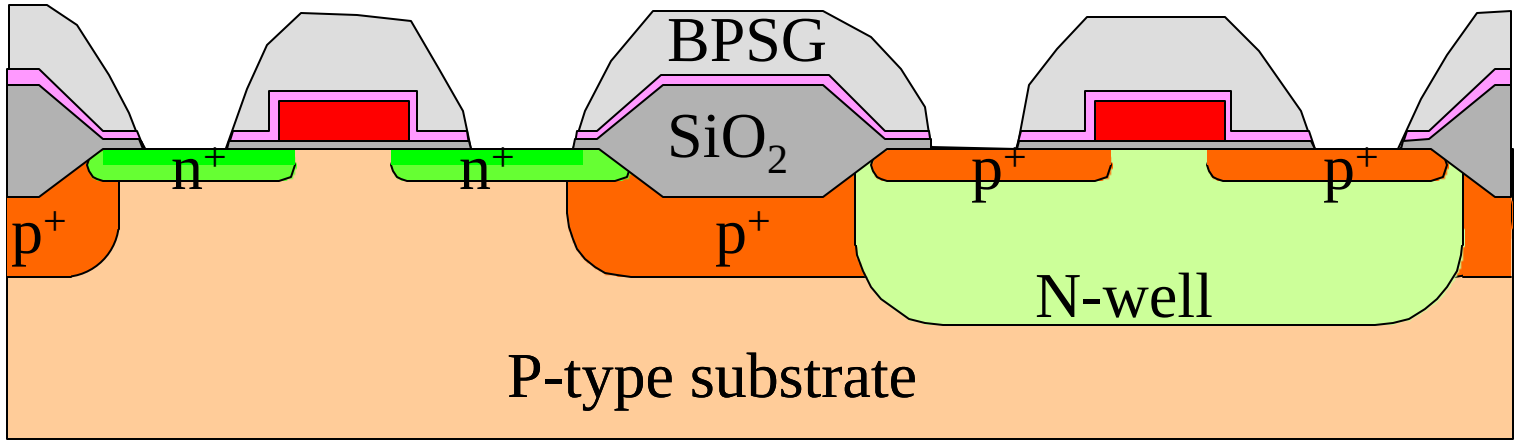
Development



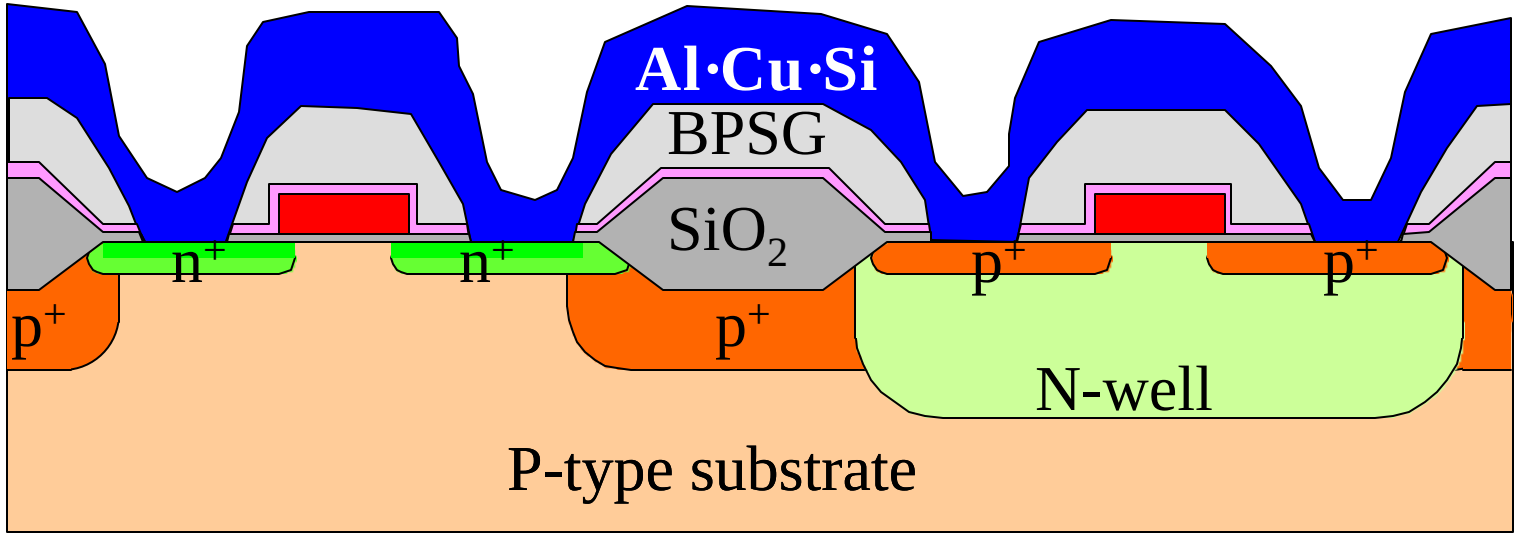
Contact Etch



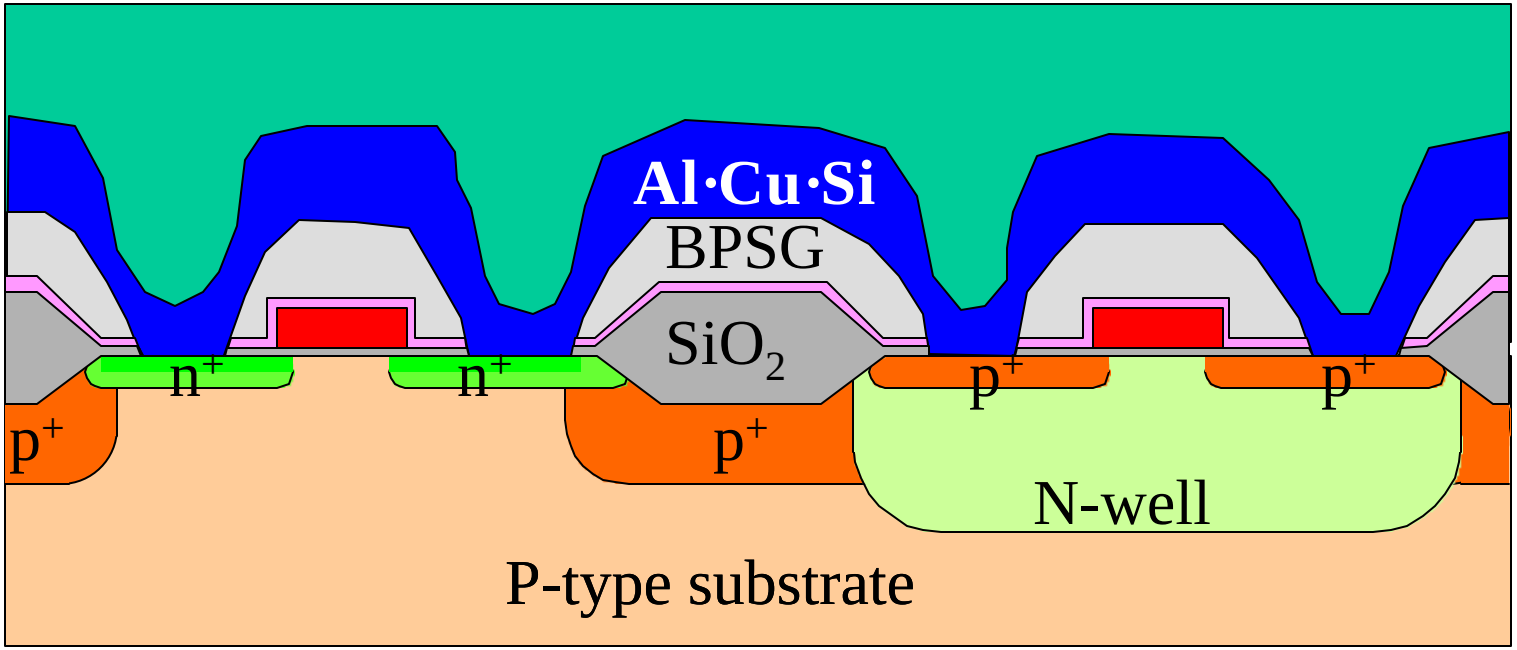
Strip Photoresist



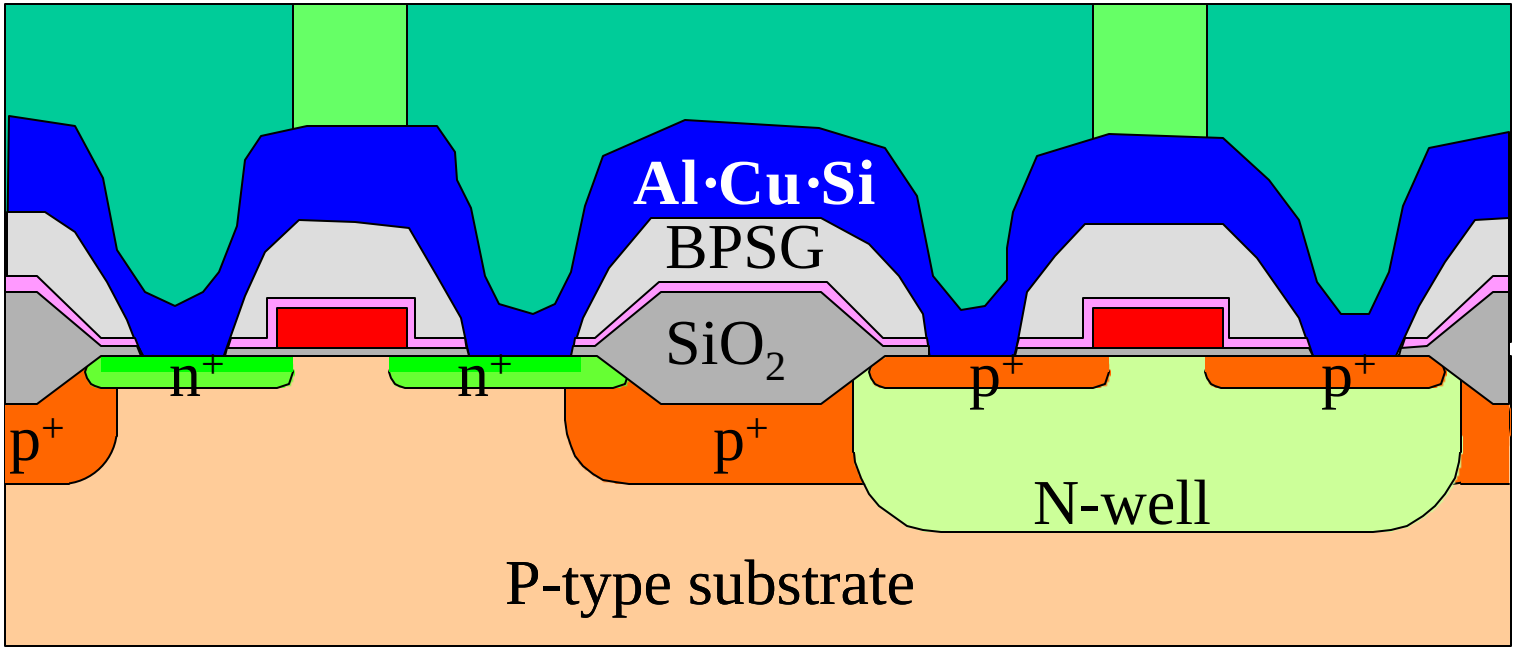
Metal Deposition



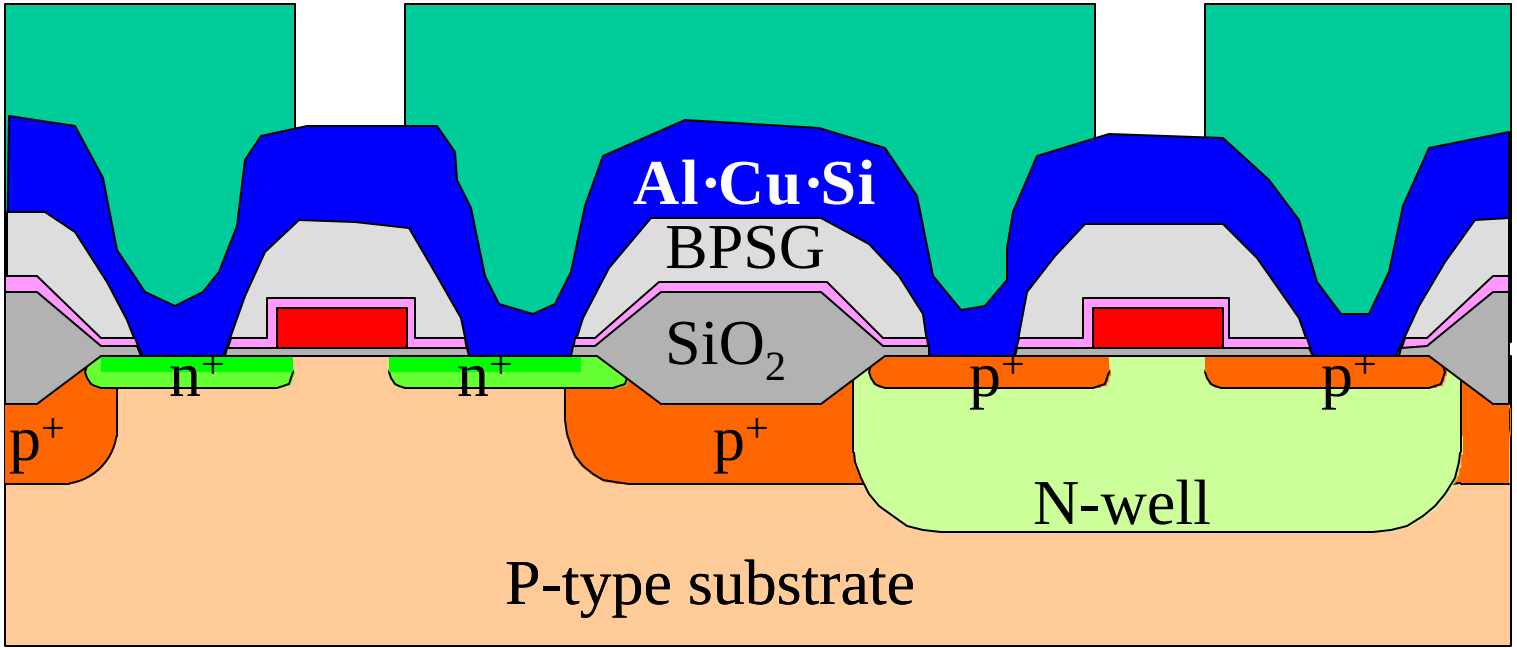
Photoresist Coating



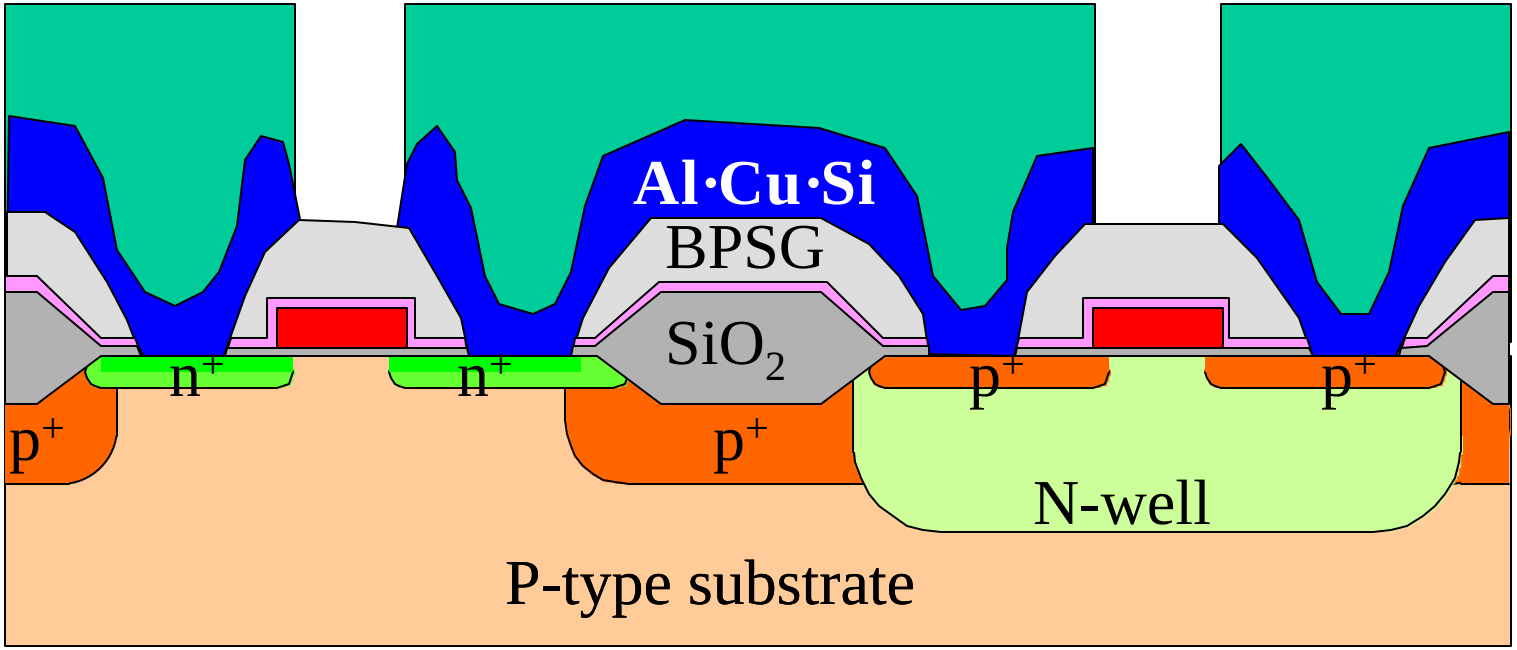
Mask 7, Metal Interconnection Exposure



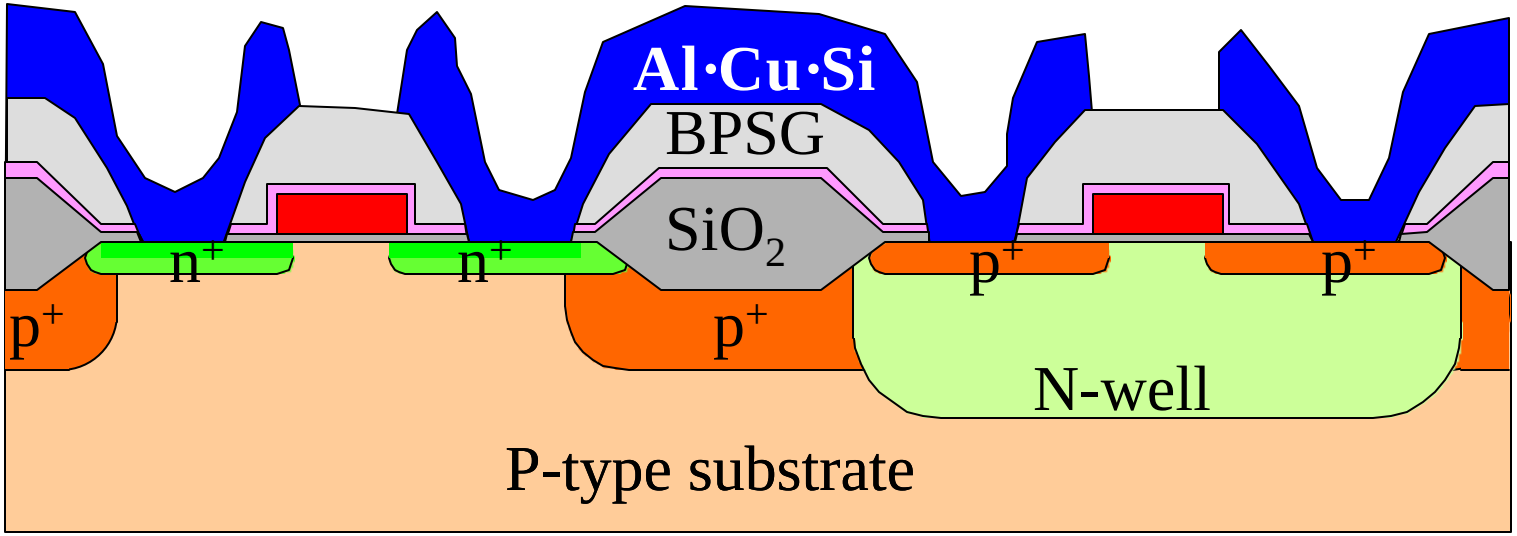
Development



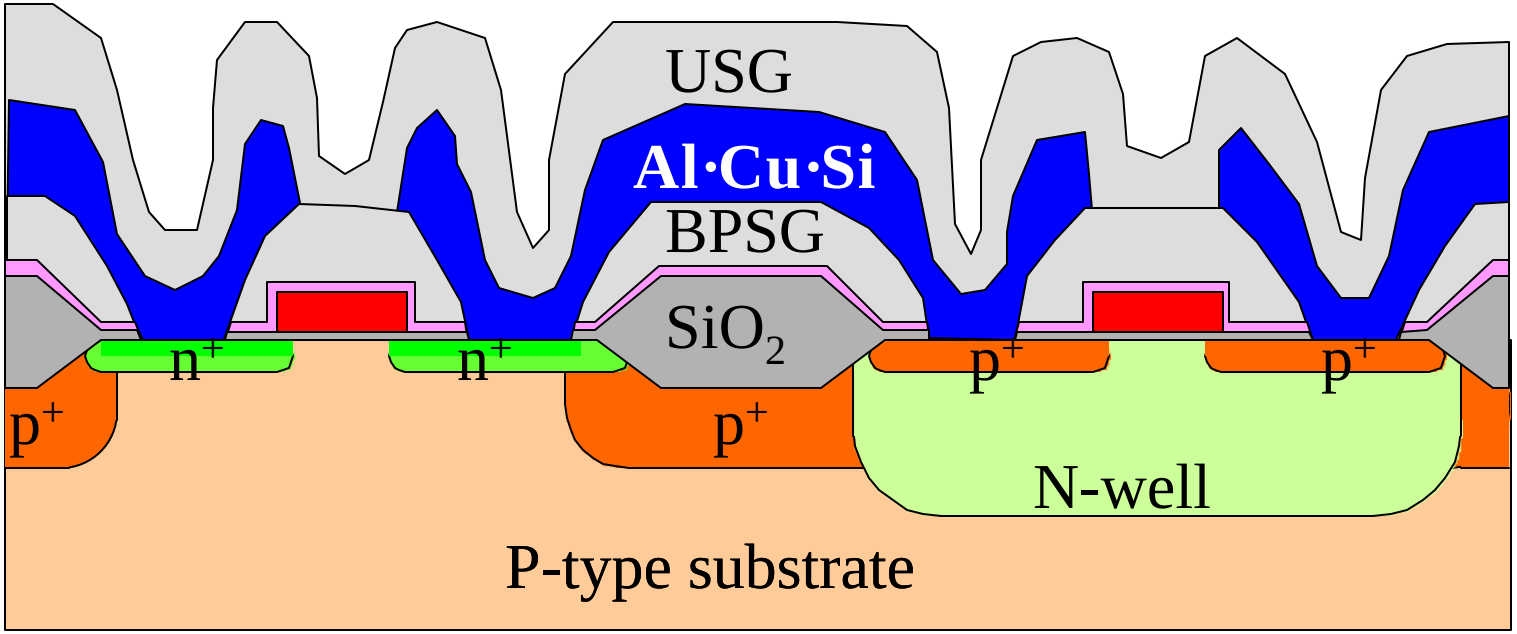
Etch Metal



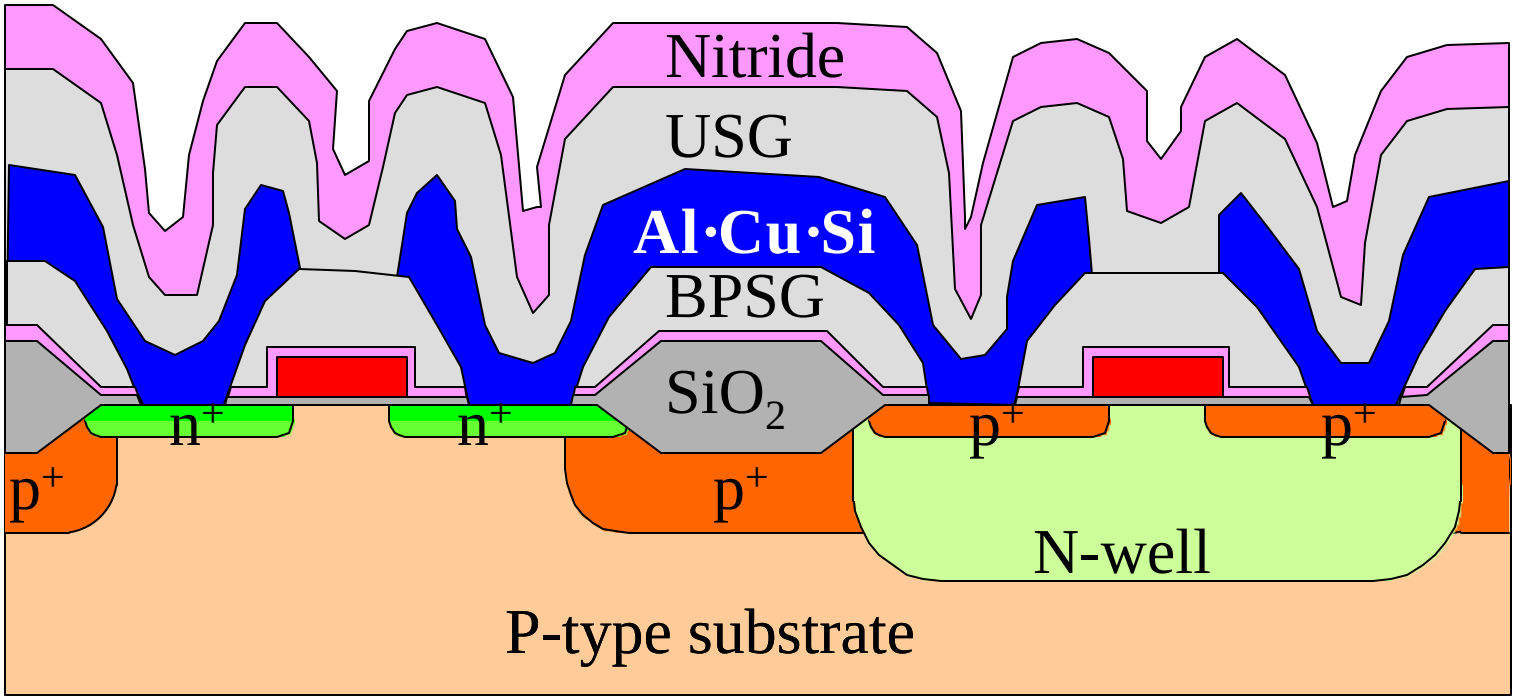
Strip Photoresist



CVD USG



CVD Nitride



1990's Technology

- Driving force: digital logic electronics
  - PC, telecommunication, and internet.
- Feature size: from 0.8 μm to 0.18 μm
- Wafer size: from 150 mm to 300 mm

1990's CMOS Technology

- Epitaxy silicon
- Shallow trench isolation
- The sidewall spacer for LDD and salicide
- Polycide gates and local interconnections reduce resistance and improve device speed
  - Tungsten silicide and titanium silicide.

1990's CMOS Technology

- Photolithography
  - G-line, I-line (365 nm), and DUV 248 nm
  - Positive photoresist
  - Steppers replaced projection printer
  - Track-stepper integrated systems
- Plasma etches for patterned etch
- Wet etches for blanket film stripping

1990's CMOS Technology

- Vertical furnaces
  - smaller footprints, better contamination control.
- RTP systems
  - post-implantation annealing
  - silicide formation,
  - faster, better process and thermal budget control.
- DC magnetron sputtering replaced evaporation

1990's CMOS Technology

- Multi-layer metal interconnection
- W CVD and CMP (or etch back) to form plugs
- Ti and TiN barrier/adhesion layer for W
- Ti welding layer for Al-Cu to reduce contact resistance
- TiN ARC

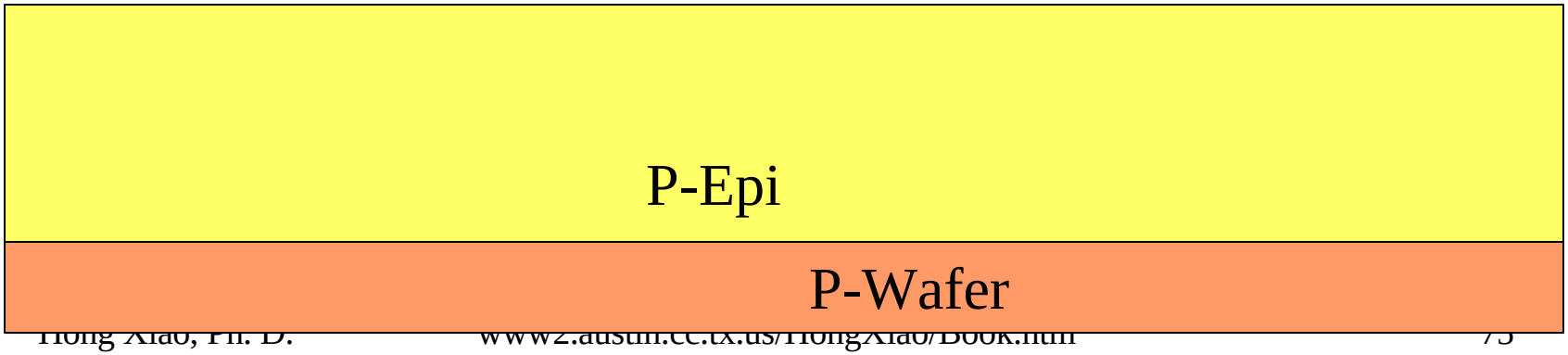
1990's CMOS Technology

- BPSG was popularly used as PMD.
- DCVD: PE-TEOS and O_3-TEOS
  - STI, sidewall spacer, PMD, and IMD
- DCVD: PE-silane
  - PMD barrier nitride, dielectric ARC, and PD nitride
- Tungsten CMP to form plug
- Dielectric CMP for planarization

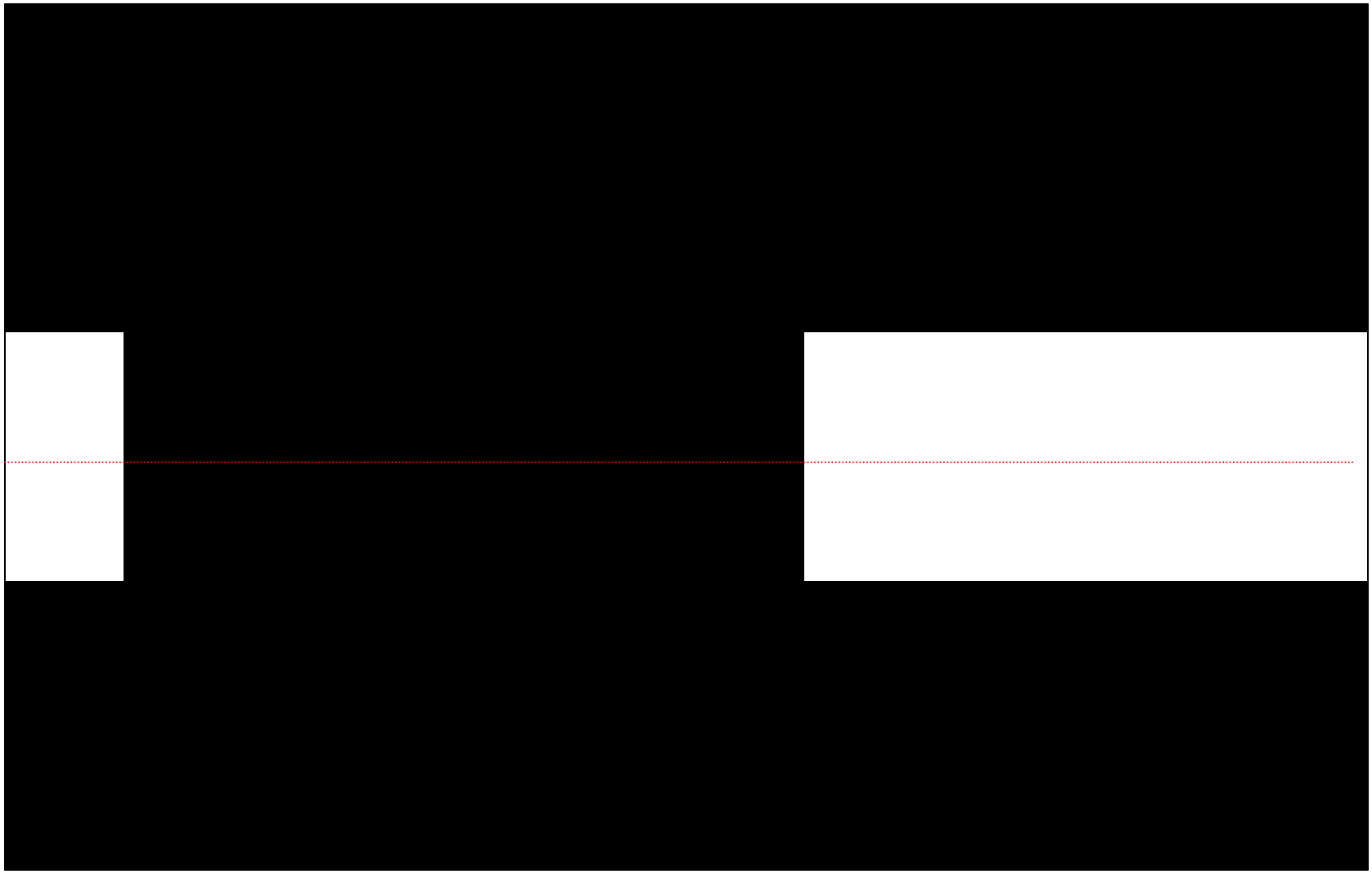
1990's CMOS Technology

- Cluster tools became very popular
- Single wafer processing systems improve wafer-to-wafer uniformity control
- Batch systems is still commonly employed in many non-critical processes for their high throughput.

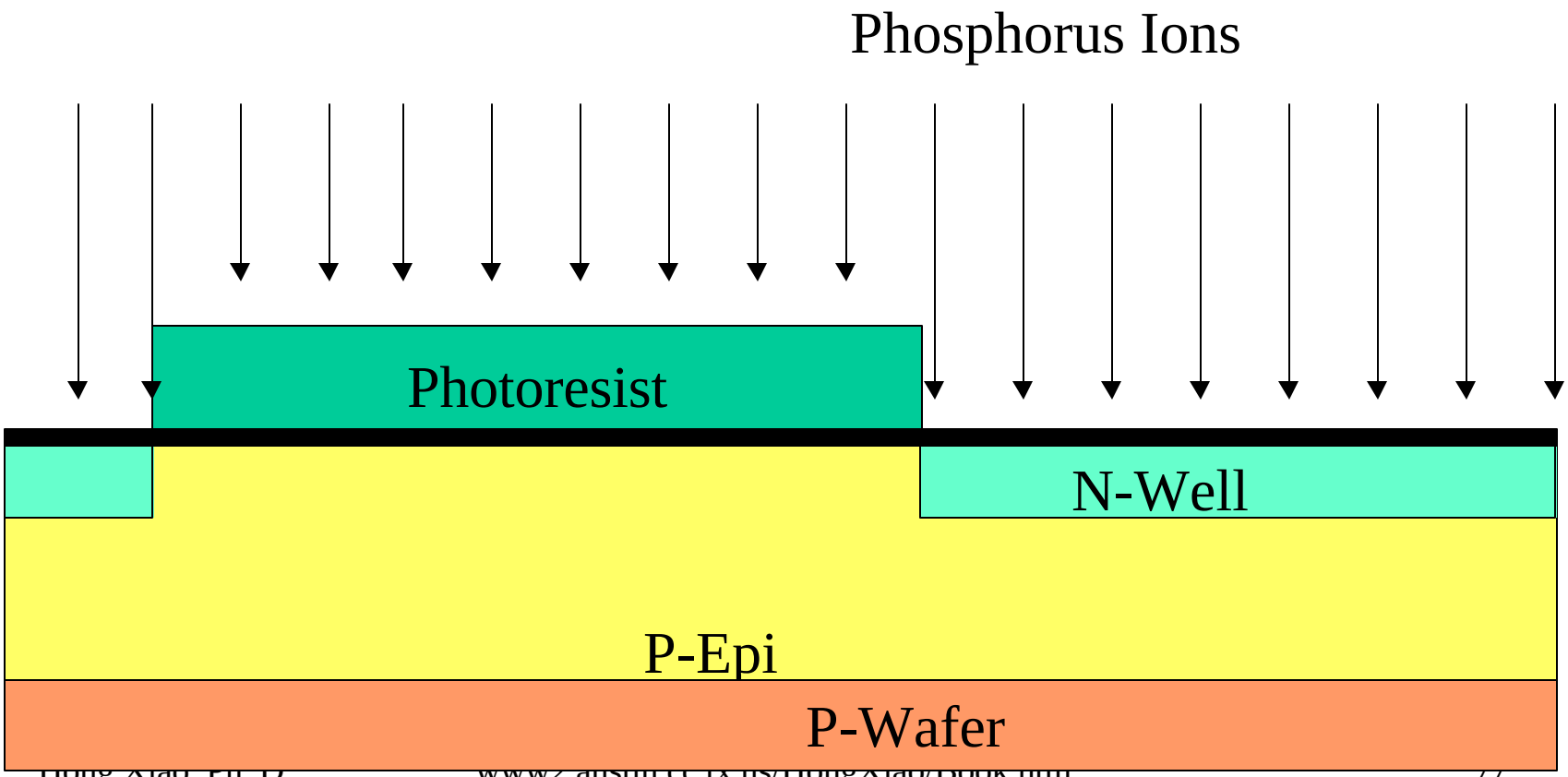
Epitaxy Deposition



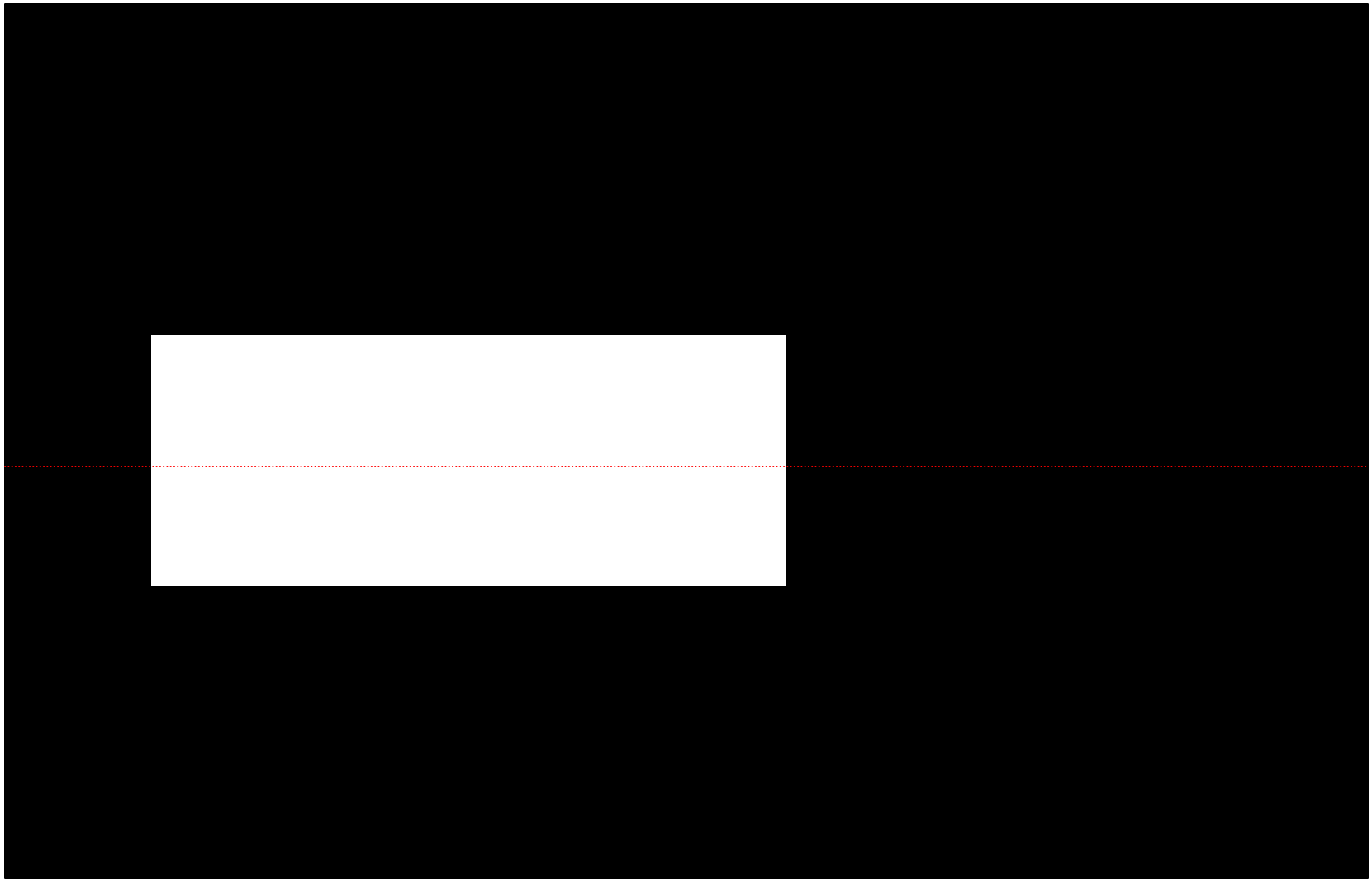
Mask 1: N-well



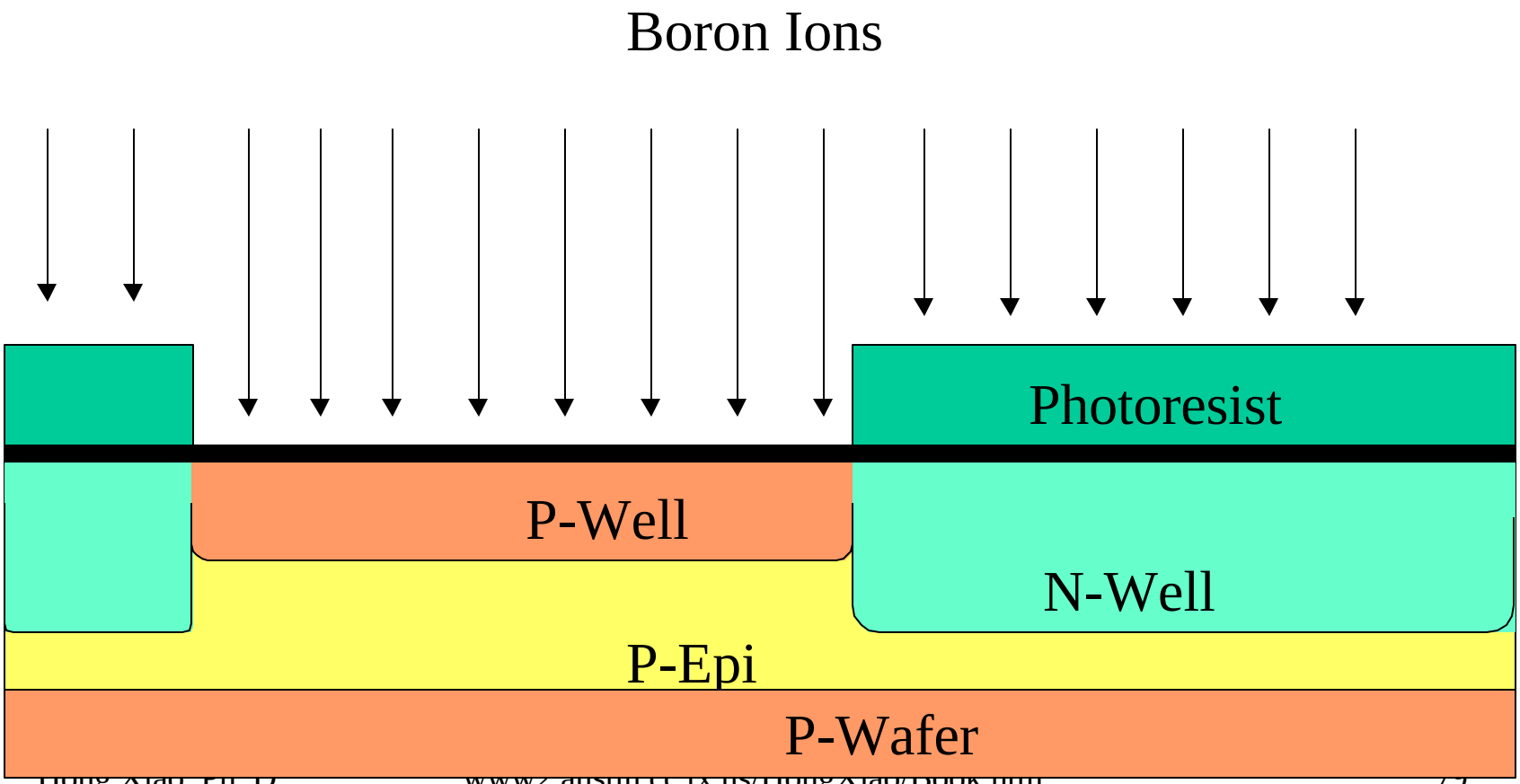
N-well Implantation



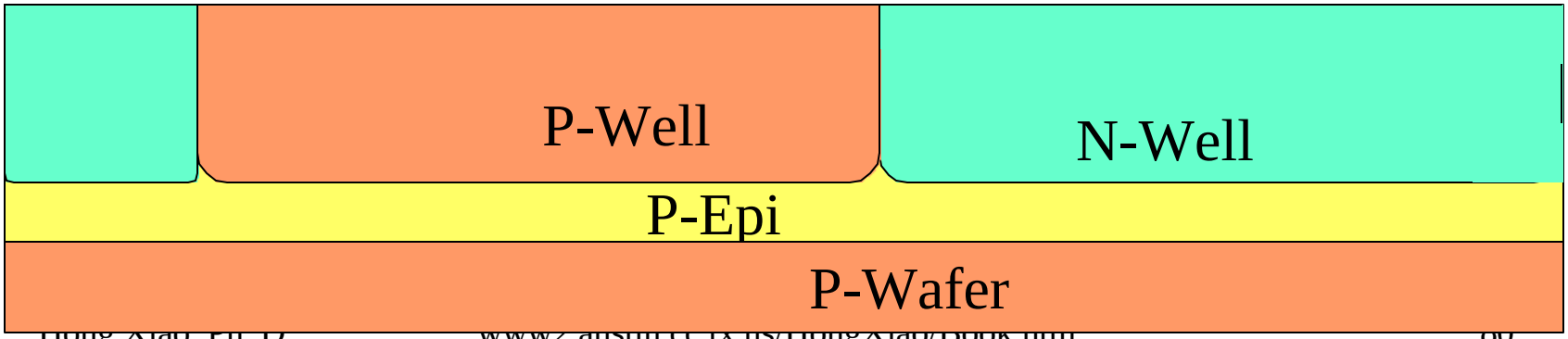
Mask 2: P-well



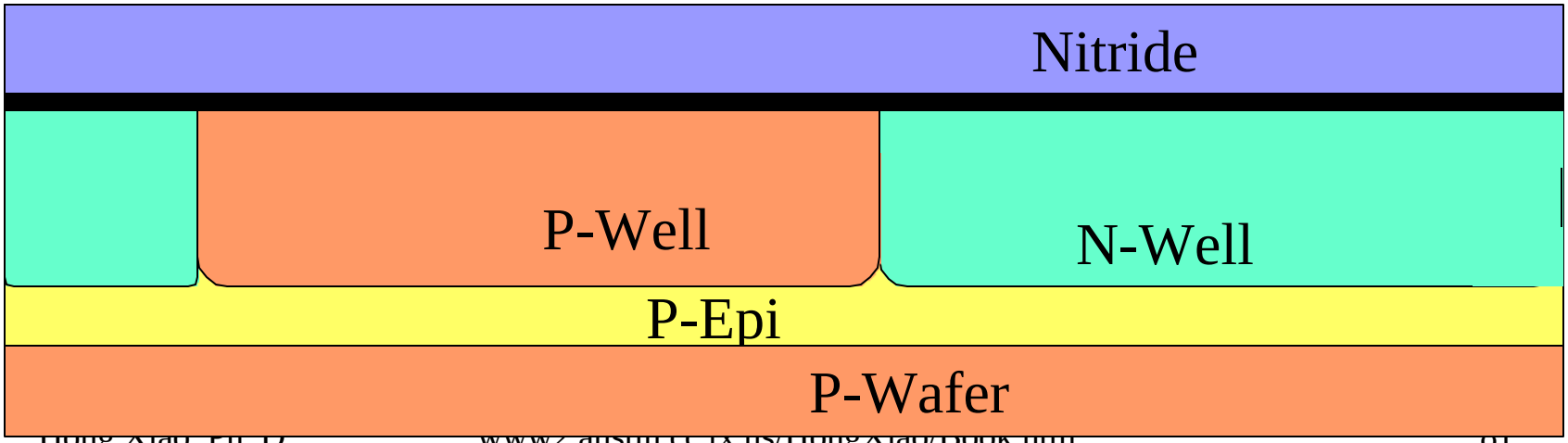
P-well Implantation



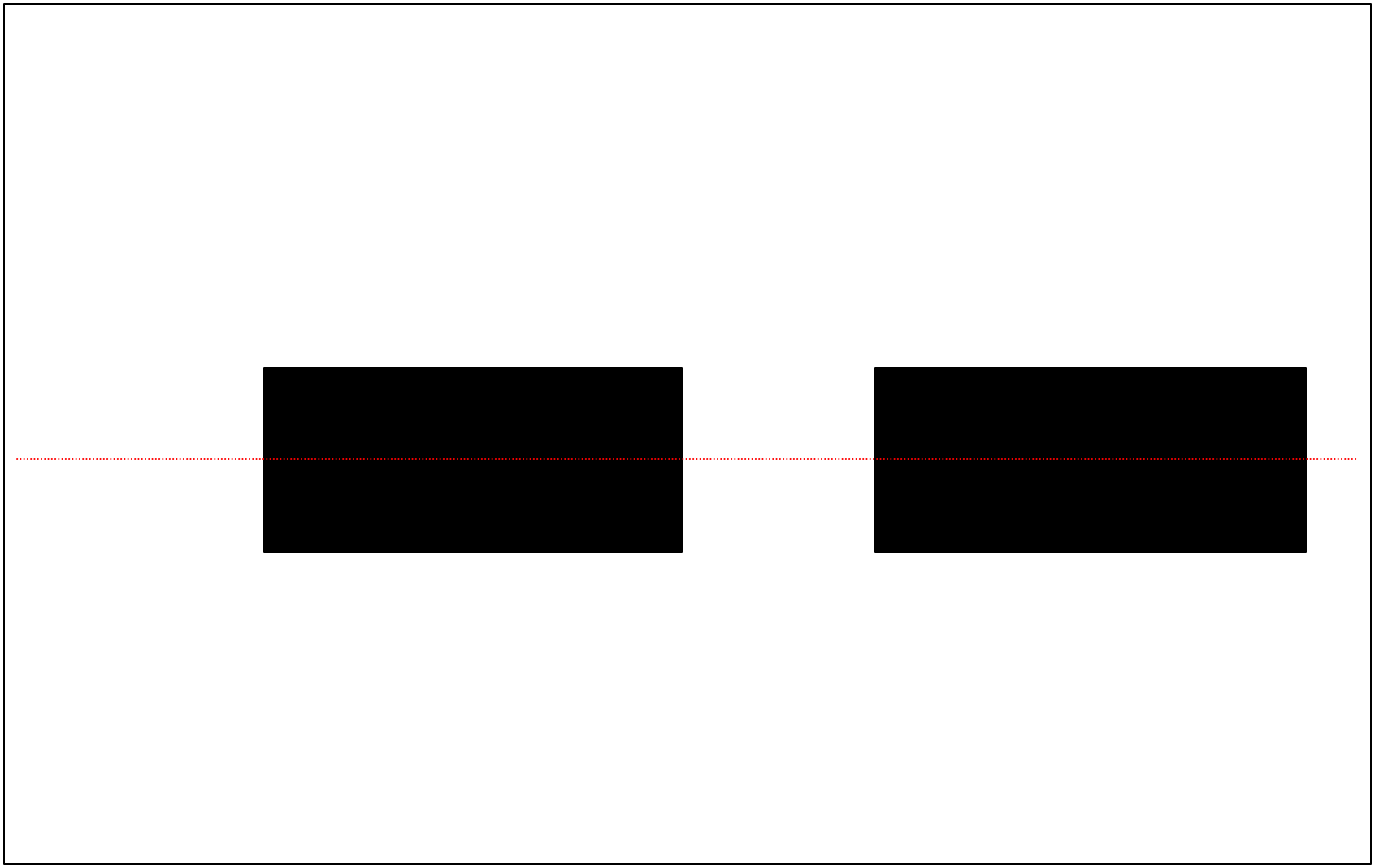
Strip PR, Strip Nitride/Pad Oxide



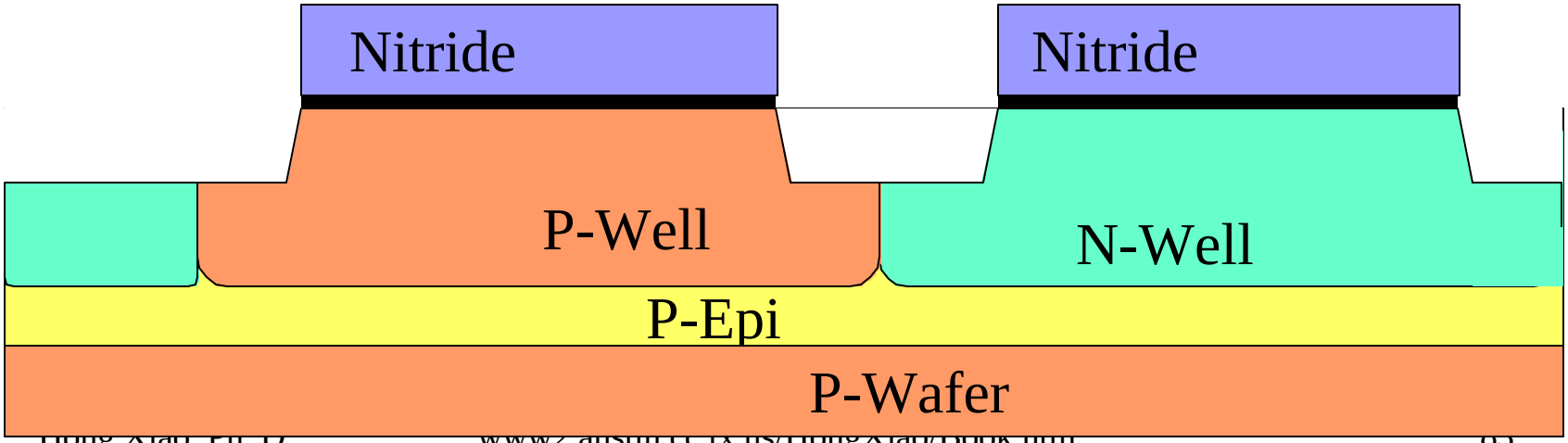
Pad Oxidation, LPCVD Nitride



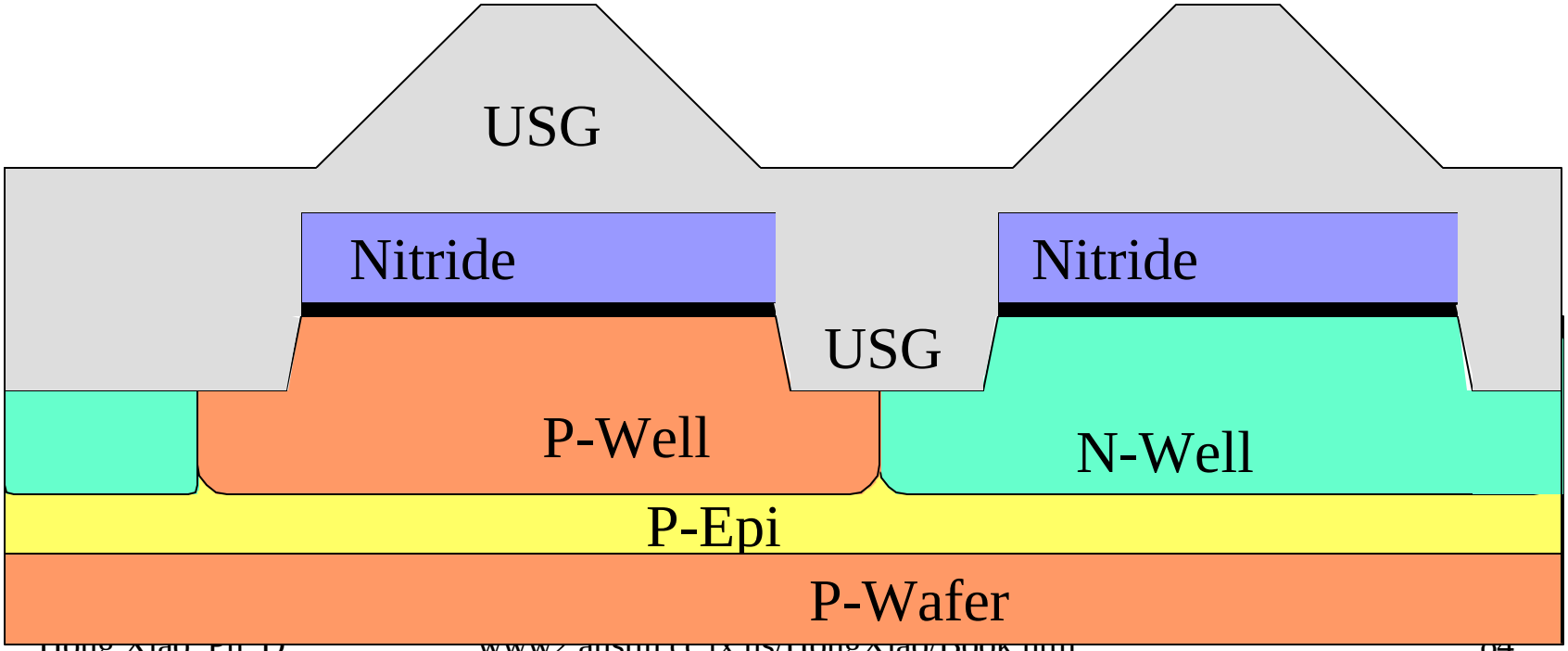
Mask 3: Shallow Trench Isolation



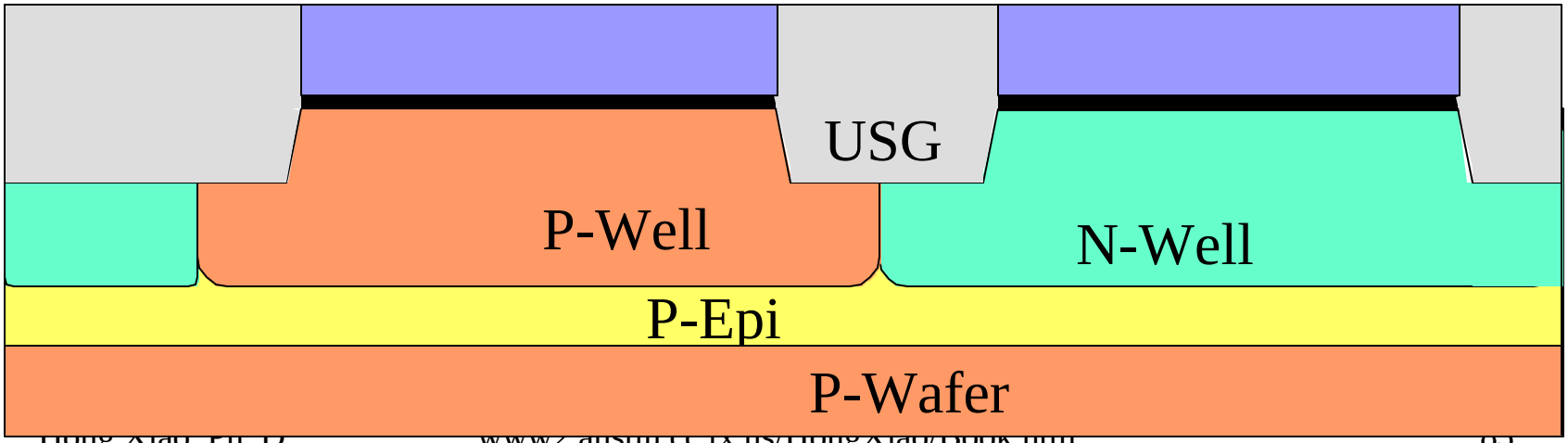
Etch Nitride, Pad Oxide and Silicon



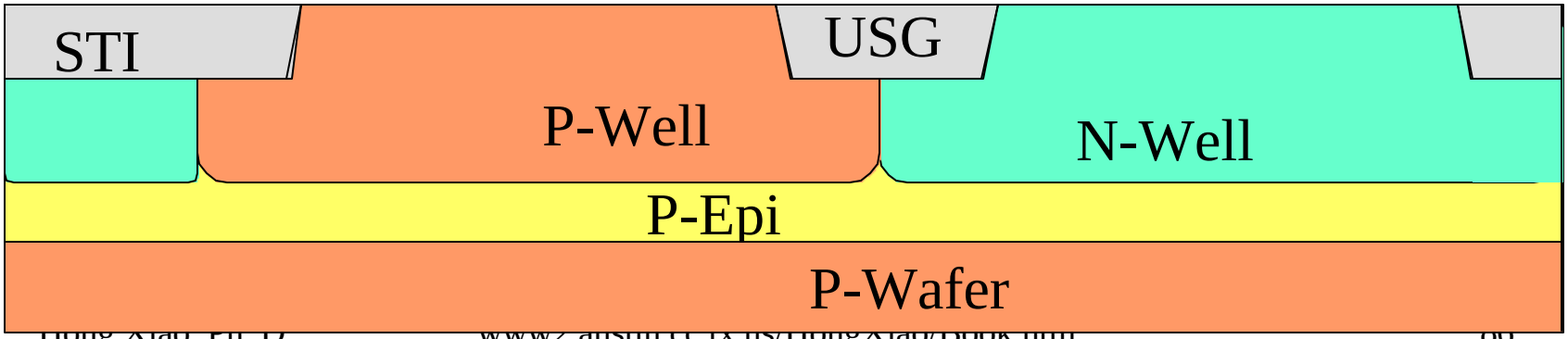
HDP-CVD USG Trench Fill



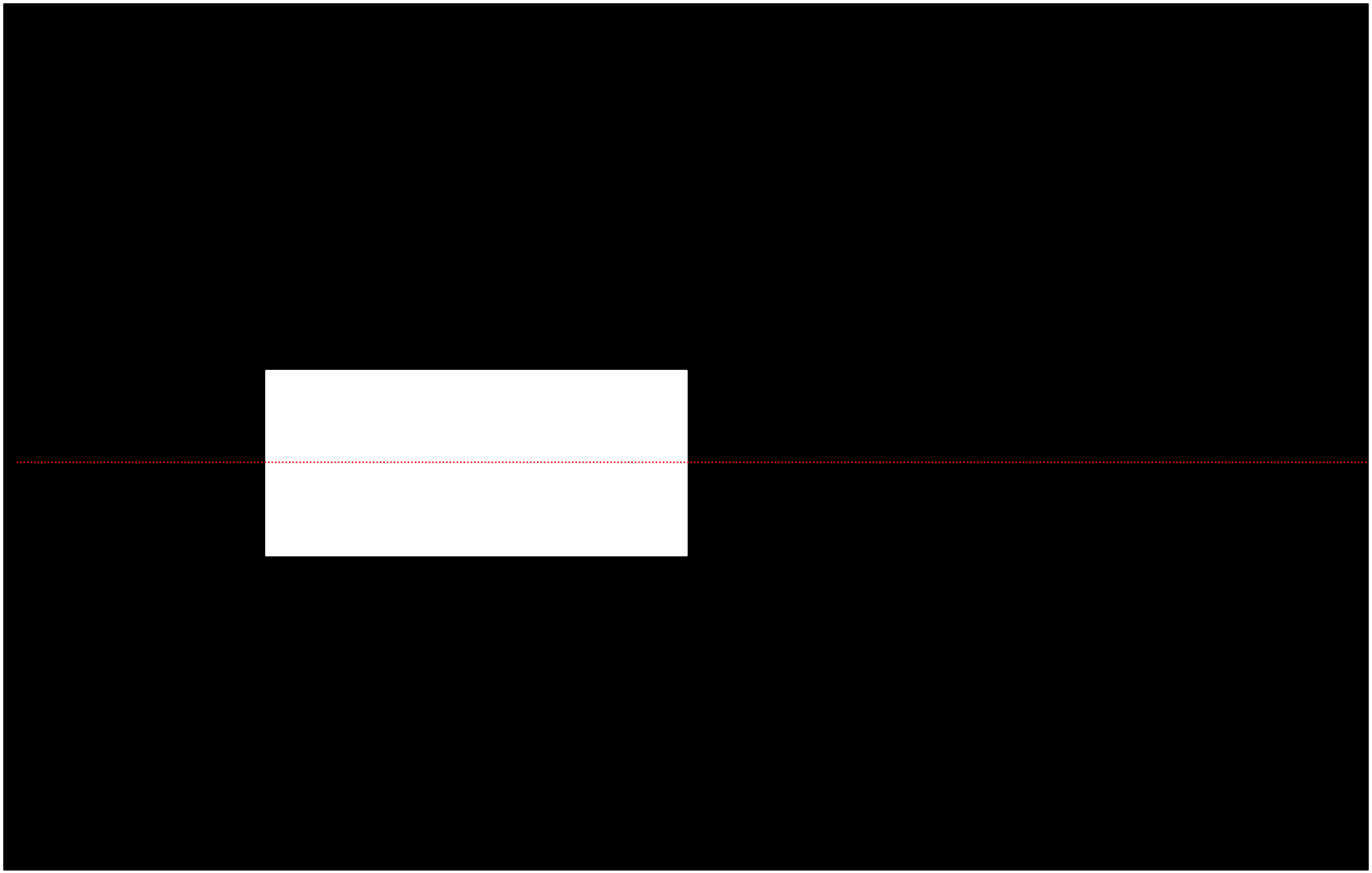
CMP USG, Stop on Nitride

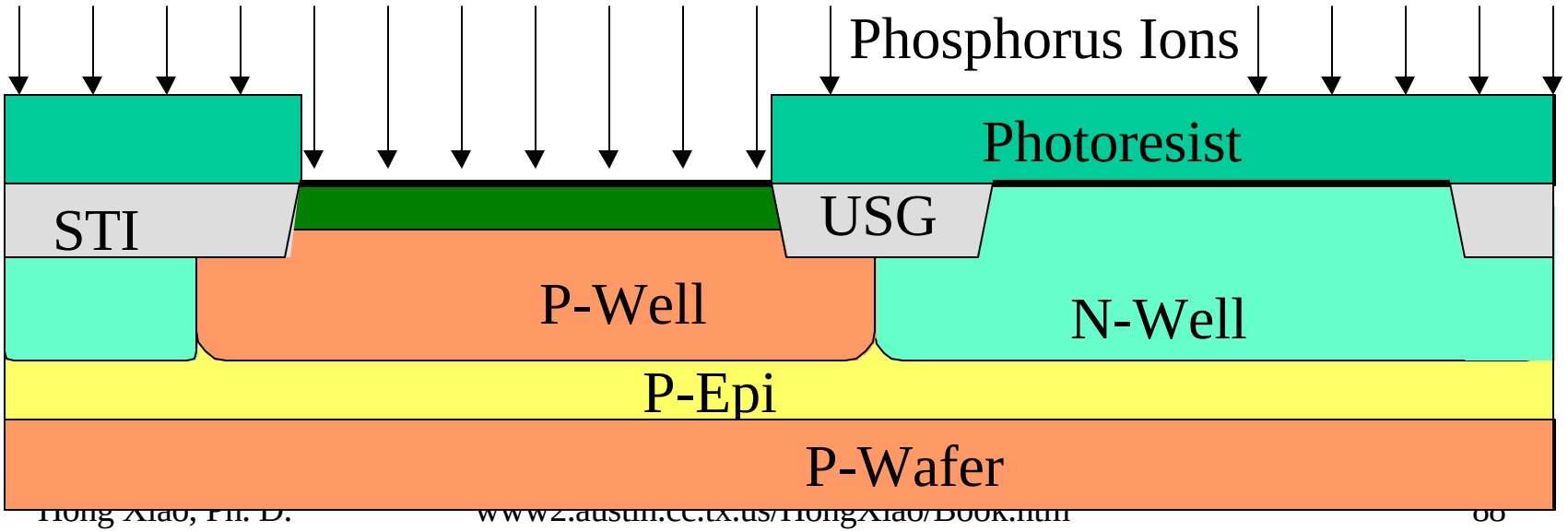


Strip Nitride and Pad Oxide, Clean

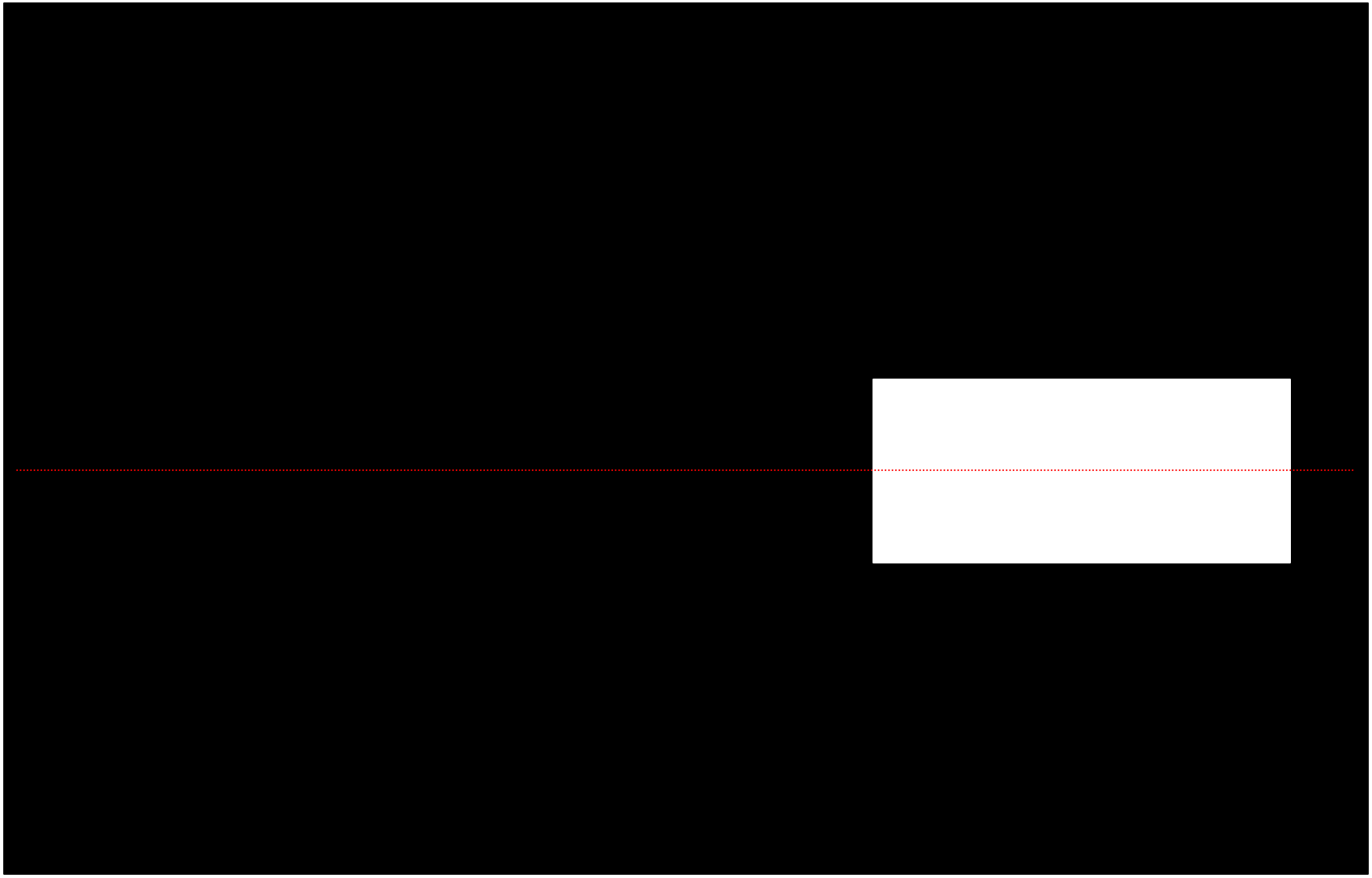


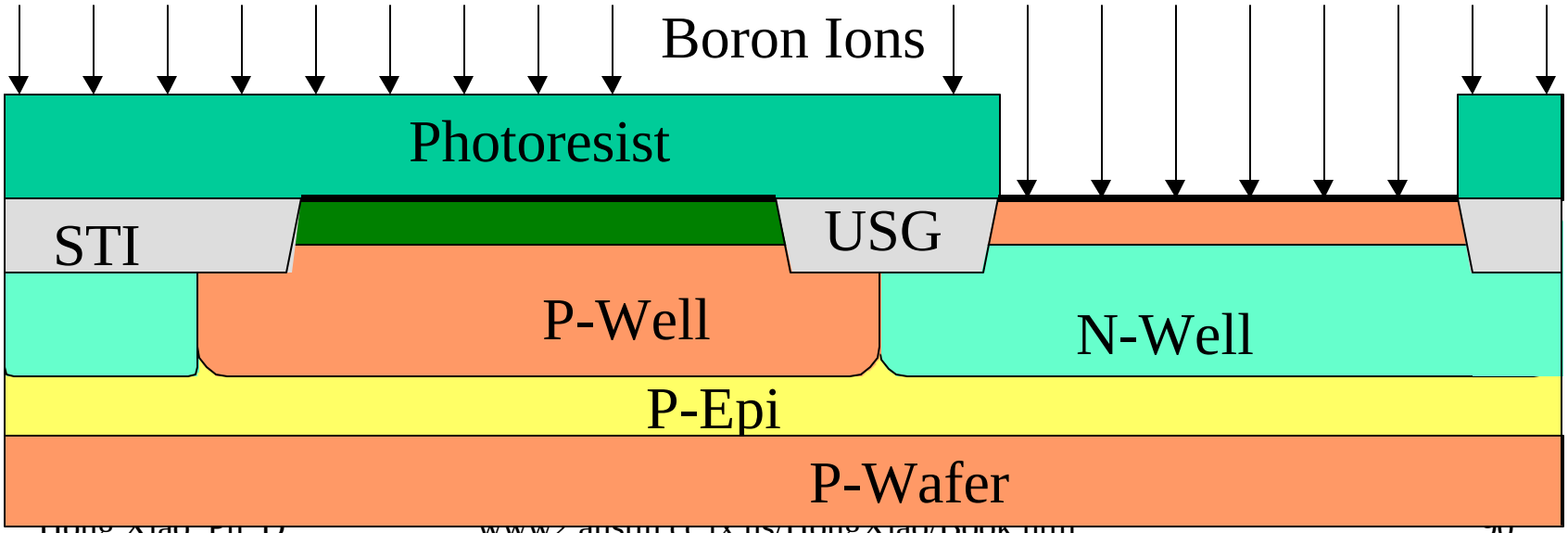
Mask 4: N-channel V_T Adjust



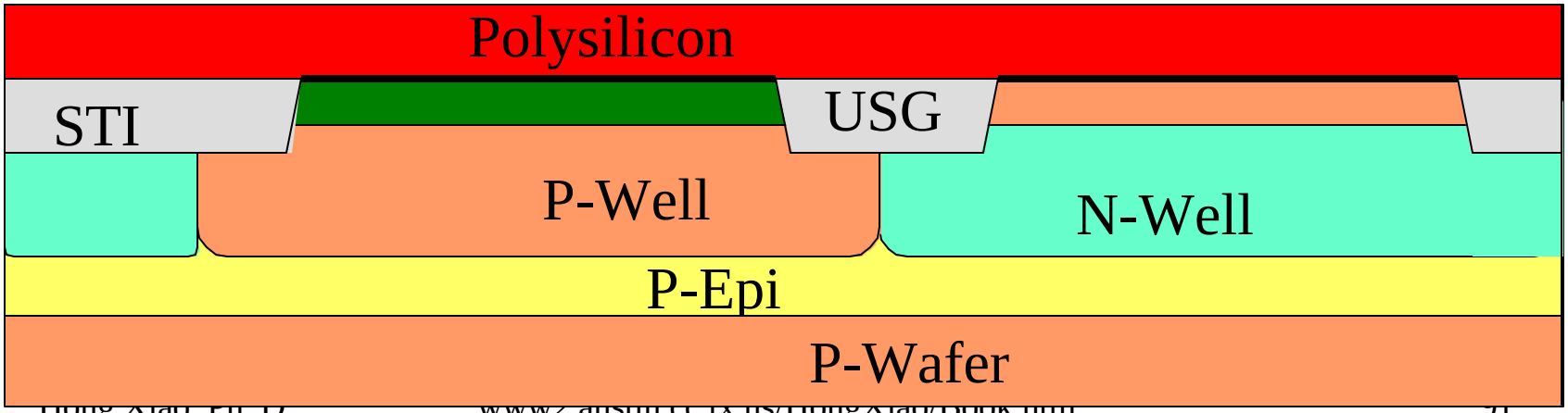

Phosphorus Ions
Photoresist
STI
USG
P-Well
N-Well
P-Epi
P-Wafer

Mask 5: P-channel V_T Adjust

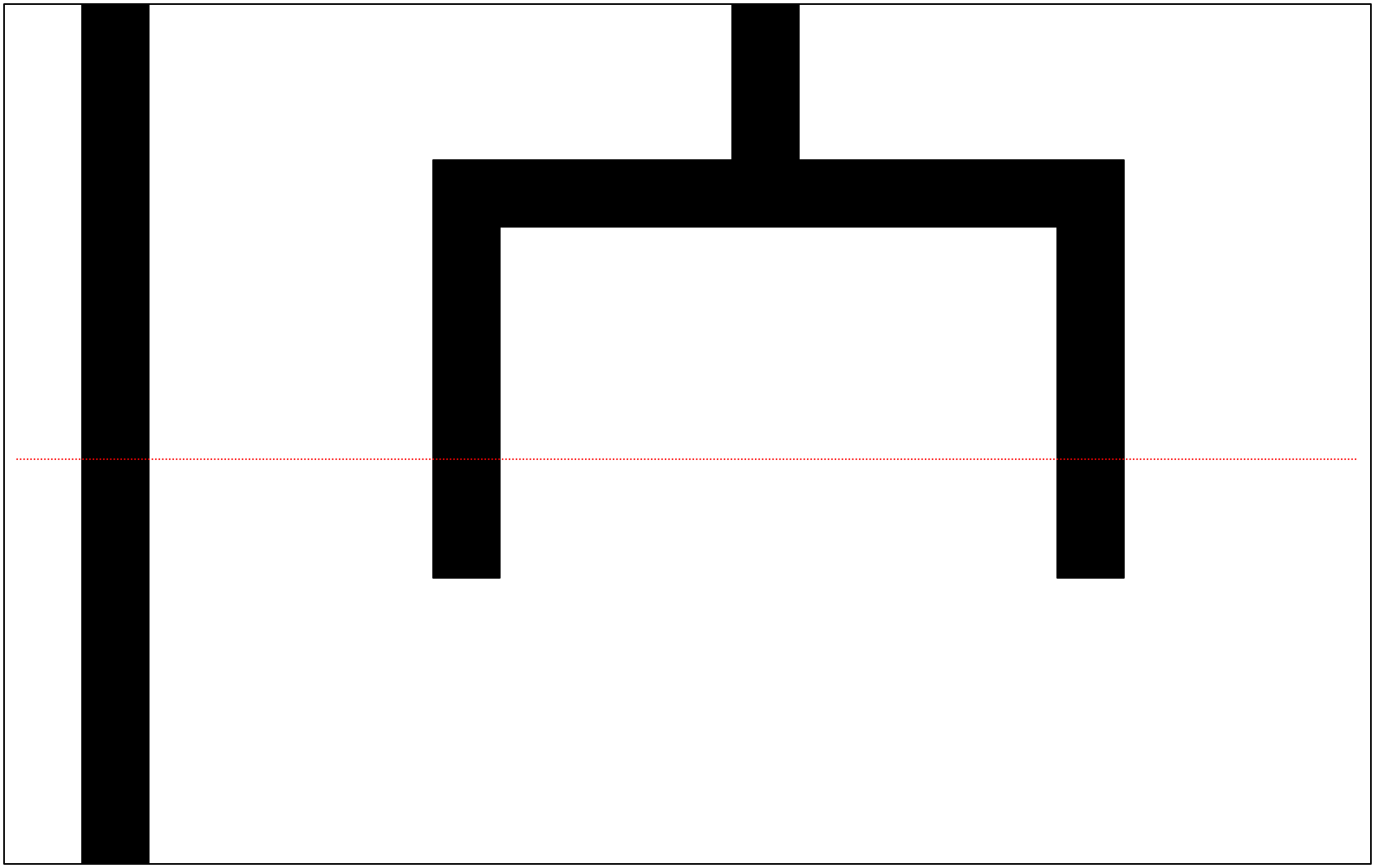



Boron Ions
Photoresist
STI
USG
P-Well
N-Well
P-Epi
P-Wafer

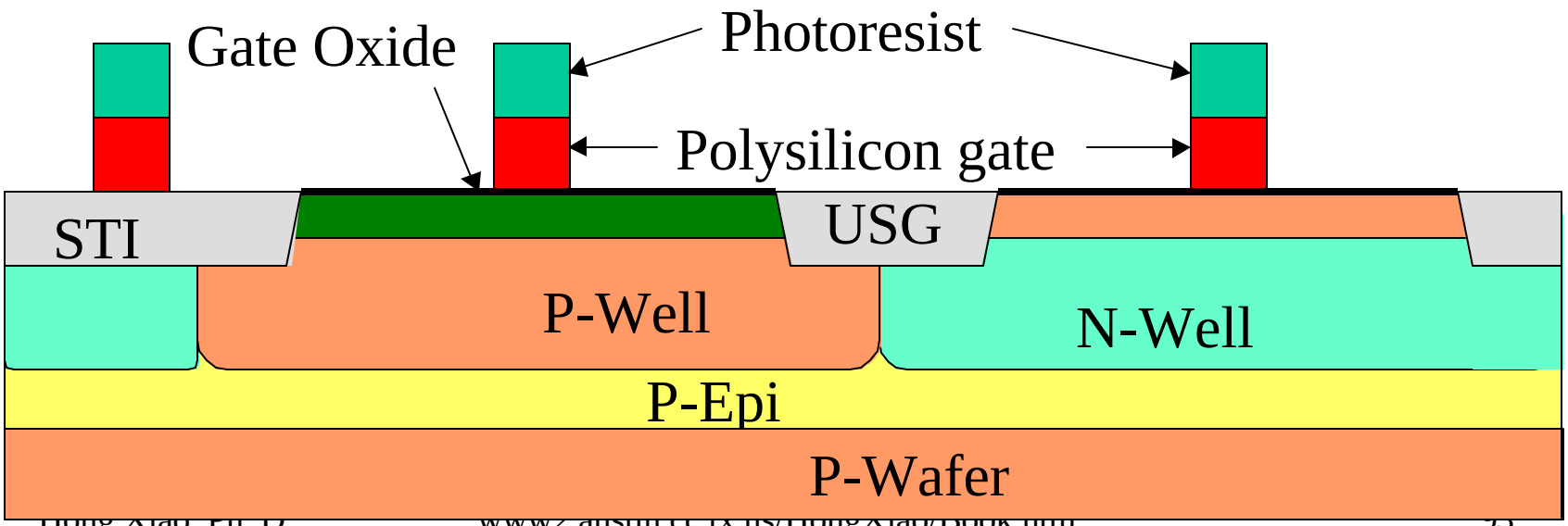
Gate Oxidation, LPCVD Polysilicon



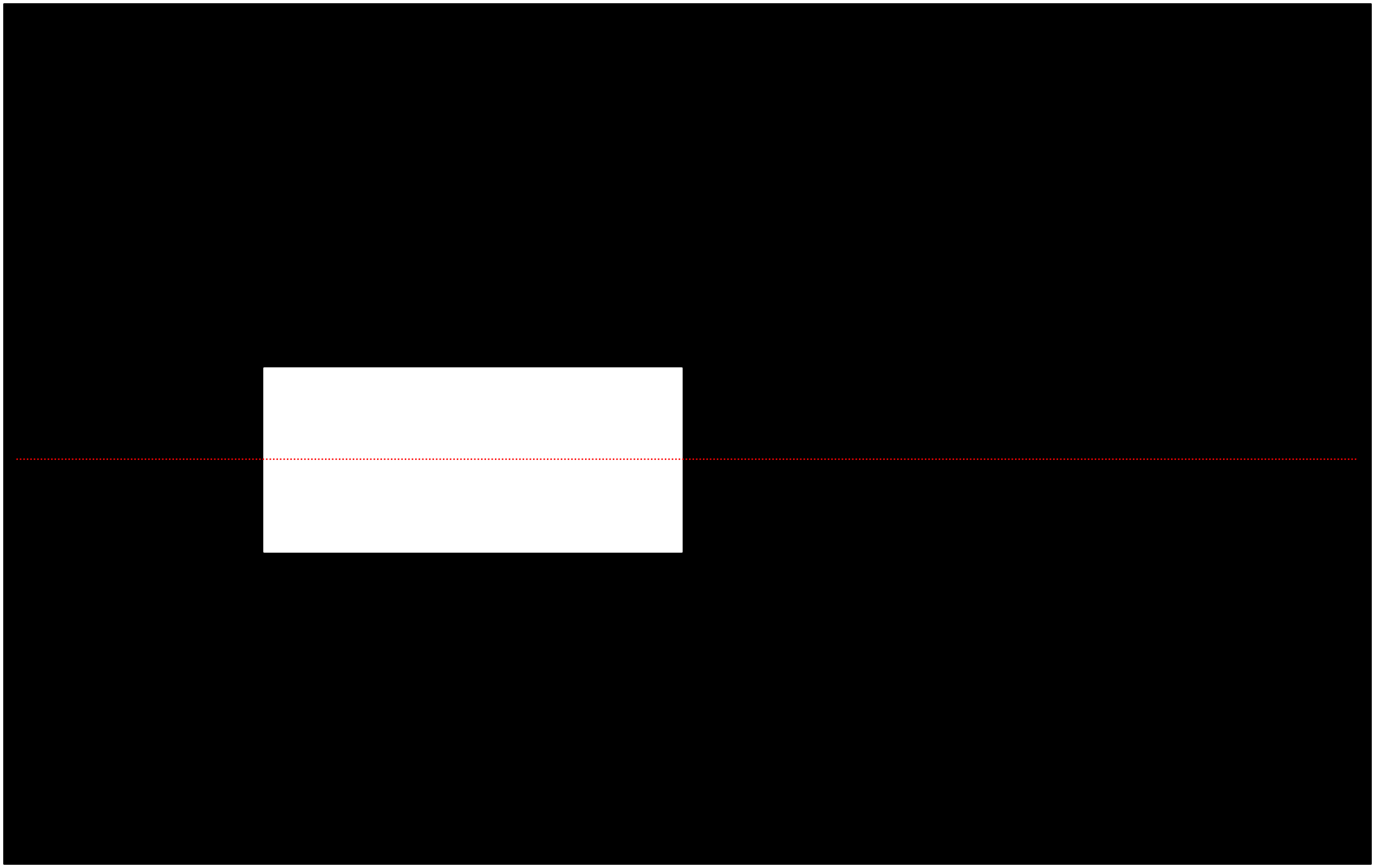
Mask 6: Gate & Local Interconnection



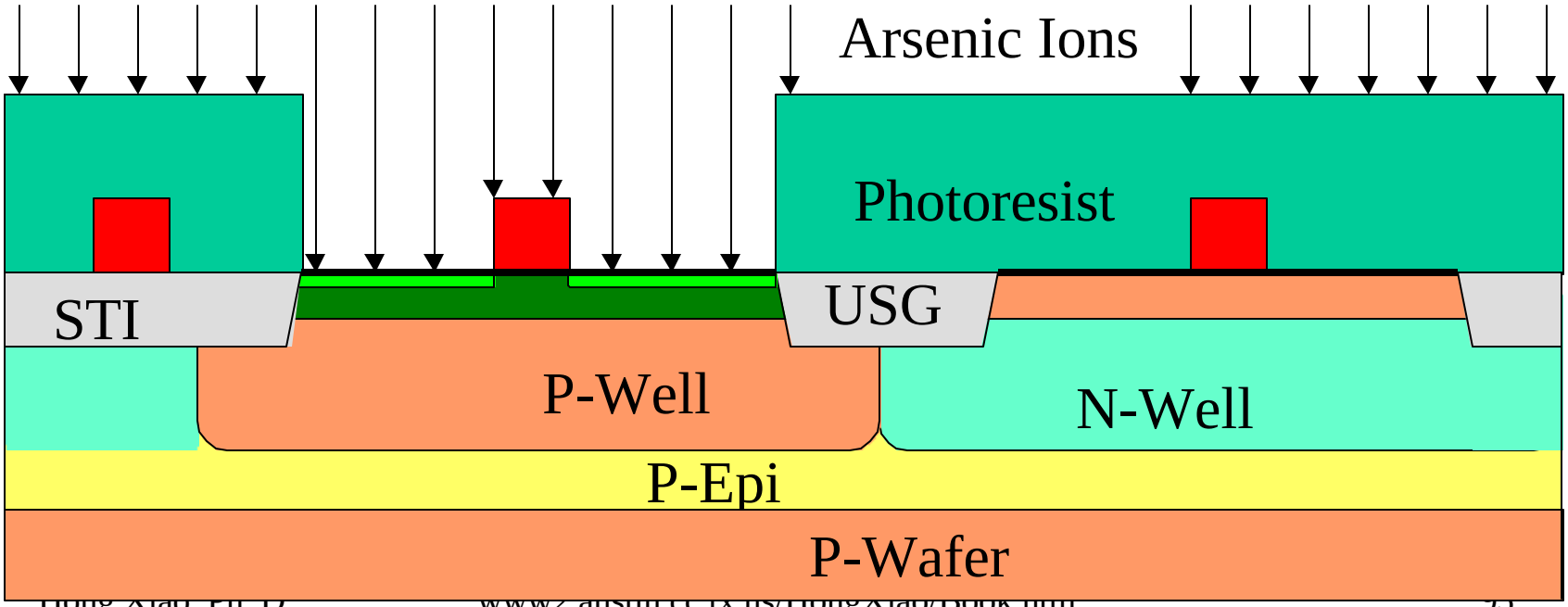
Etch Polysilicon



Mask 7: N-channel LDD

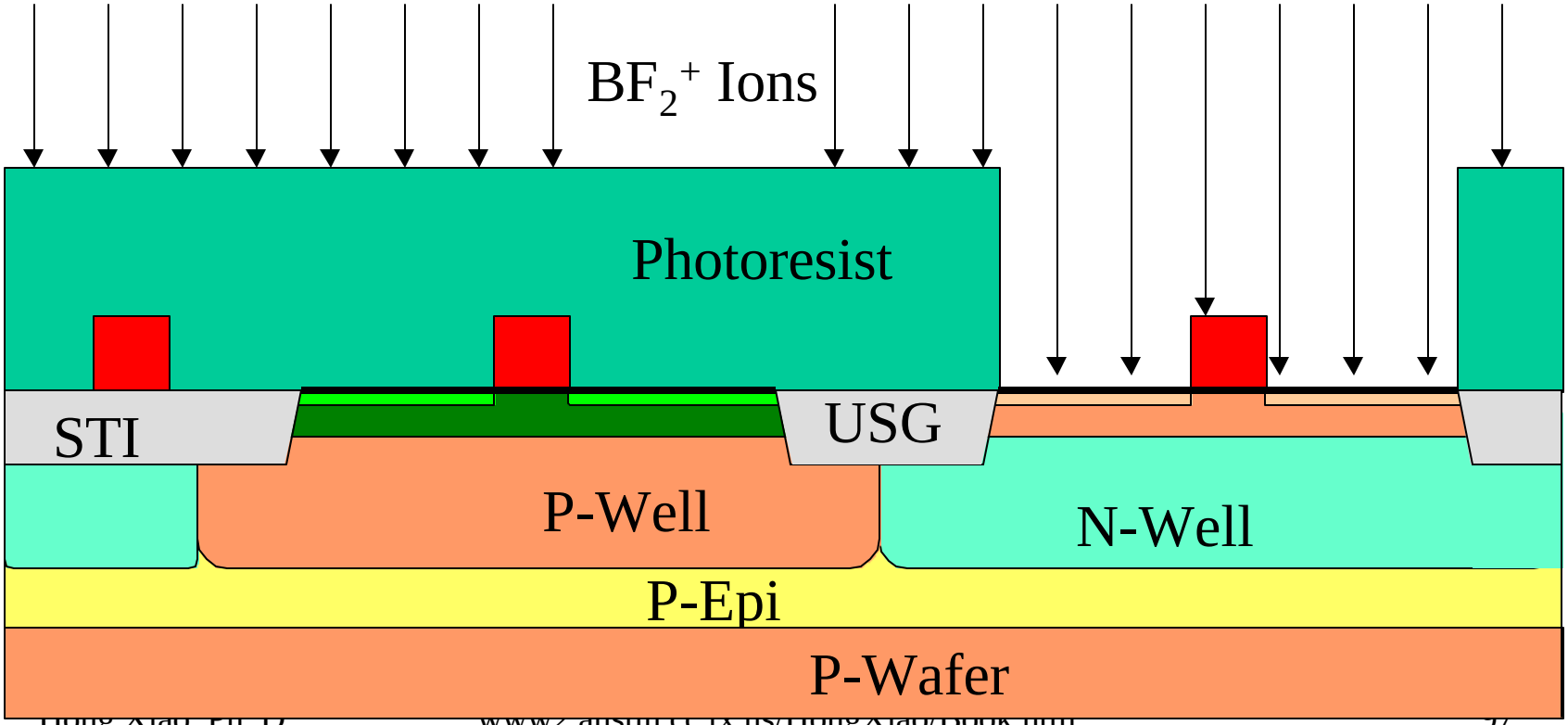


N-channel LDD Implantation, Arsenic

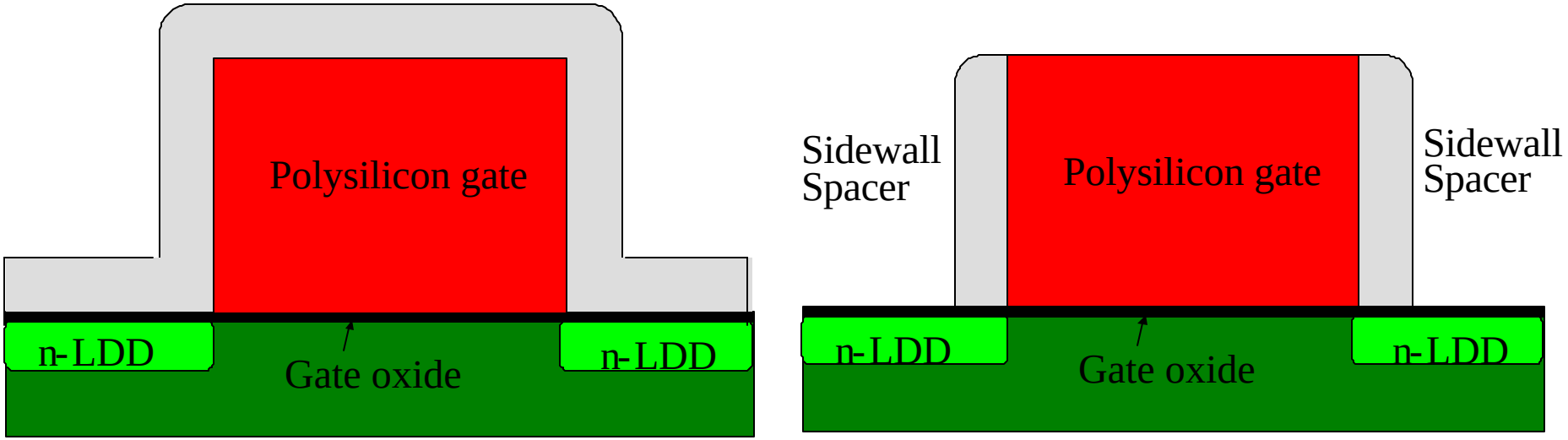


Mask 8: P-channel LDD

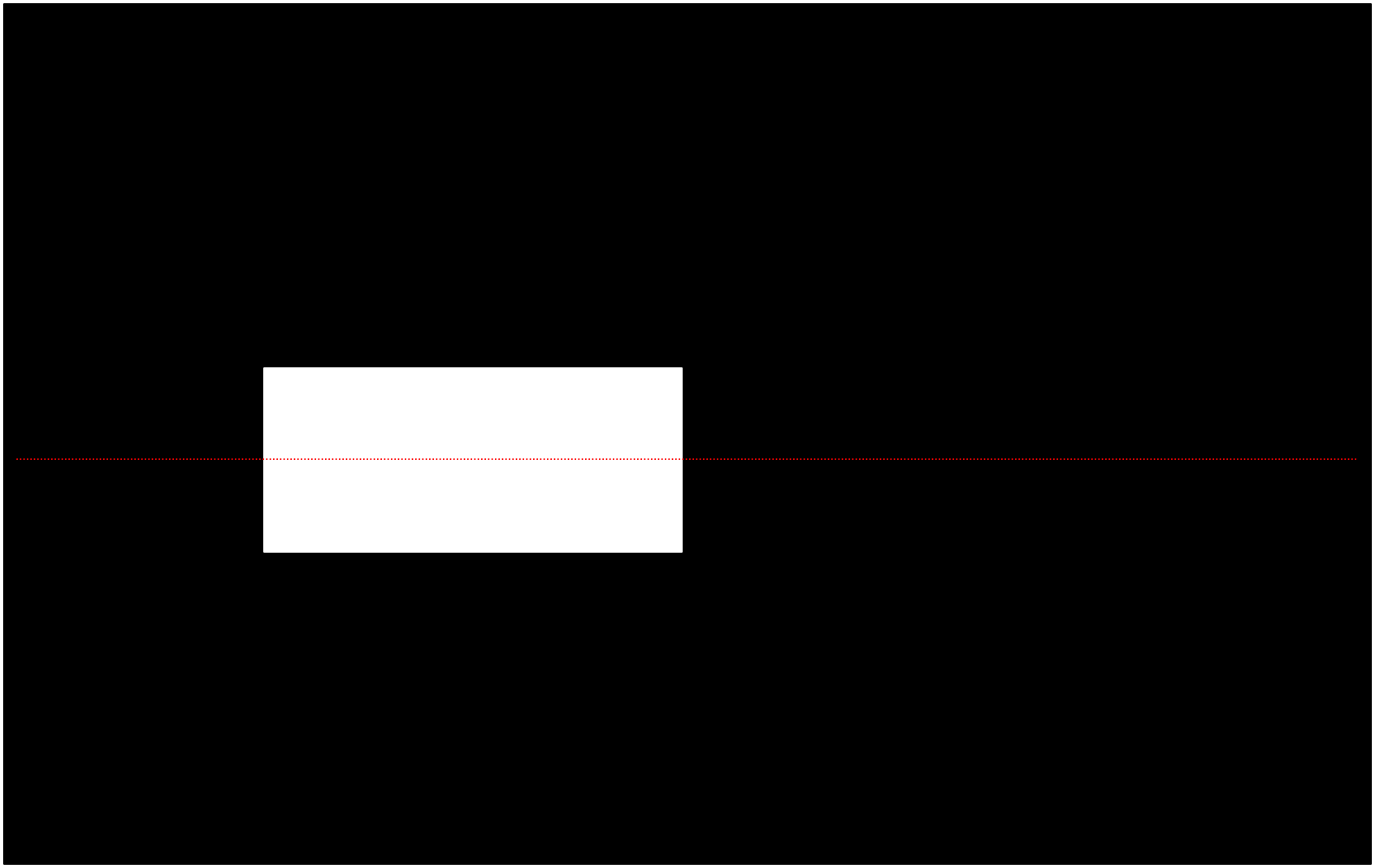
P-channel LDD Implantation, BF_2^+



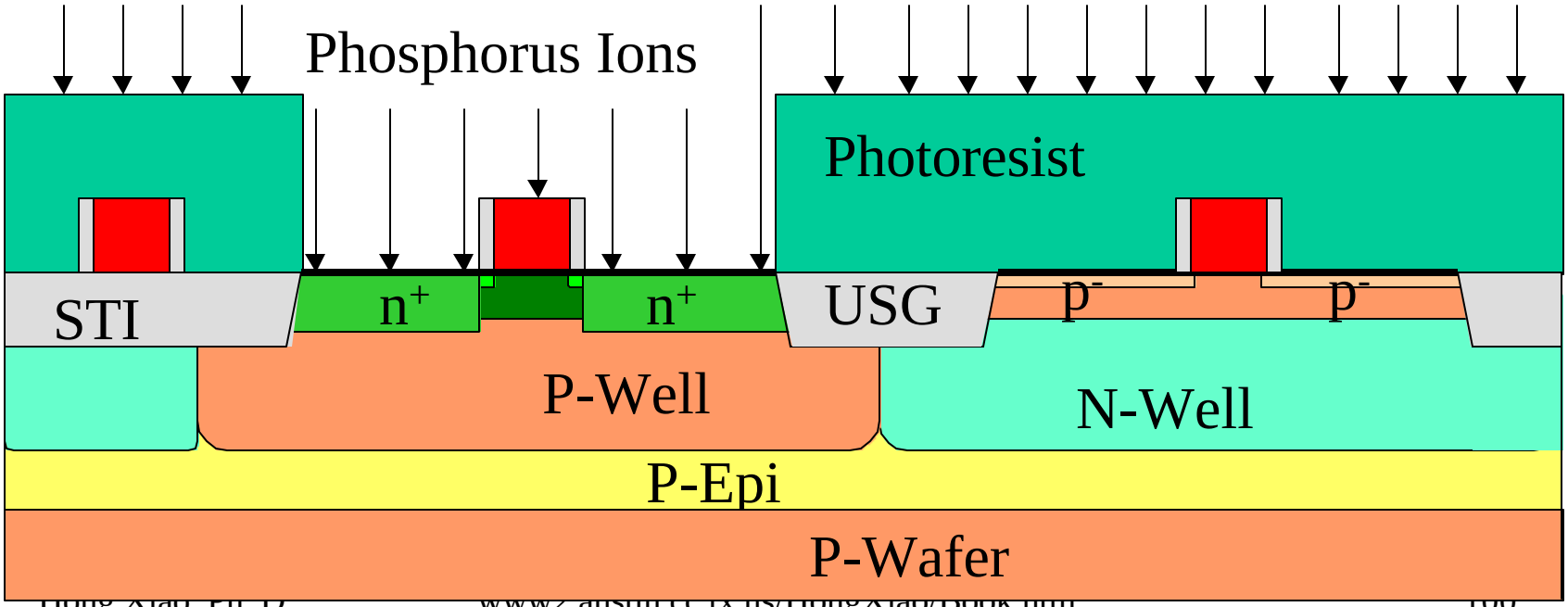
Sidewall Spacer



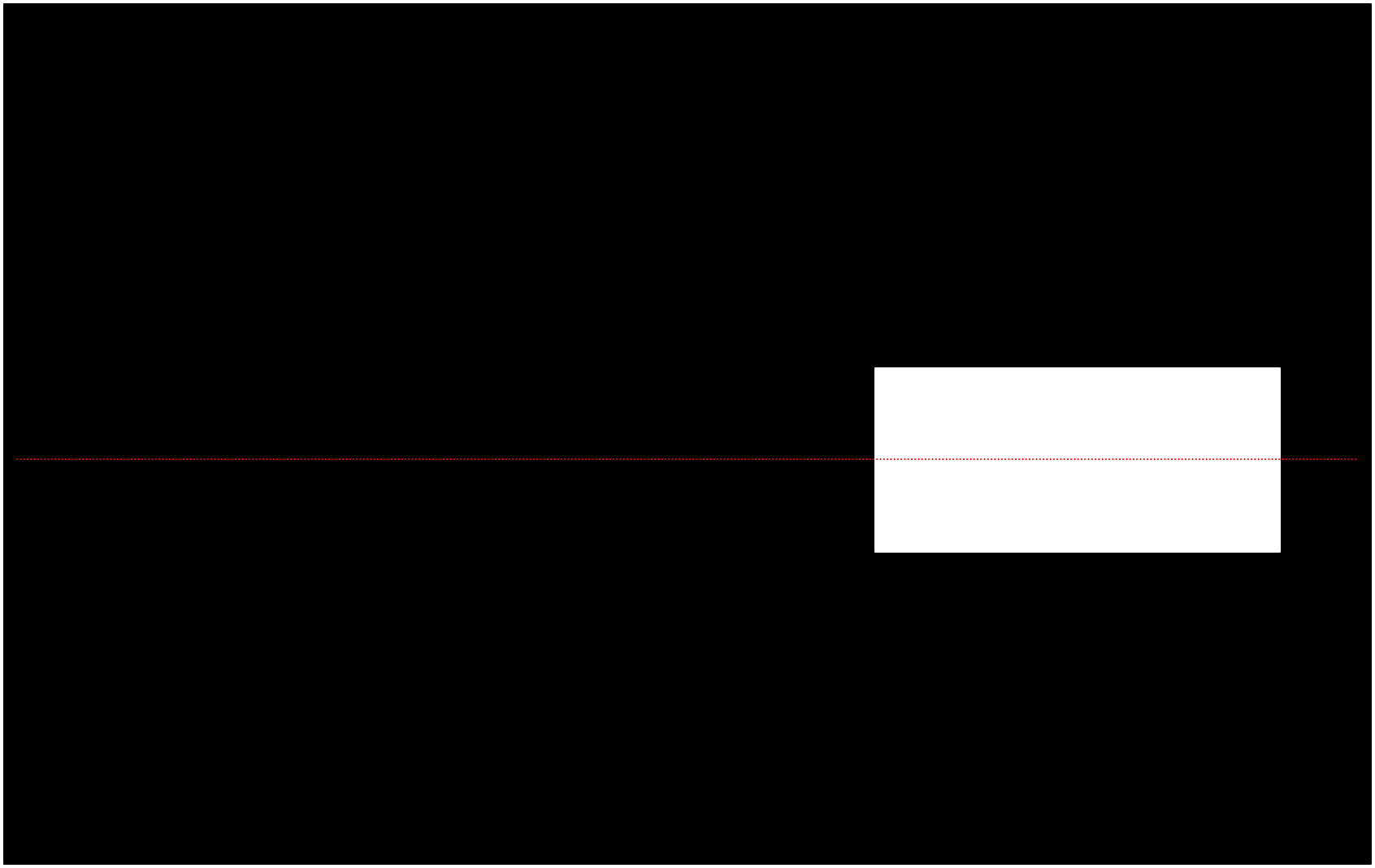
Mask 9: N-channel Source/Drain



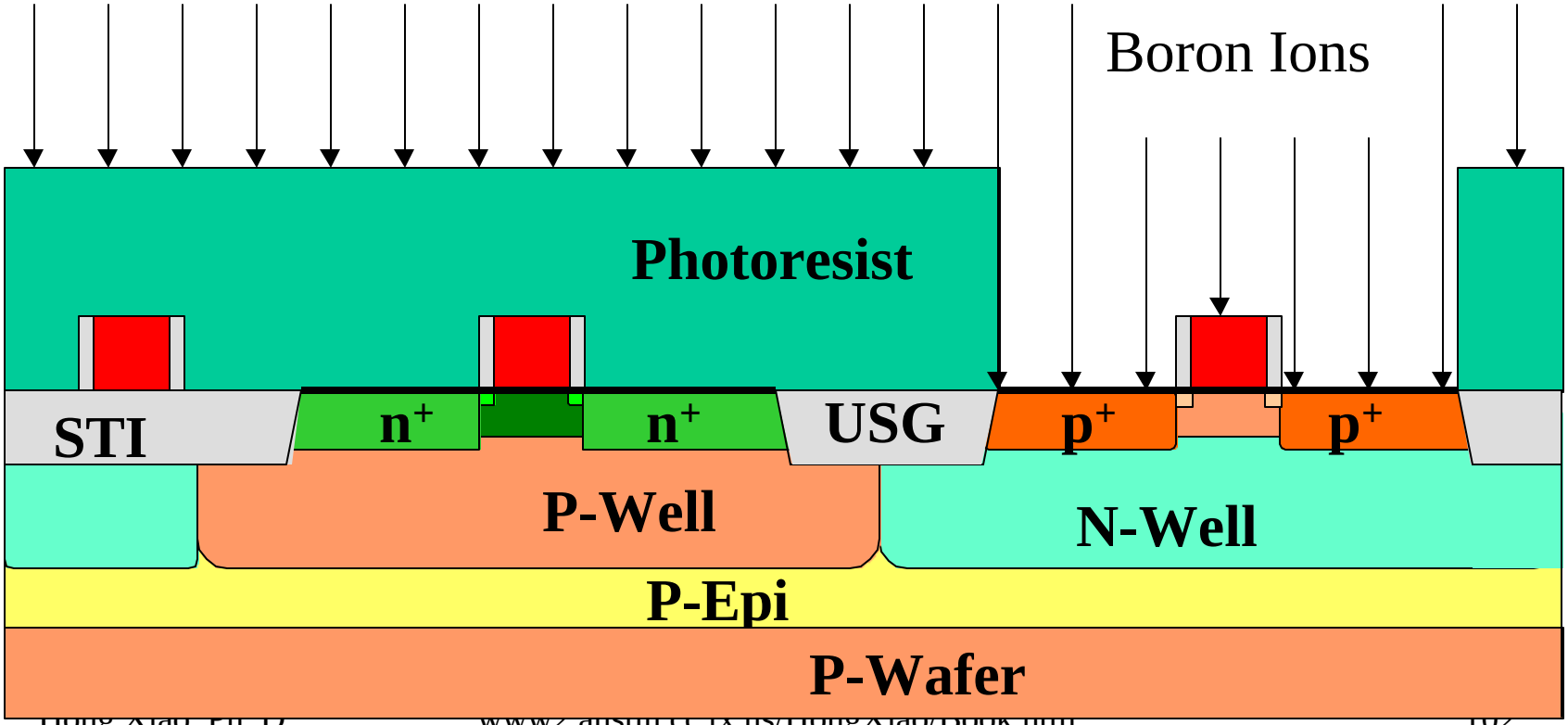
N-channel Source/Drain Implantation



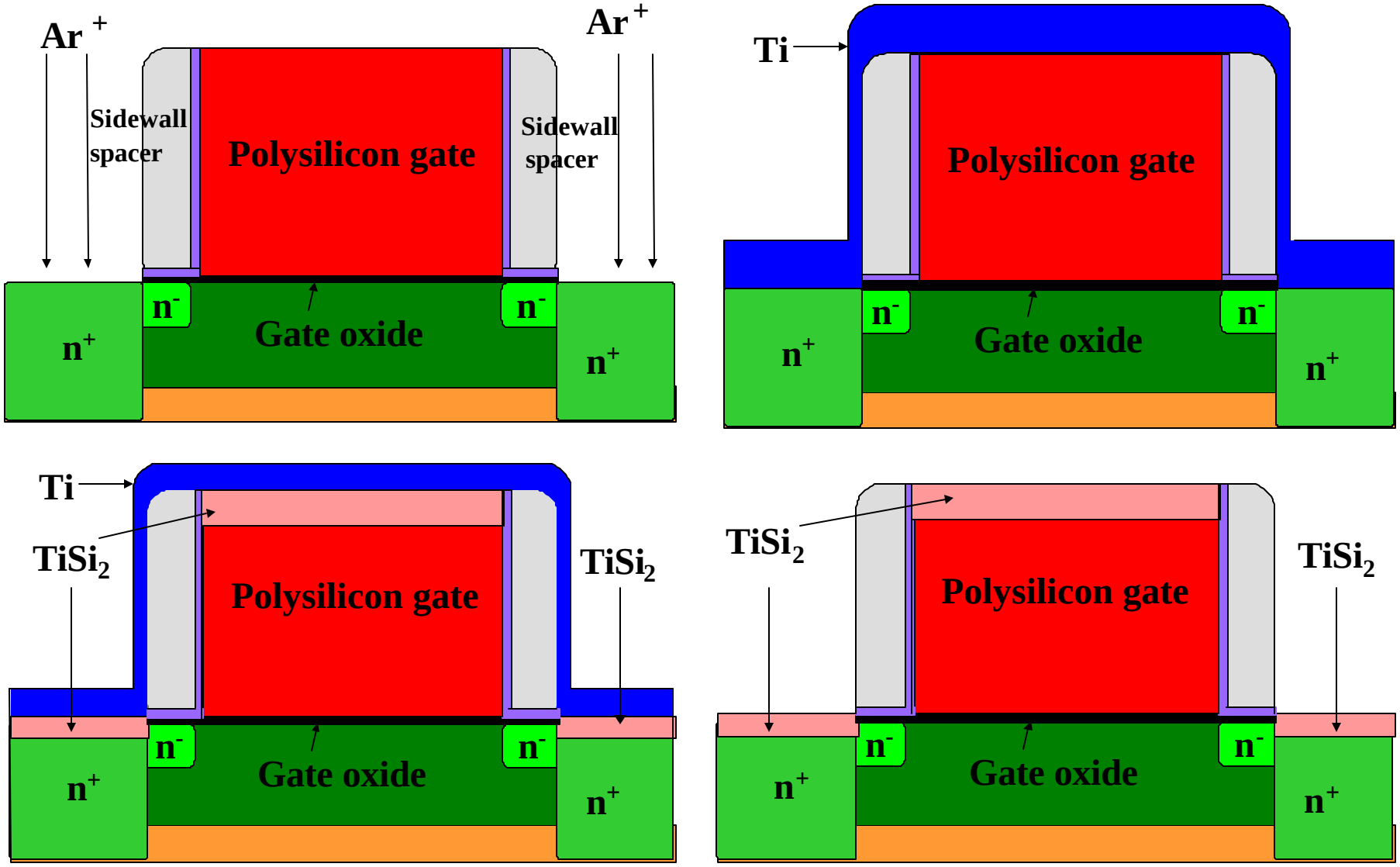
Mask 9: P-channel Source/Drain



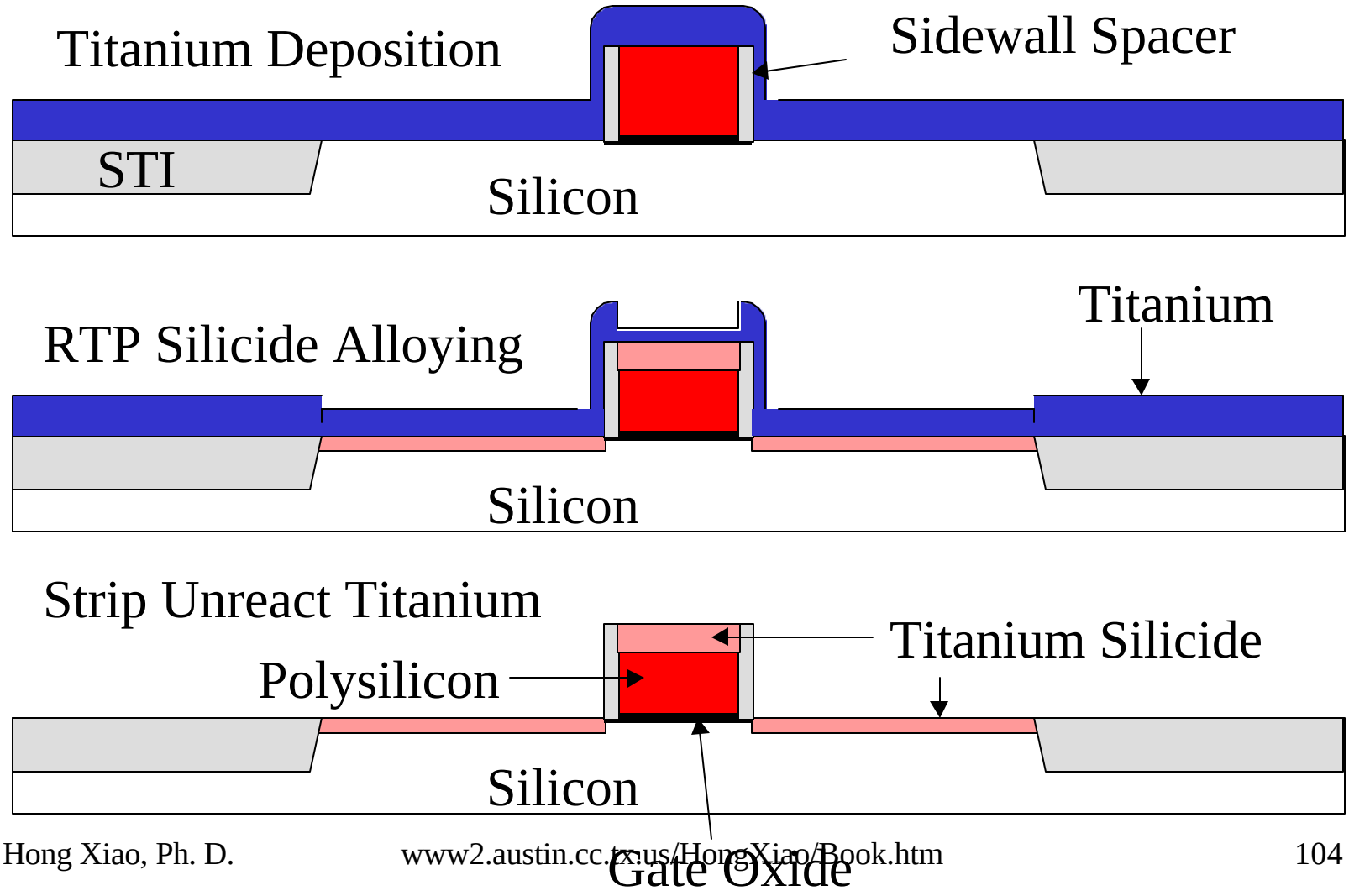
P-channel Source/Drain Implantation



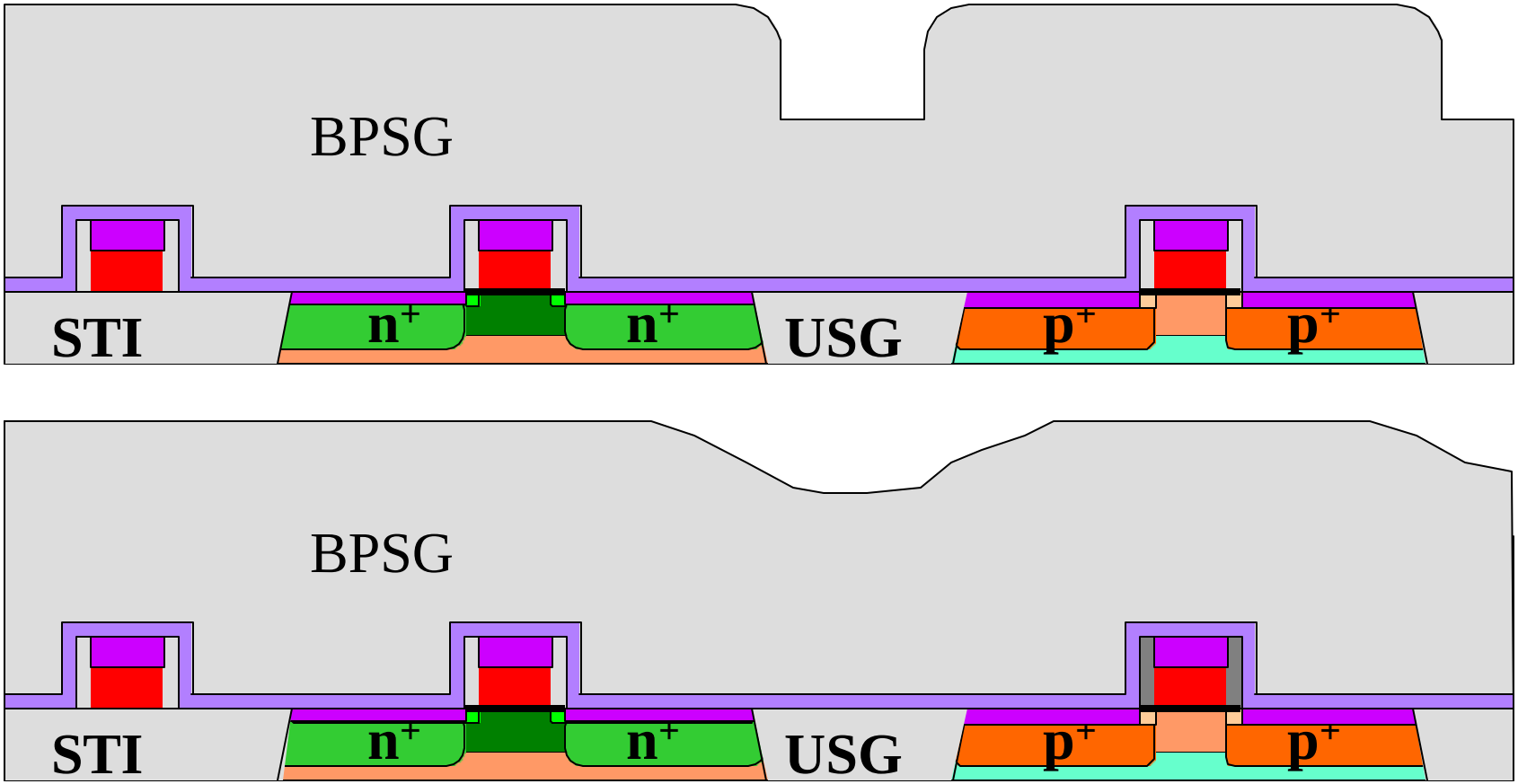
Titanium Salicide Process



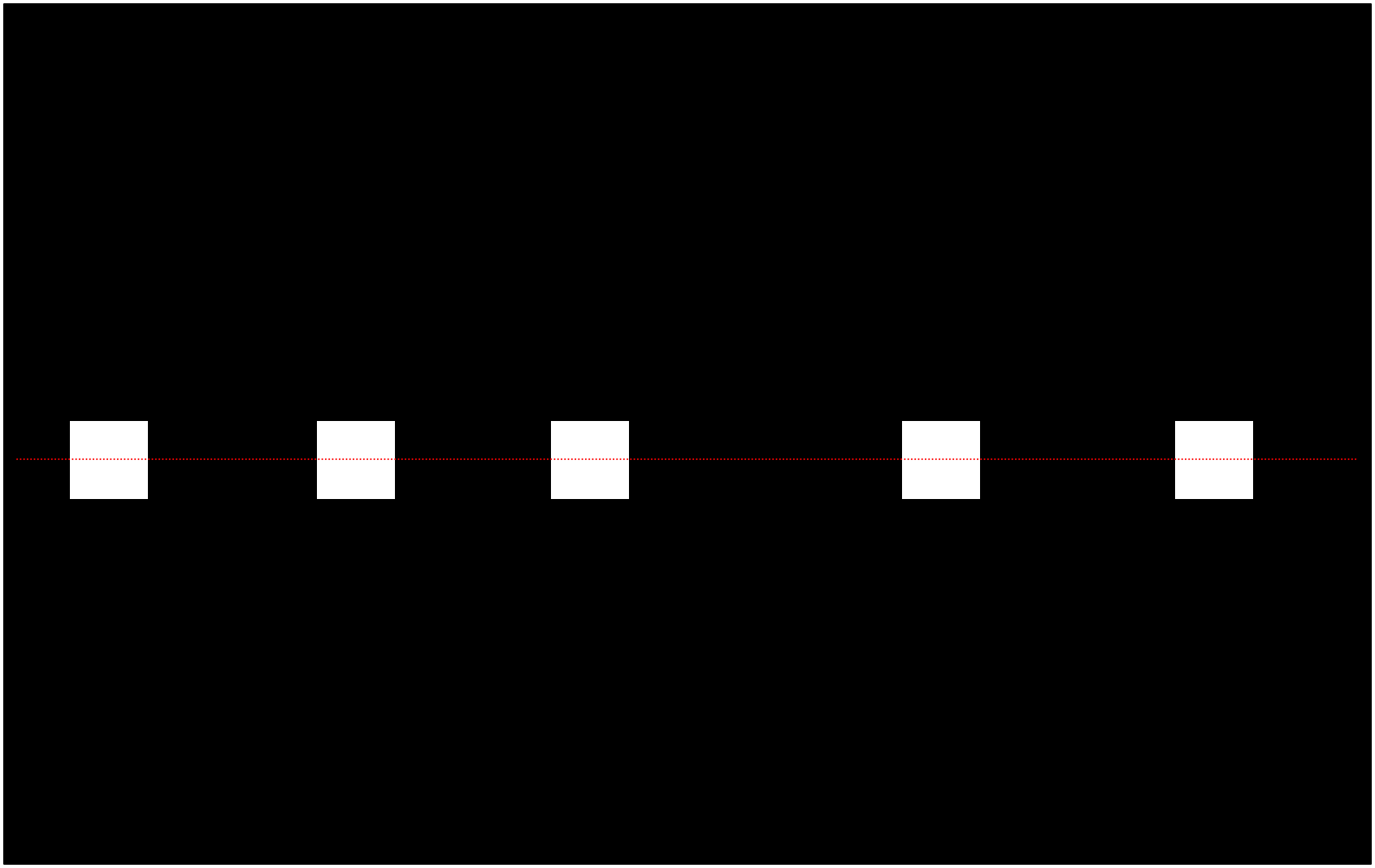
Titanium Self-aligned silicide Process



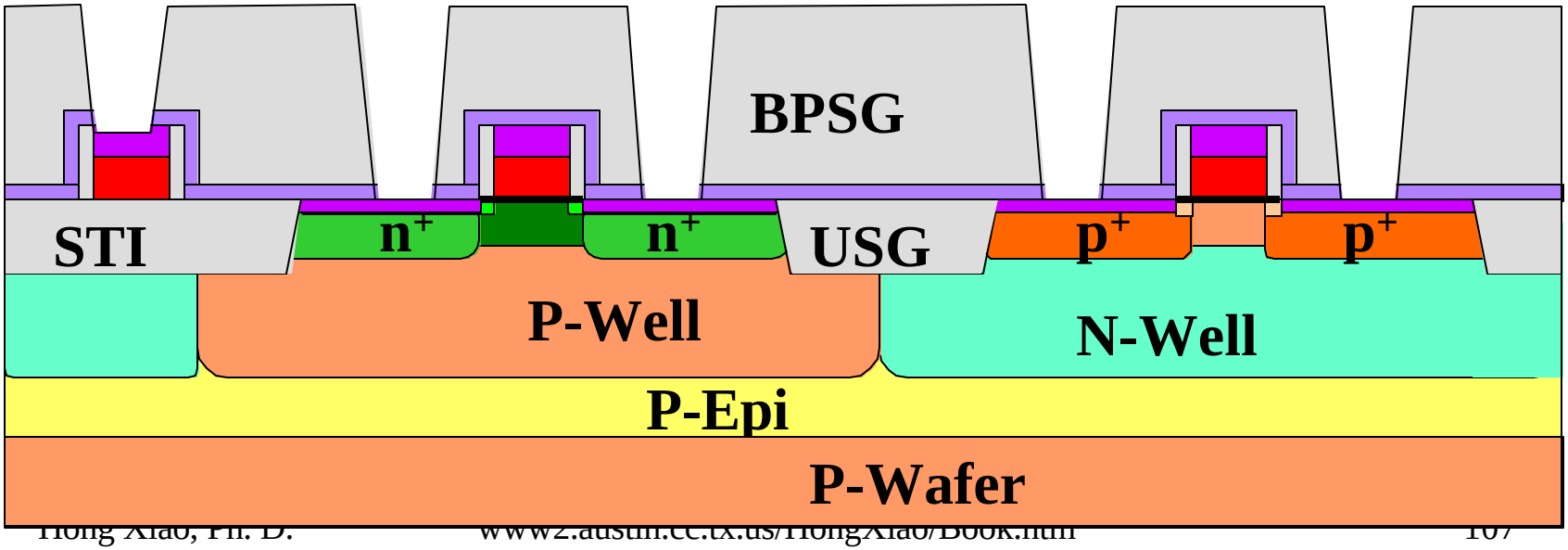
BPSG Deposition and Reflow



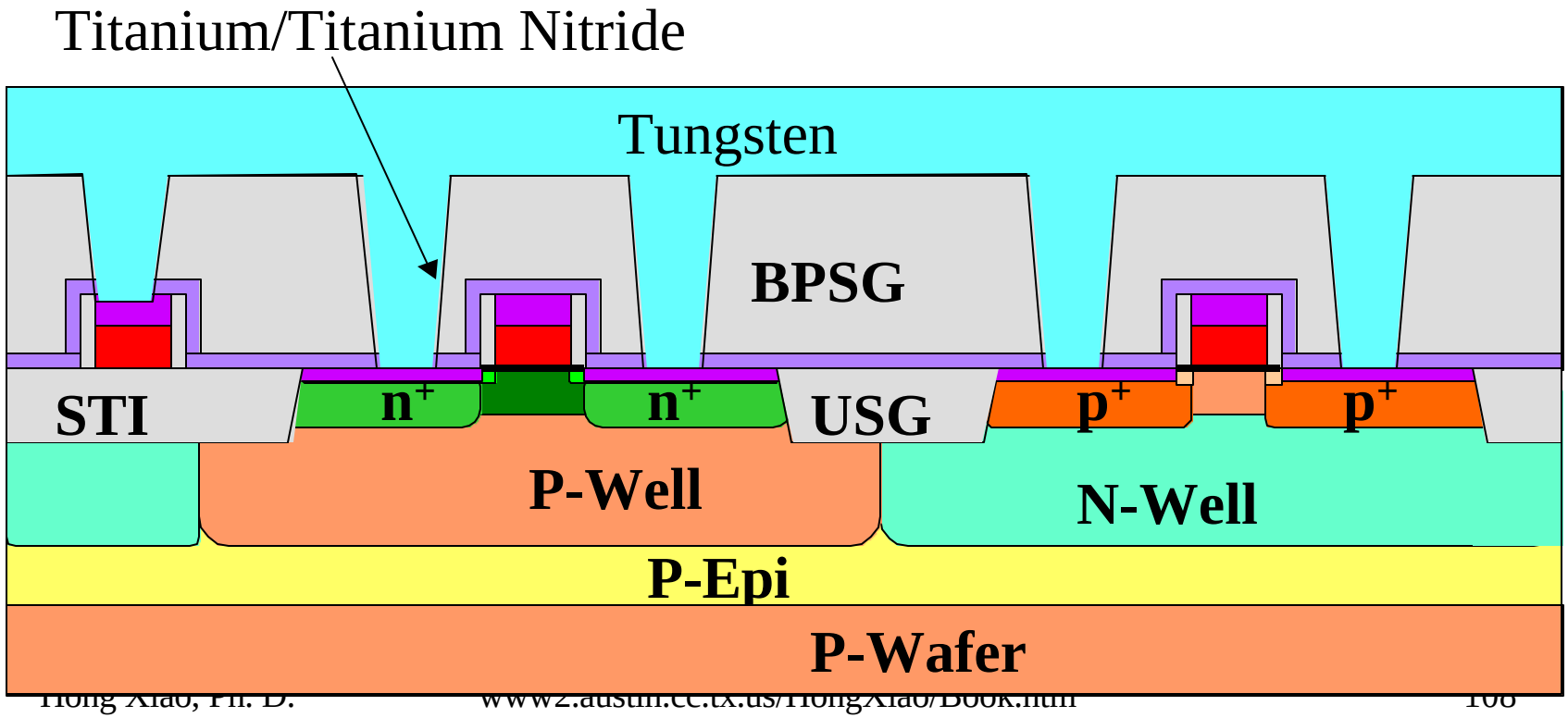
Mask 10: Contact Hole



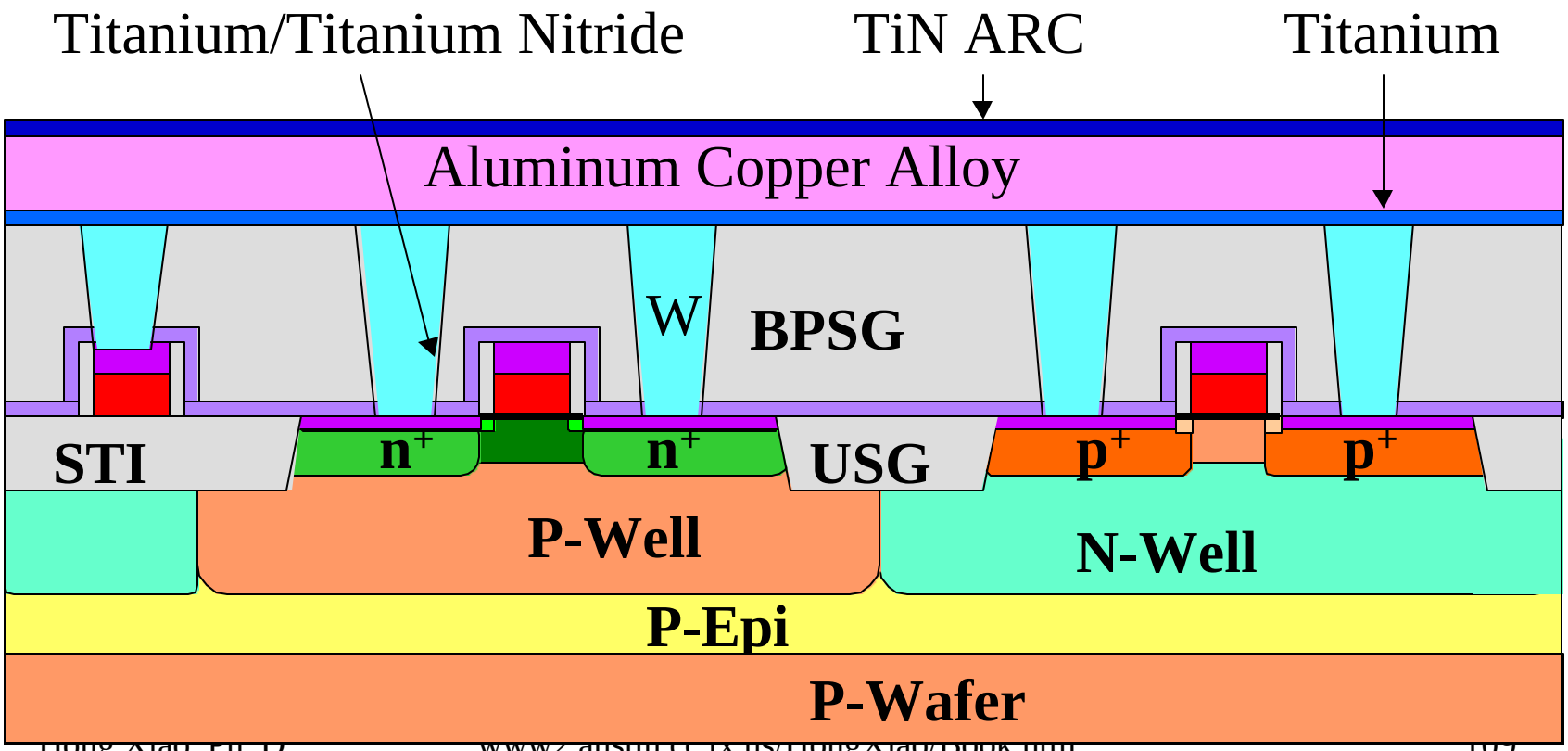
Contact Hole Etch, BPSG Etch



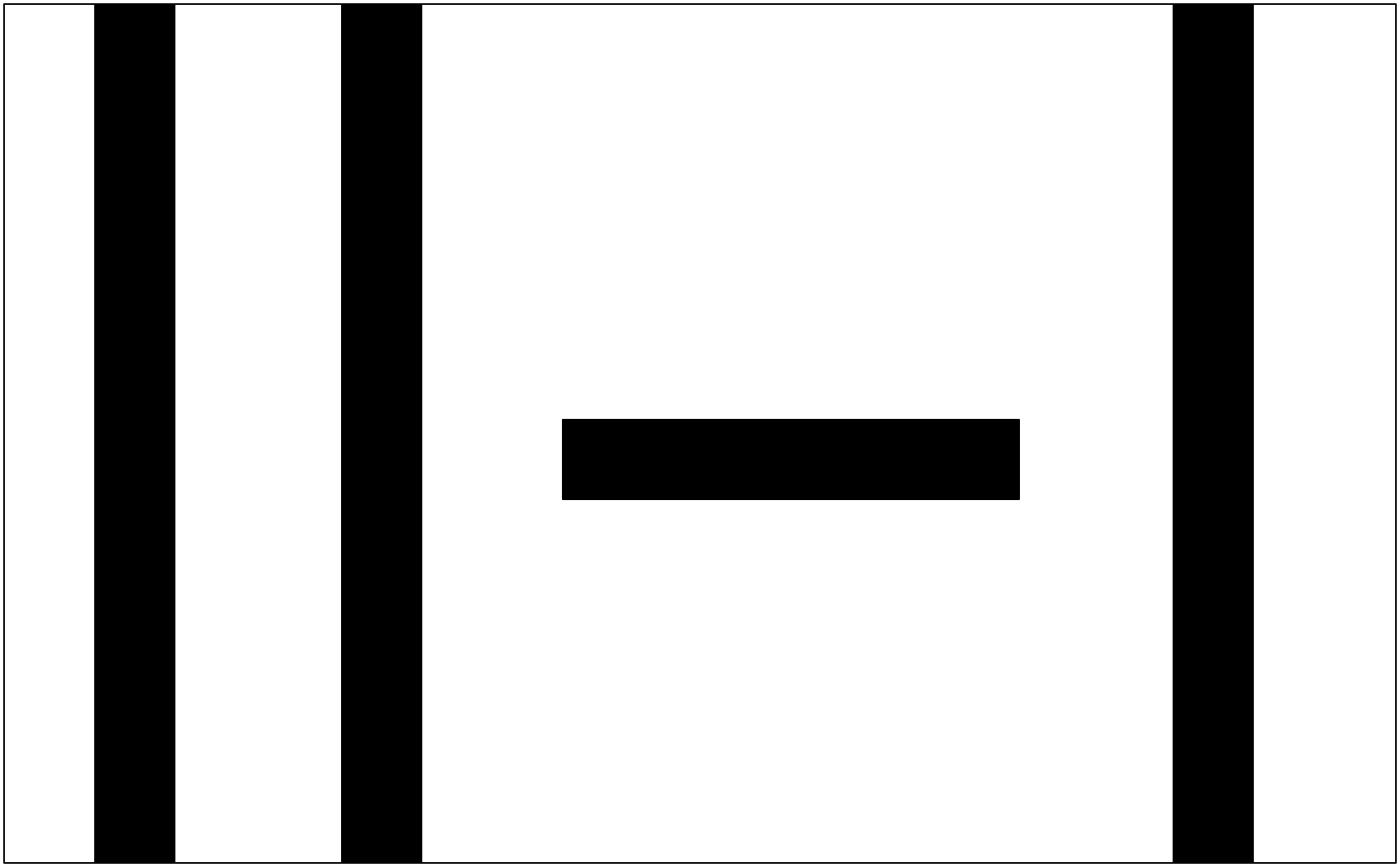
Contact Hole Etch, BPSG Etch



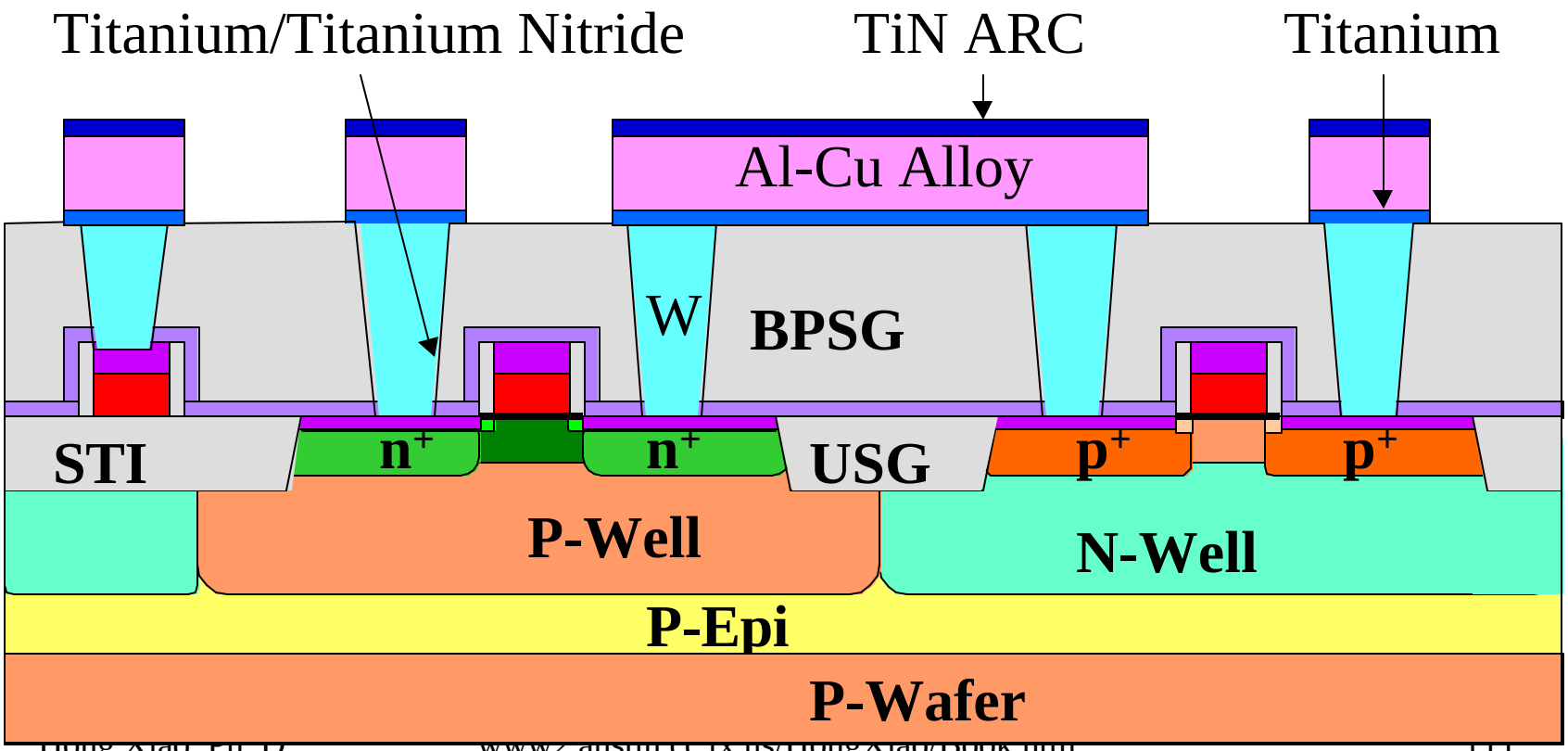
Contact Hole Etch, BPSG Etch



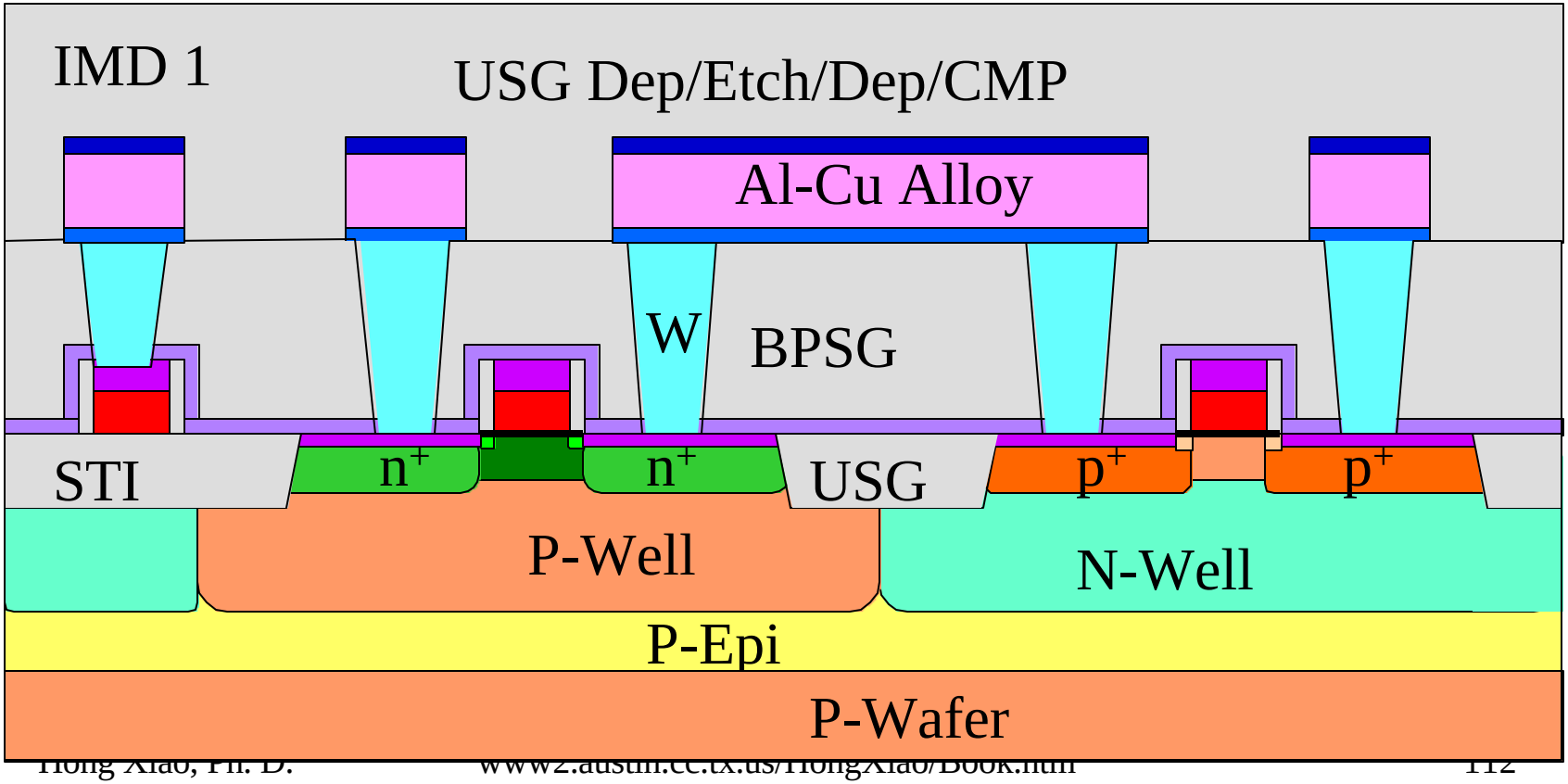
Mask 11: Metal 1 Interconnect



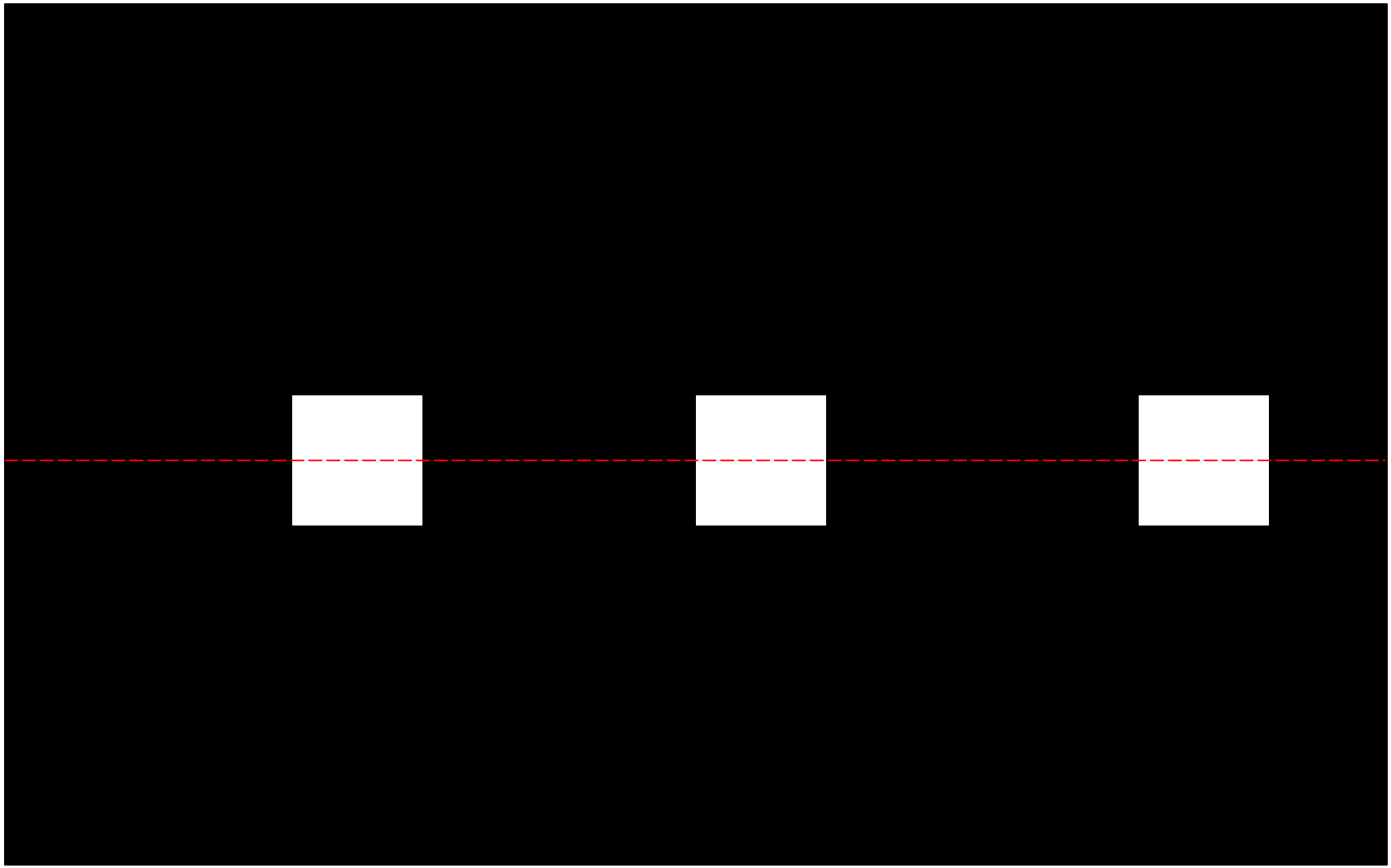
Metal Etch


Titanium/Titanium Nitride
TiN ARC
Titanium
Al-Cu Alloy
W
BPSG
STI
n+
n+
USG
p+
p+
P-Well
N-Well
P-Epi
P-Wafer

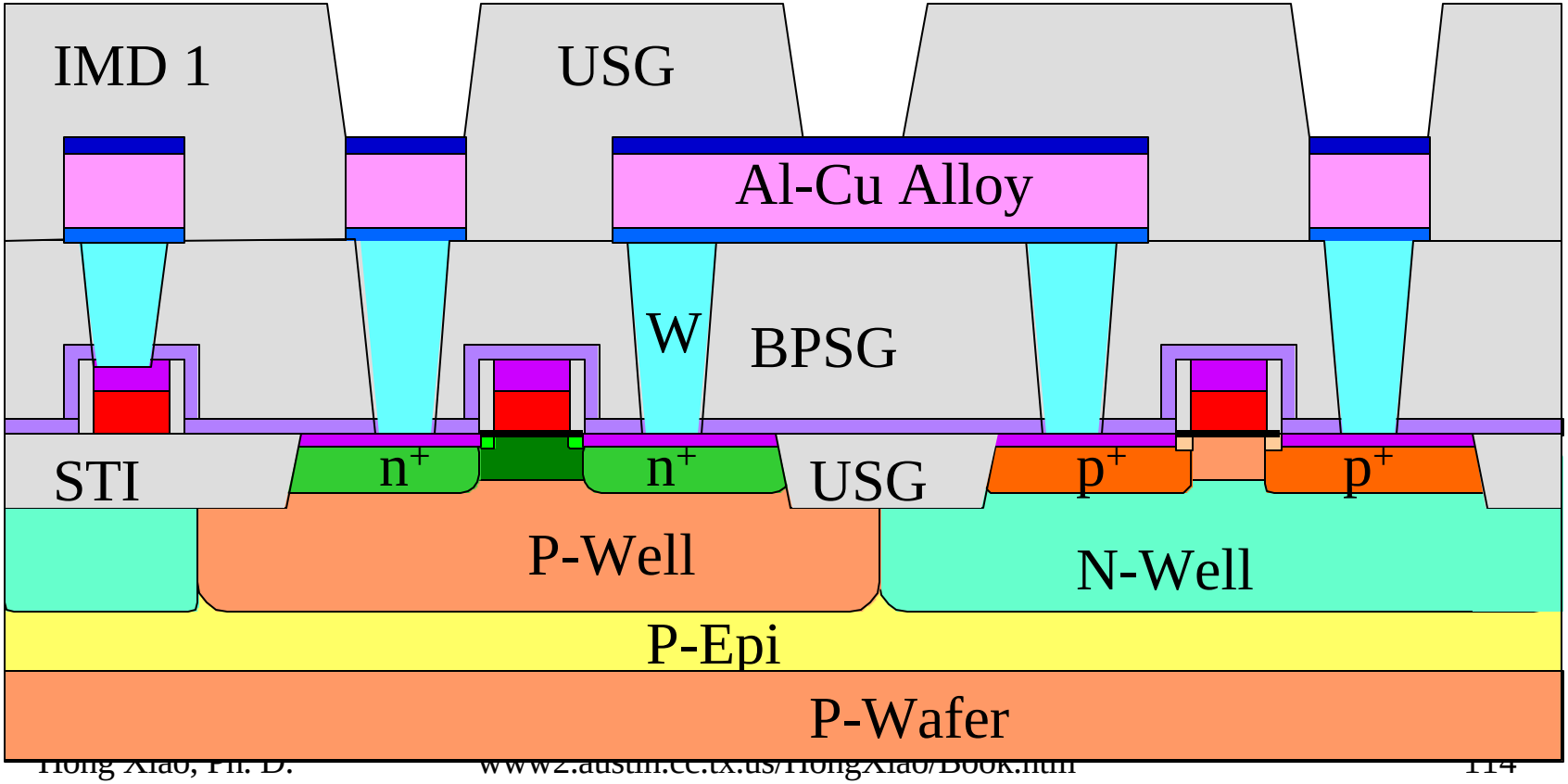
PE-TEOS USG Dep/Etch/Dep/CMP



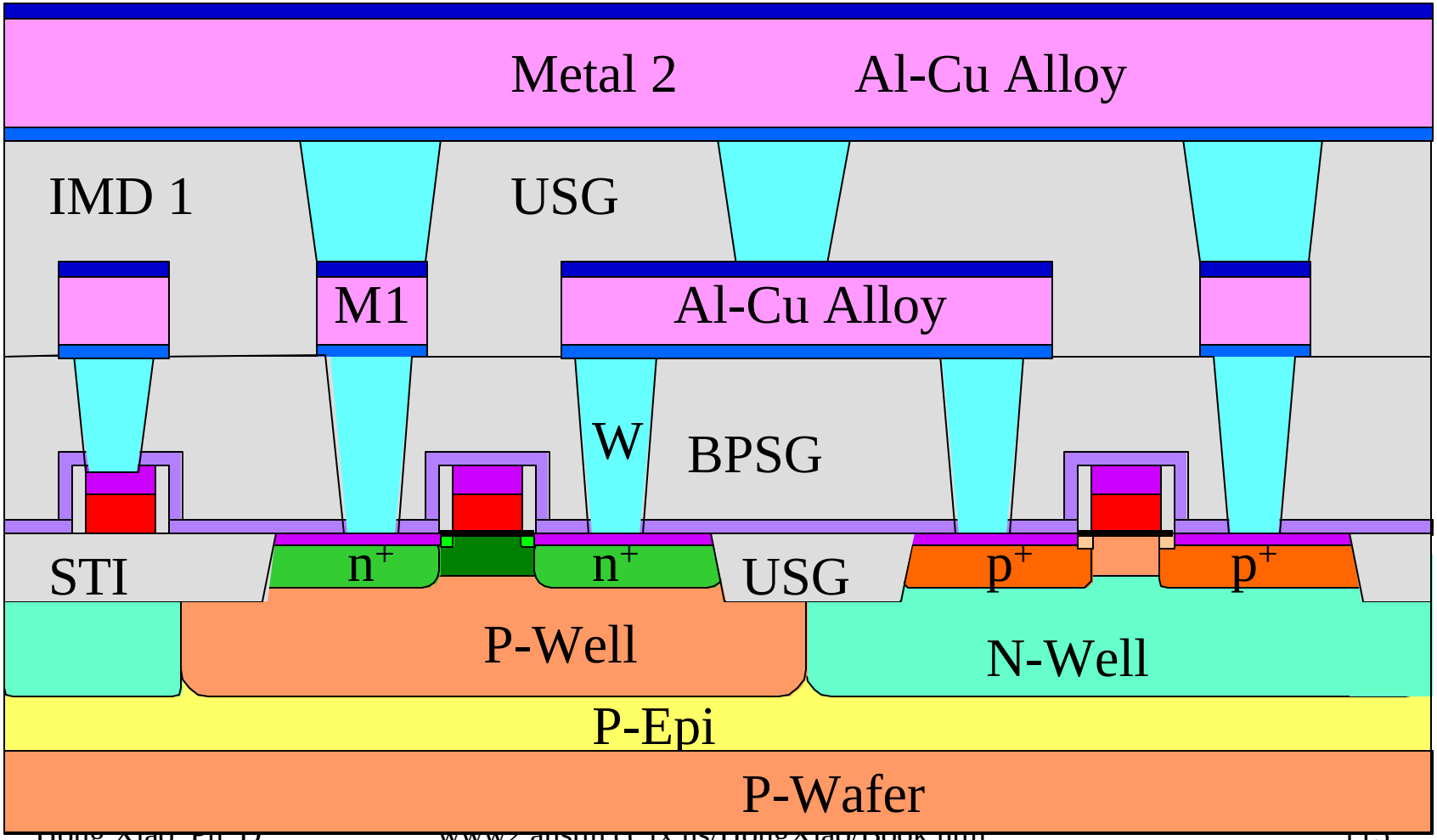
Mask 12: Via 1



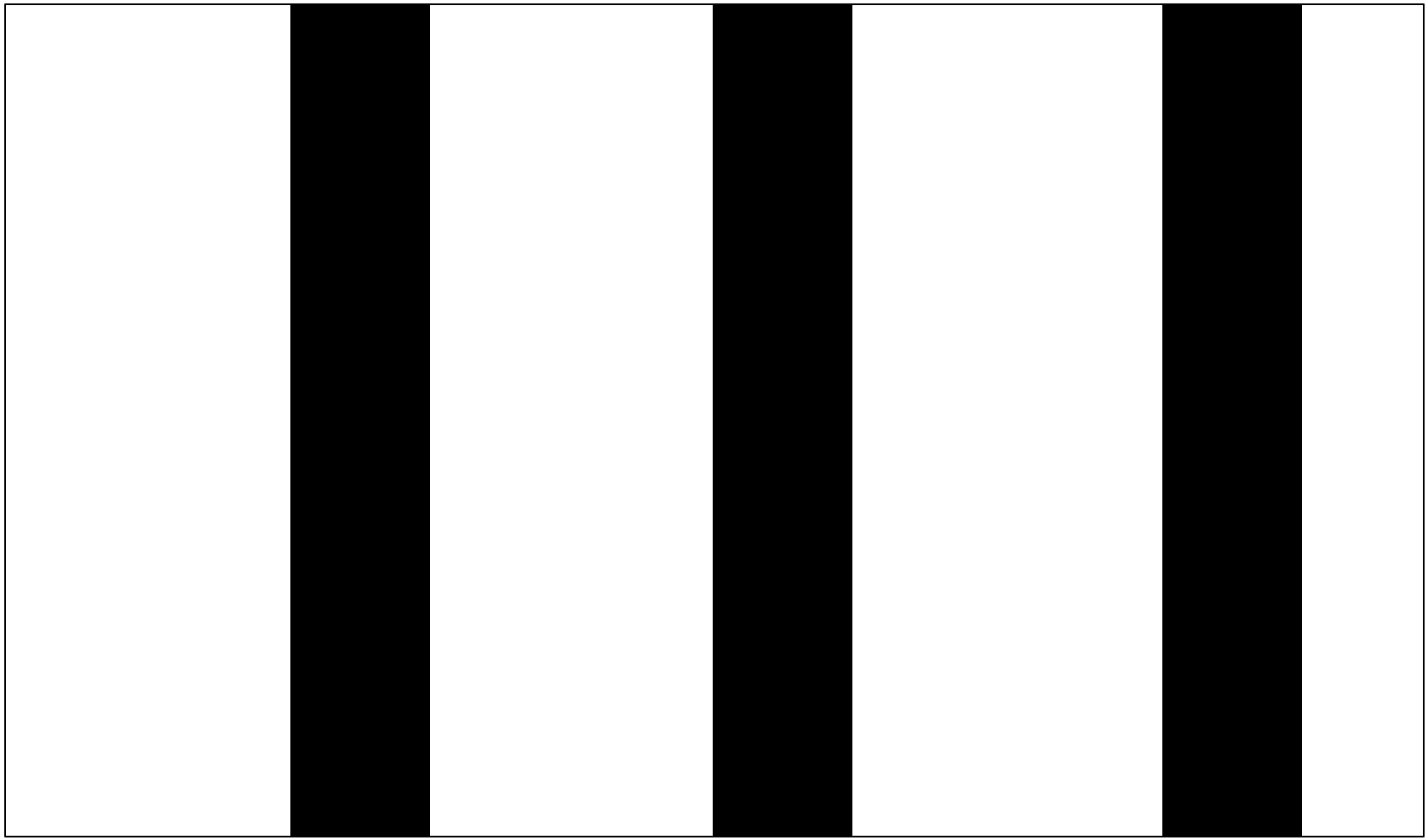
Via Etch, Etch USG



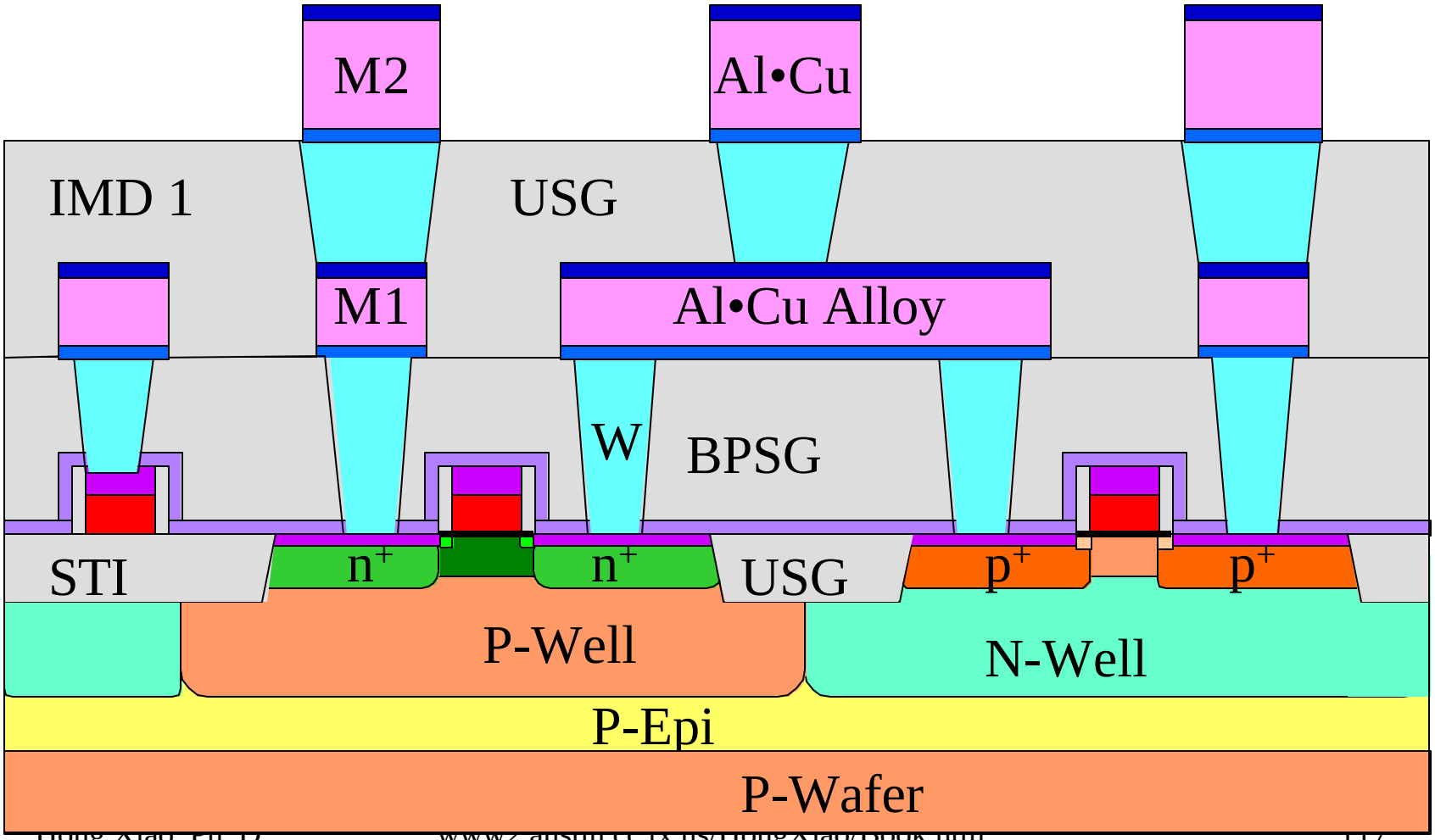
Via Etch, Etch USG



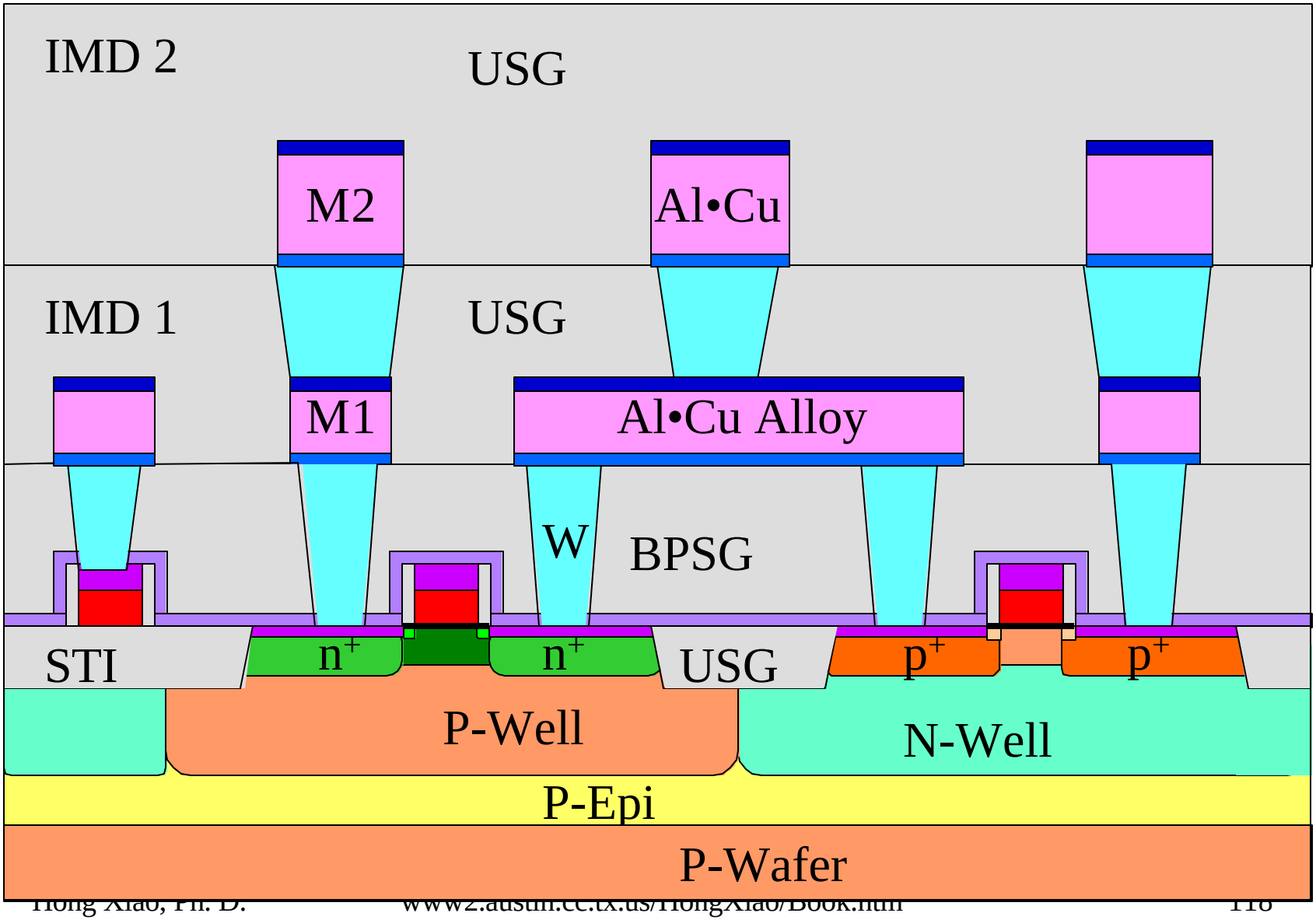
Mask 13: Metal 2 Interconnect



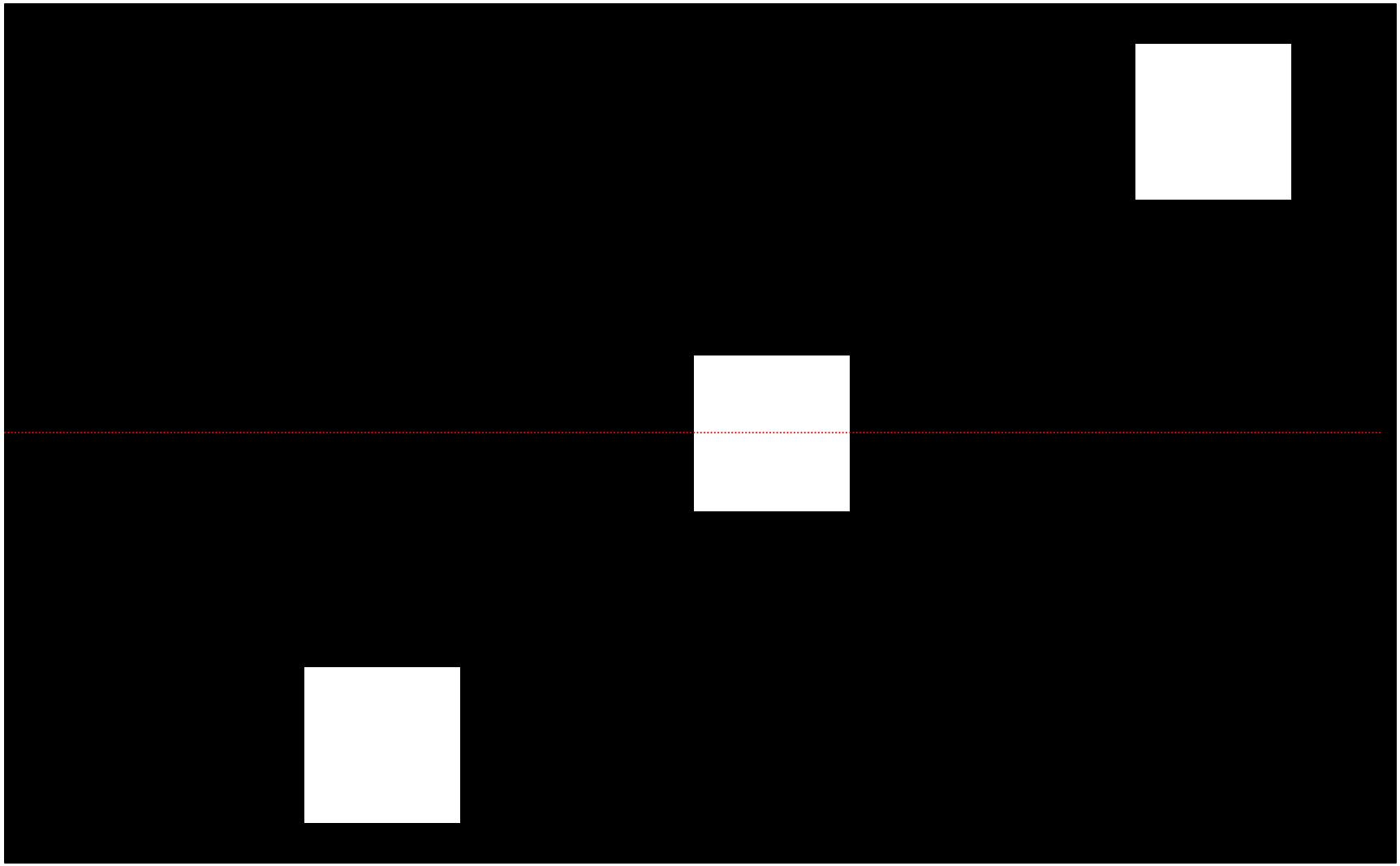
Etch Metal 2


M2
Al•Cu
IMD 1
USG
M1
Al•Cu Alloy
W
BPSG
STI
n+
n+
USG
p+
p+
P-Well
N-Well
P-Epi
P-Wafer

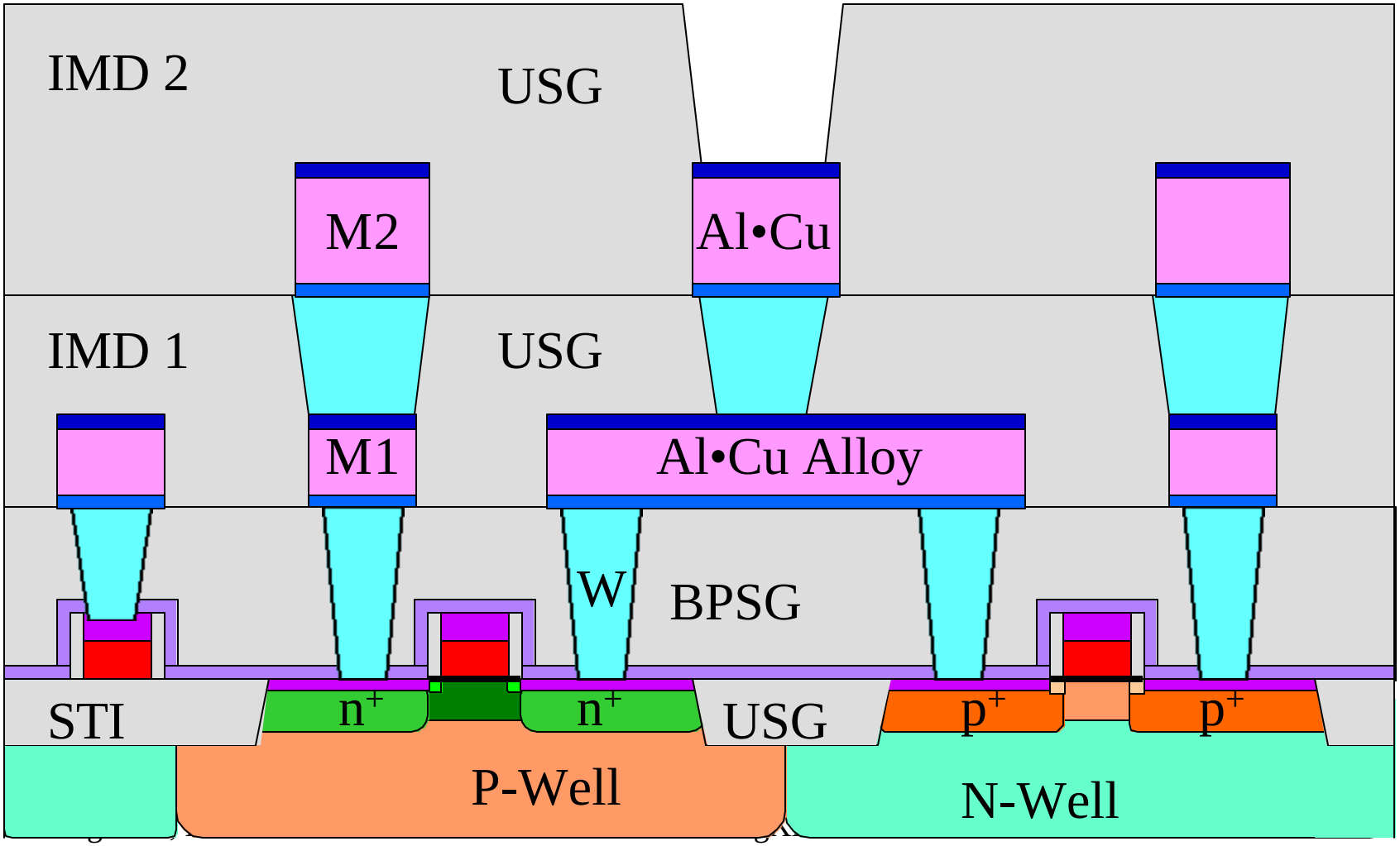
USG Dep/Etch/Dep/CMP



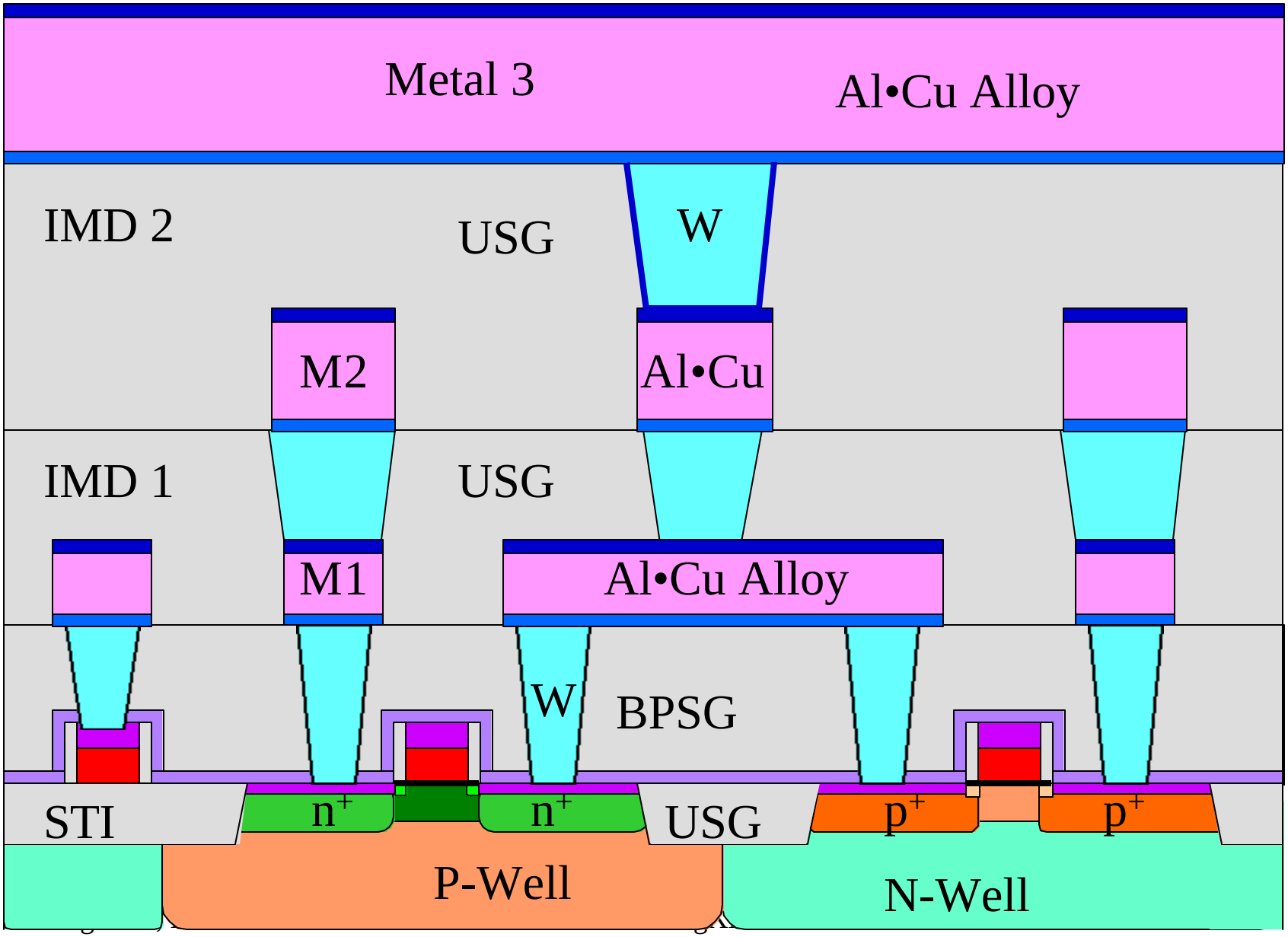
Mask 14: Via 2



Via 2 Etch, Etch USG

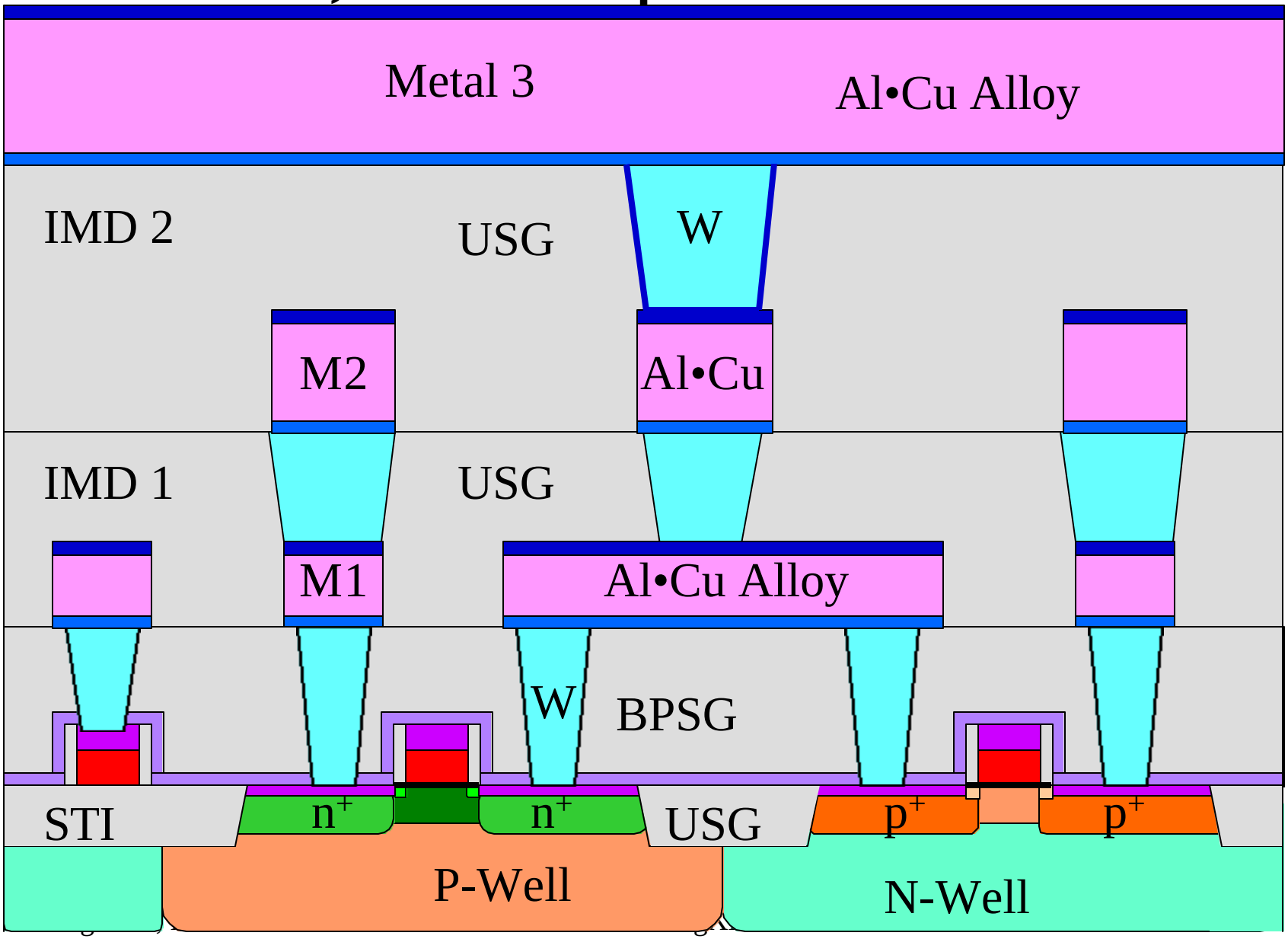


Metallization of Metal 3

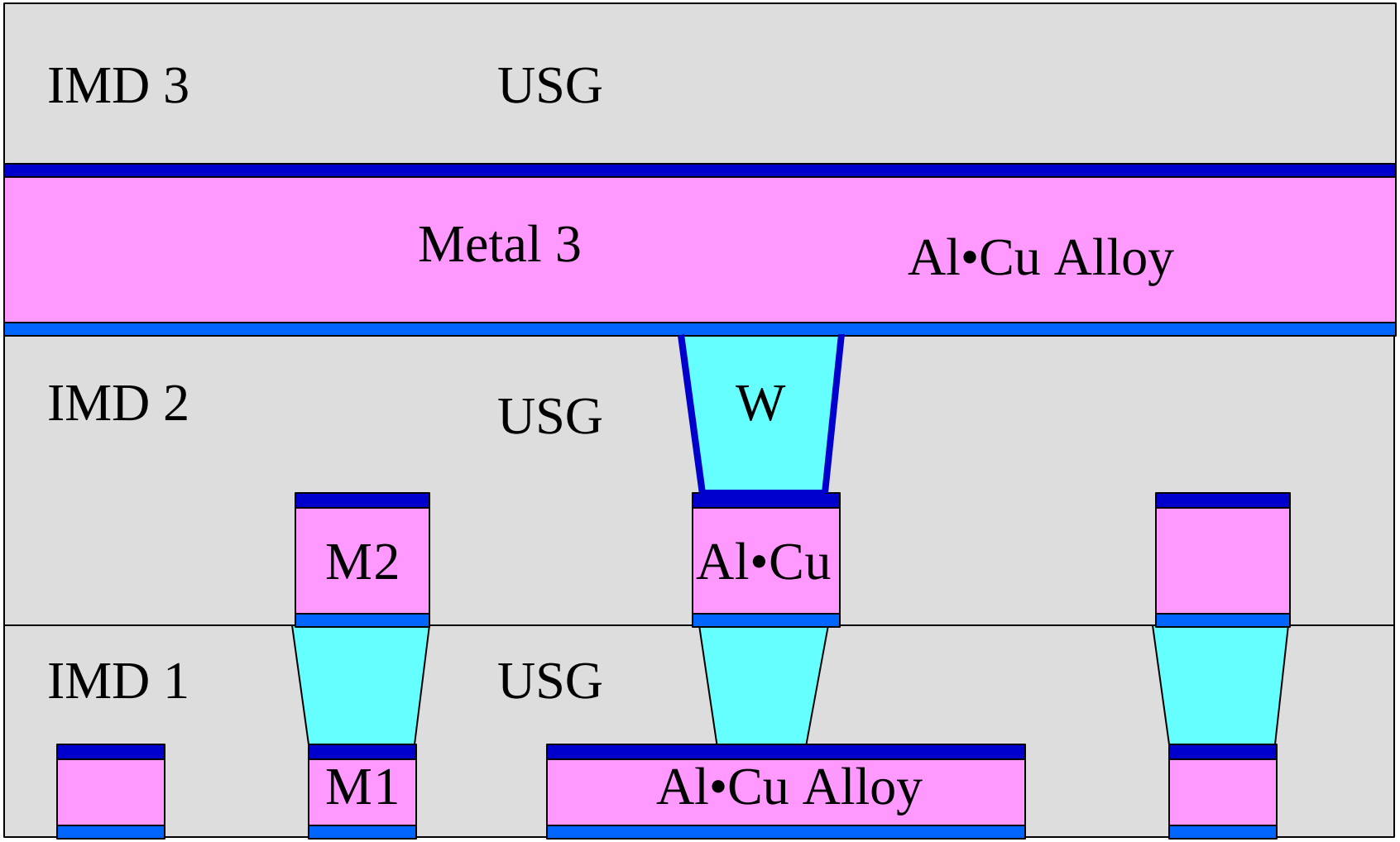


Mask 15: Metal 3 Interconnects

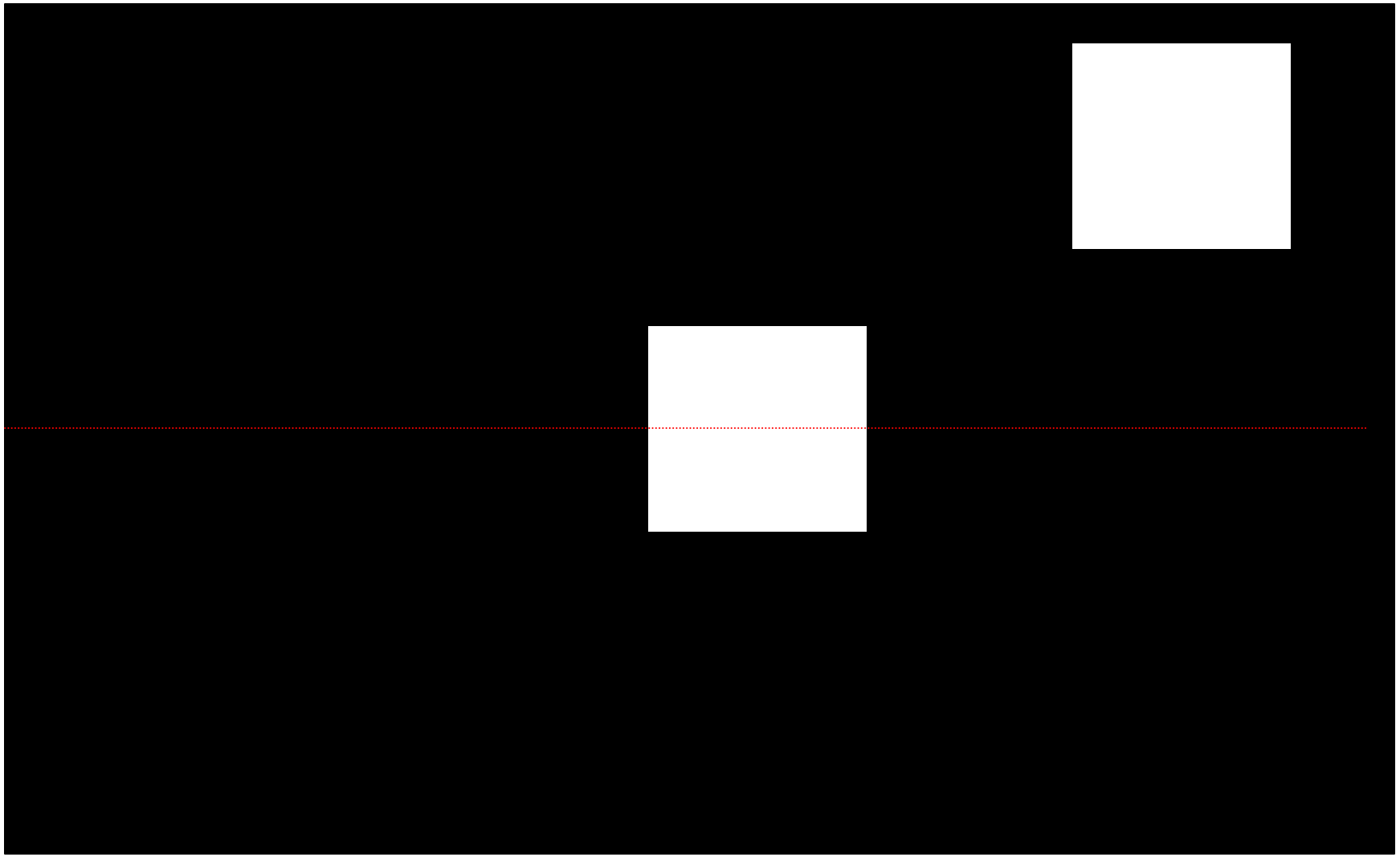
Metal Etch, PR Strip and Metal Anneal



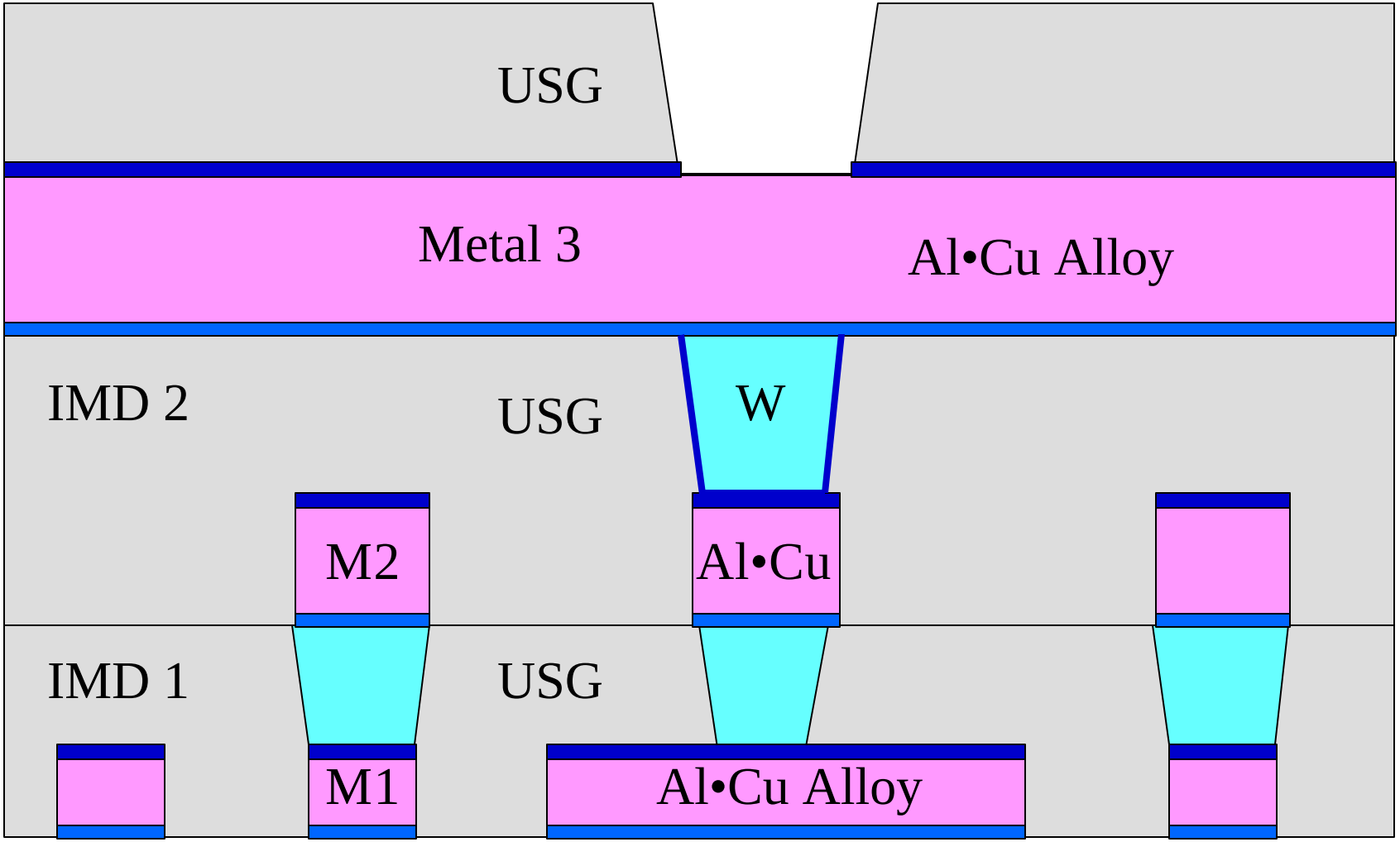
PE-TEOS USG Dep/Etch/Dep/CMP



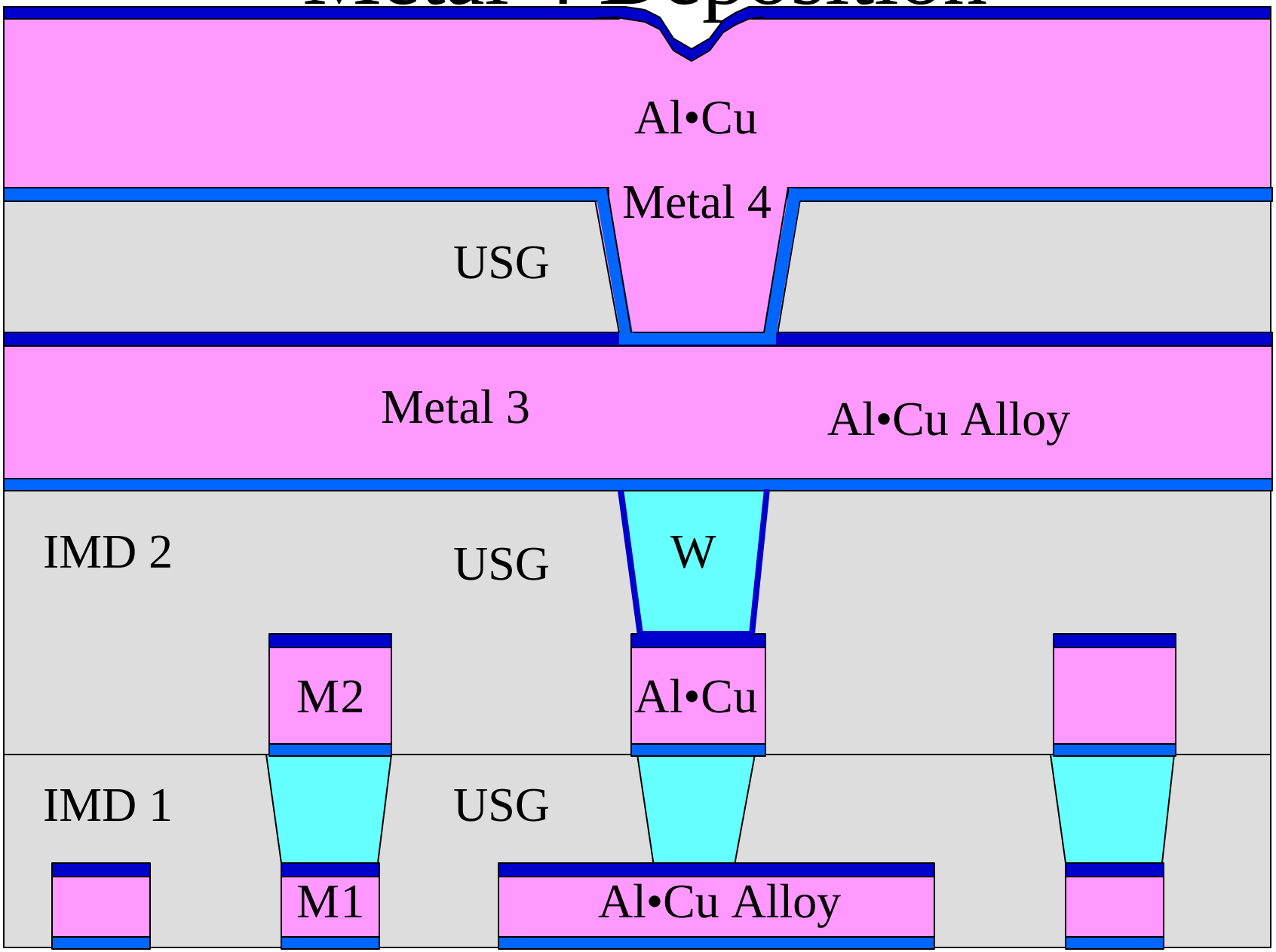
Mask 16: Via 3



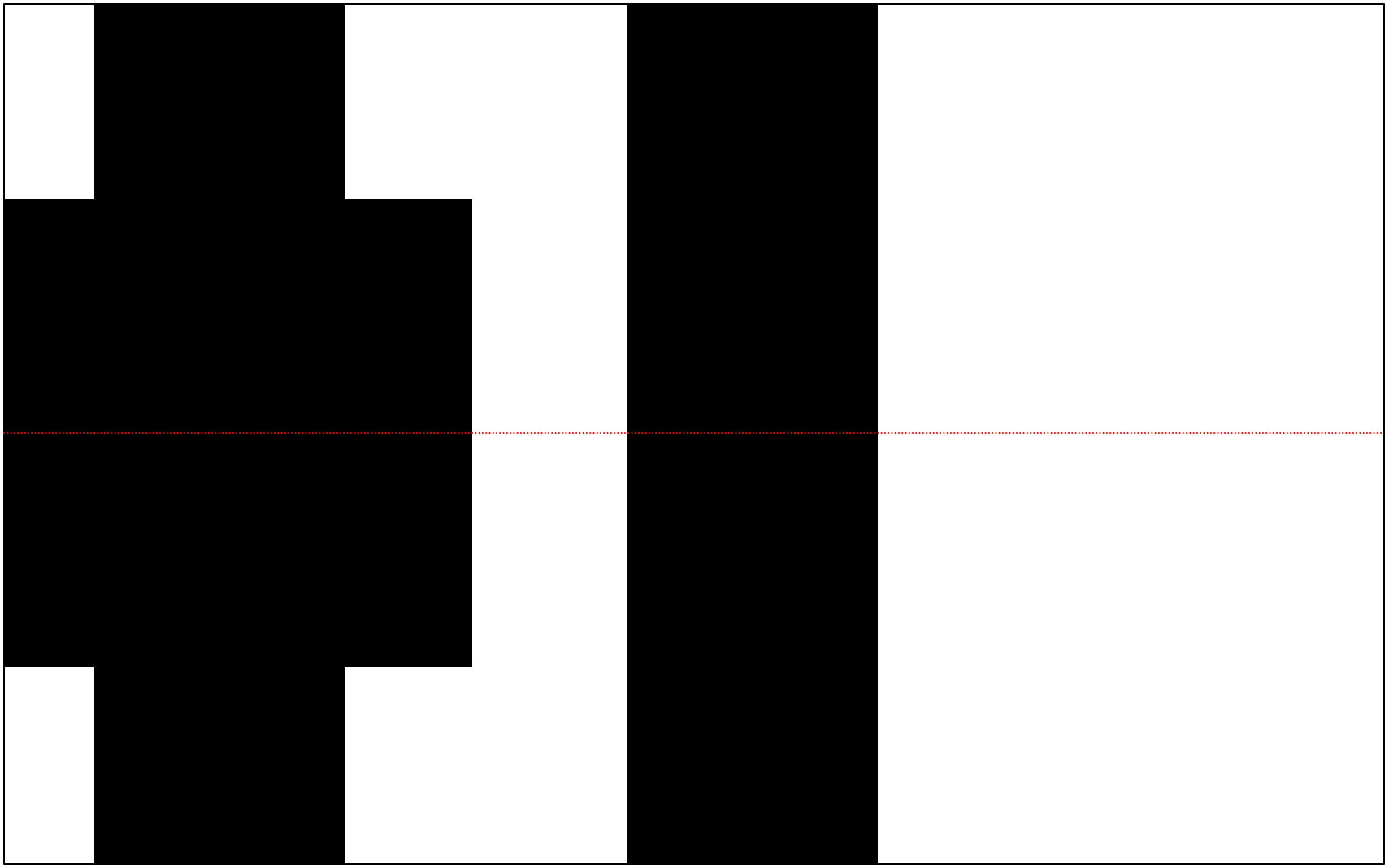
Via 3 Etch and PR Strip



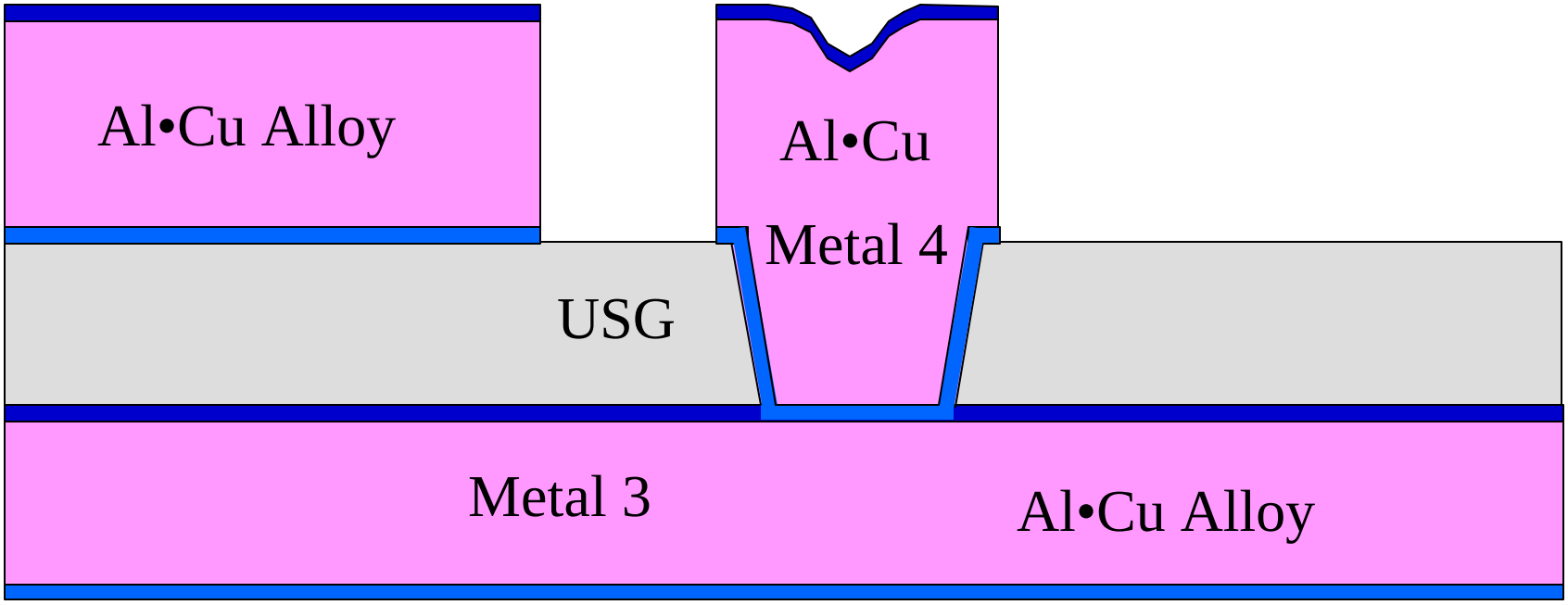
Metal 4 Deposition



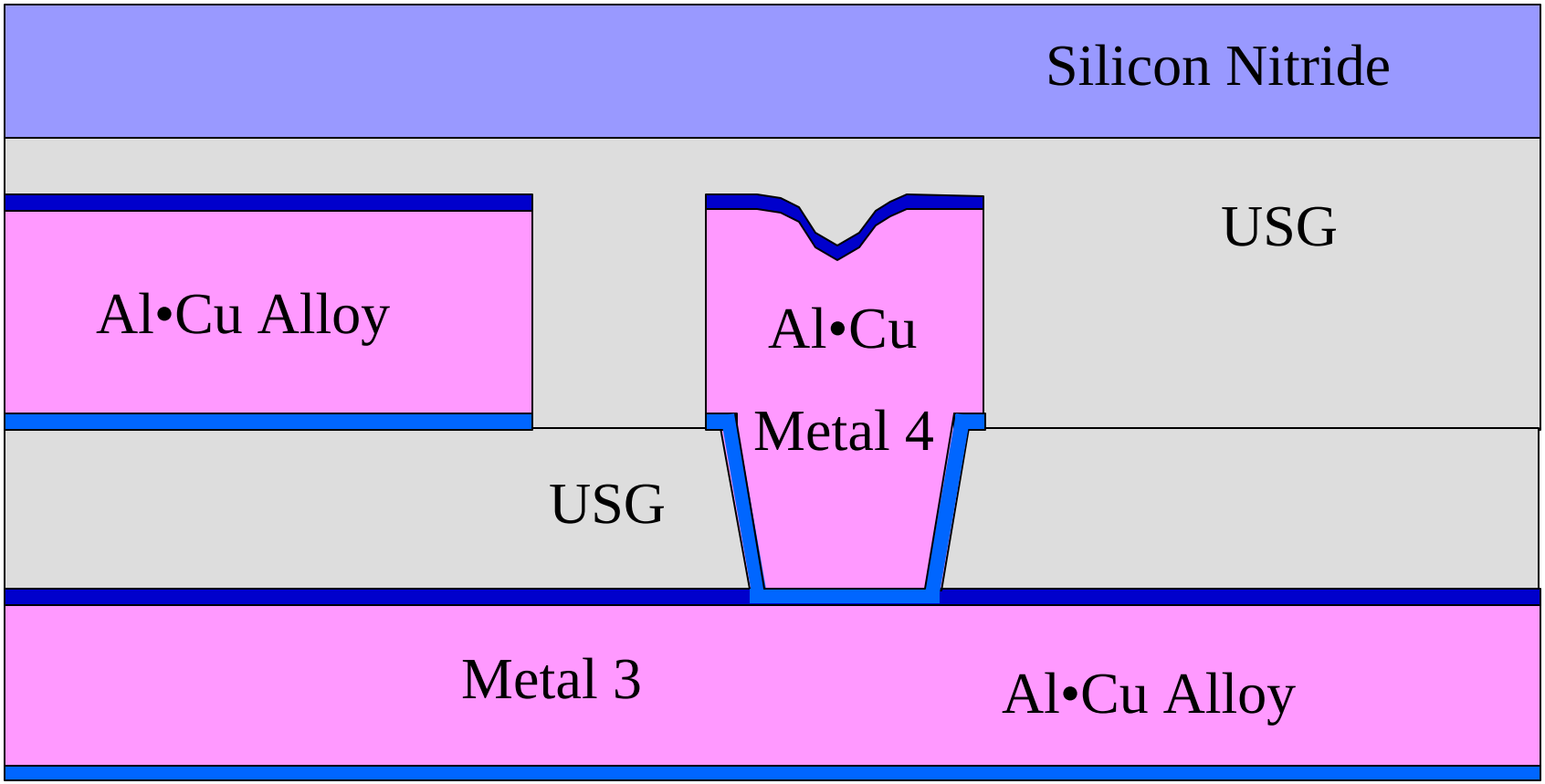
Mask 17: Metal 4 Interconnects



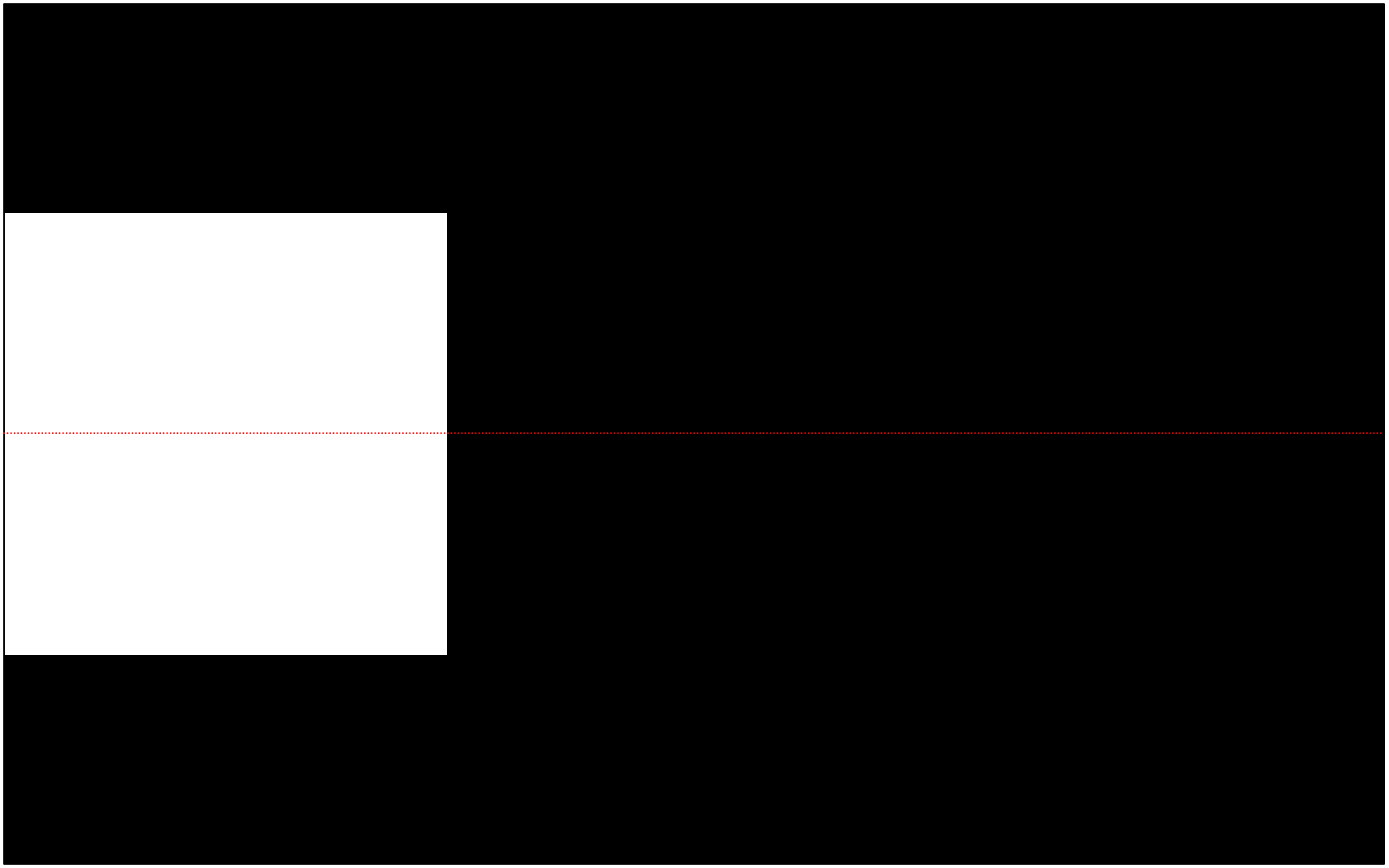
Etch Metal 4



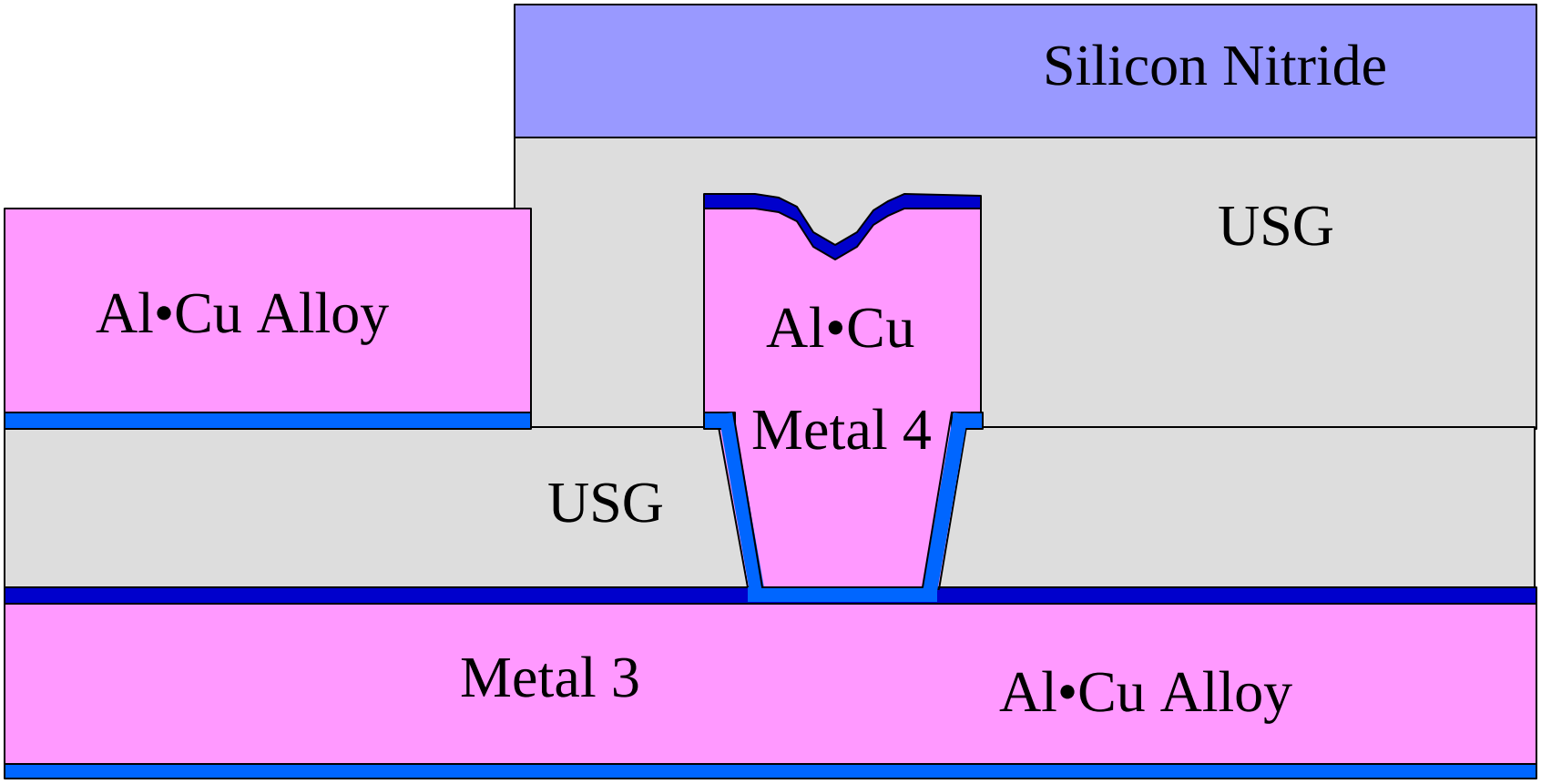
Passivation Dielectric Deposition

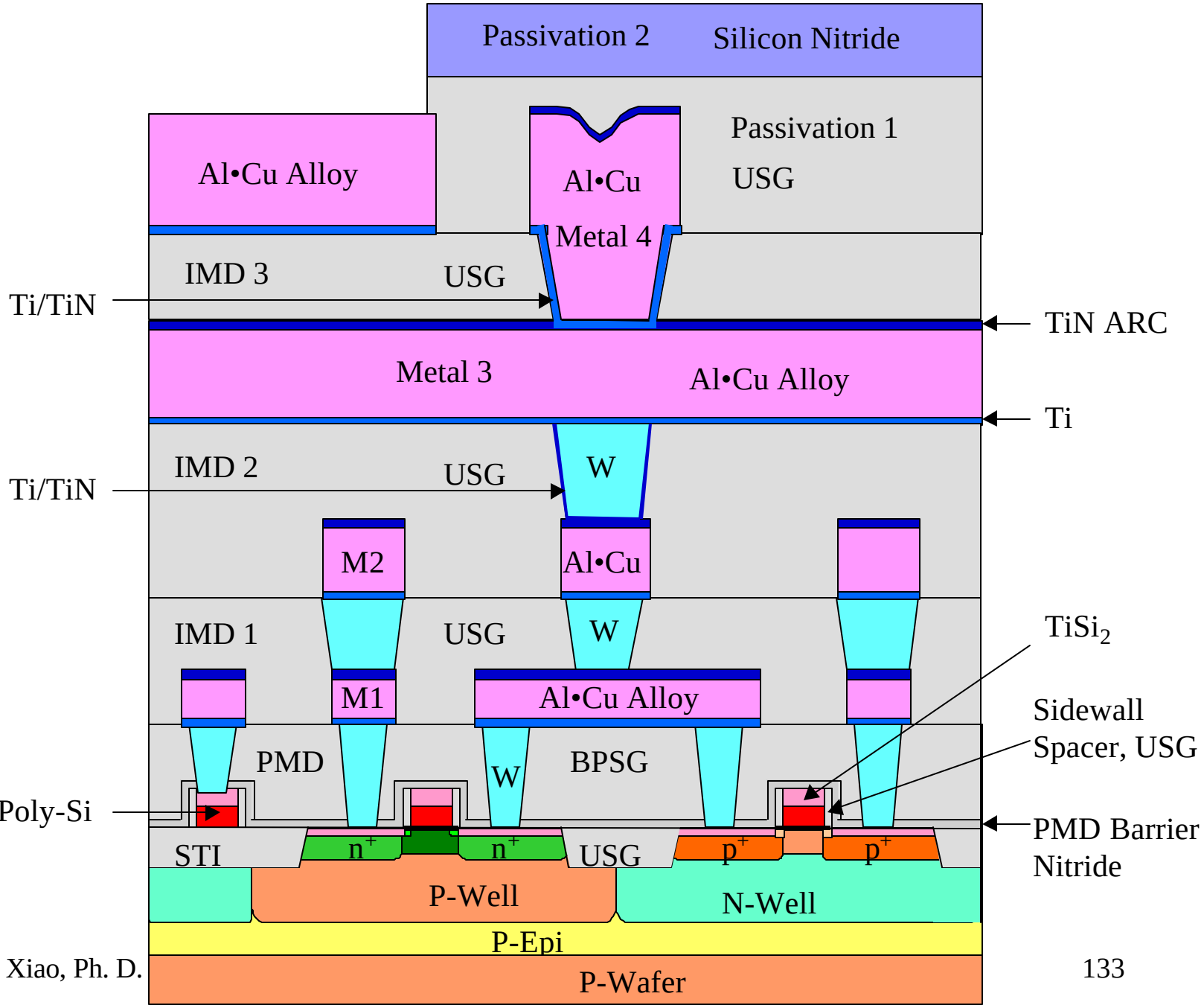


Mask 18: Bonding Pad



Etch Bonding Pad, Strip PR




Passivation 2
Silicon Nitride
Passivation 1
USG
Al•Cu Alloy
Al•Cu
Metal 4
IMD 3
USG
Ti/TiN
TiN ARC
Metal 3
Al•Cu Alloy
Ti
IMD 2
USG
W
Ti/TiN
M2
Al•Cu
IMD 1
USG
W
TiSi2
M1
Al•Cu Alloy
Sidewall
Spacer, USG
PMD
W
BPSG
Poly-Si
PMD Barrier
Nitride
STI
n+
n+
USG
p+
p+
P-Well
N-Well
P-Epi
P-Wafer

State-of-art Technology

- The 2000's Technology
- Feature size 0.13 μm or smaller
- Wafer size 200 mm or 300 mm

State-of-art Technology

- Silicon on isolator (SOI) with STI
  - Completely isolate the transistor on the silicon surface from the bulk silicon substrate
  - Eliminate radiation-induced soft error.
- Increase the packing density of IC chip.
- High radiation resistance
- SOI chips will become the mainstream for the high-performance electronics

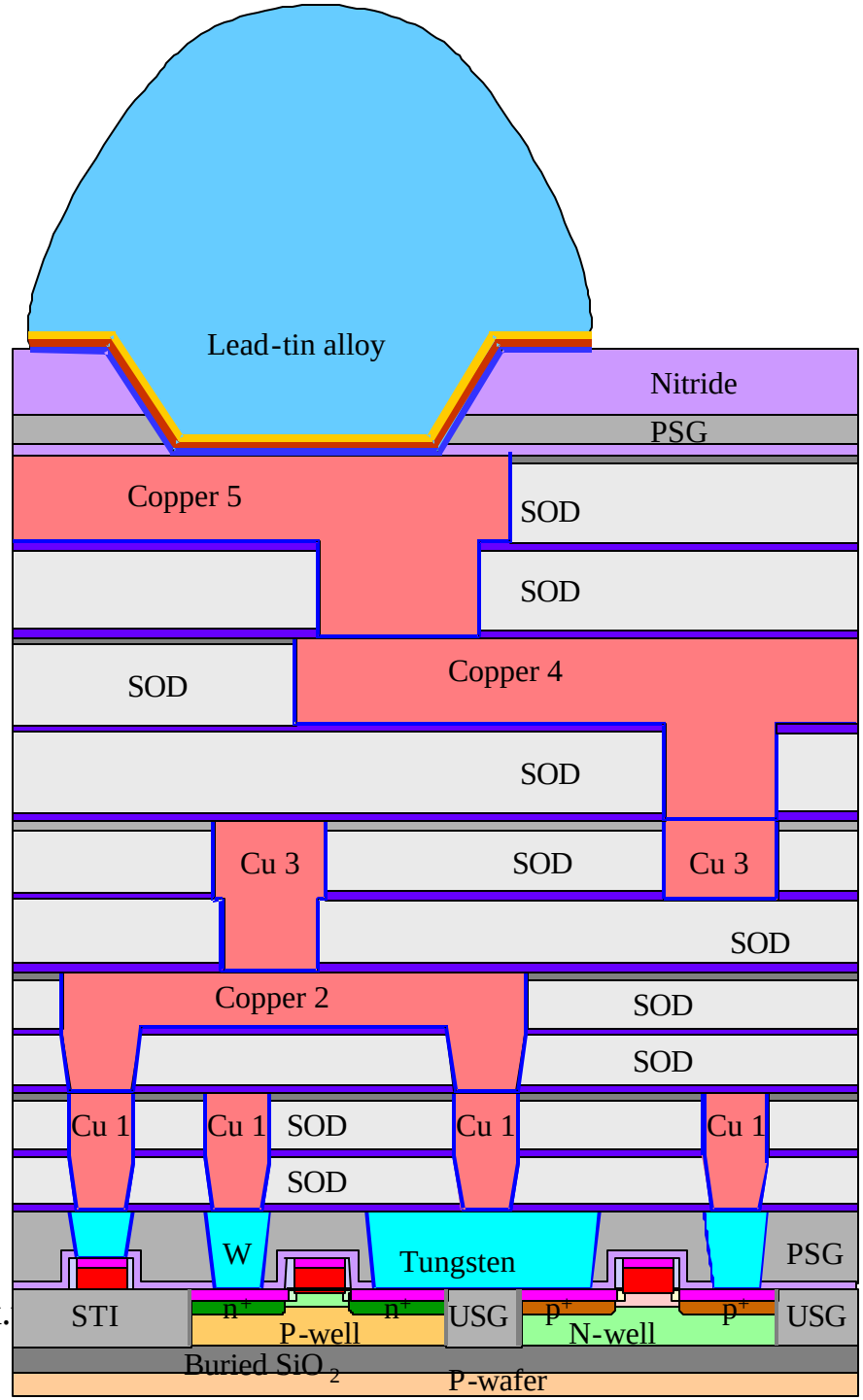
State-of-art Technology

- Copper and low-κ to reduce *RC* delay,
- Lower power consumption, higher IC speed
- Dual damascene process
  - Two dielectric etches, no metal etch
  - Uses metal CMP instead of metal etch
- Main challenges: dielectric etch, metal deposition, and metal polish

State-of-art Technology

- Copper metallization: Cu seed, Ta/TaN barrier, Cu ECP, anneal, and metal CMP
- Low-κ dielectric: still in development
  - CVD and spin-on dielectric (SOD).
  - CVD: familiar technologies, existing process equipment and experience
  - SOD: extendibility to very low dielectric constant ($\kappa<2$) with porous silica

State-of-Art SOI CMOS IC with Copper and Low-κ Interconnection



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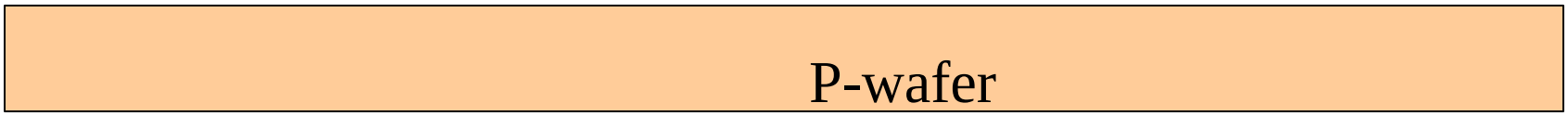
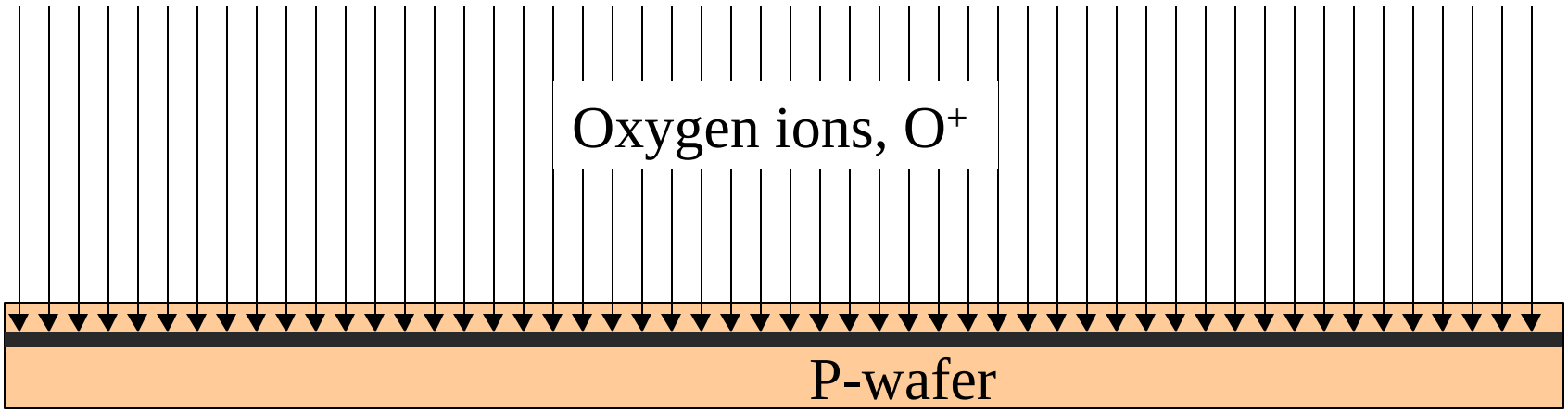
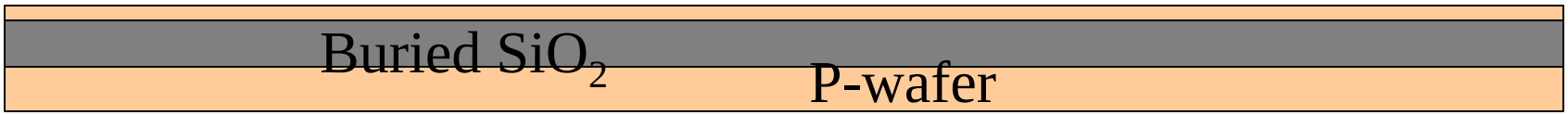
Bare wafer



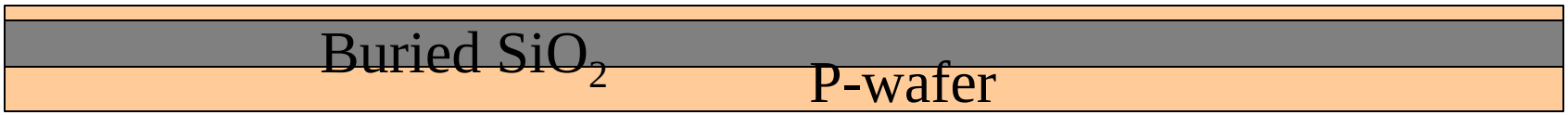
High Current Oxygen Ion Implantation



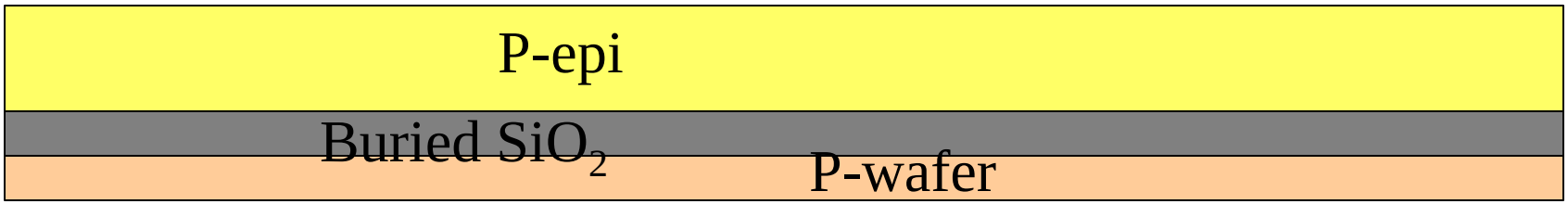
Oxide Anneal



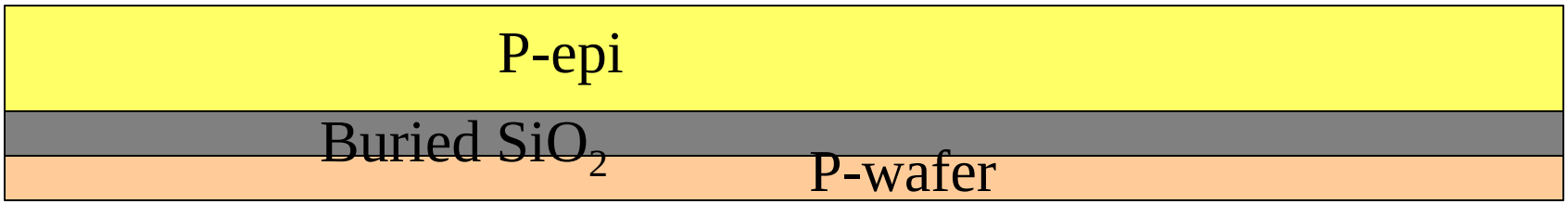
Wafer Clean



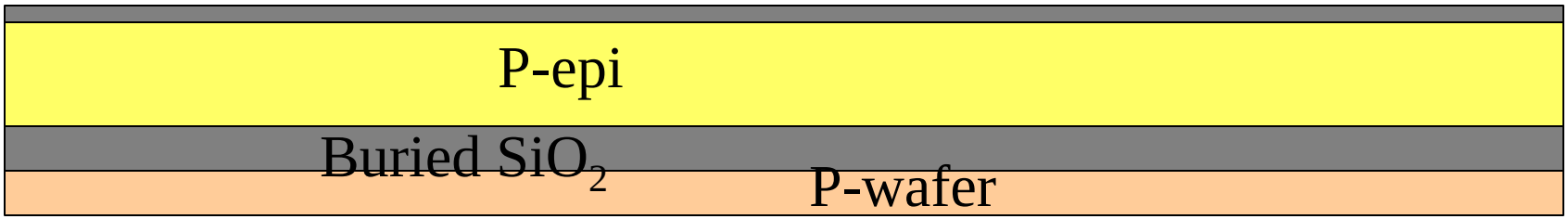
Epitaxial Silicon Deposition



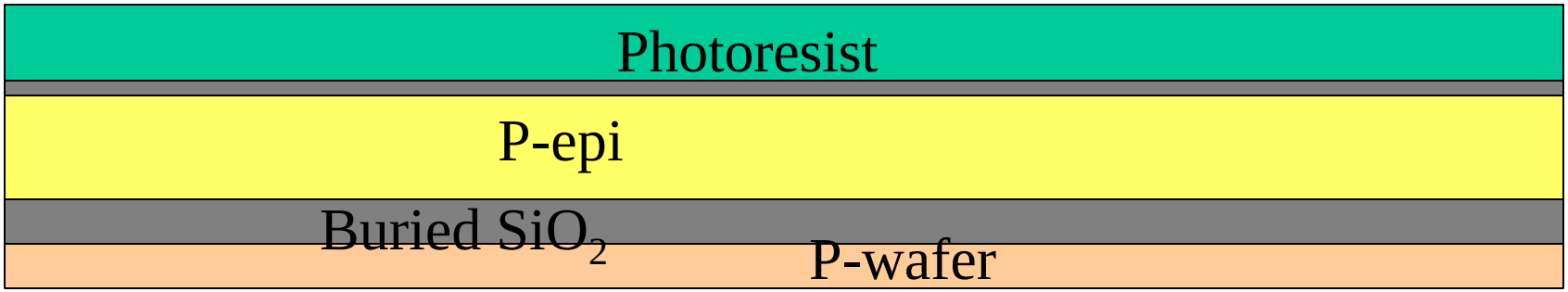
Wafer Clean



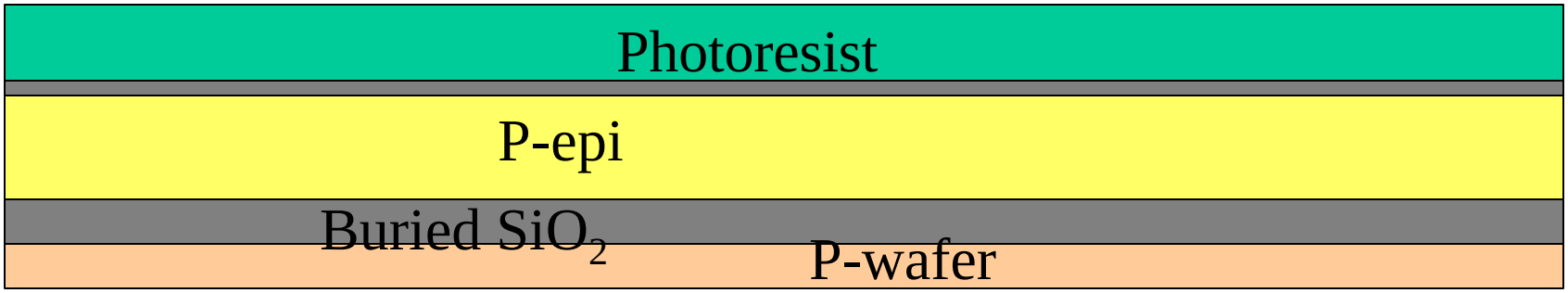
Oxidation, Screen Oxide



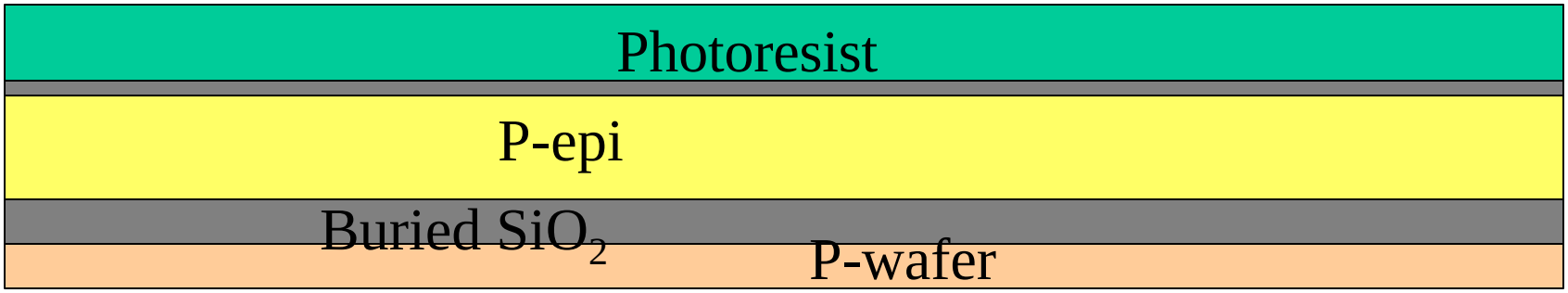
Photoresist Coating and Baking



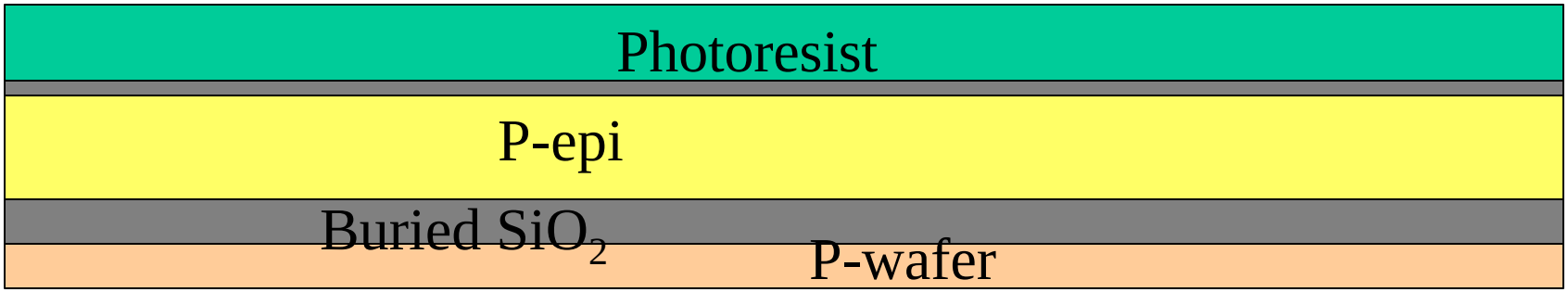
Mask 0, Alignment Mark



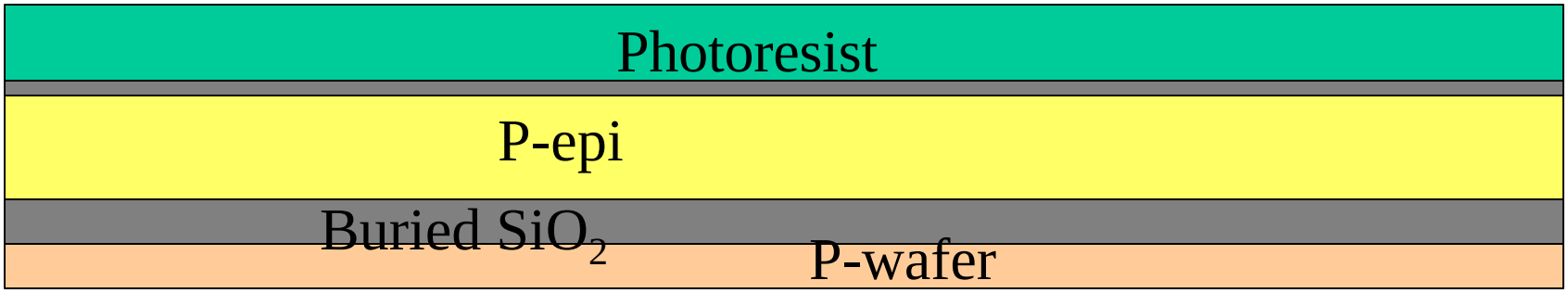
Exposure



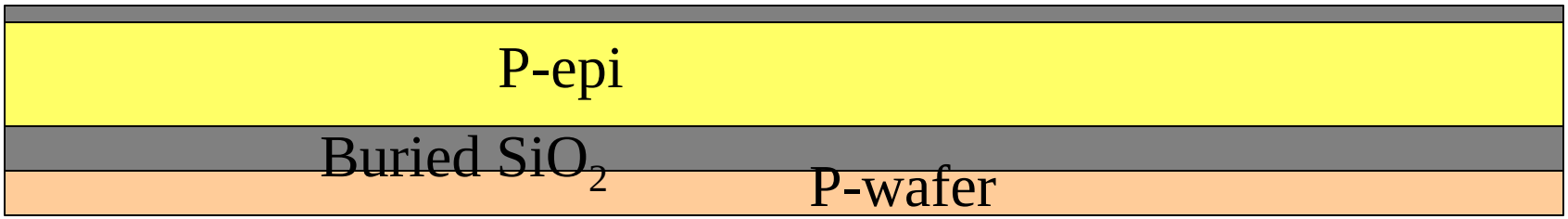
PEB, Development, and Inspection



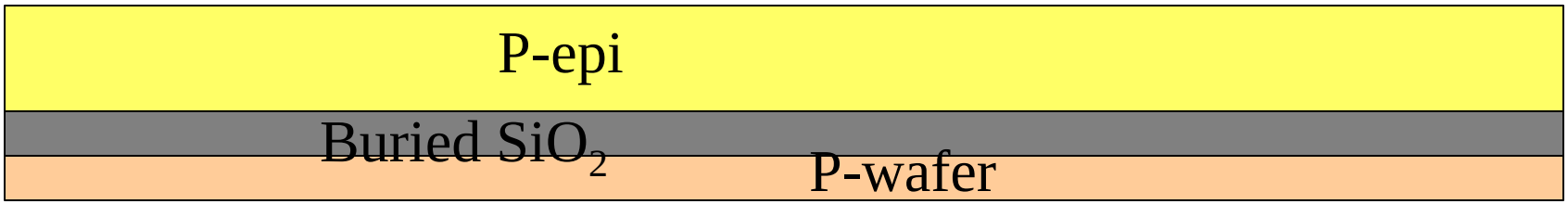
Etch Oxide, Etch silicon



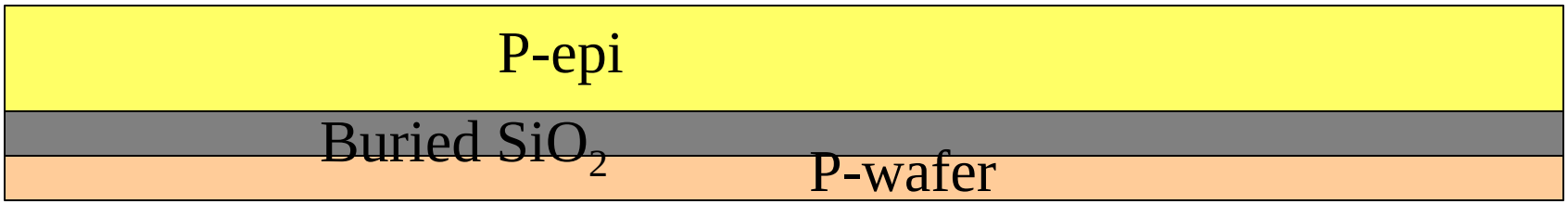
Strip Photoresist



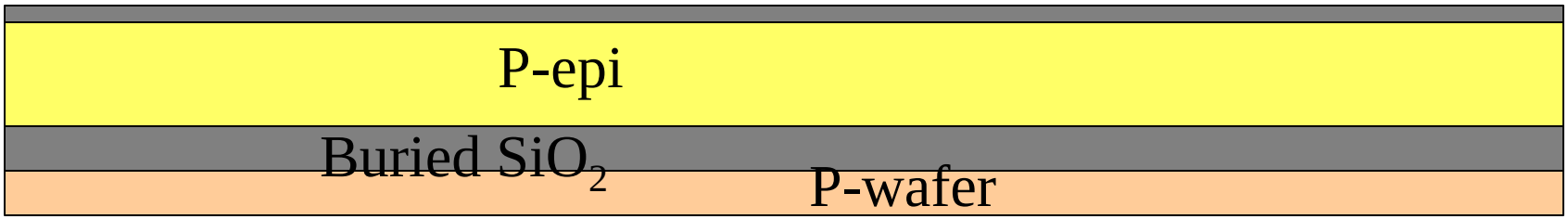
Strip Screen Oxide



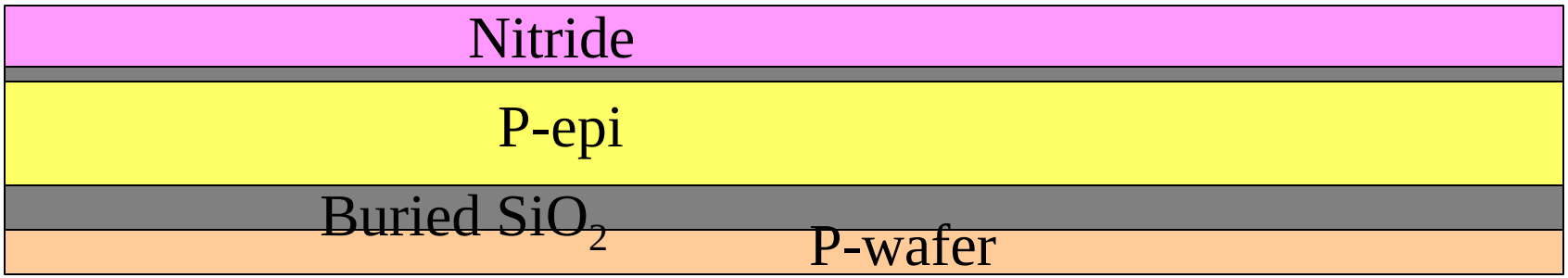
Wafer Clean



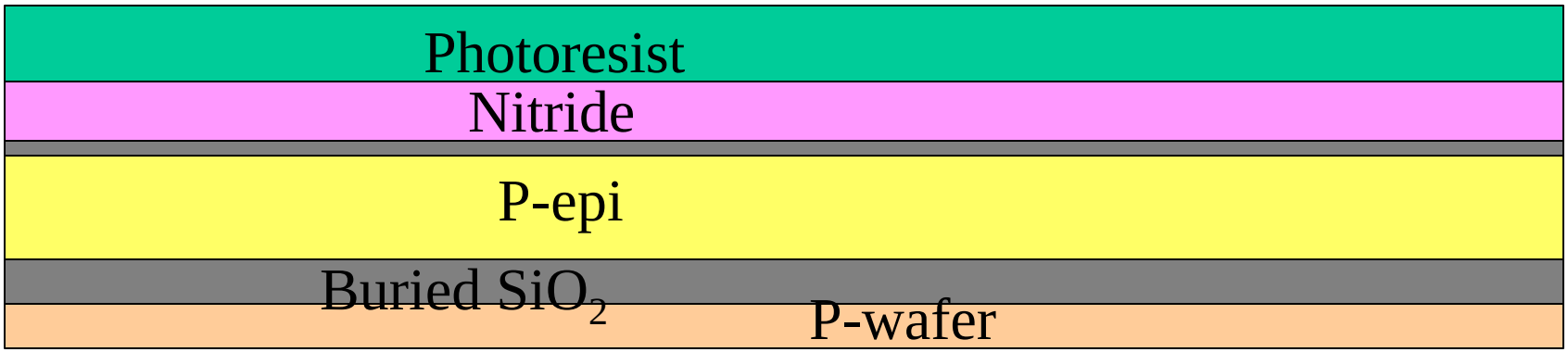
Oxidation, Pad Oxide



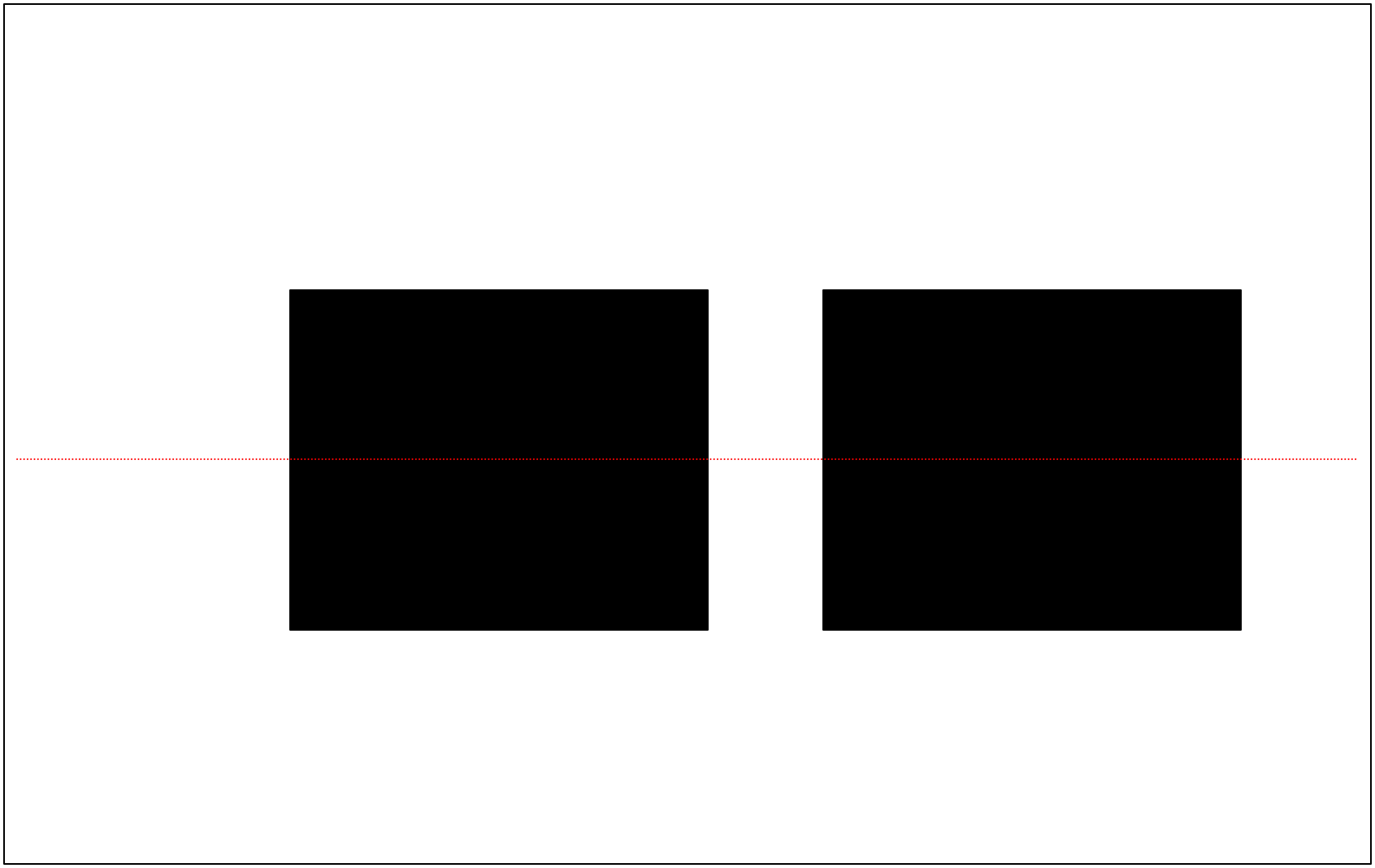
LPCVD Silicon Nitride



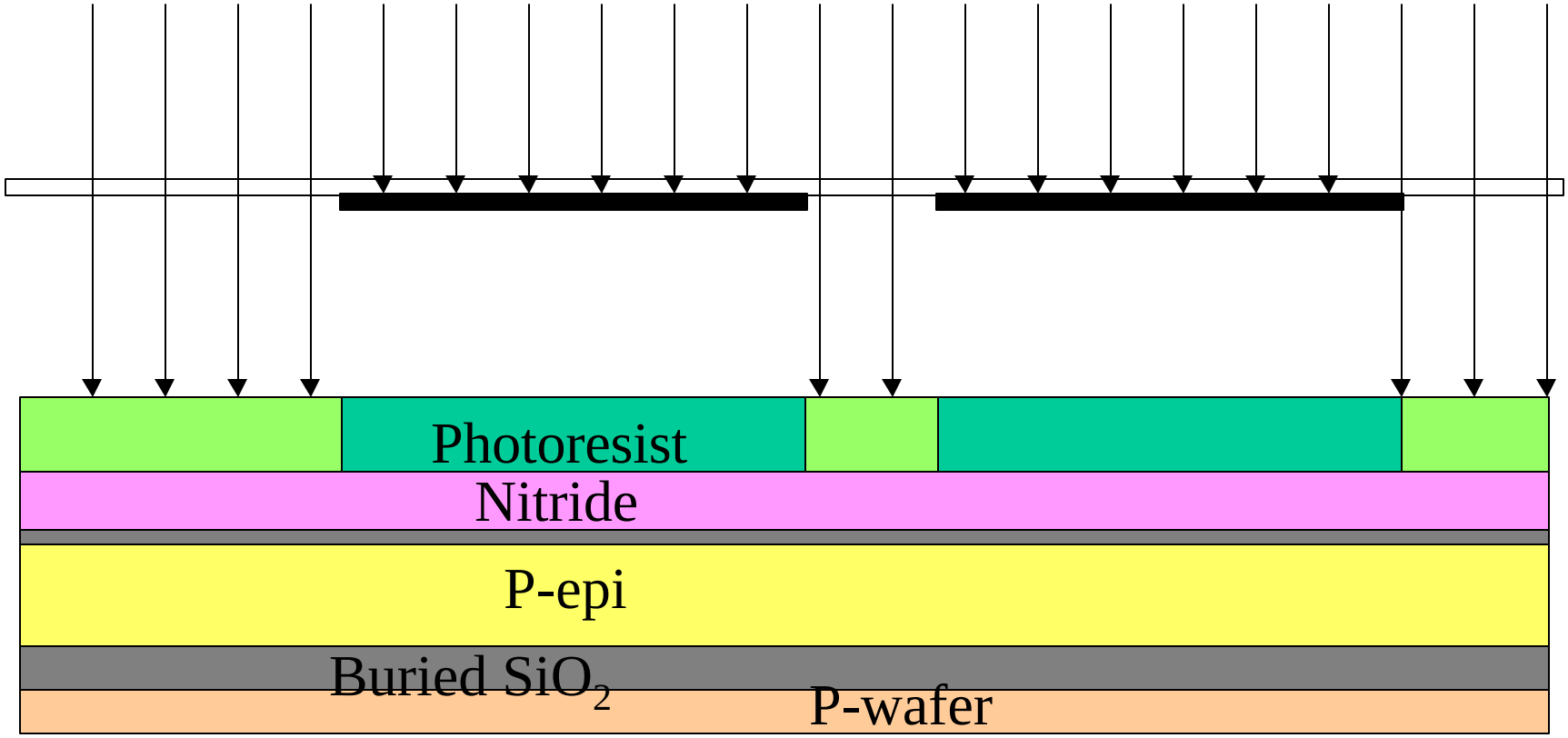
Photoresist Coating and Baking



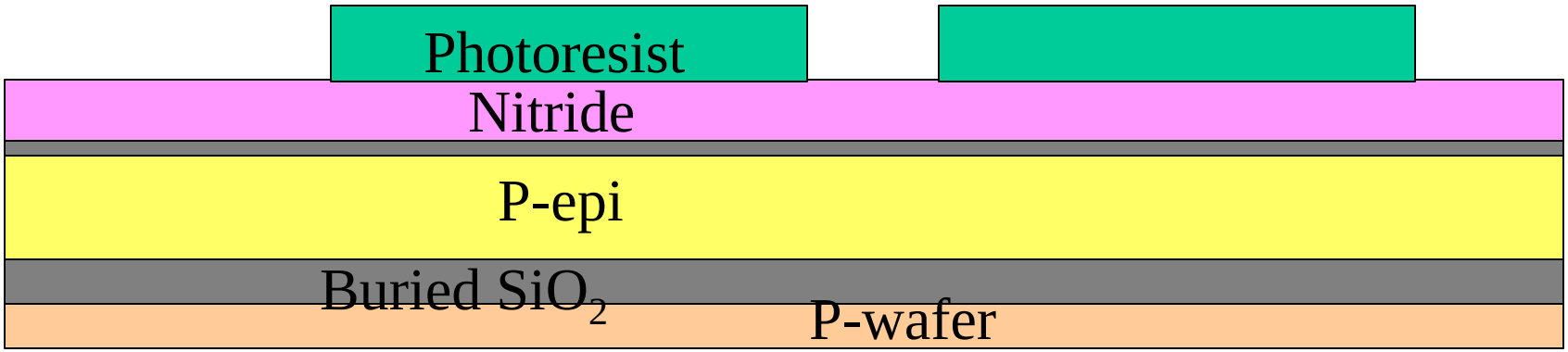
Mask 1: Shallow Trench Isolation



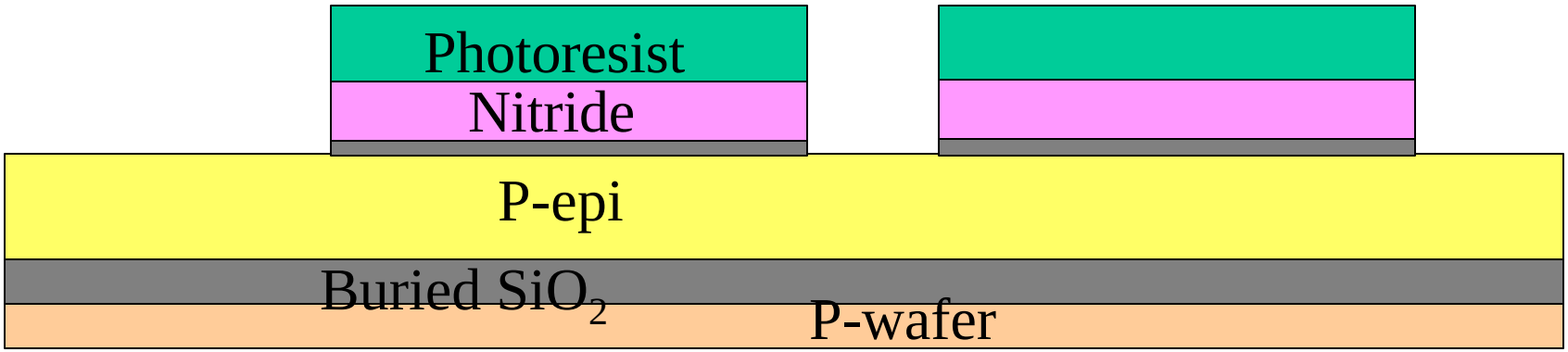
Alignment and Exposure



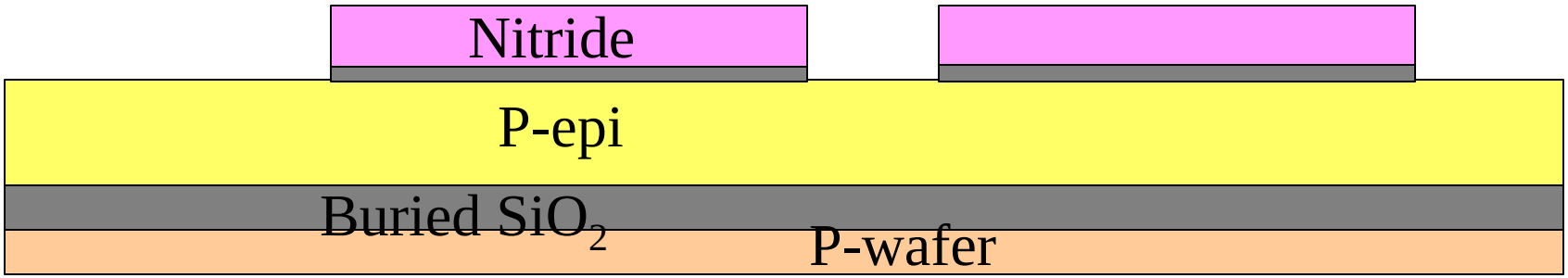
PEB, Development, and Inspection



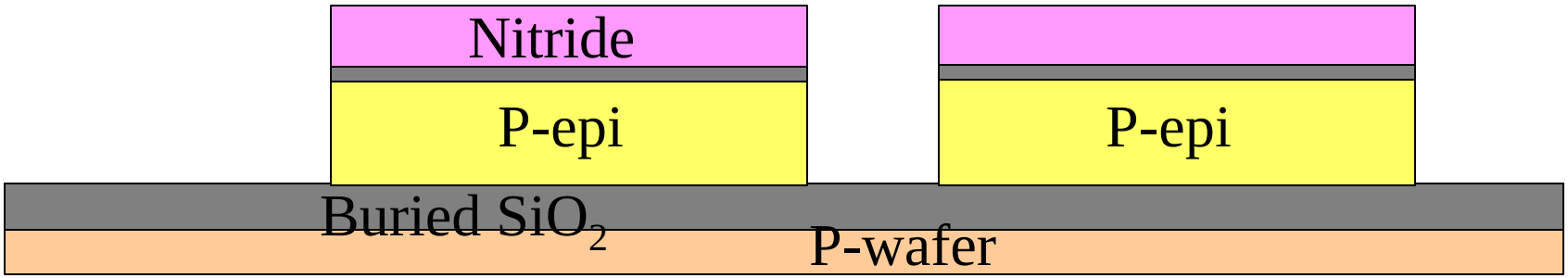
Etch Nitride and Pad Oxide



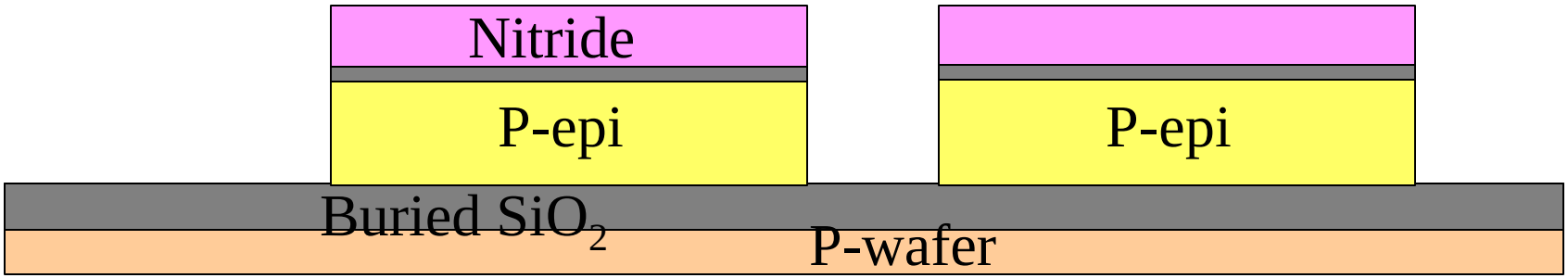
Strip Photoresist



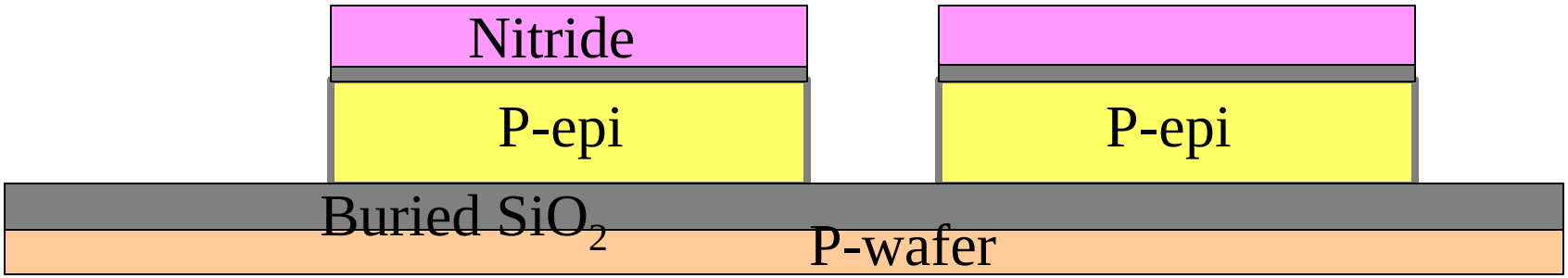
Etch Silicon



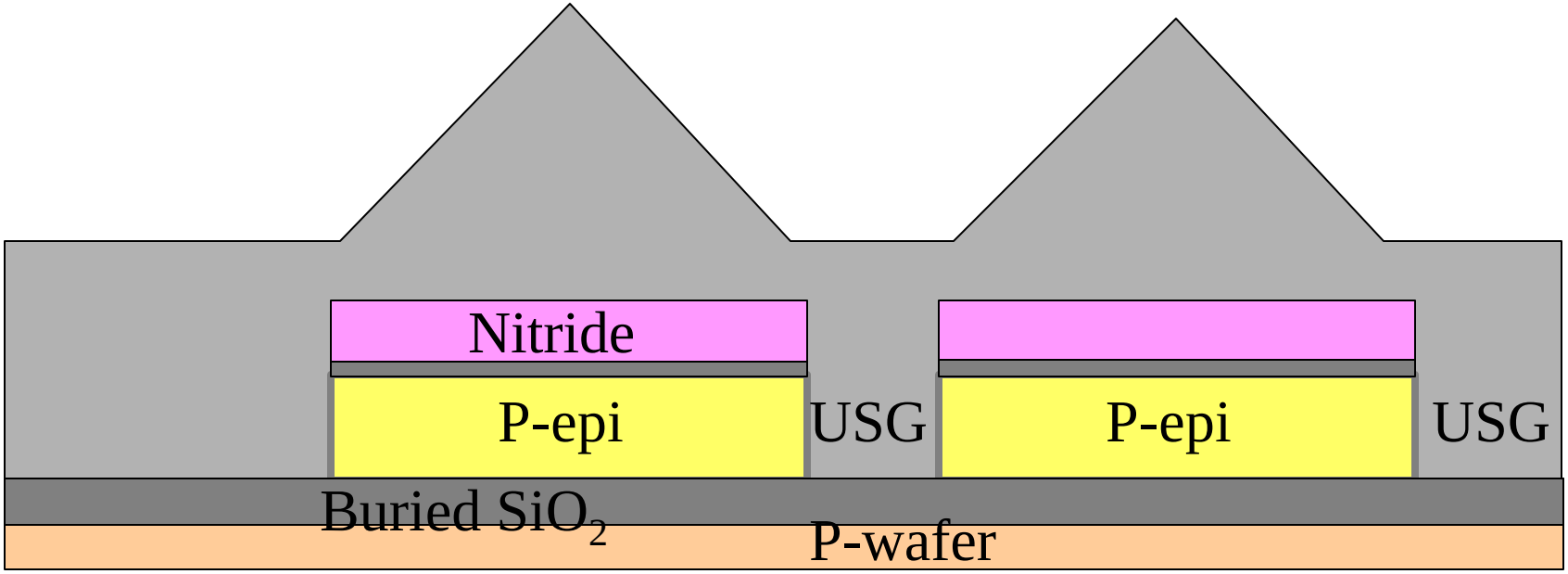
Wafer Clean



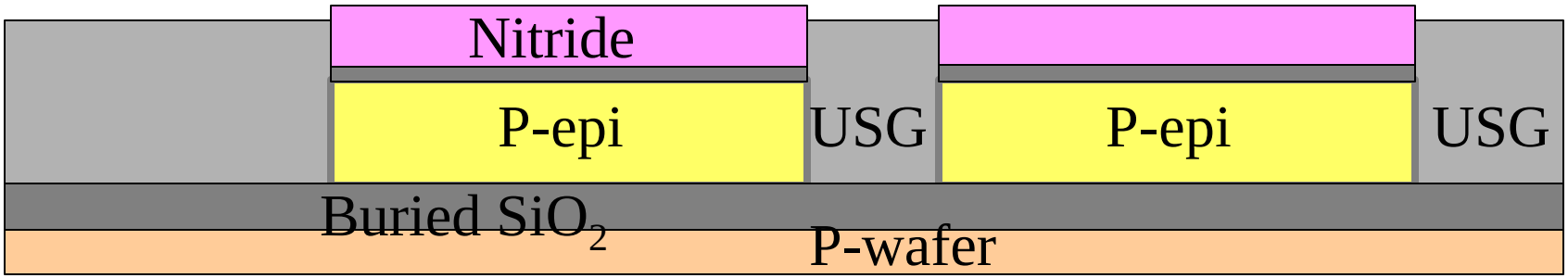
Oxidation, Barrier Oxide



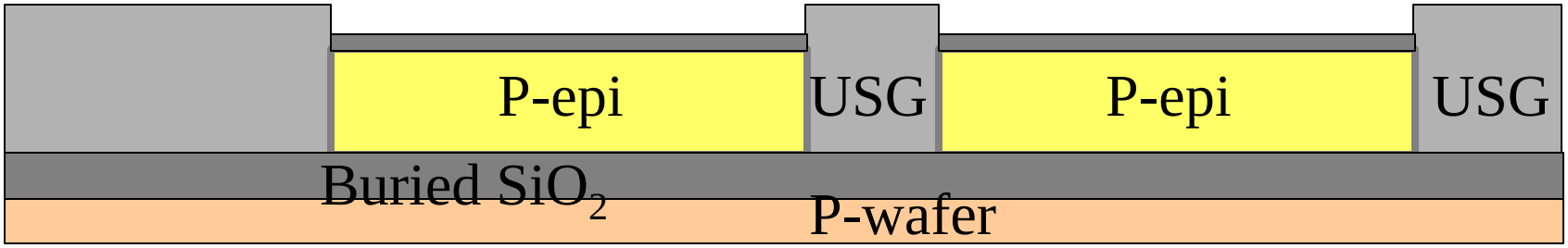
HDP CVD USG



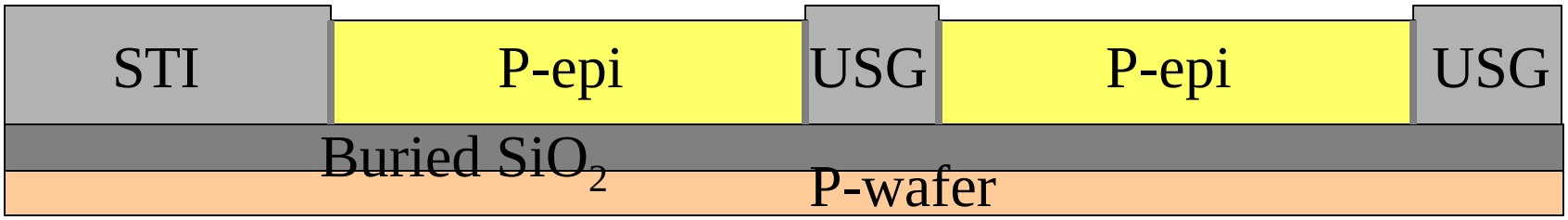
CMP USG



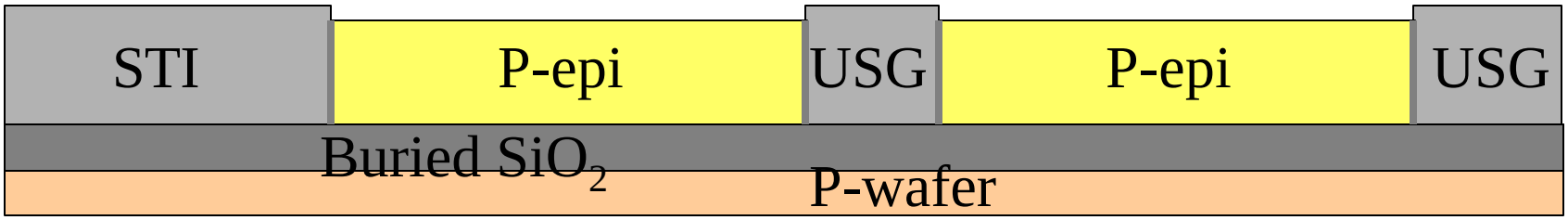
Strip Nitride



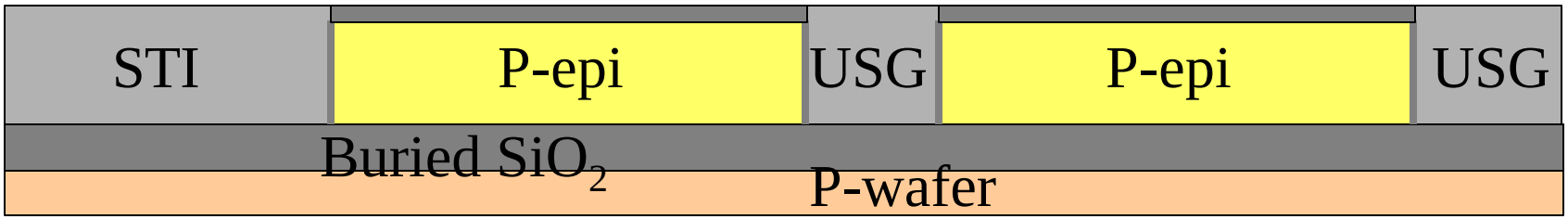
Strip Pad Oxide



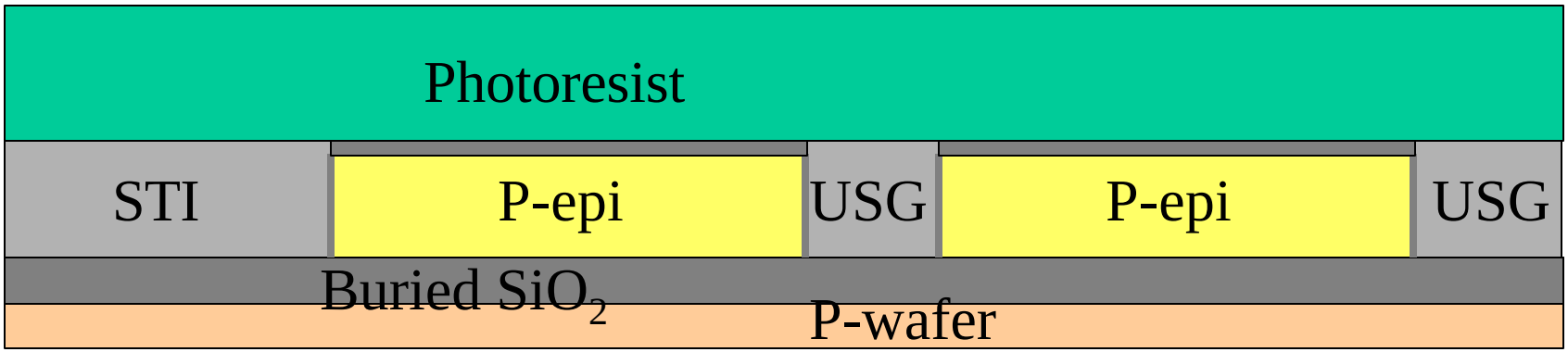
Wafer Clean



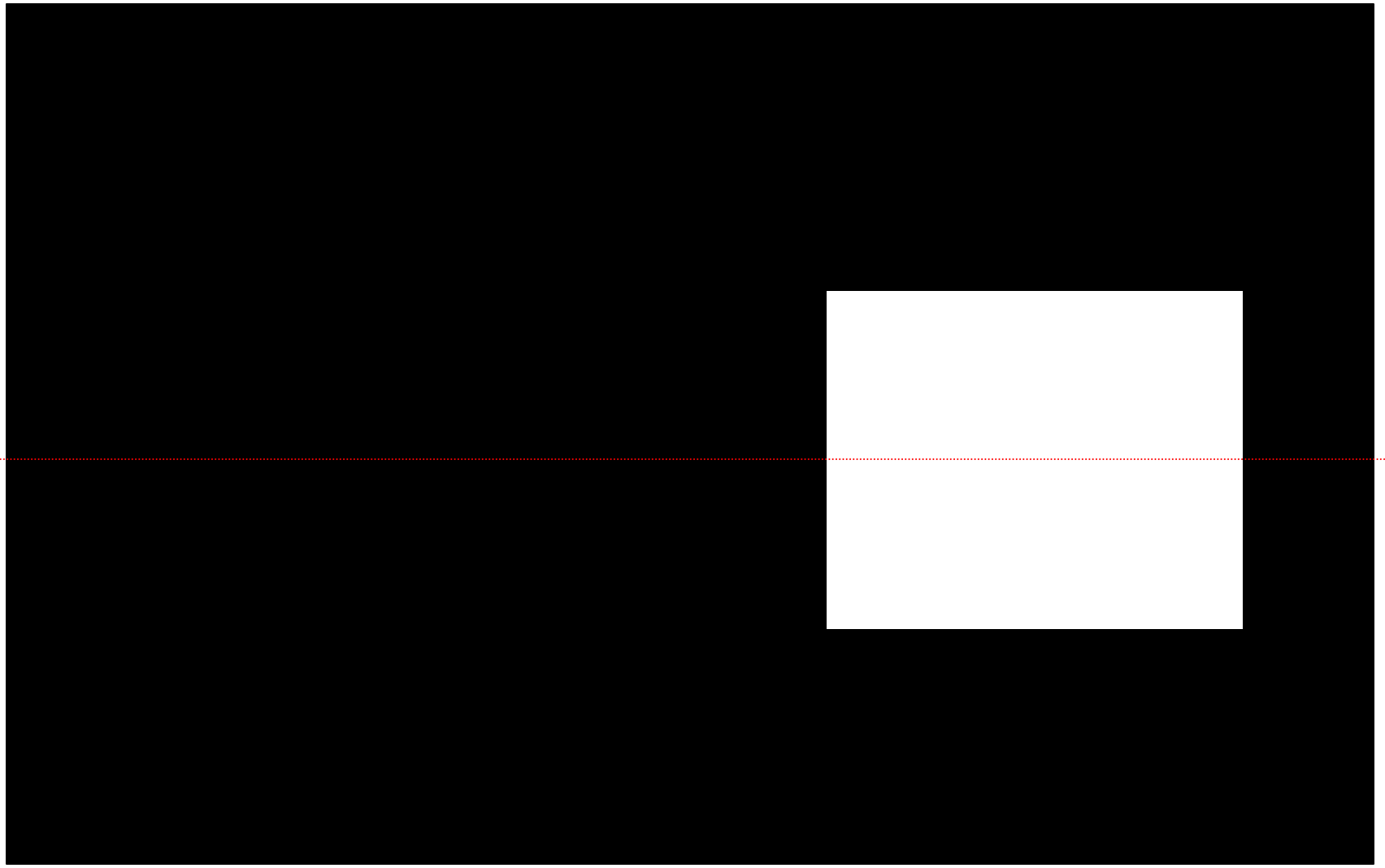
Oxidation, Sacrificial Oxide



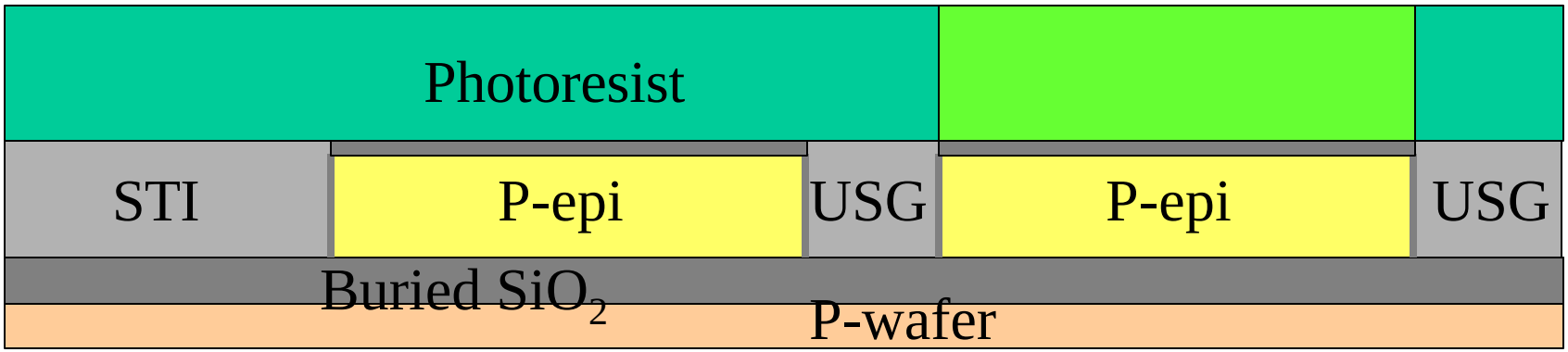
Photoresist Coating and Baking



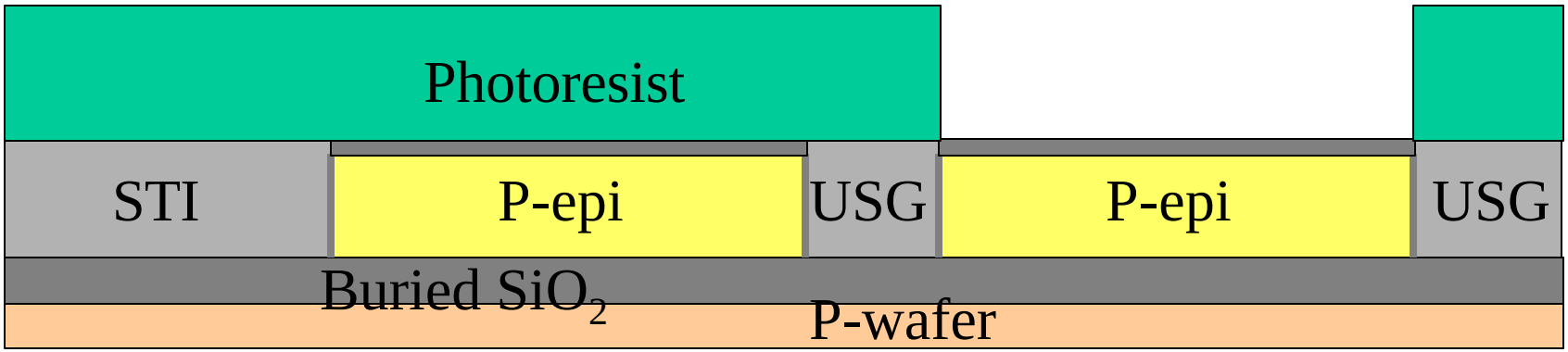
Mask 2: N-well



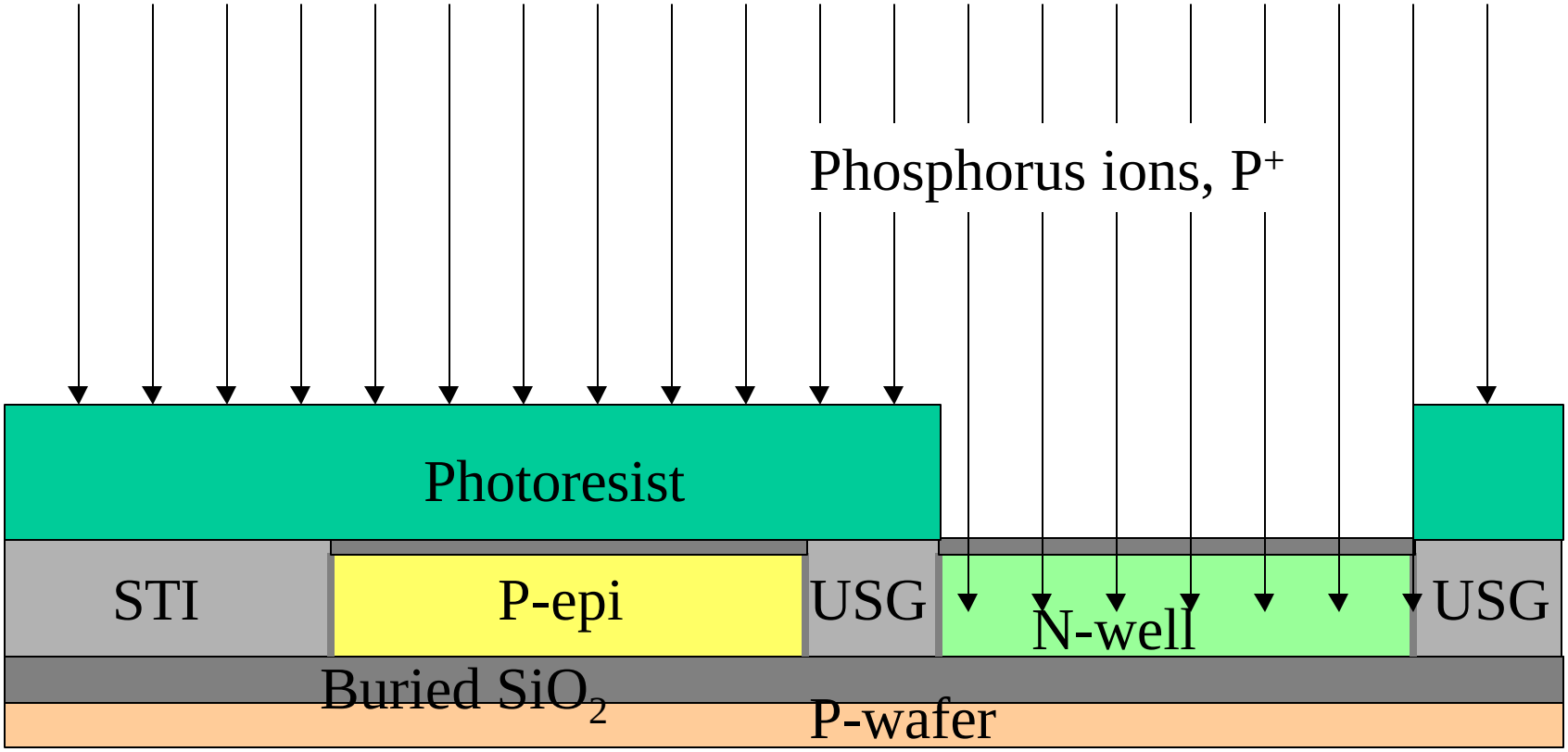
Alignment and Exposure



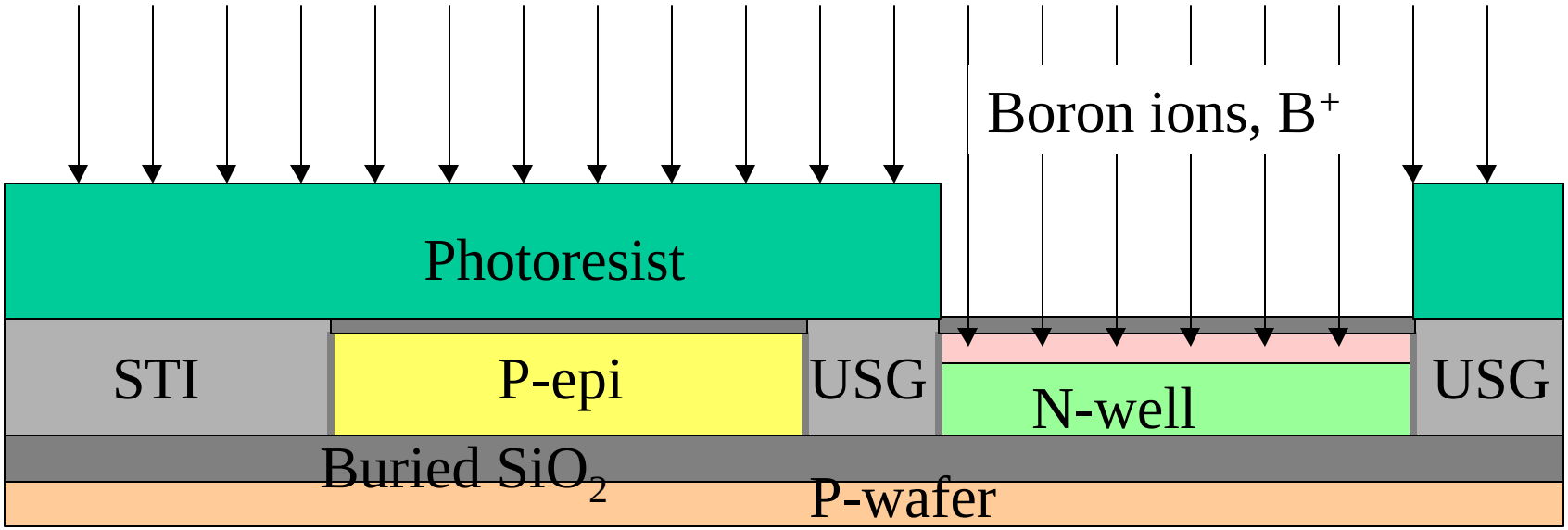
PEB, Development, and Inspection



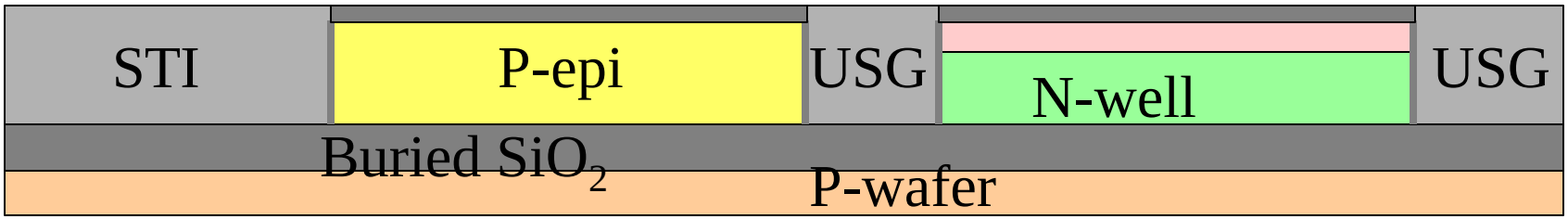
N-well Implantations



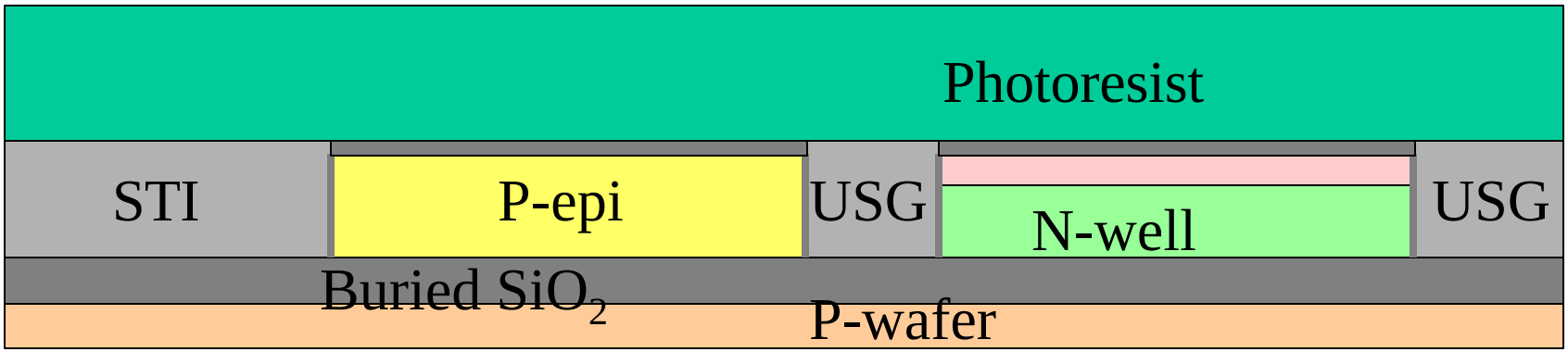
PMOS V_T Adjust Implantation



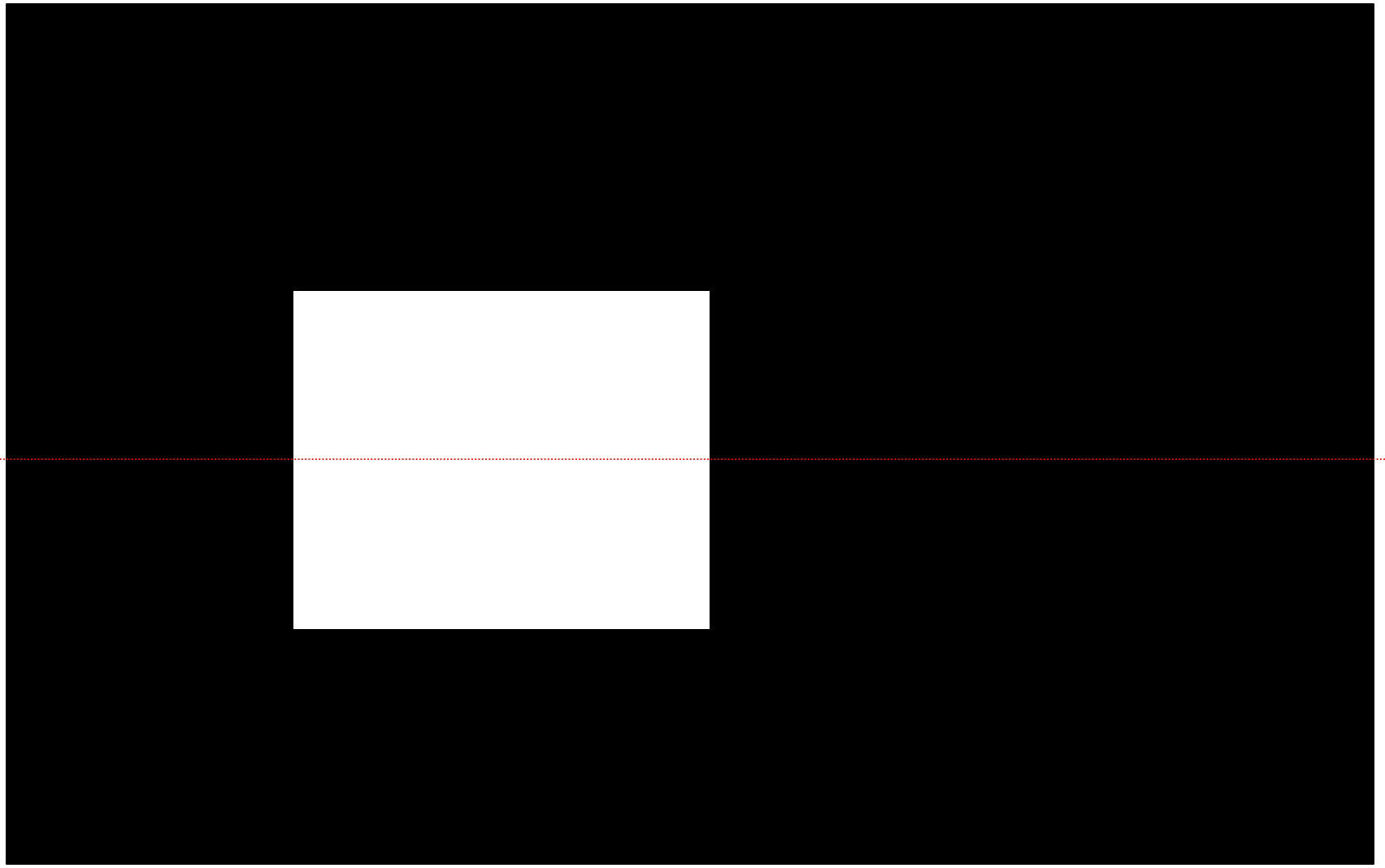
Strip Photoresist



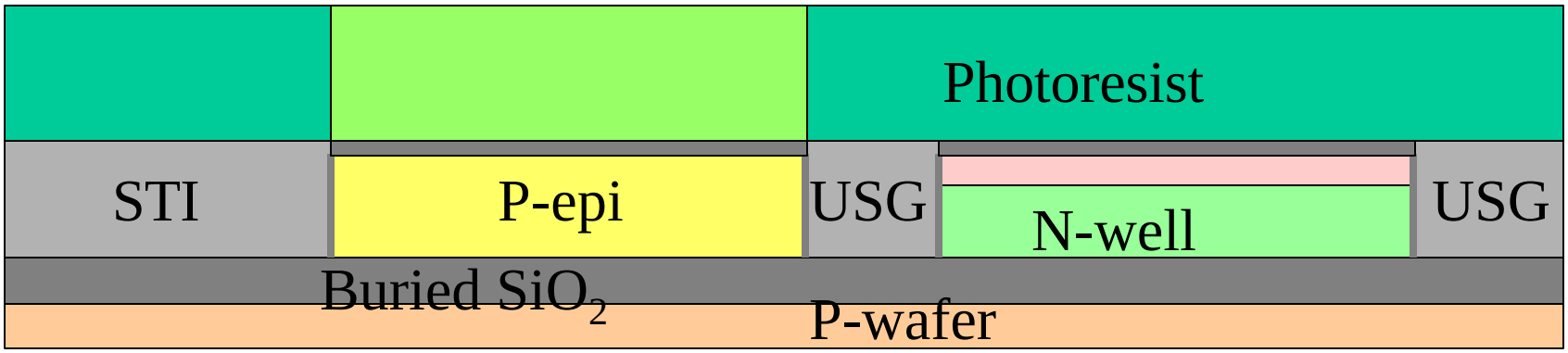
Photoresist Coating and Baking



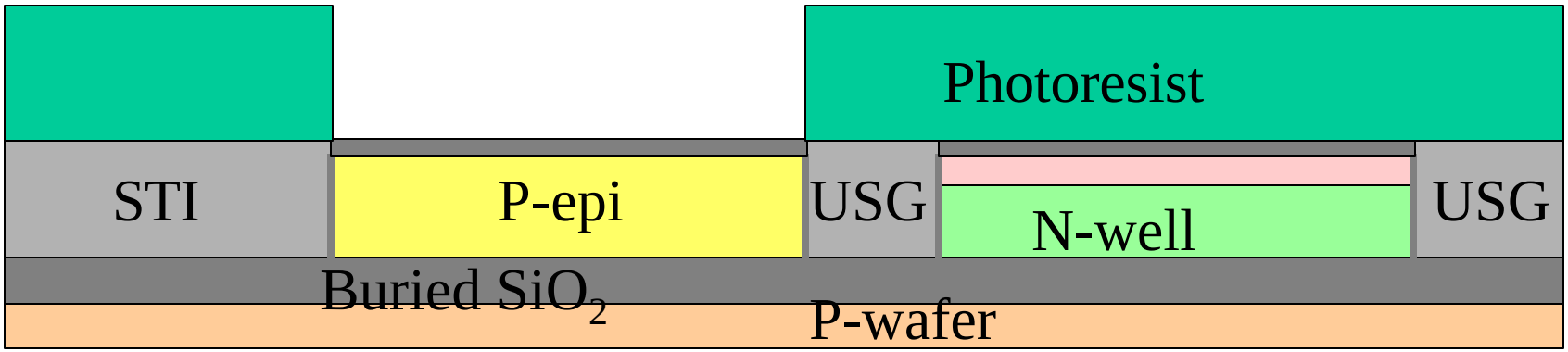
Mask 3: P-well



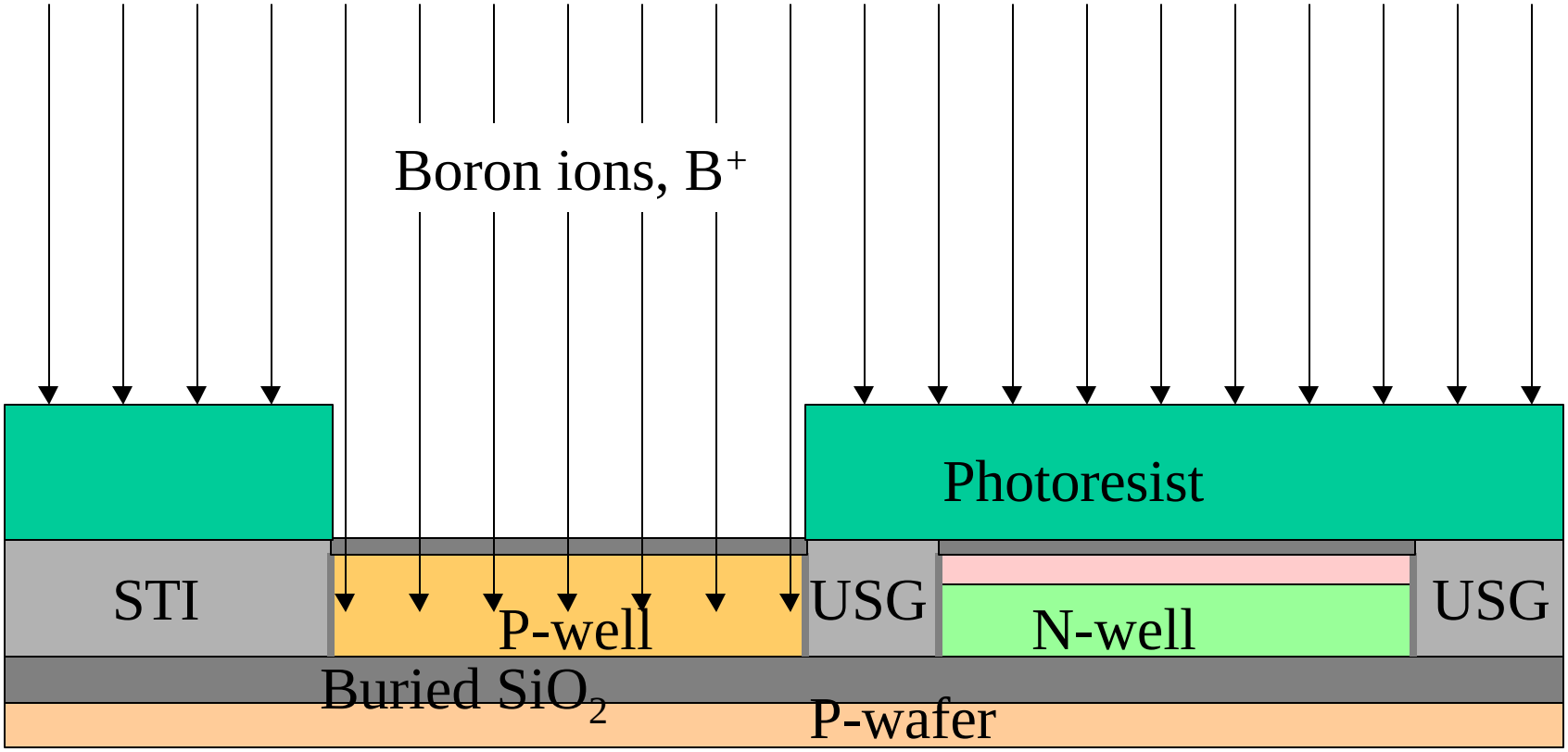
Alignment and Exposure



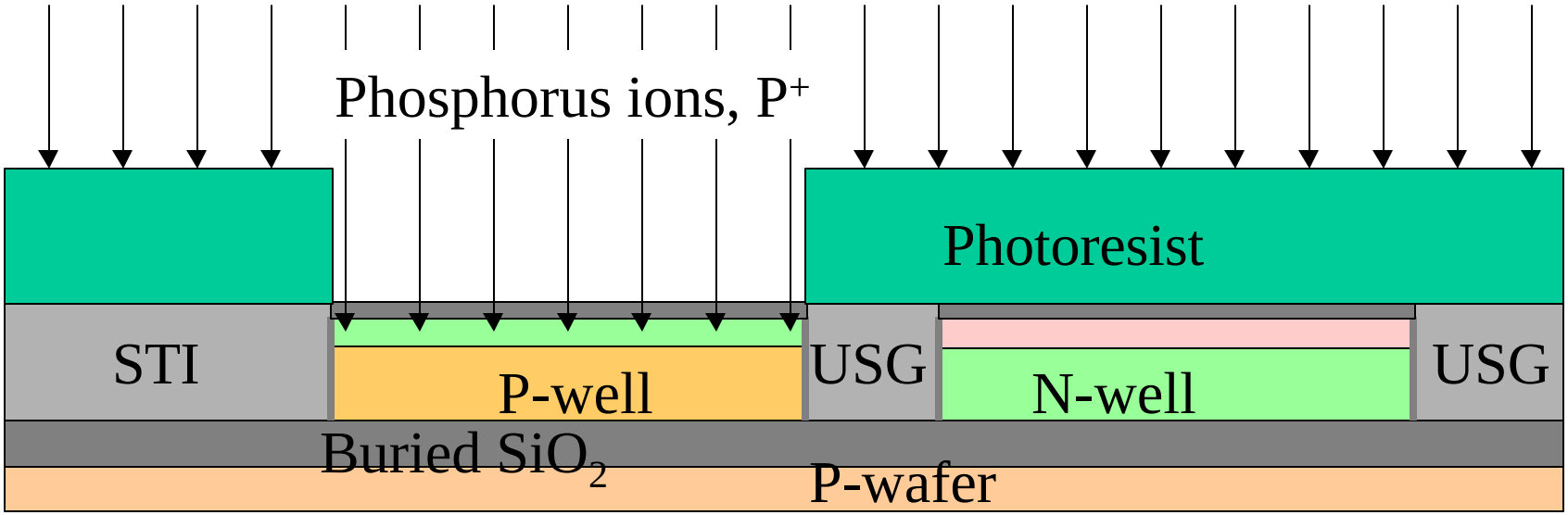
PEB, Development, and Inspection



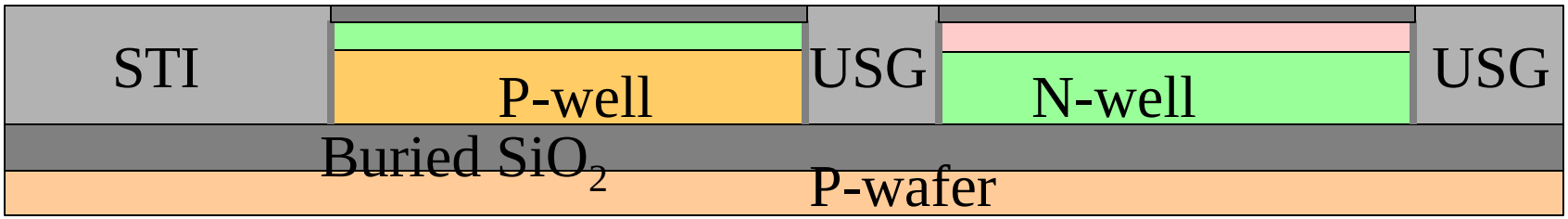
P-well Implantations



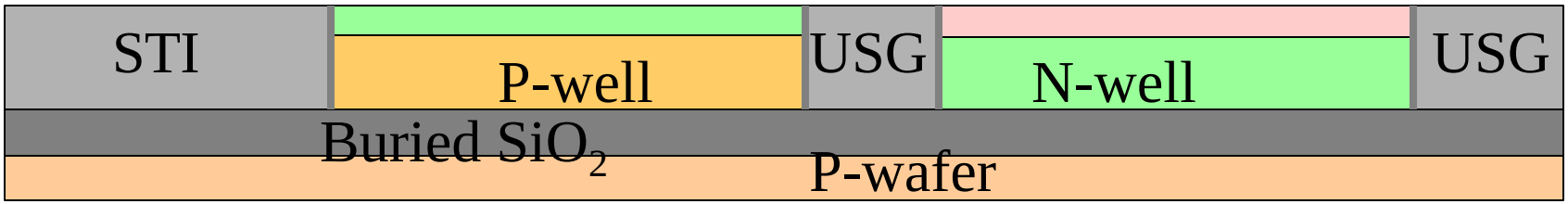
NMOS V_T Adjust Implantation



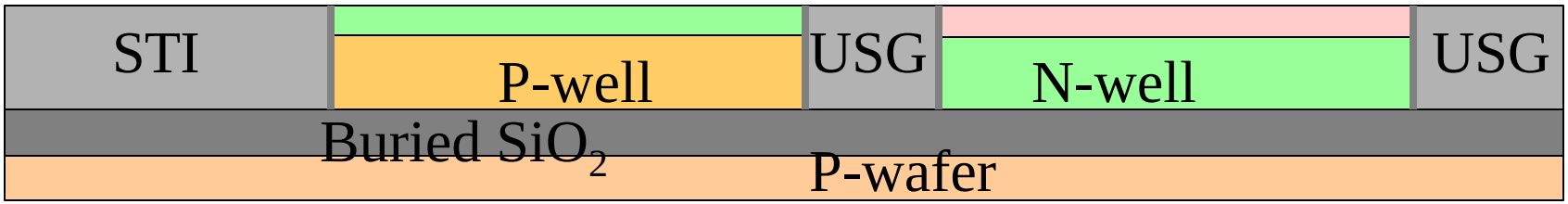
Strip Photoresist



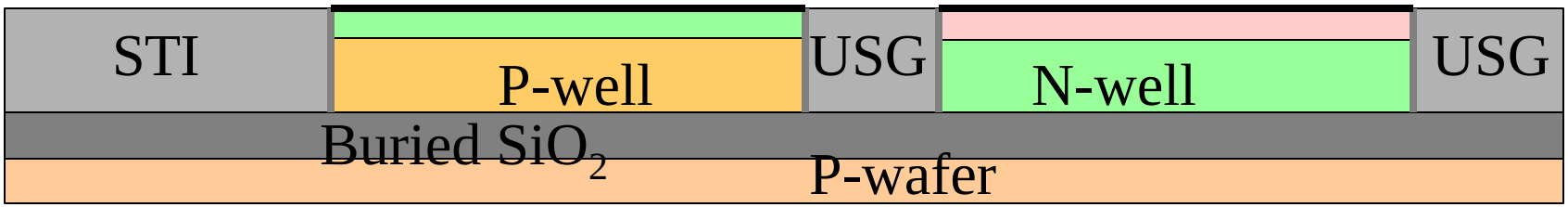
Strip Sacrificial Oxide



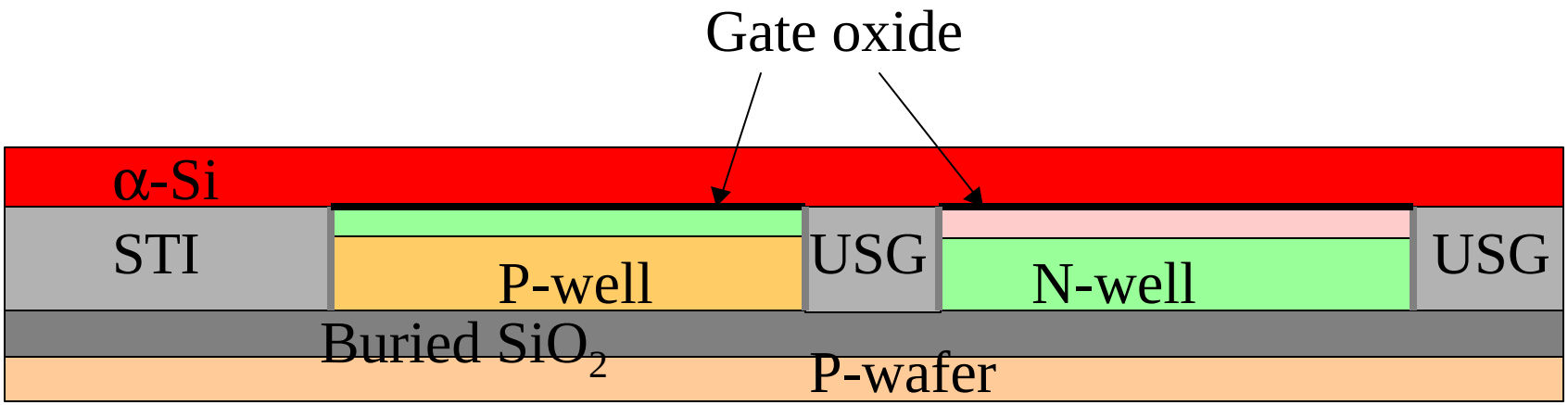
Wafer Clean



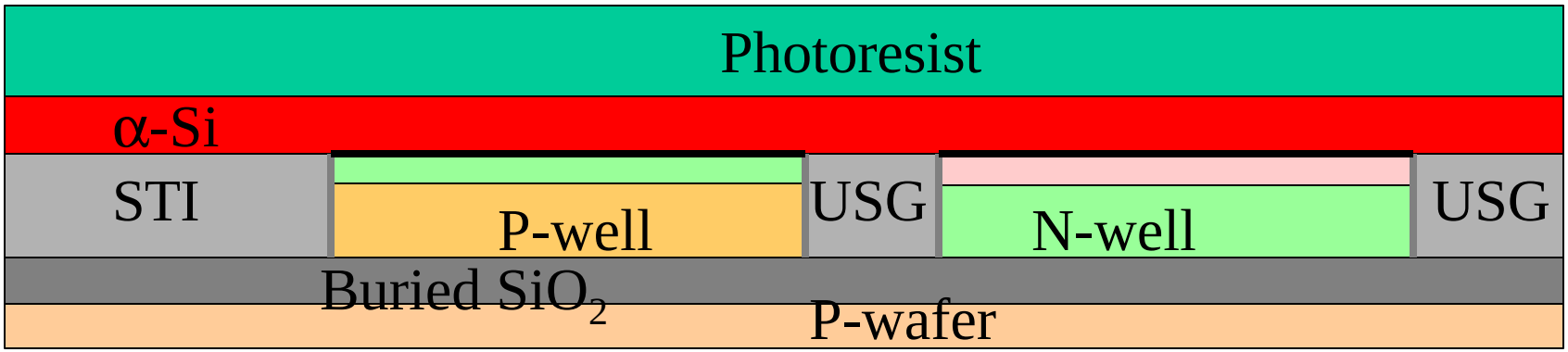
Gate Oxidation



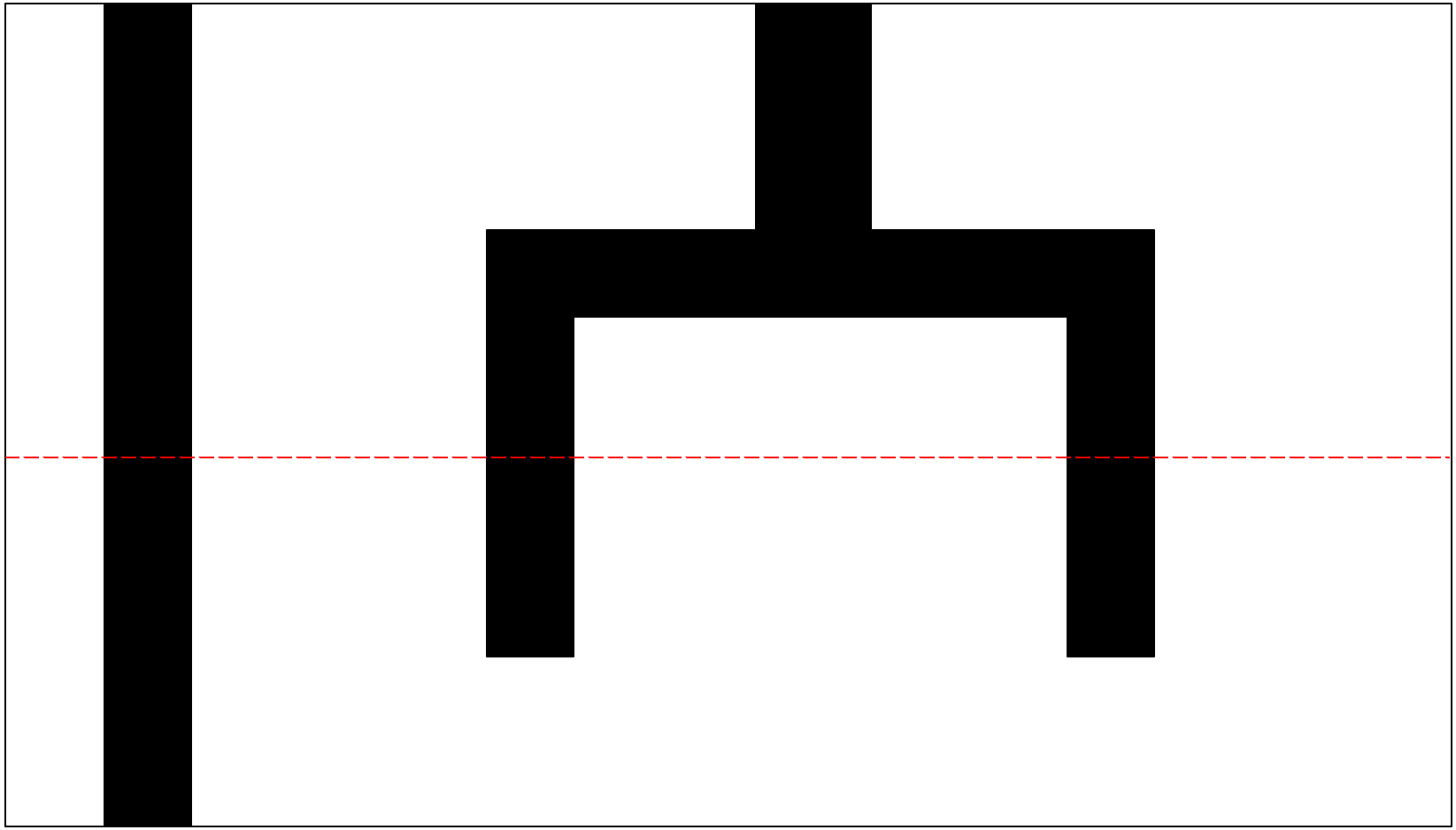
LPCVD Amorphous Silicon



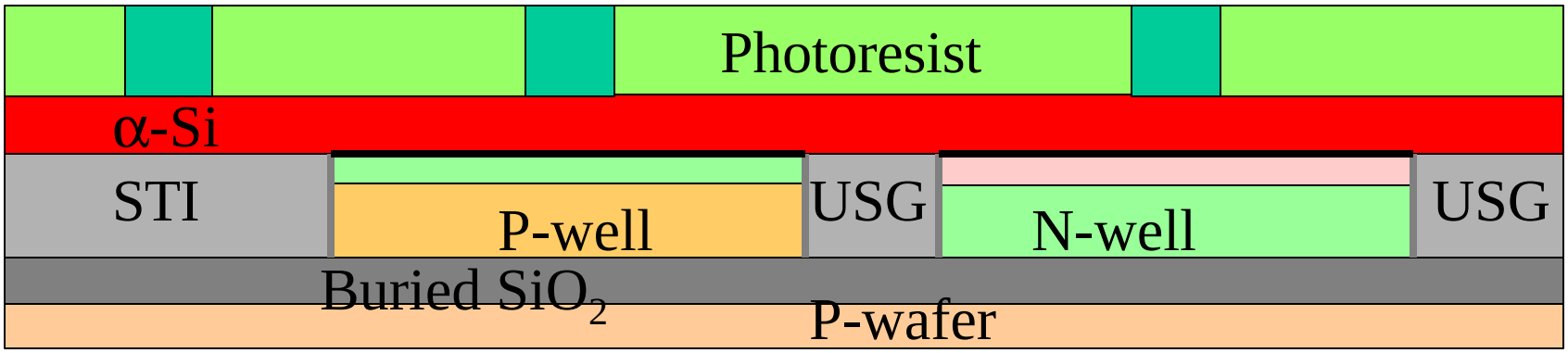
Photoresist Coating and Baking



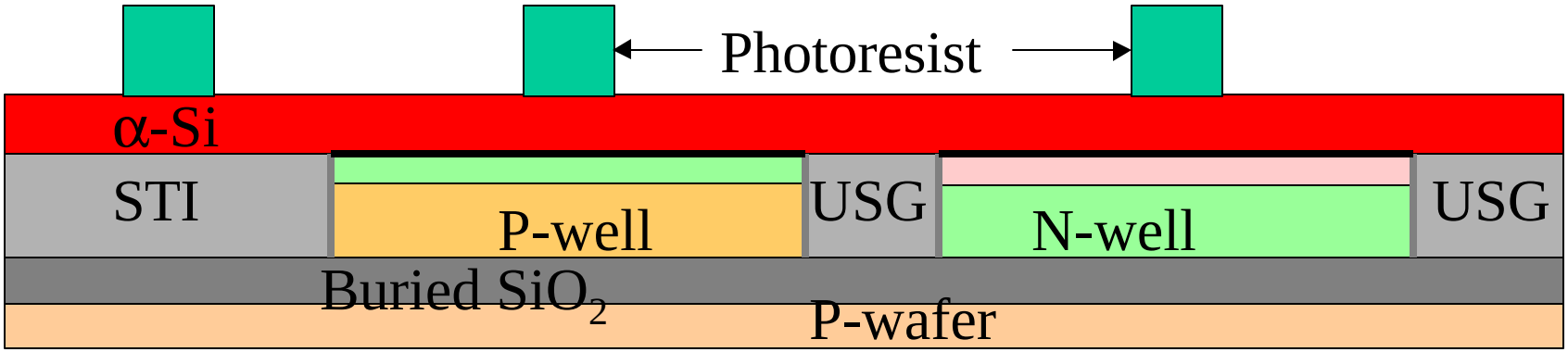
Mask 4, Gate and Local Interconnection



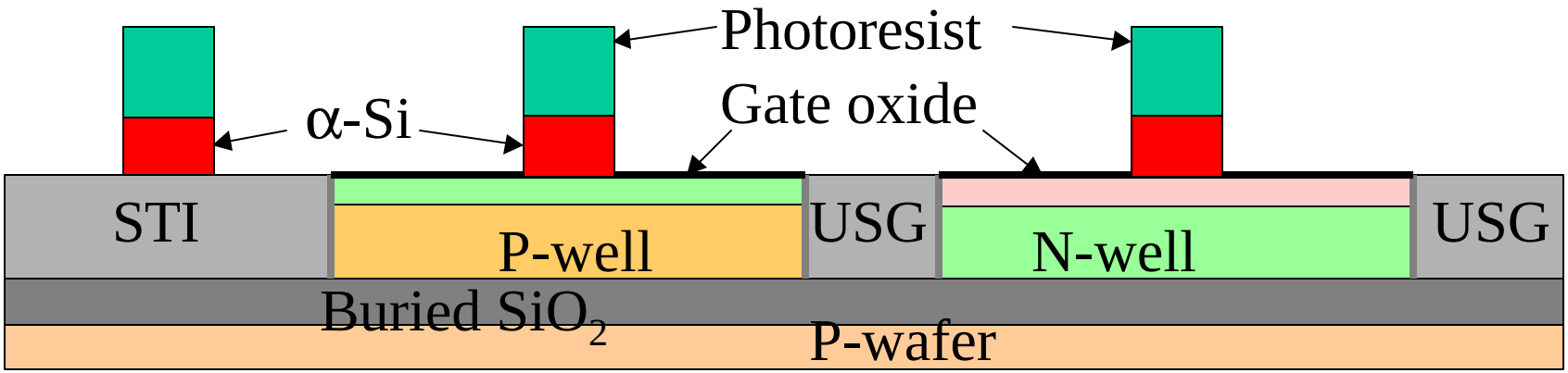
Alignment and Exposure



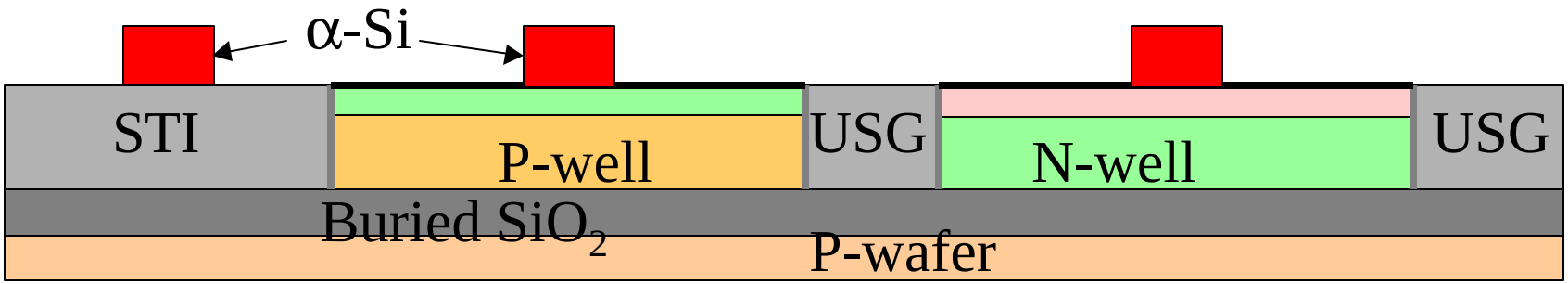
PEB, Development, and Inspection



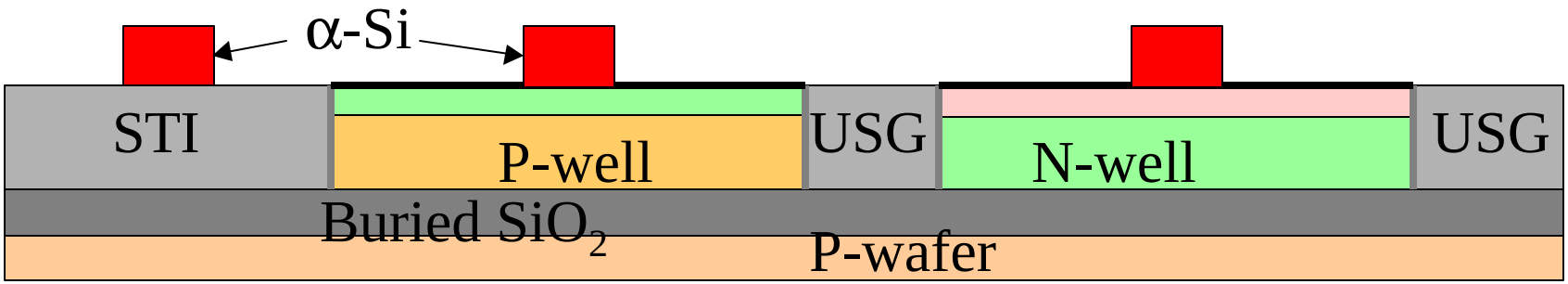
Etch Amorphous Silicon



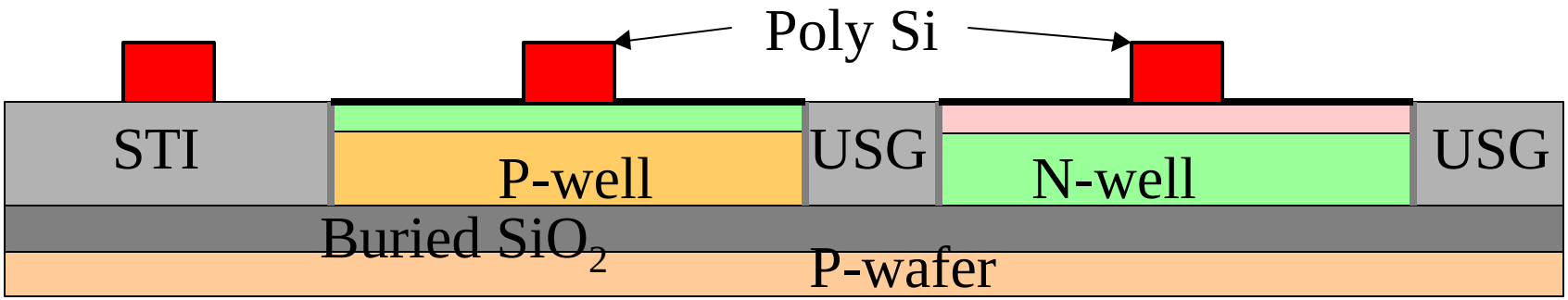
Strip Photoresist



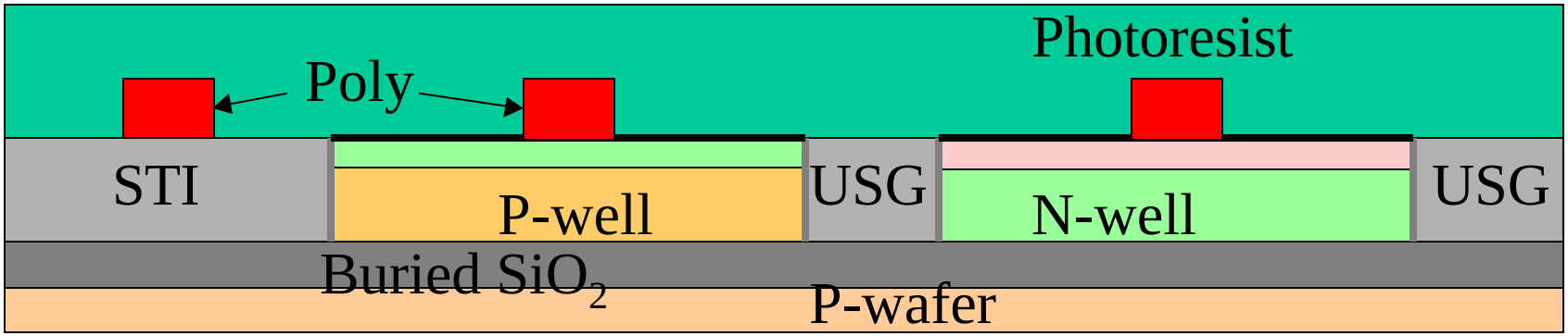
Wafer Clean



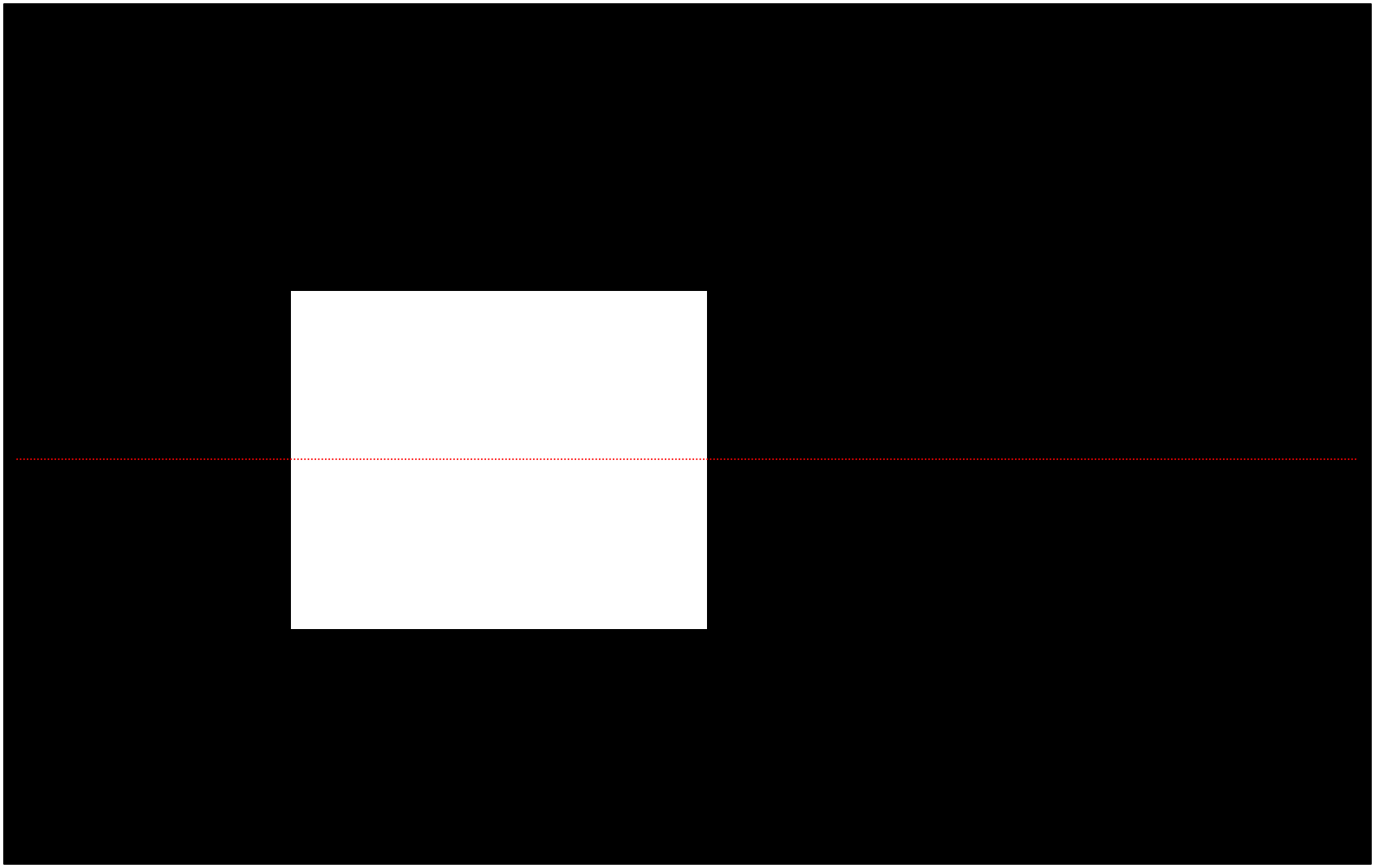
Polysilicon Annealing and Oxidation



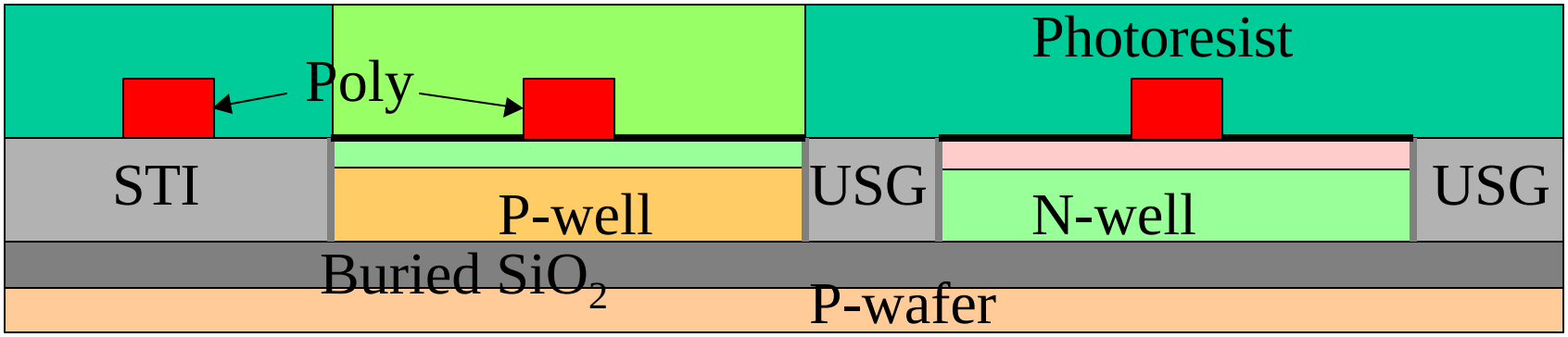
Photoresist Coating and Baking



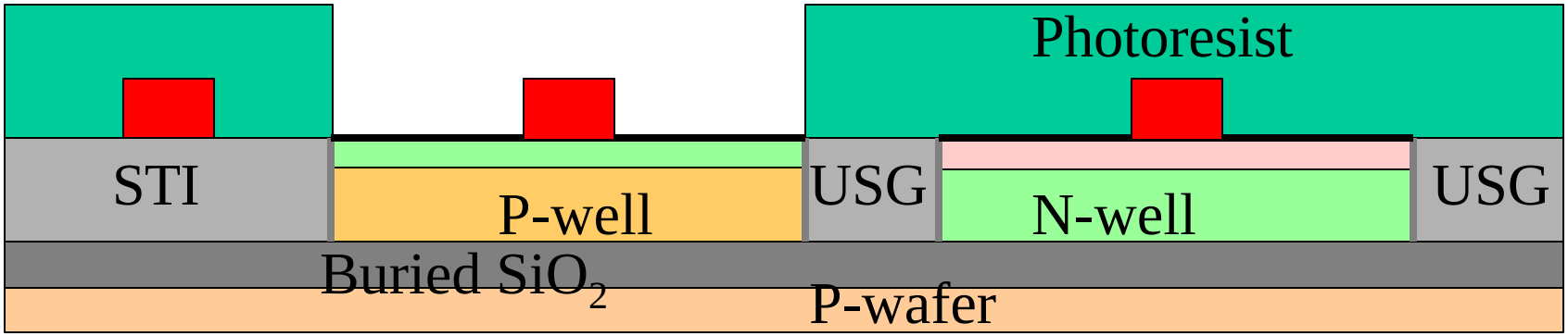
Mask 5, NMOS LDD Implantation



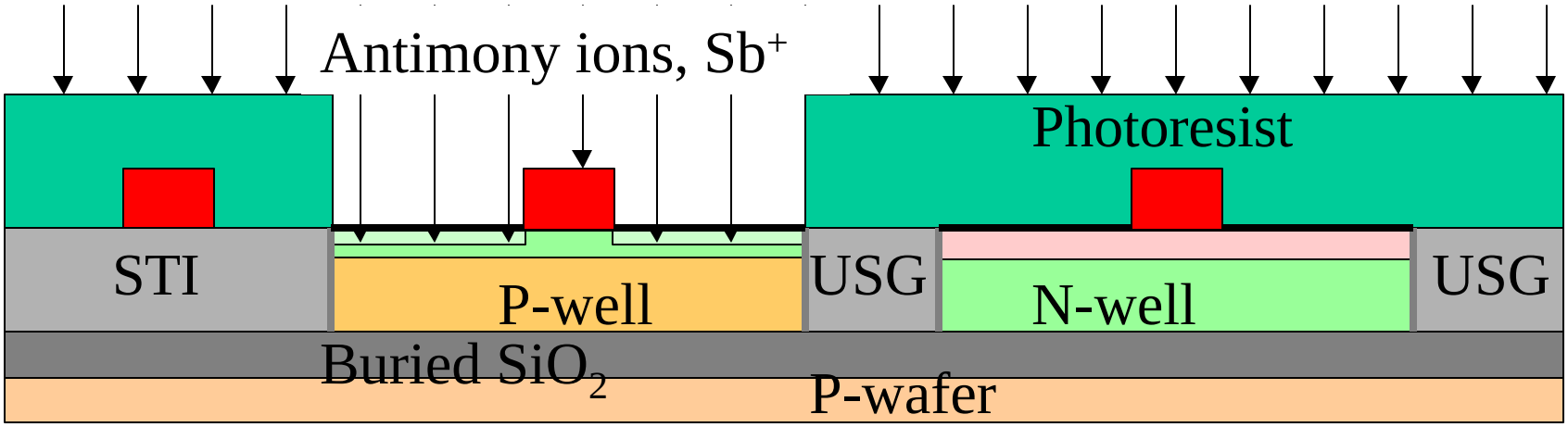
Alignment and Exposure



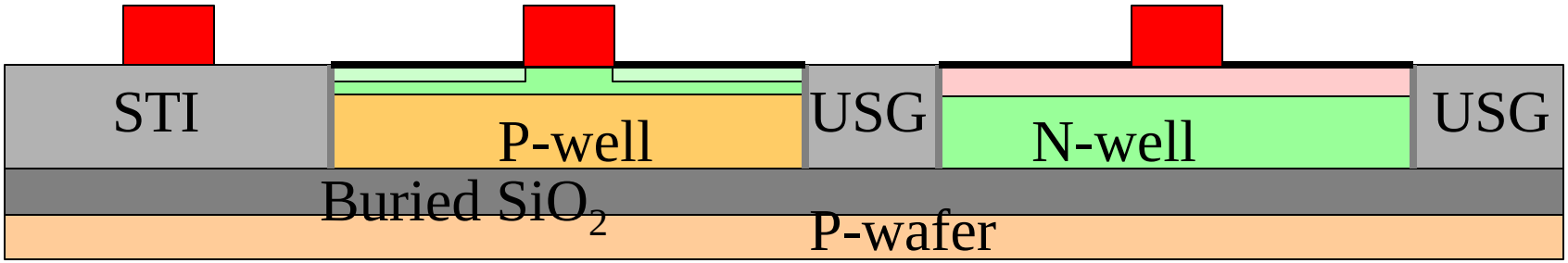
PEB, Development, and Inspection



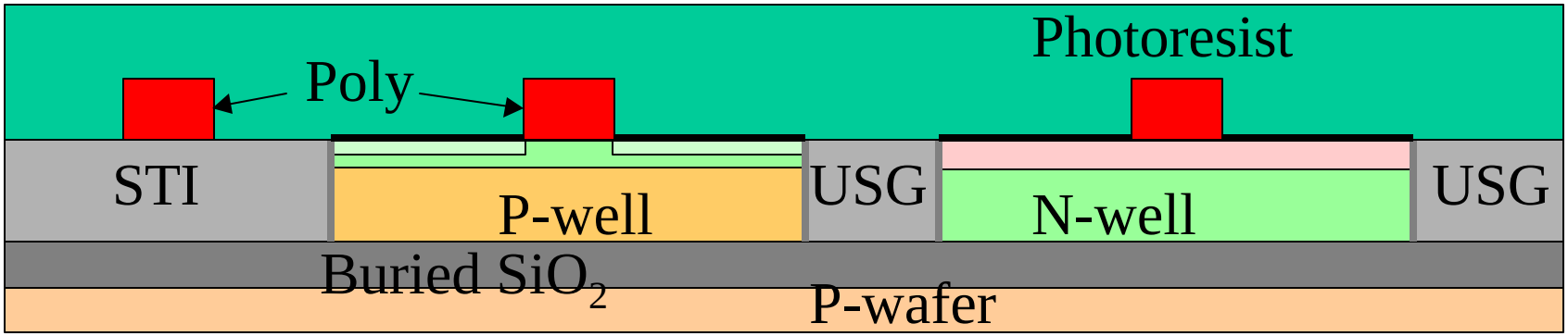
NMOS LDD Implantation



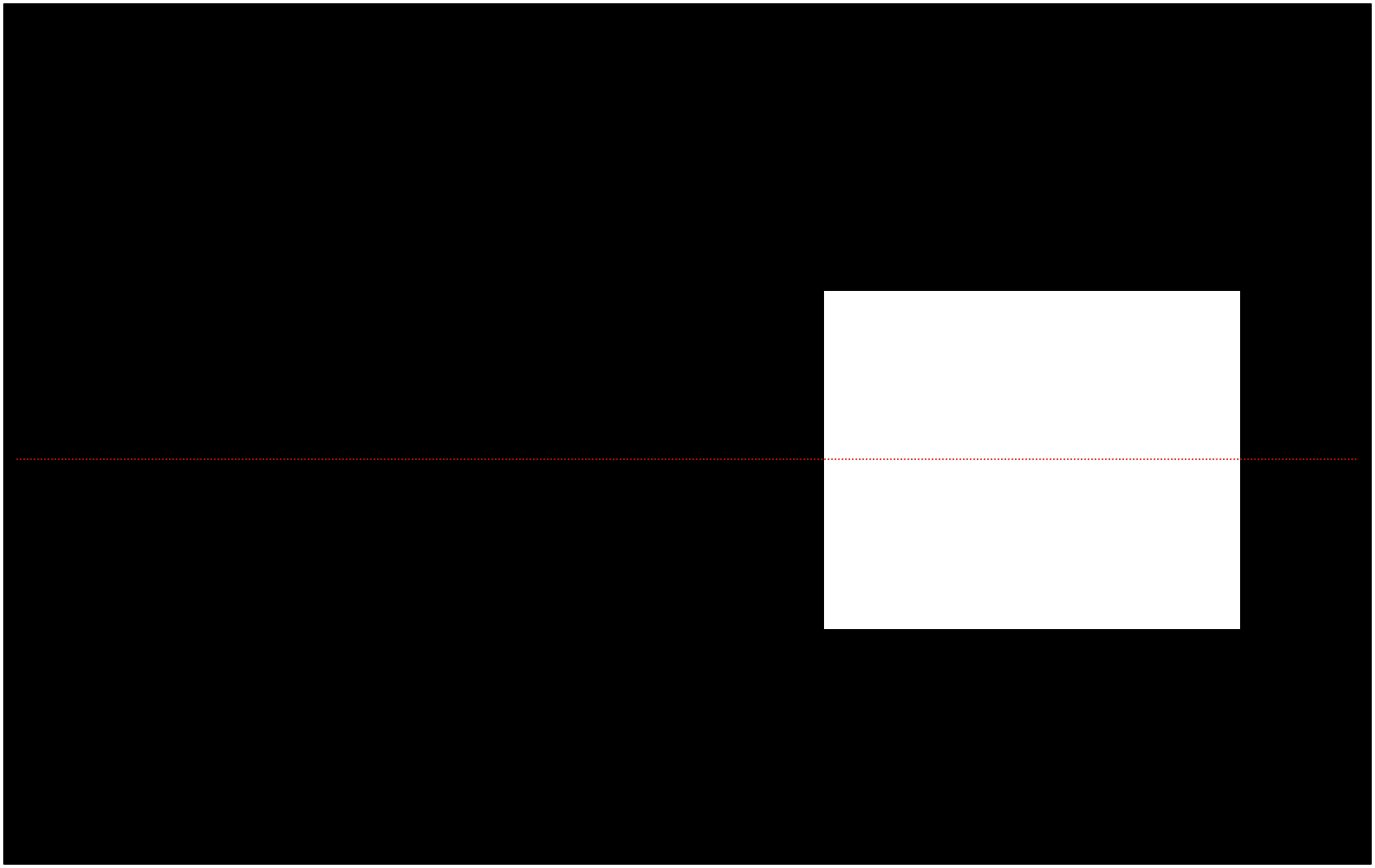
Strip Photoresist



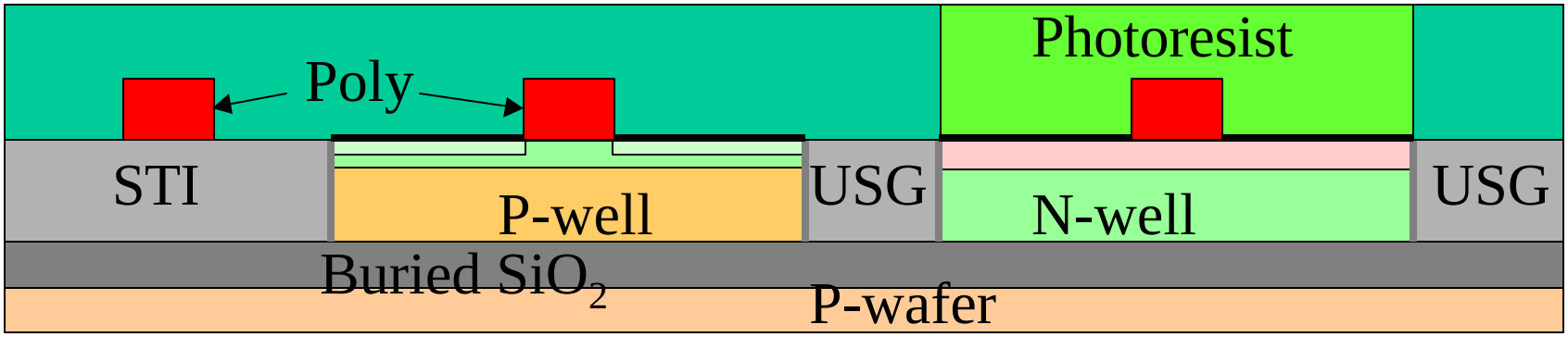
Photoresist Coating and Baking



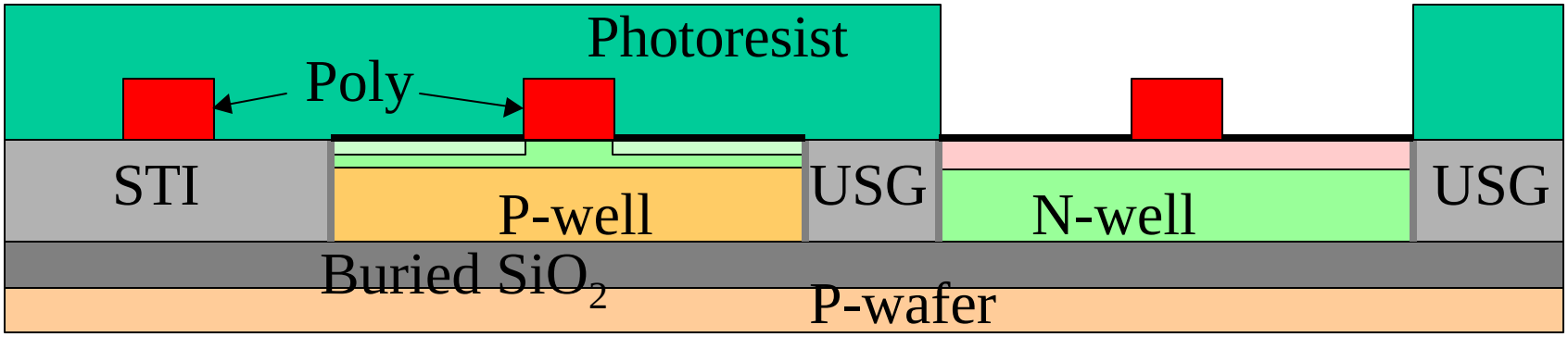
Mask 6: PMOS LDD Implantation



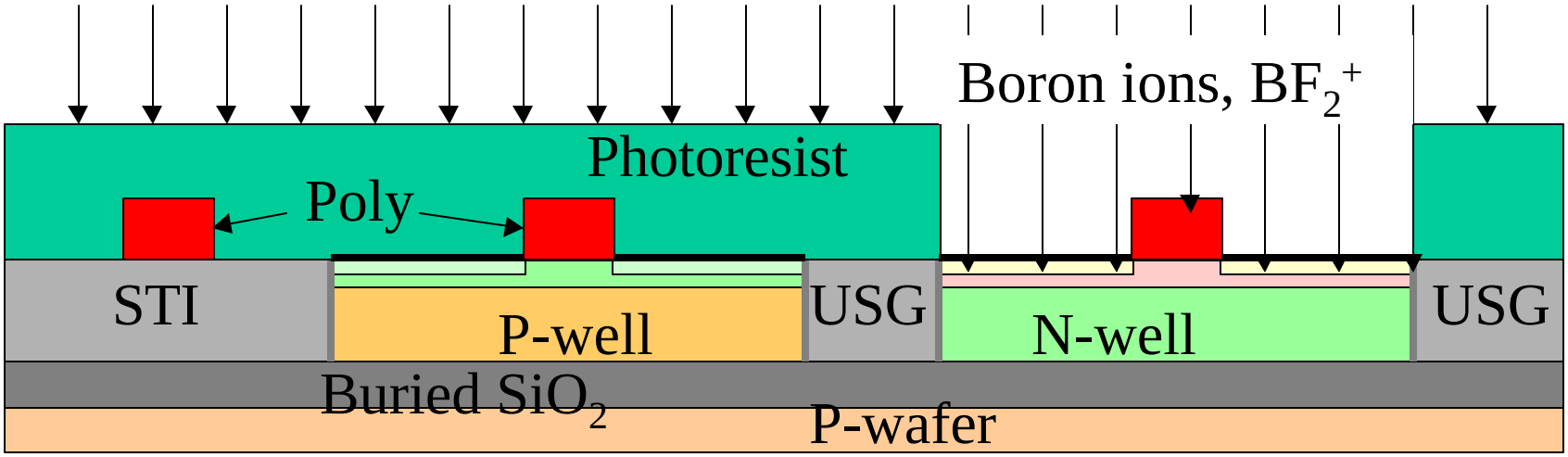
Alignment and Exposure



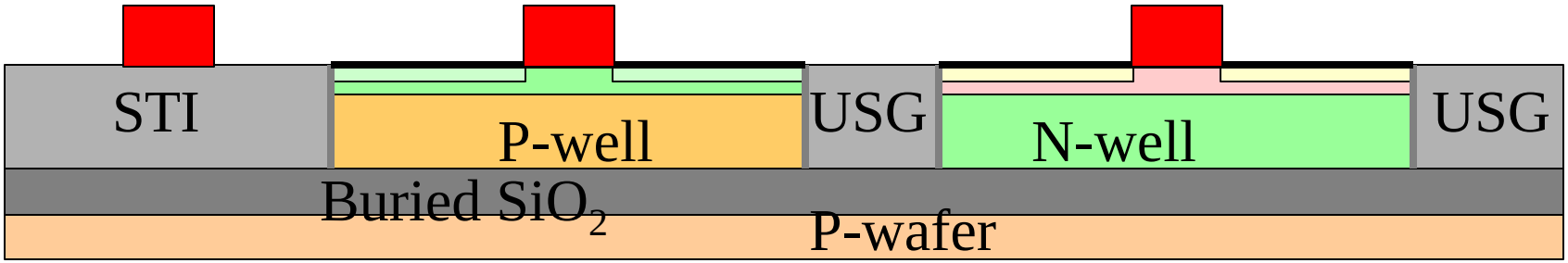
PEB, Development, and Inspection



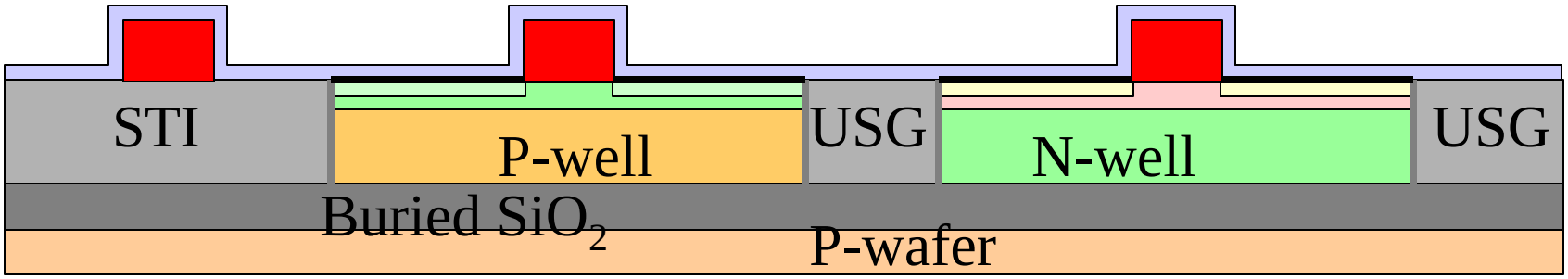
PMOS LDD Implantation



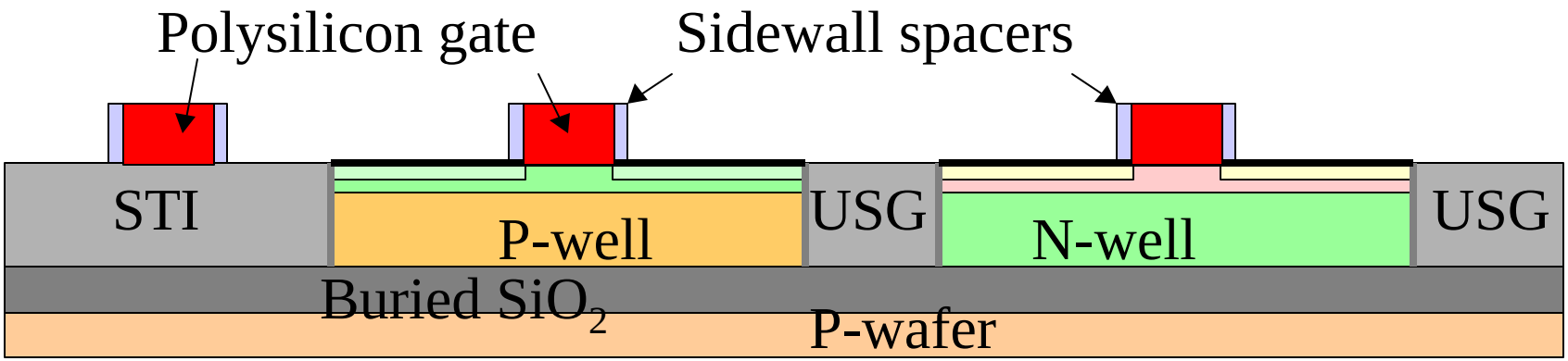
Strip Photoresist



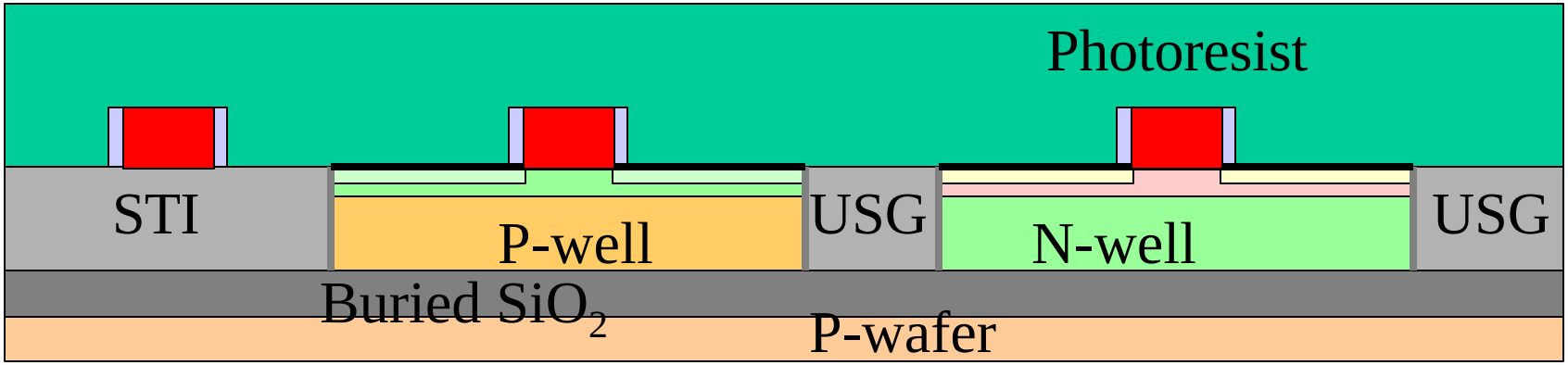
CVD USG, CVD Nitride



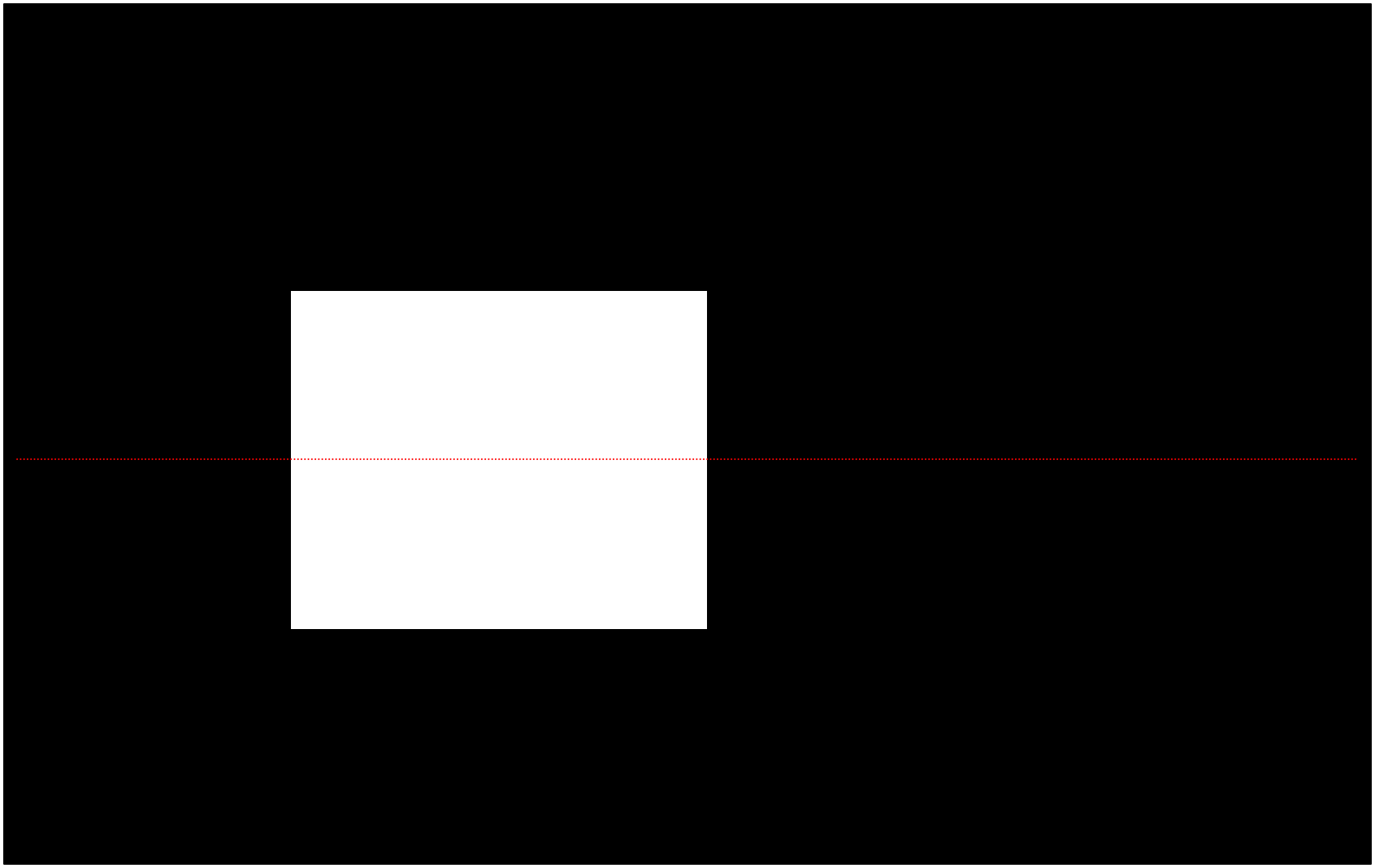
Nitride and USG Etchback



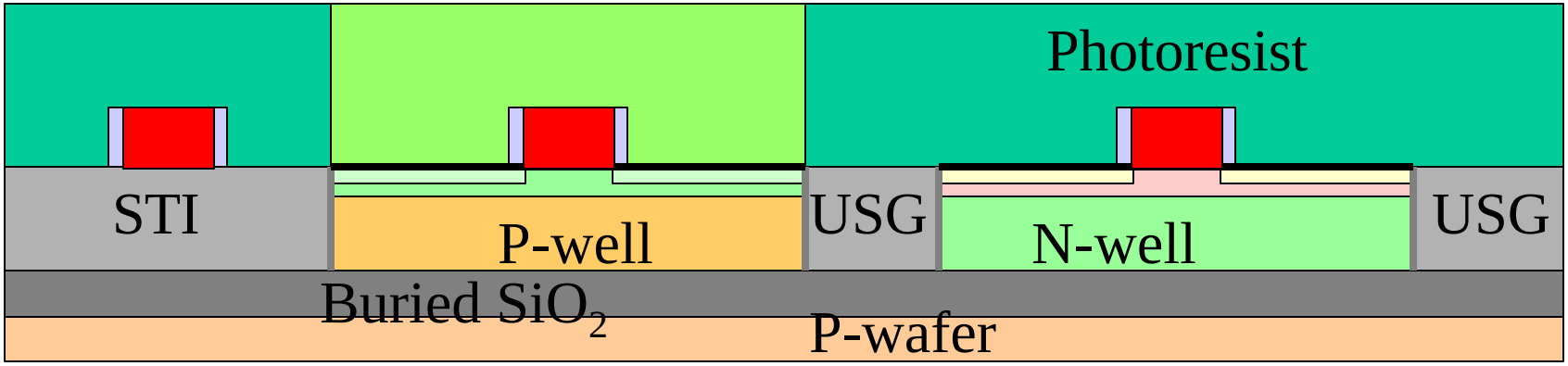
Photoresist Coating and Baking



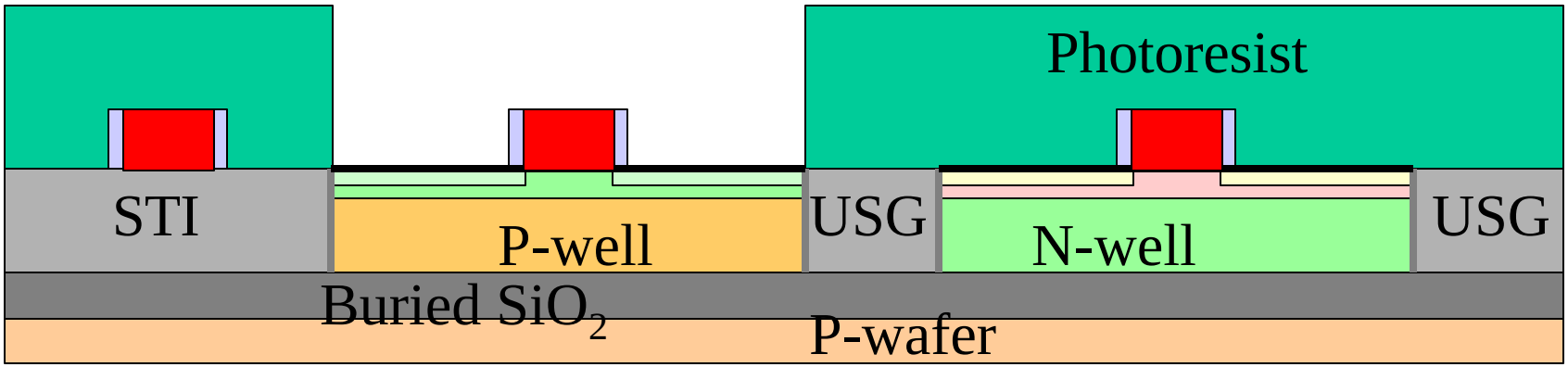
Mask 7, NMOS S/D Implantation



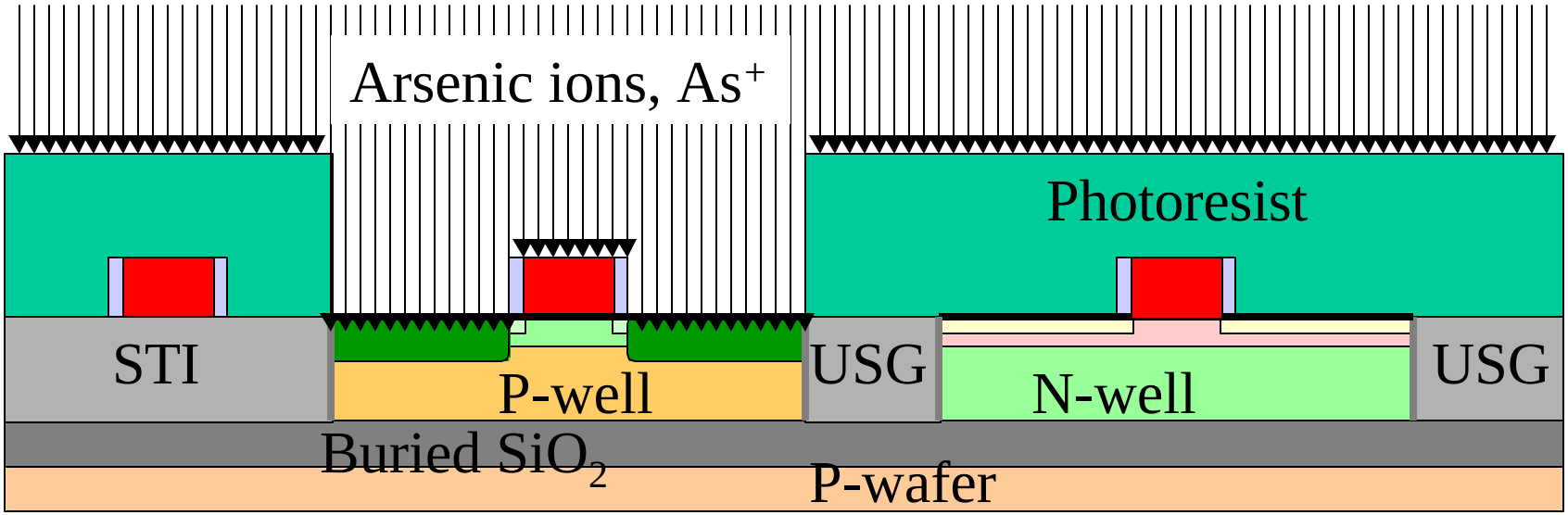
Alignment and Exposure



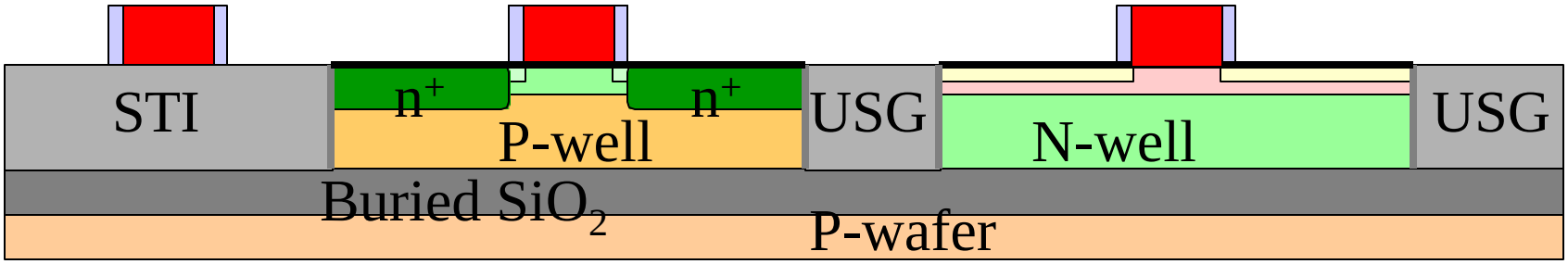
PEB, Development, and Inspection



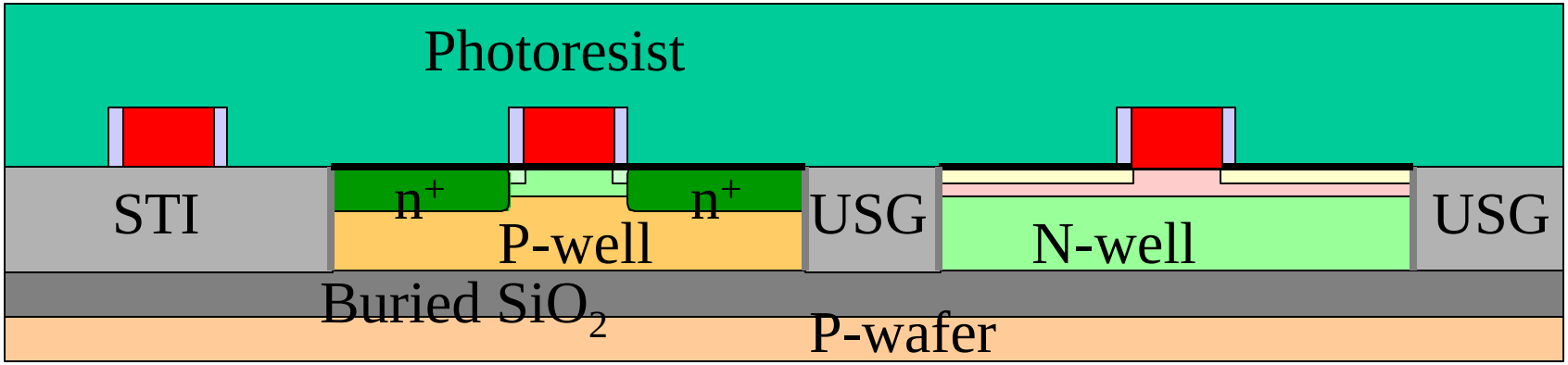
NMOS S/D Implantation



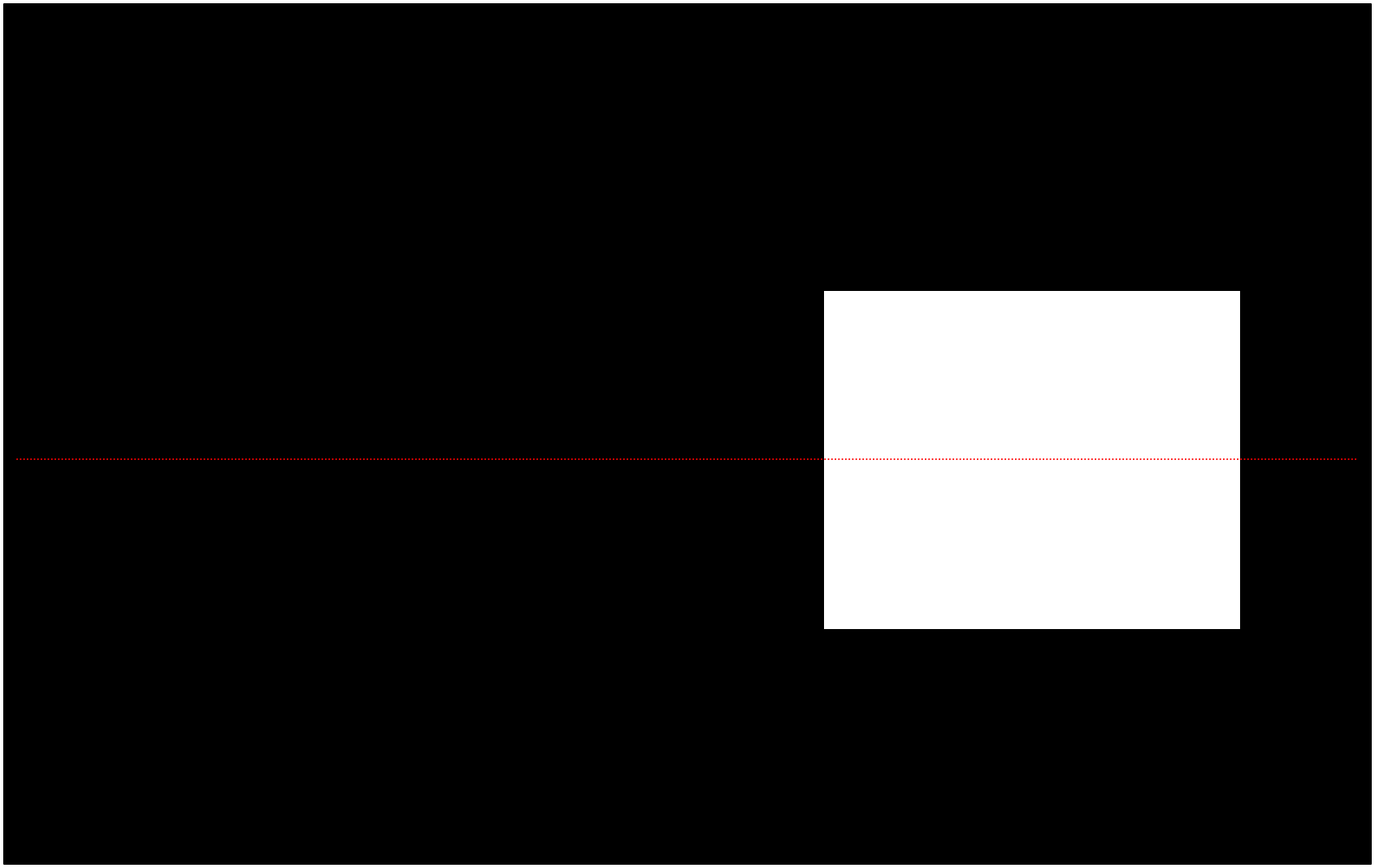
Strip Photoresist



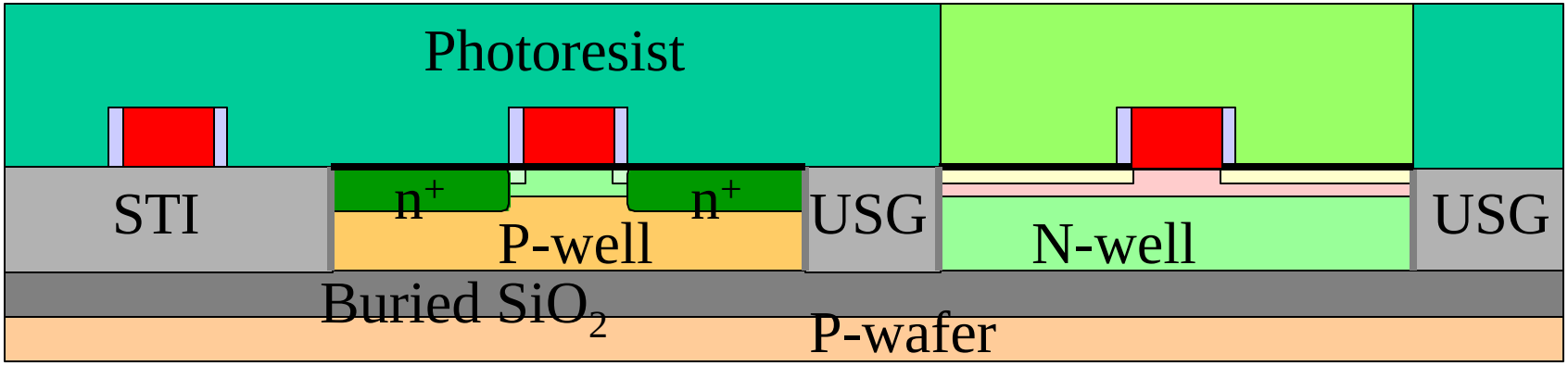
Photoresist Coating and Baking



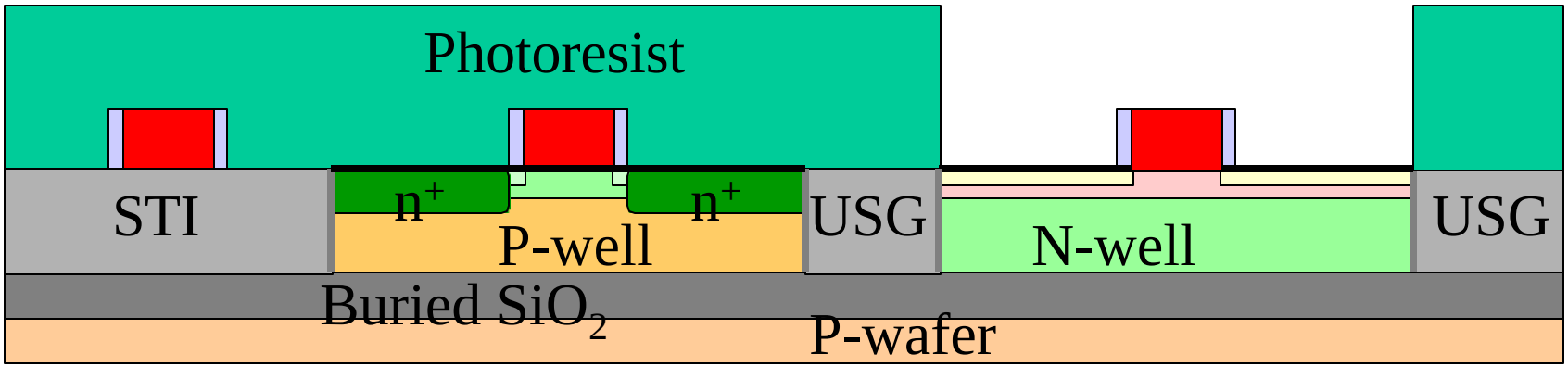
Mask 8, PMOS S/D Implantation



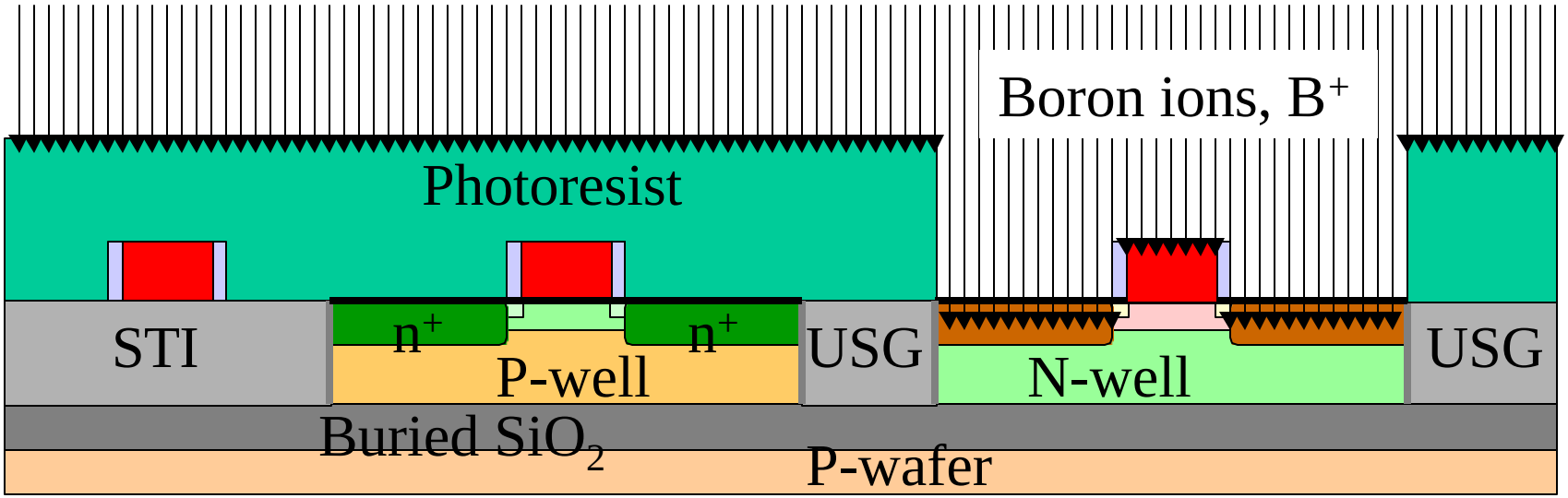
Alignment and Exposure



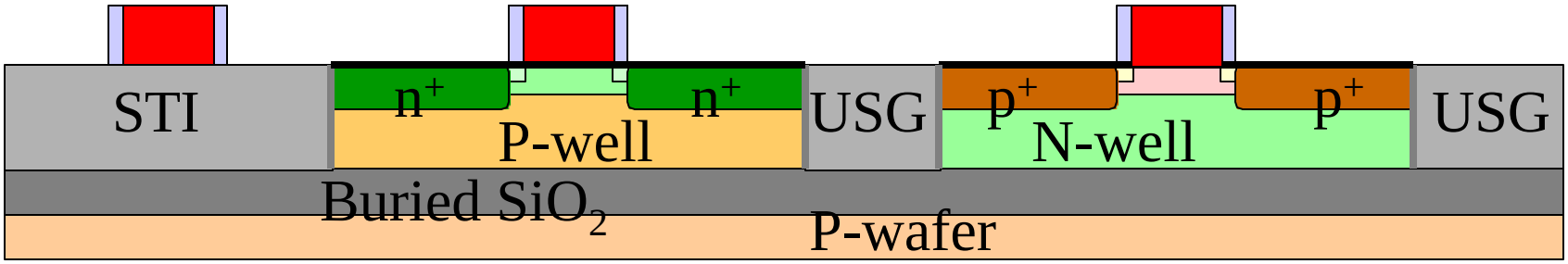
PEB, Development, and Inspection



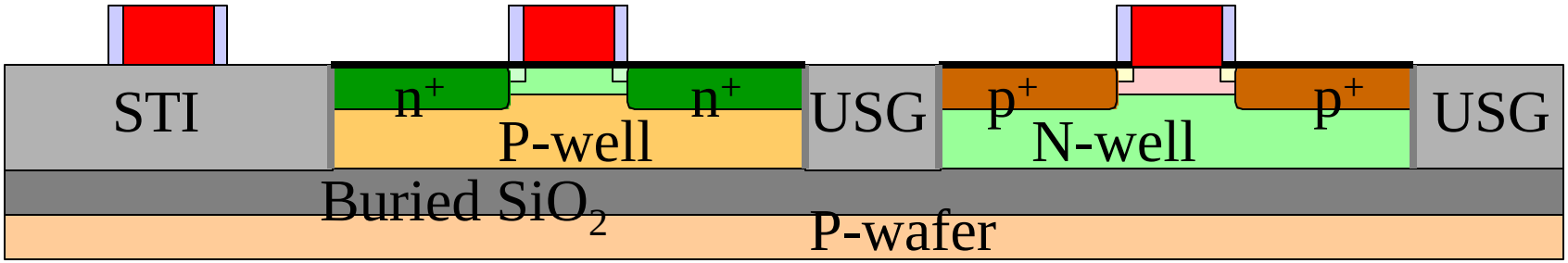
PMOS S/D Implantation



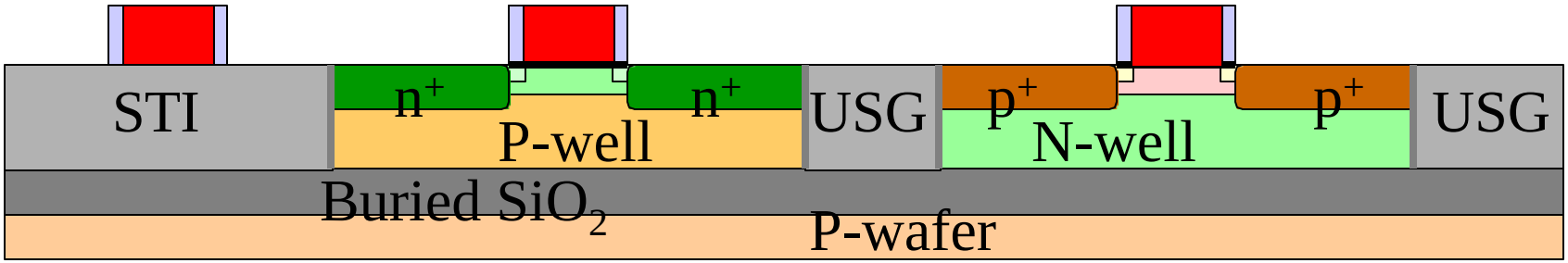
Strip Photoresist



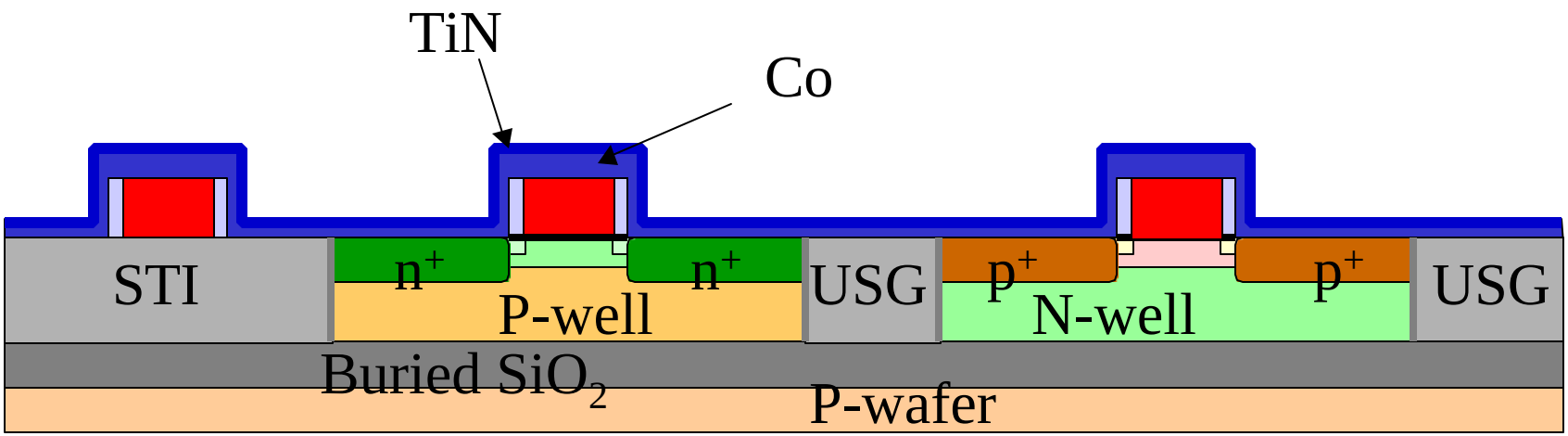
Rapid Thermal Annealing



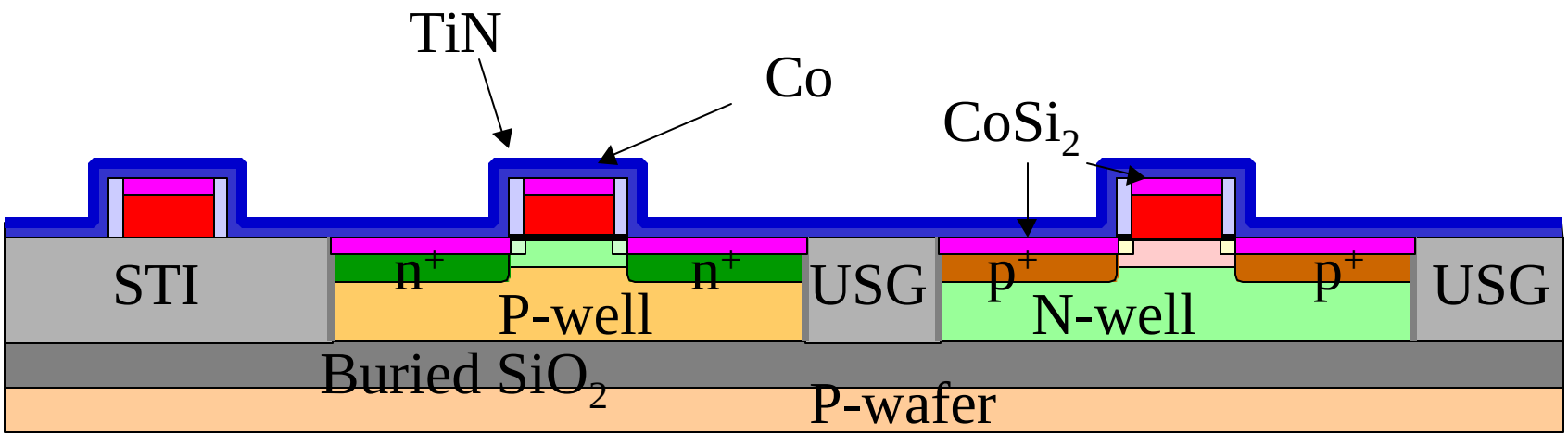
Argon Sputtering Etch



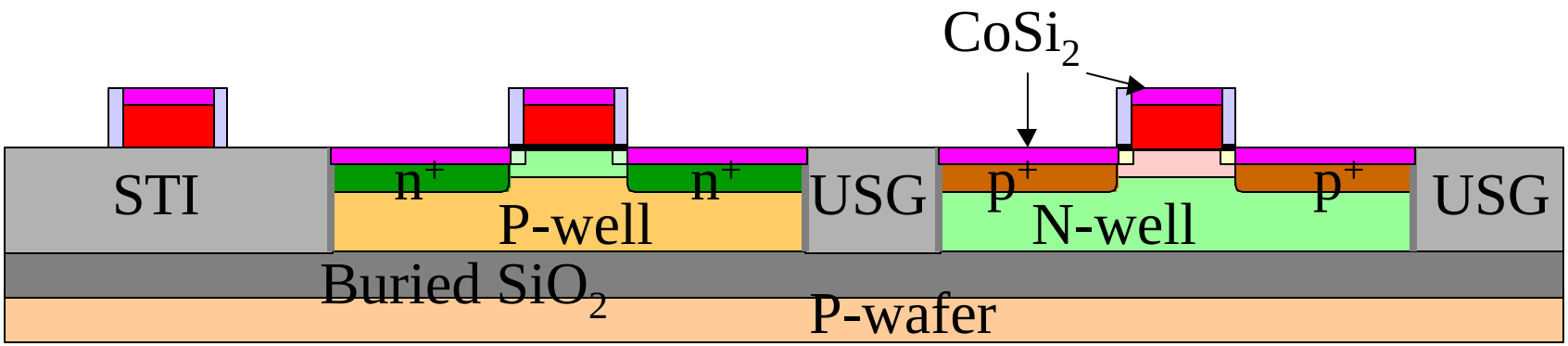
Co and TiN Sputtering Deposition



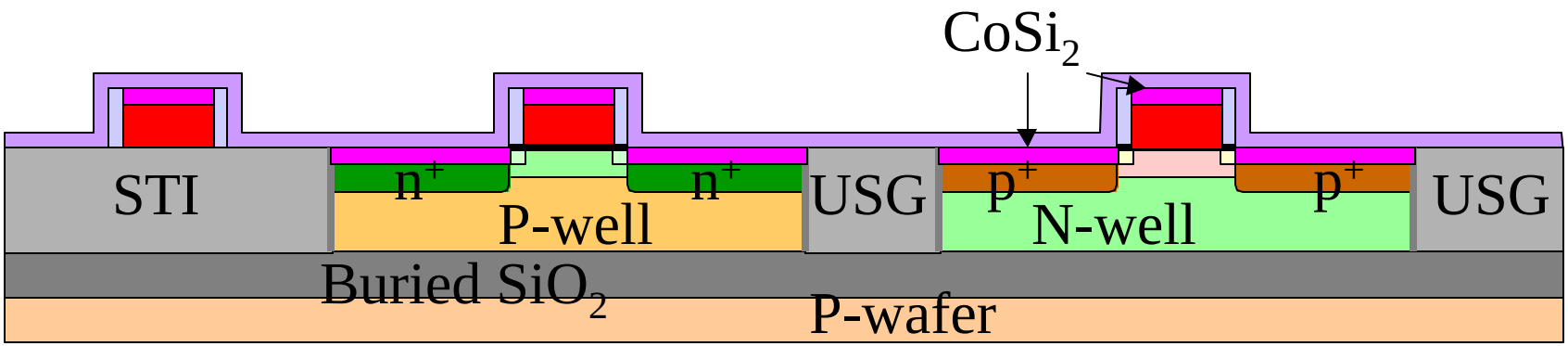
Rapid Thermal Annealing



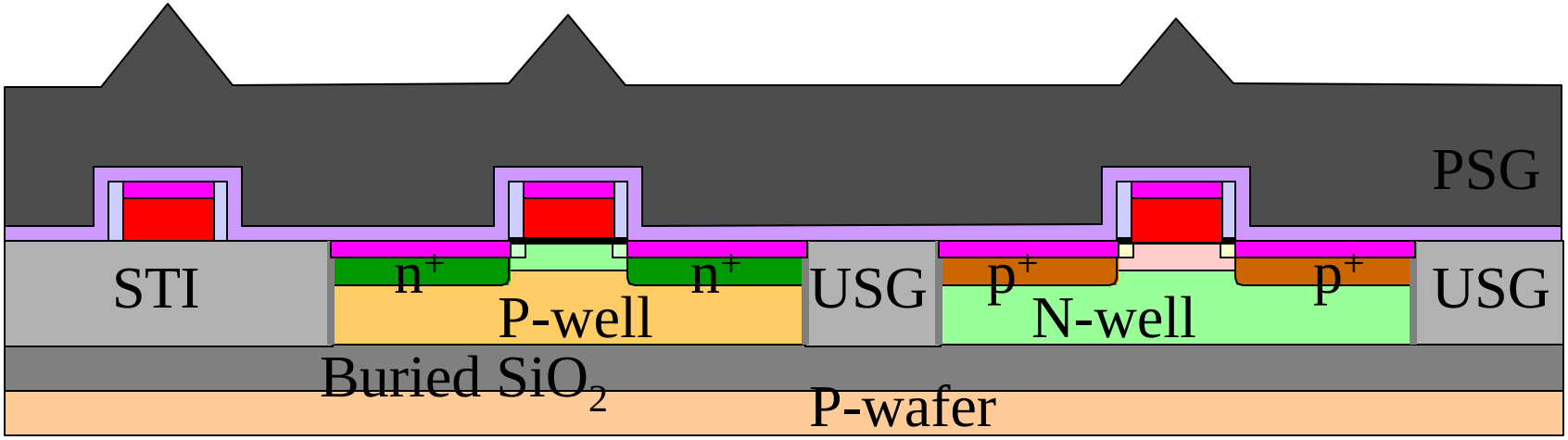
Strip Titanium Nitride and Cobalt



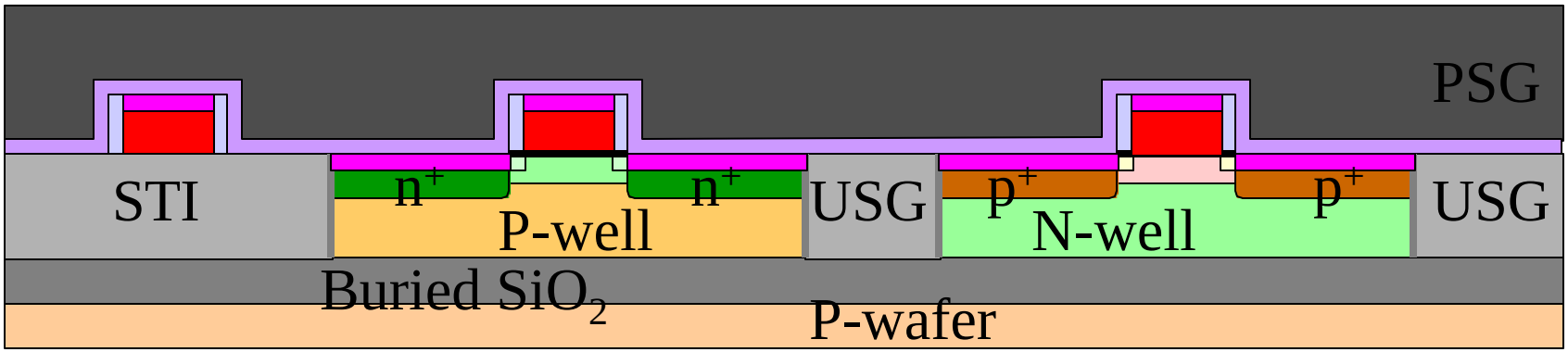
PECVD Nitride



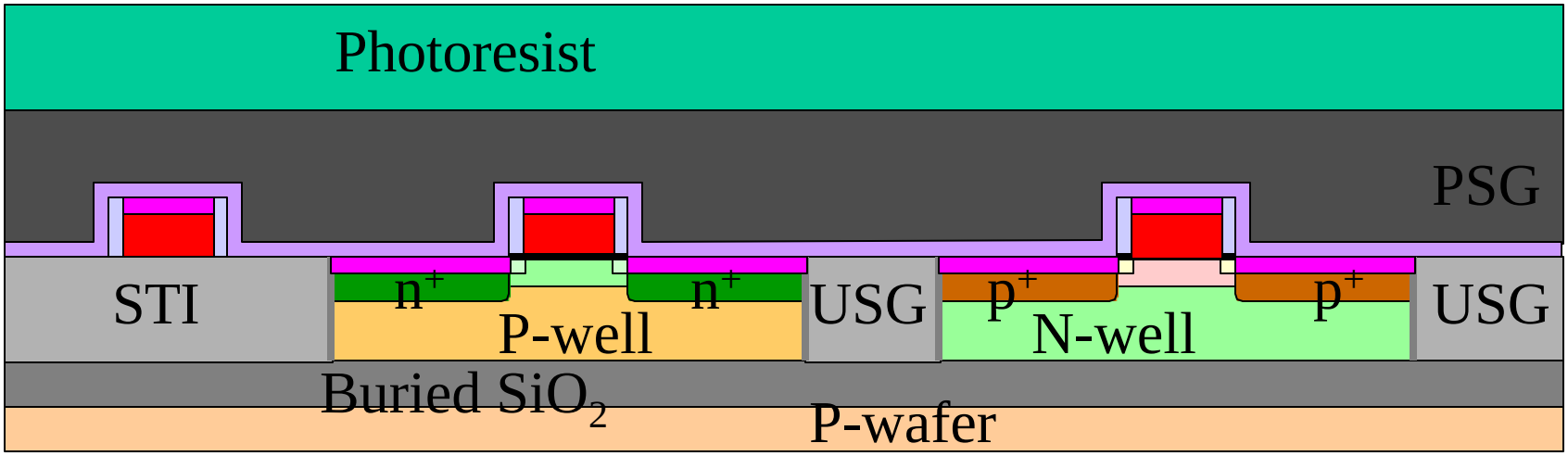
HDP CVD PSG



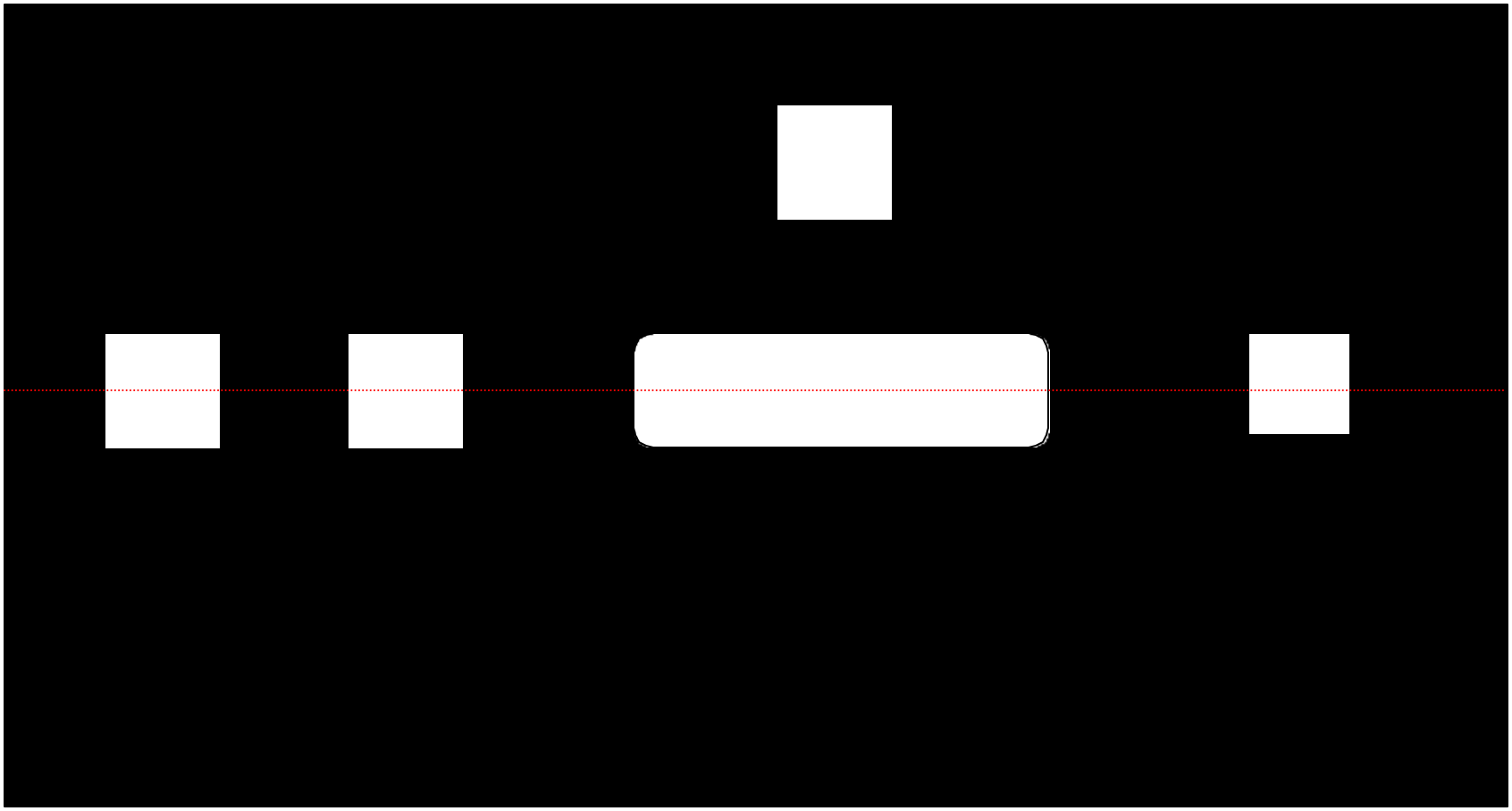
CMP PSG



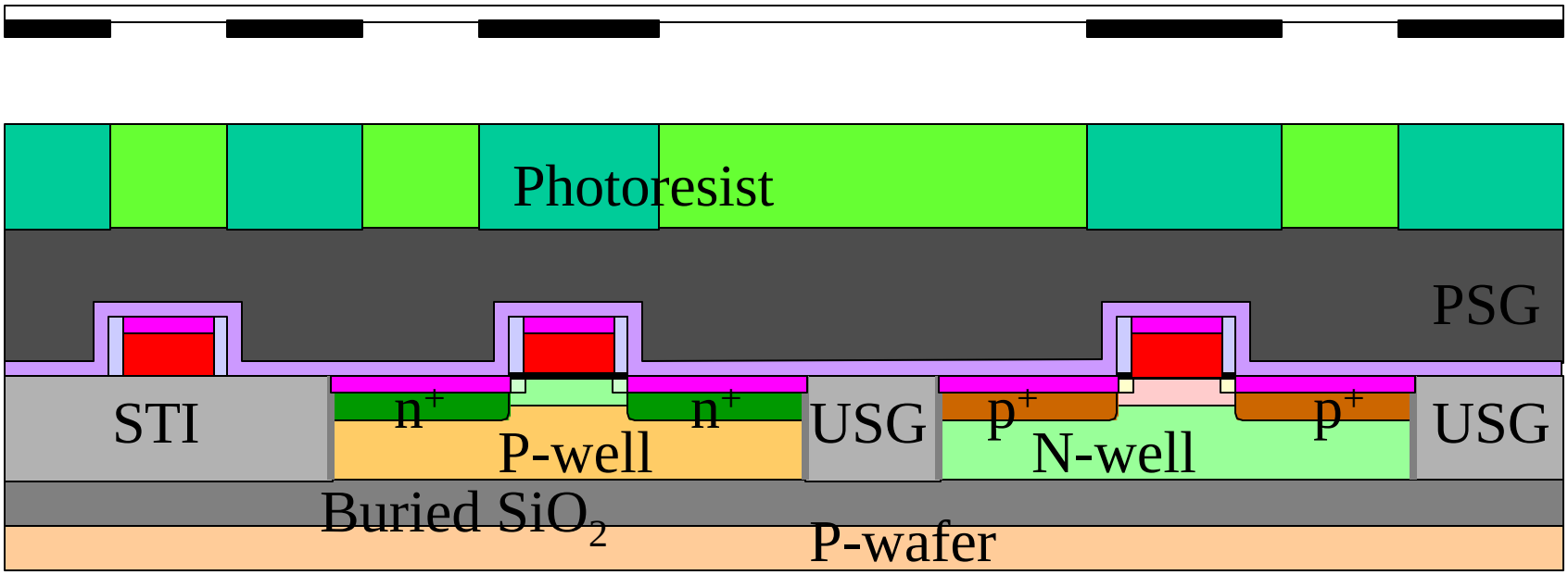
Photoresist Coating and Baking



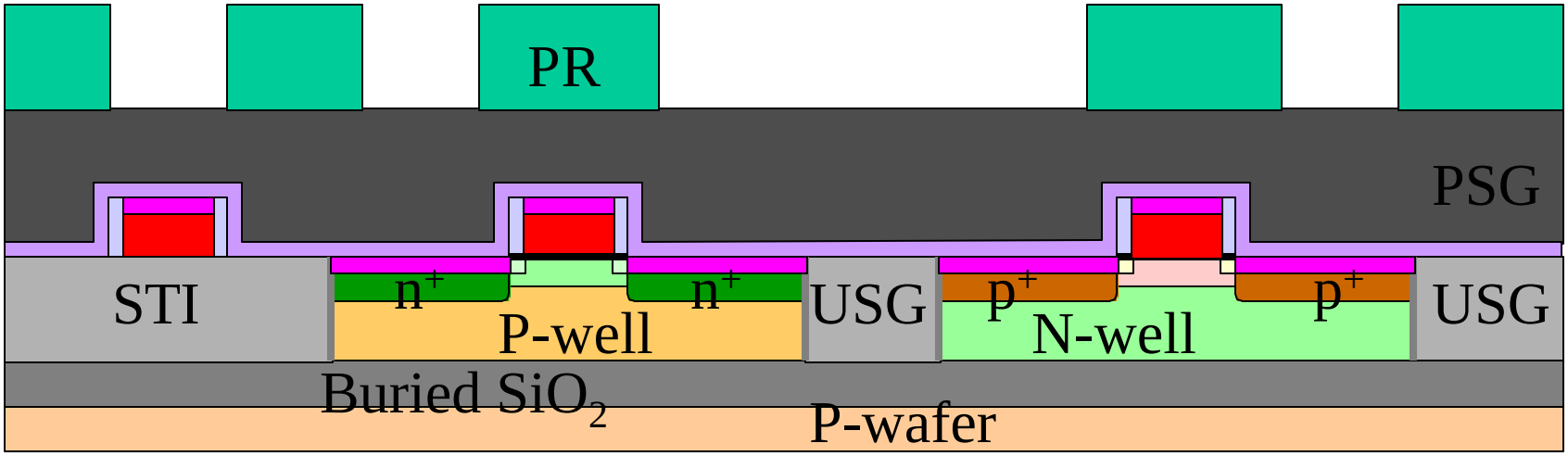
Mask 9, Contact and Local Interconnection



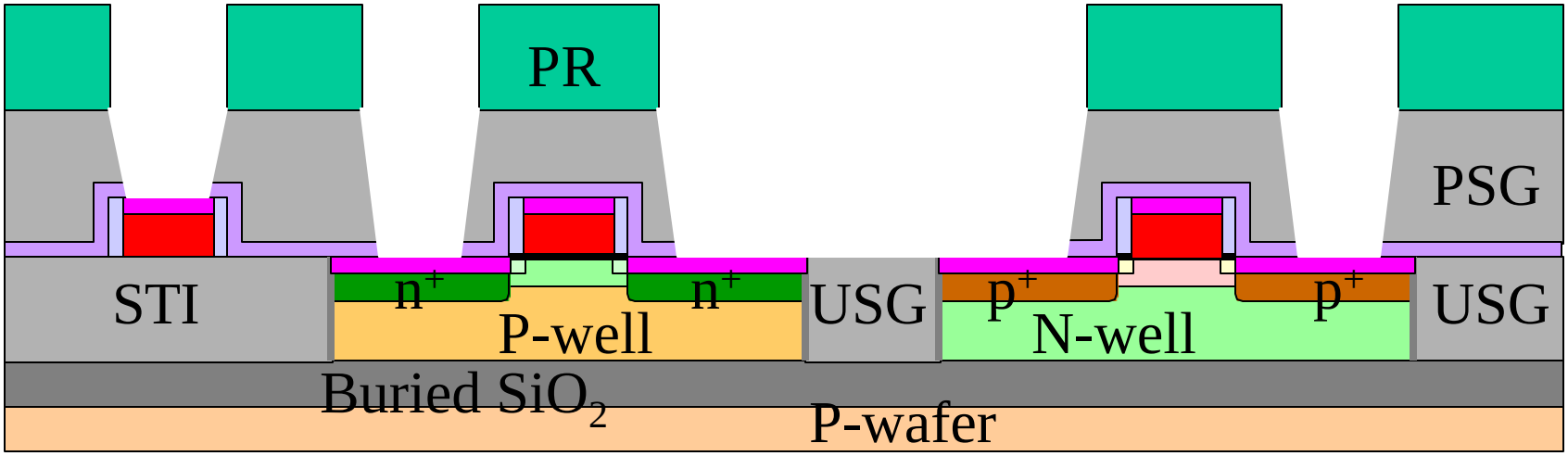
Alignment and Exposure



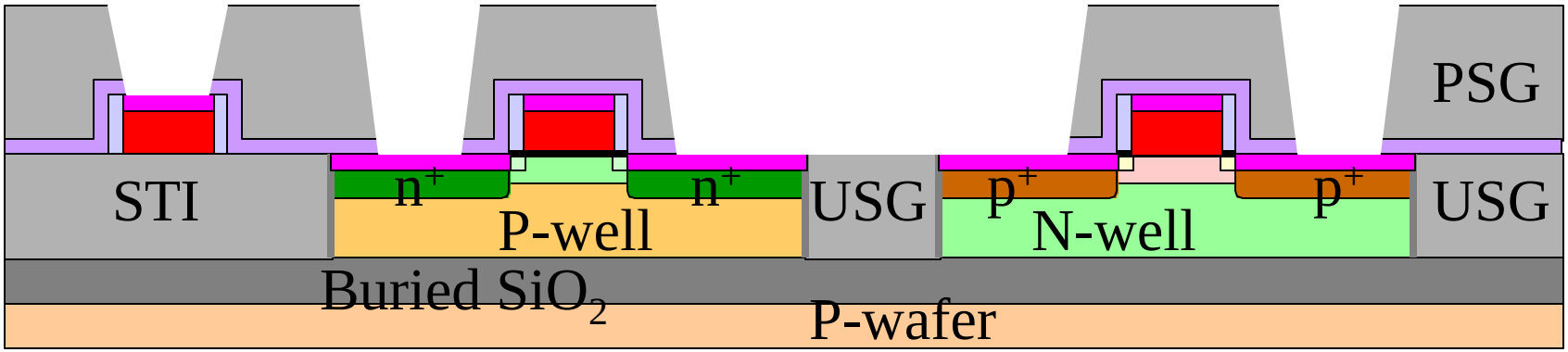
PEB, Development, and Inspection



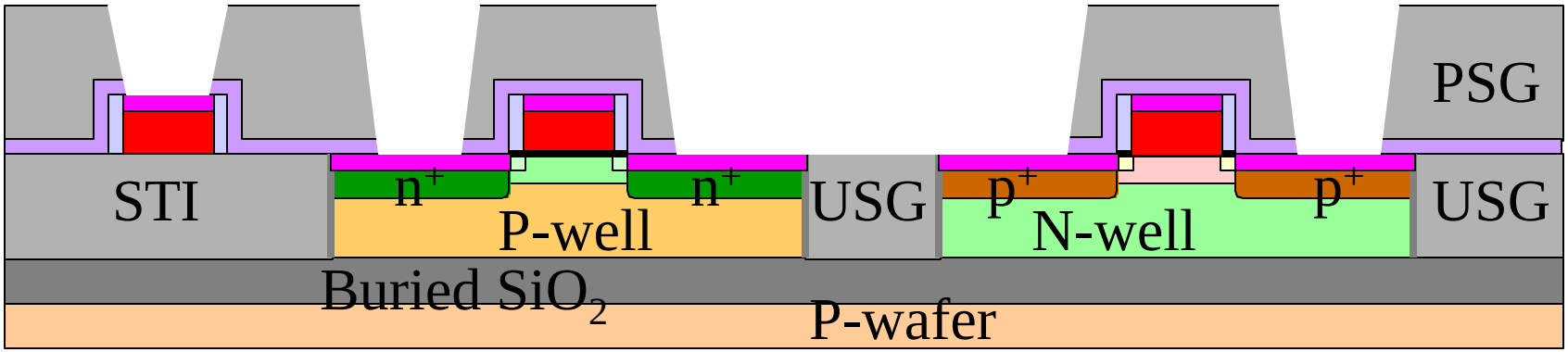
Etch PSG



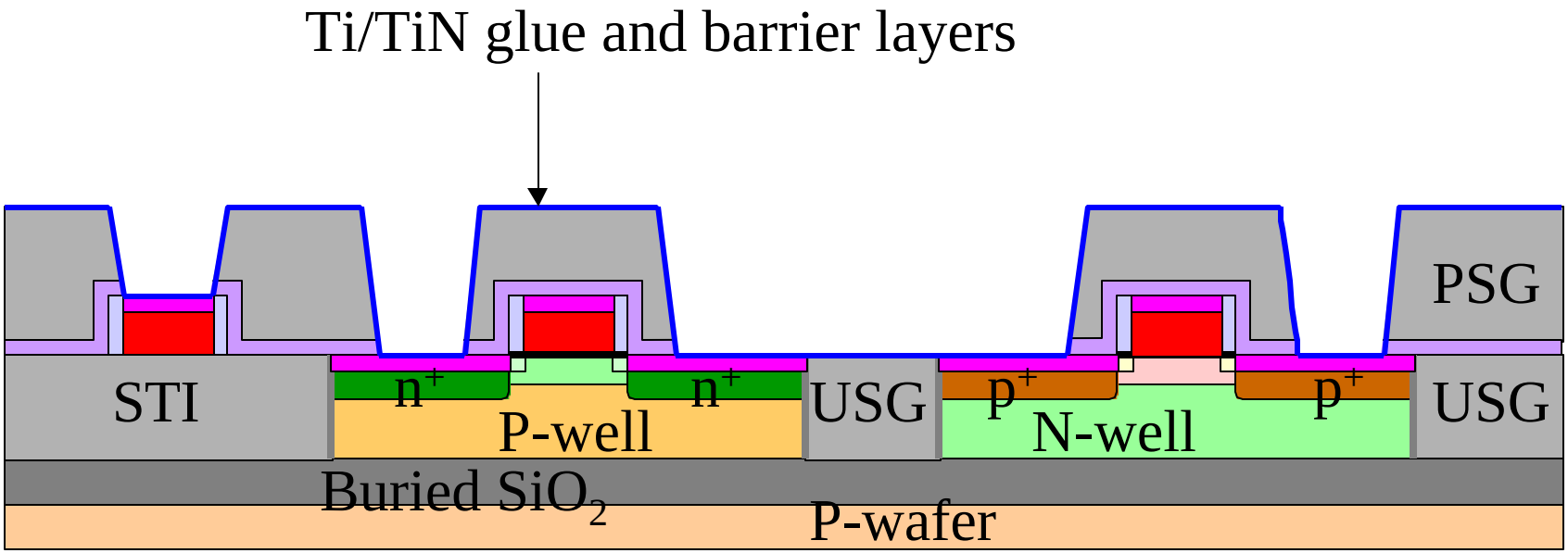
Strip Photoresist



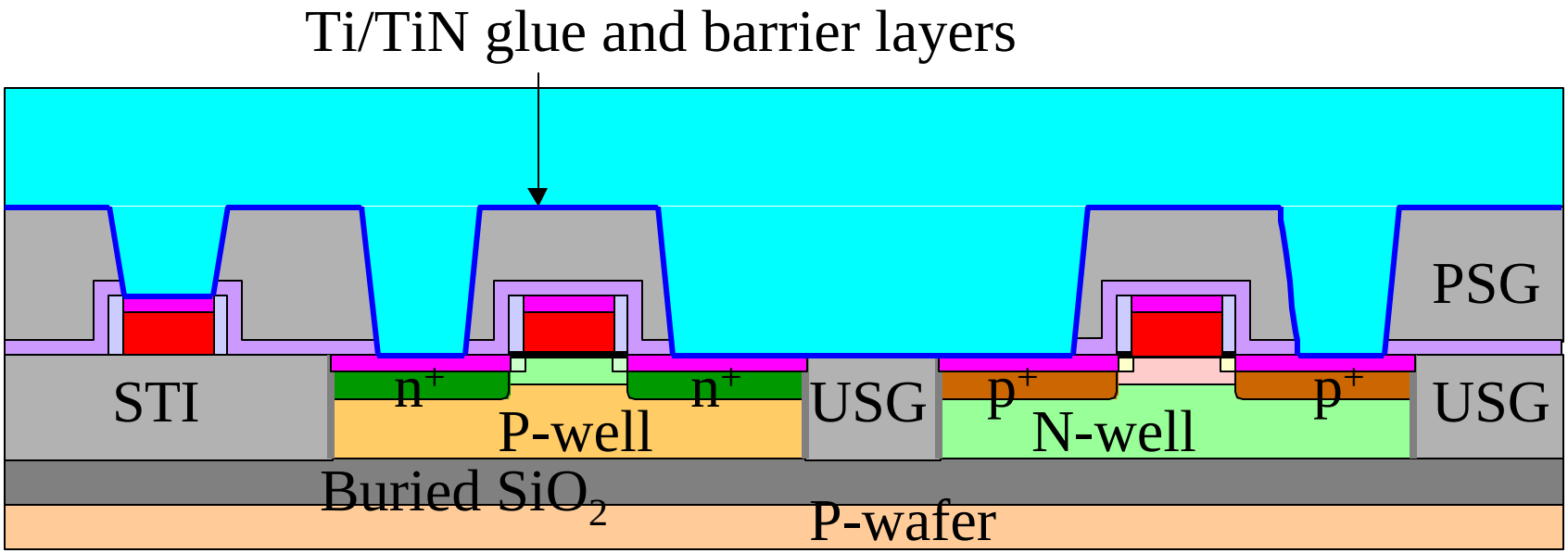
Argon Sputtering Etch



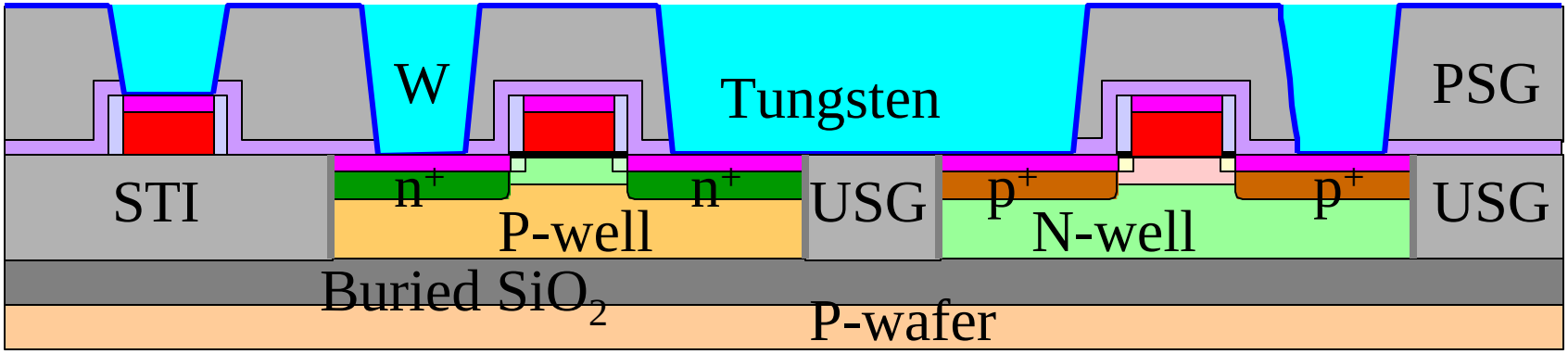
Ti and TiN Sputtering Deposition



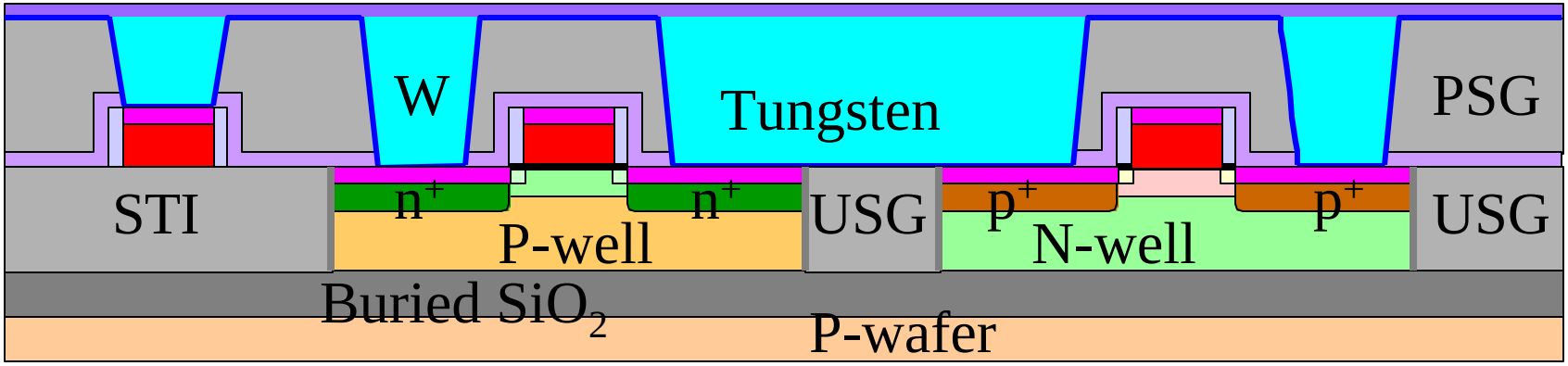
Tungsten CVD



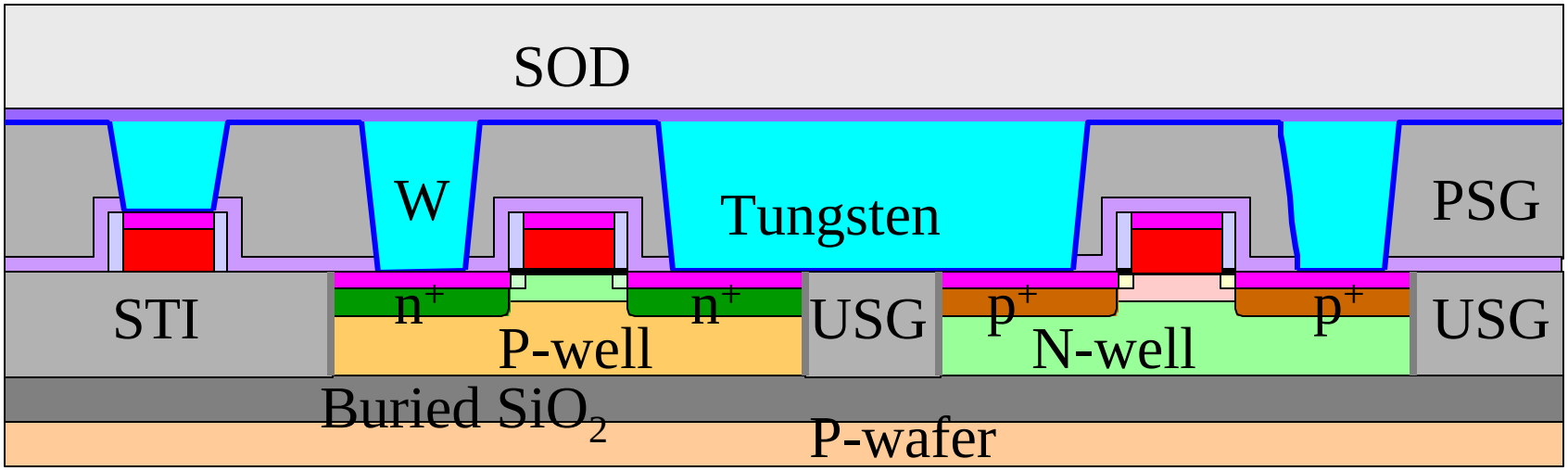
W, TiN, and Ti CMP



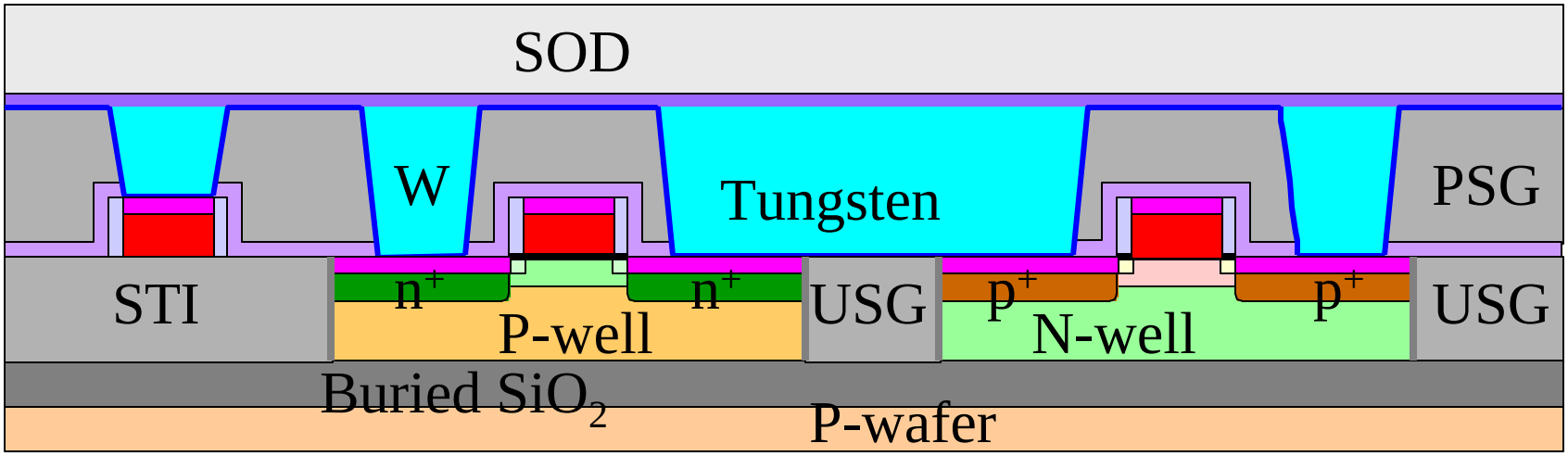
PECVD Silicon Carbide Seal Layer



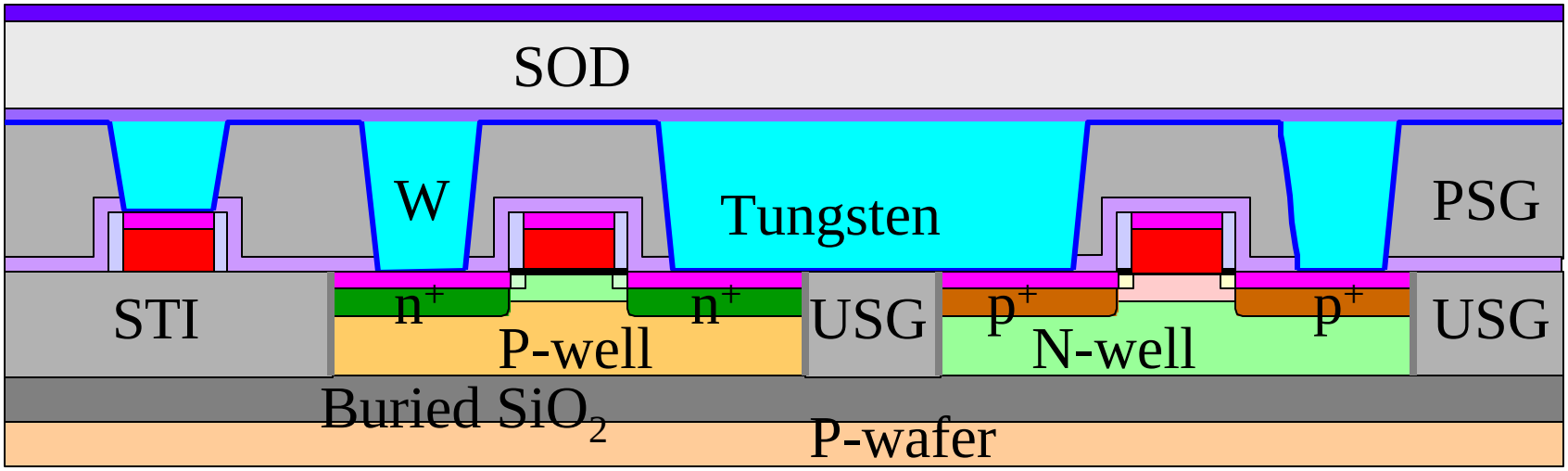
Spin-on Dielectric (SOD) Coating



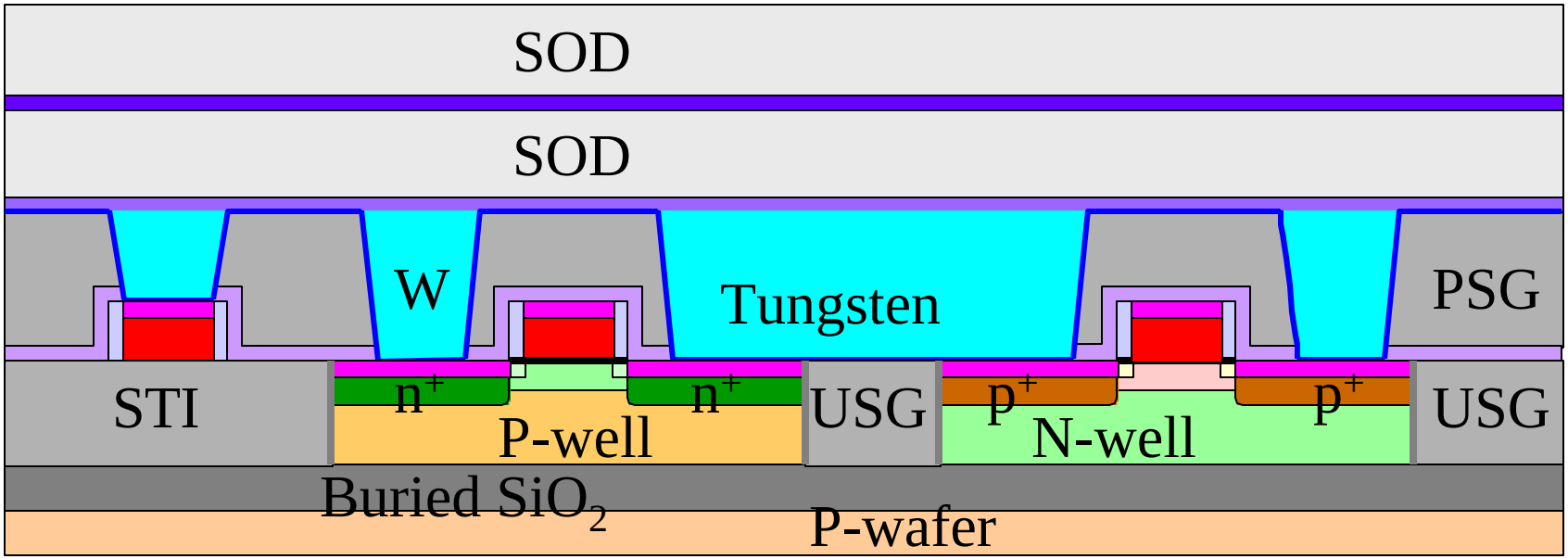
SOD Cure


SOD
W
Tungsten
PSG
STI
n+
n+
USG
p+
p+
USG
P-well
N-well
Buried SiO2
P-wafer

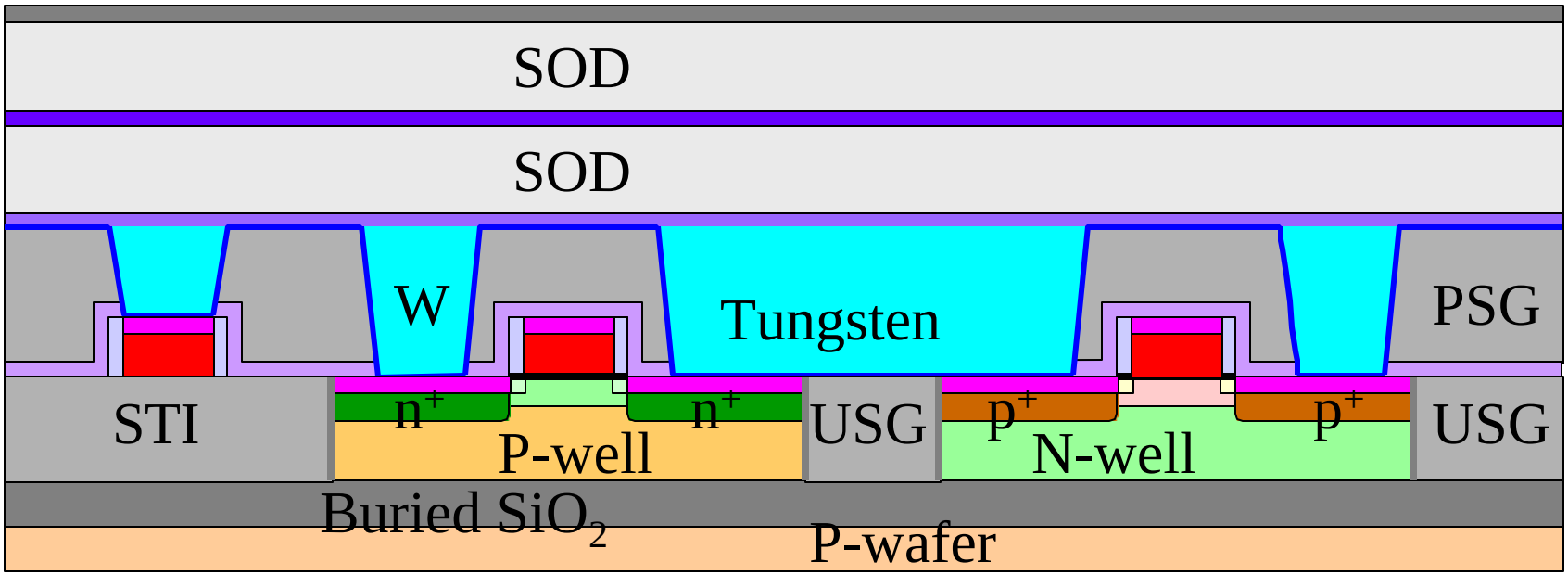
PECVD SiC Etch Stop Layer



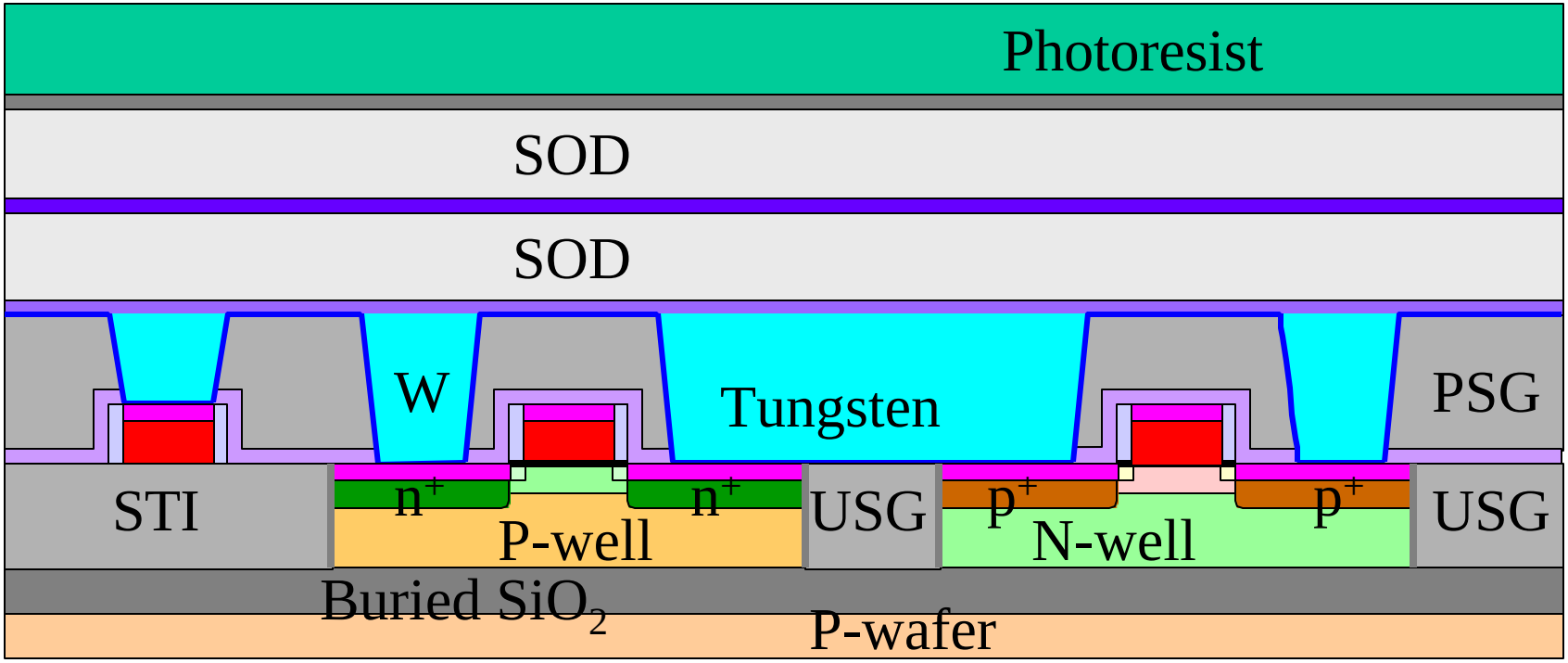
SOD Coating and Curing



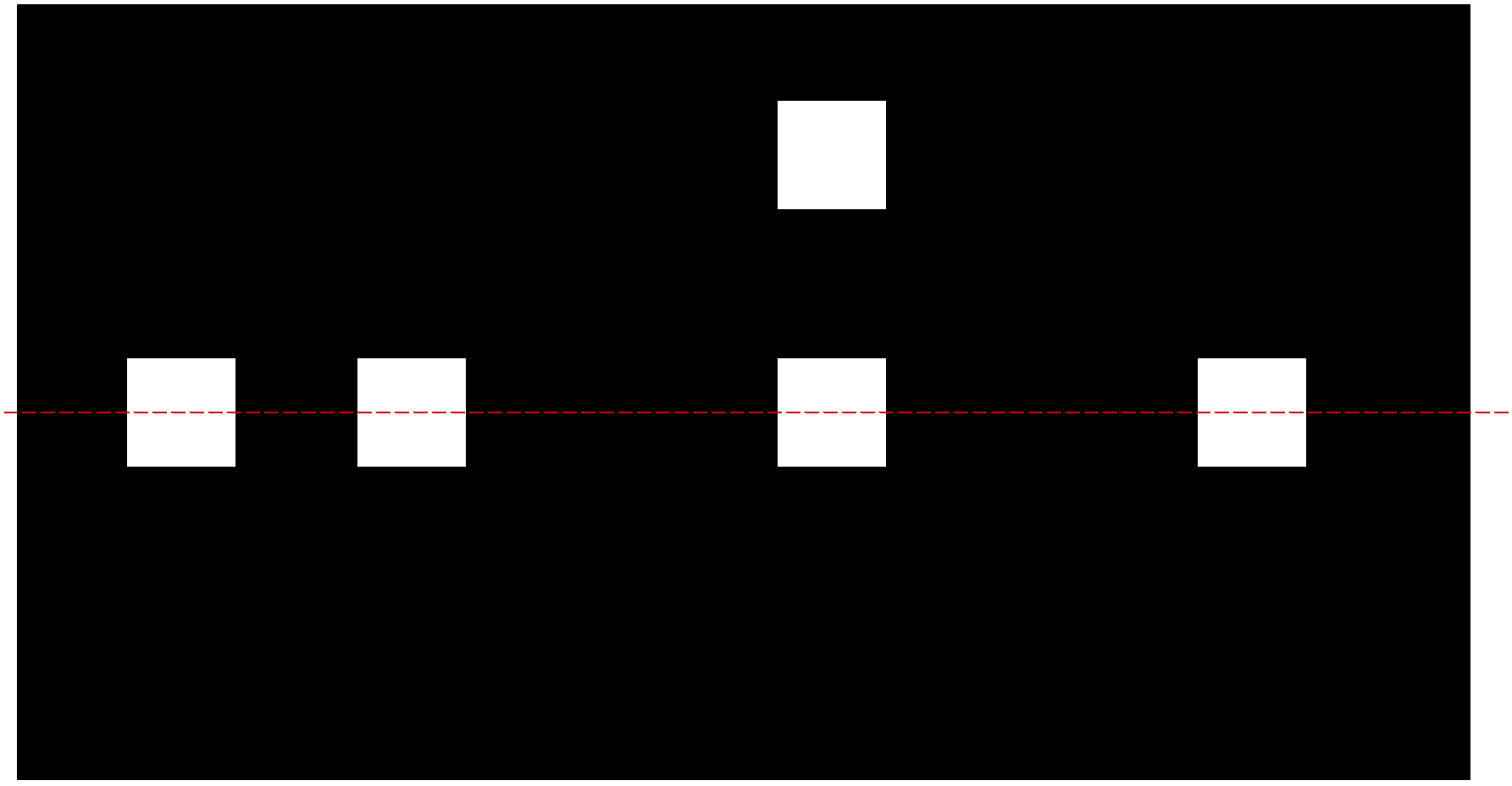
PE-TEOS Cap


SOD
SOD
W
Tungsten
PSG
STI
n+
n+
USG
p+
p+
USG
P-well
N-well
Buried SiO2
P-wafer

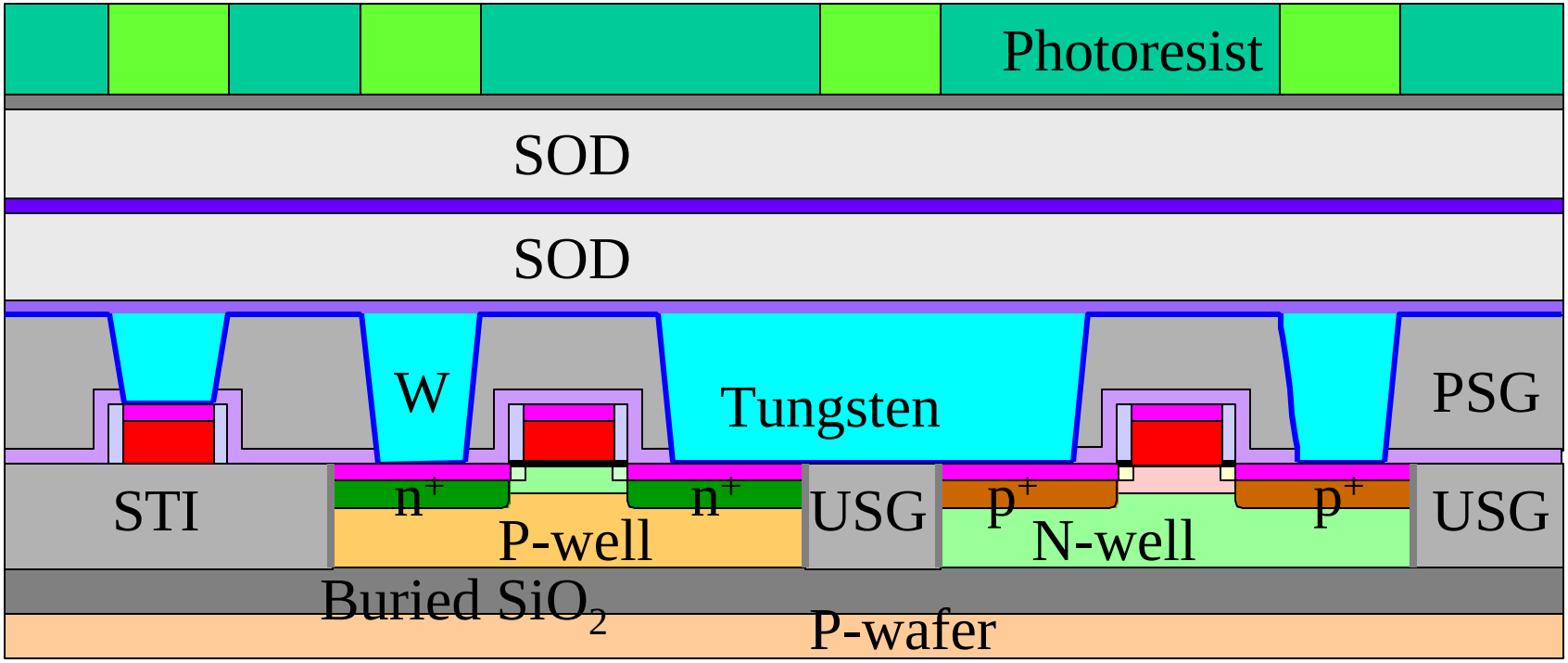
Photoresist Coating and Baking



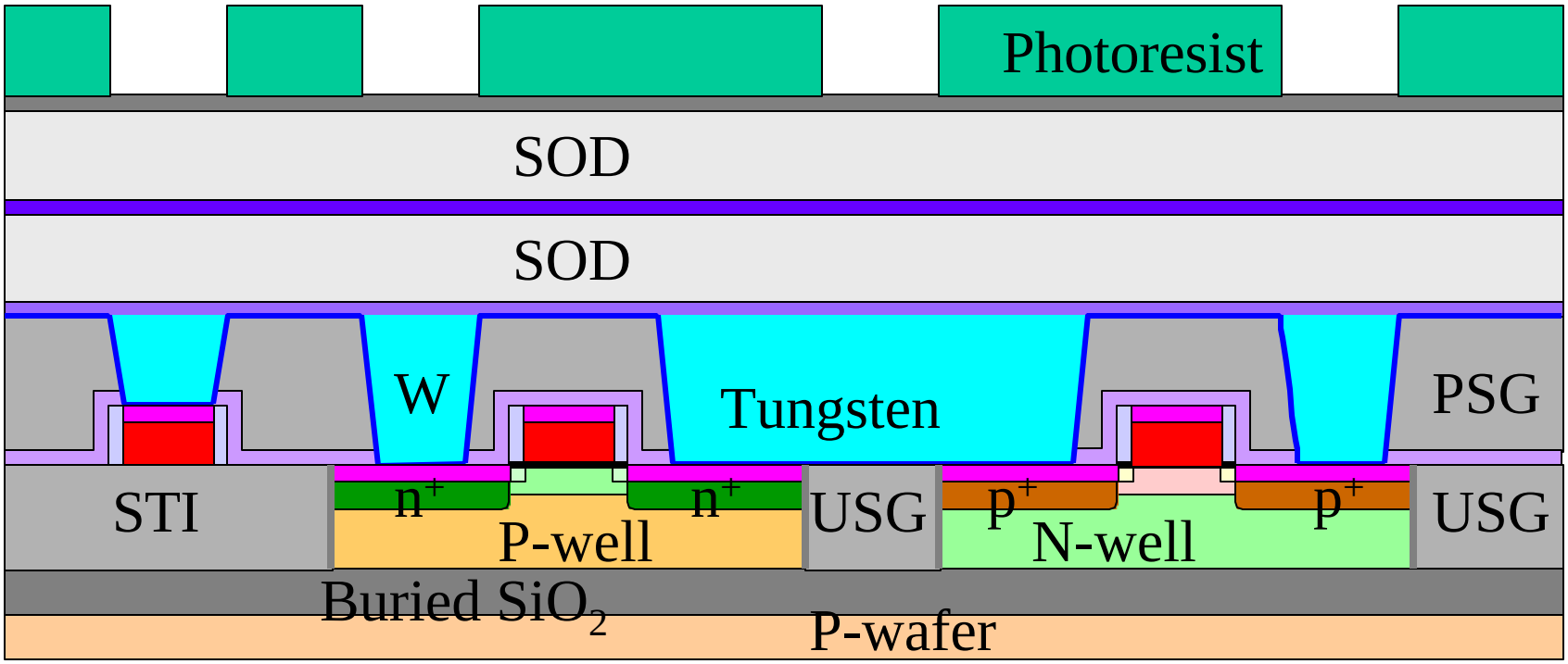
Mask 10, Via 1



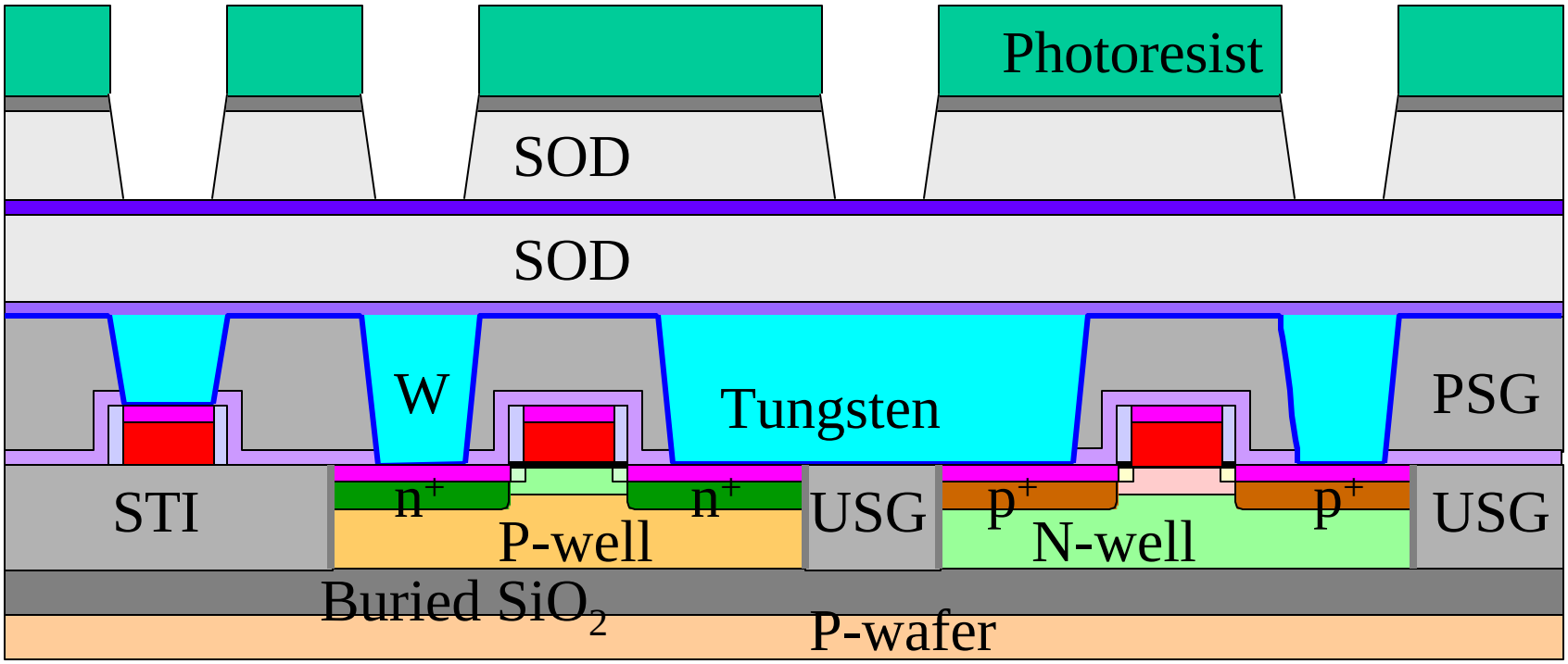
Alignment and Exposure



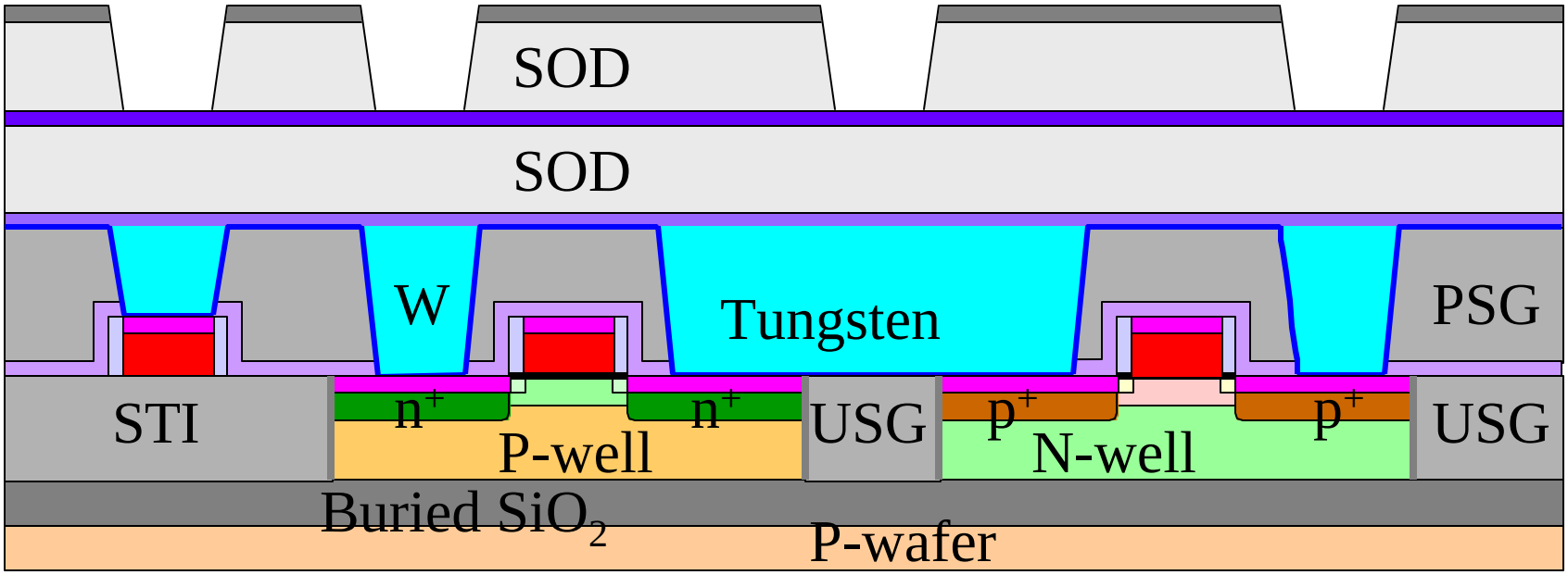
PEB, Development, and Inspection



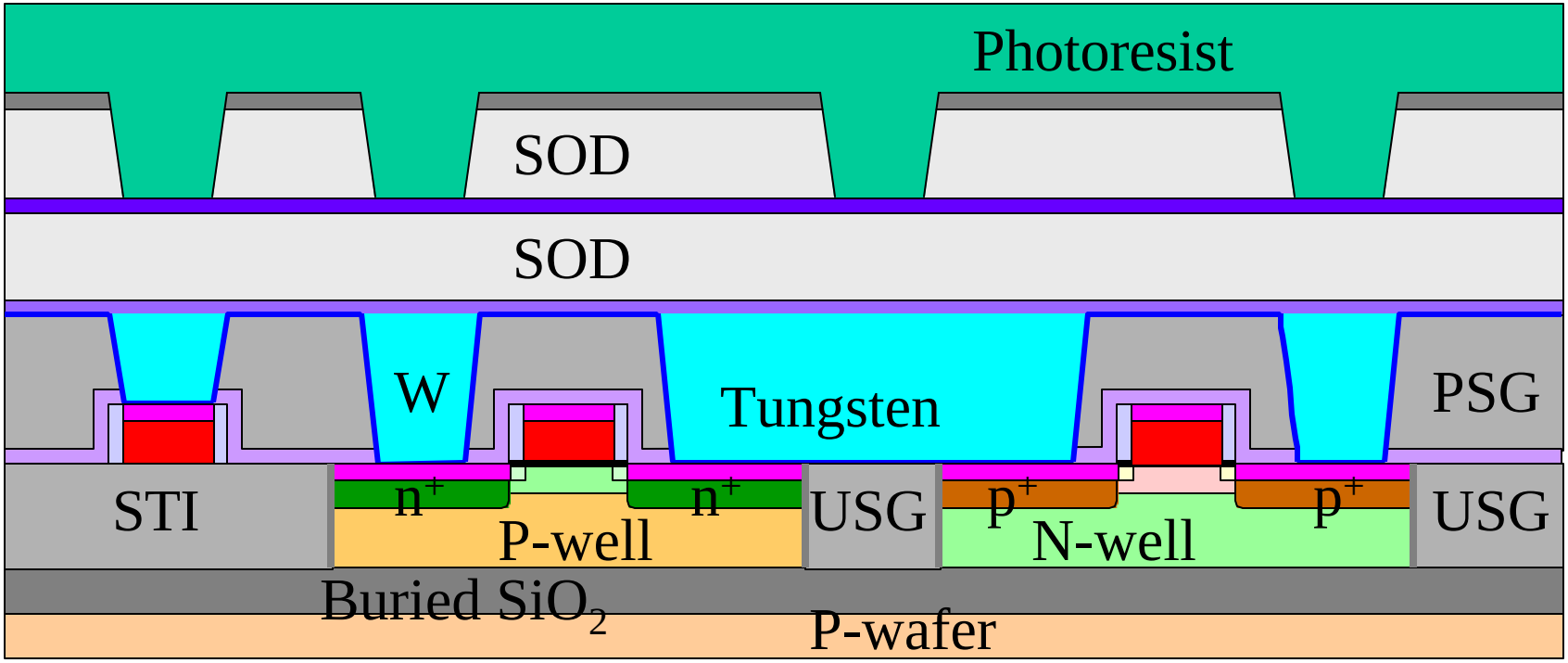
Etch PE-TEOS&SOD, Stop on SiC



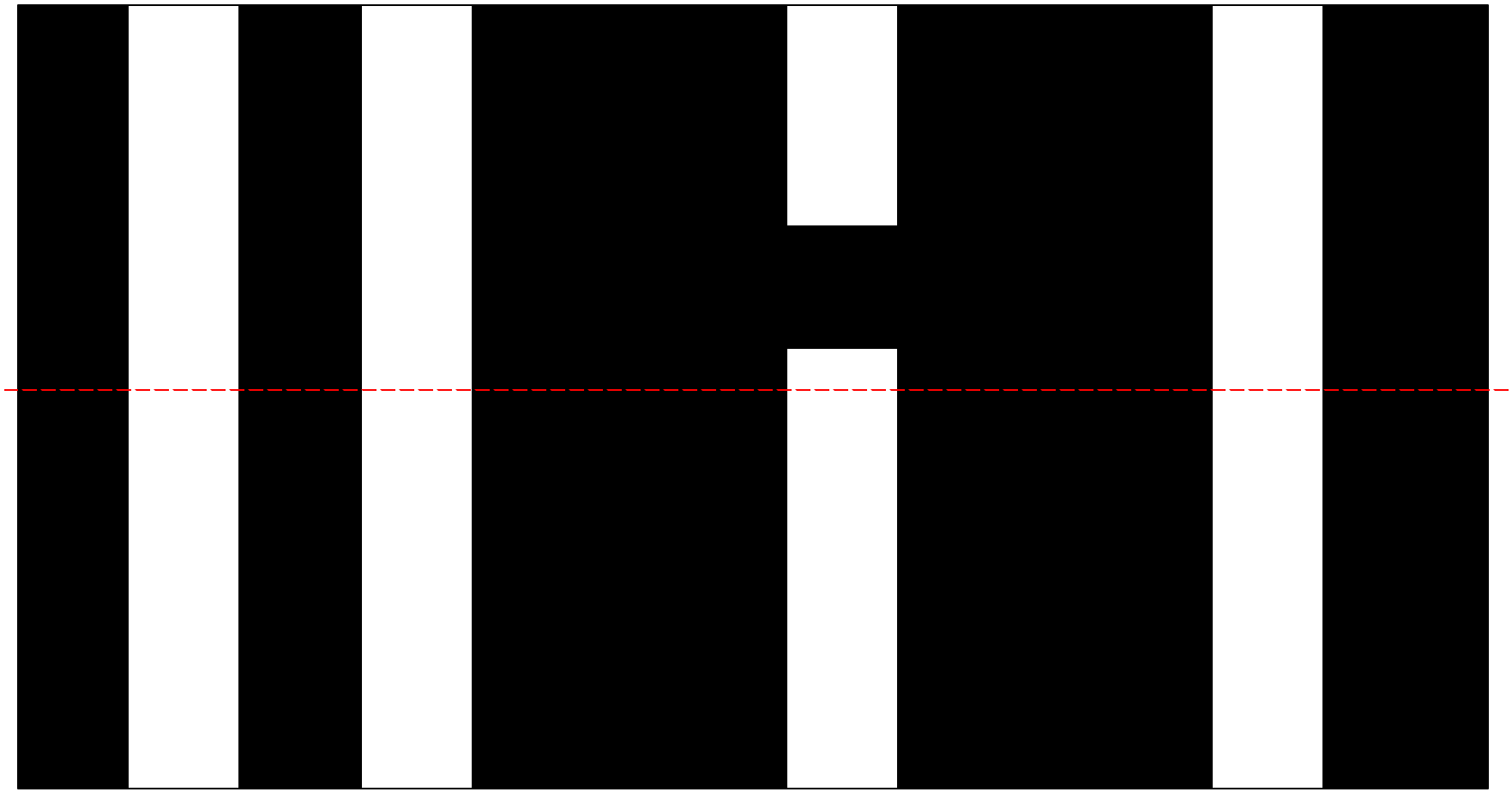
Strip Photoresist



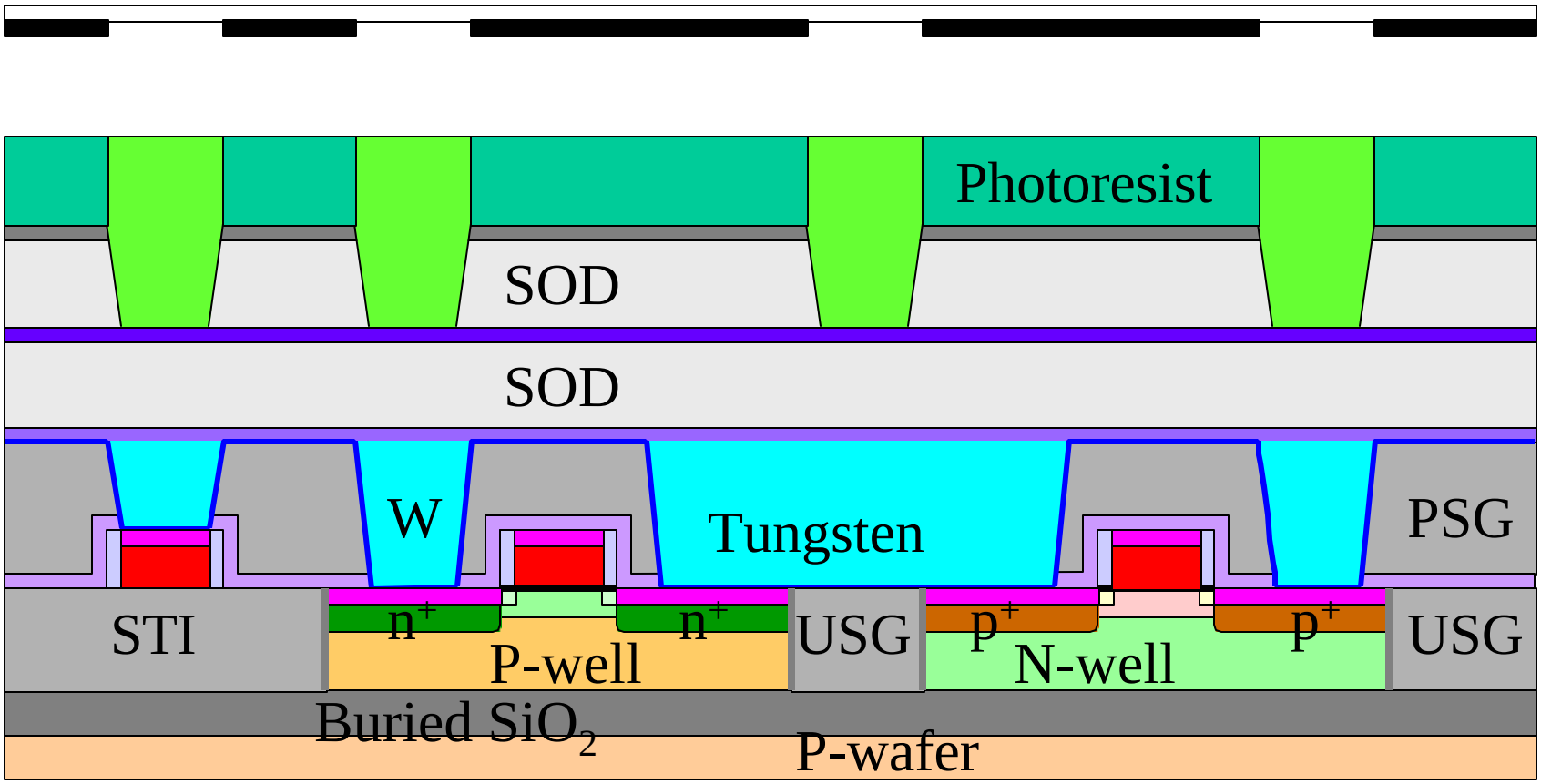
Photoresist Coating and Baking



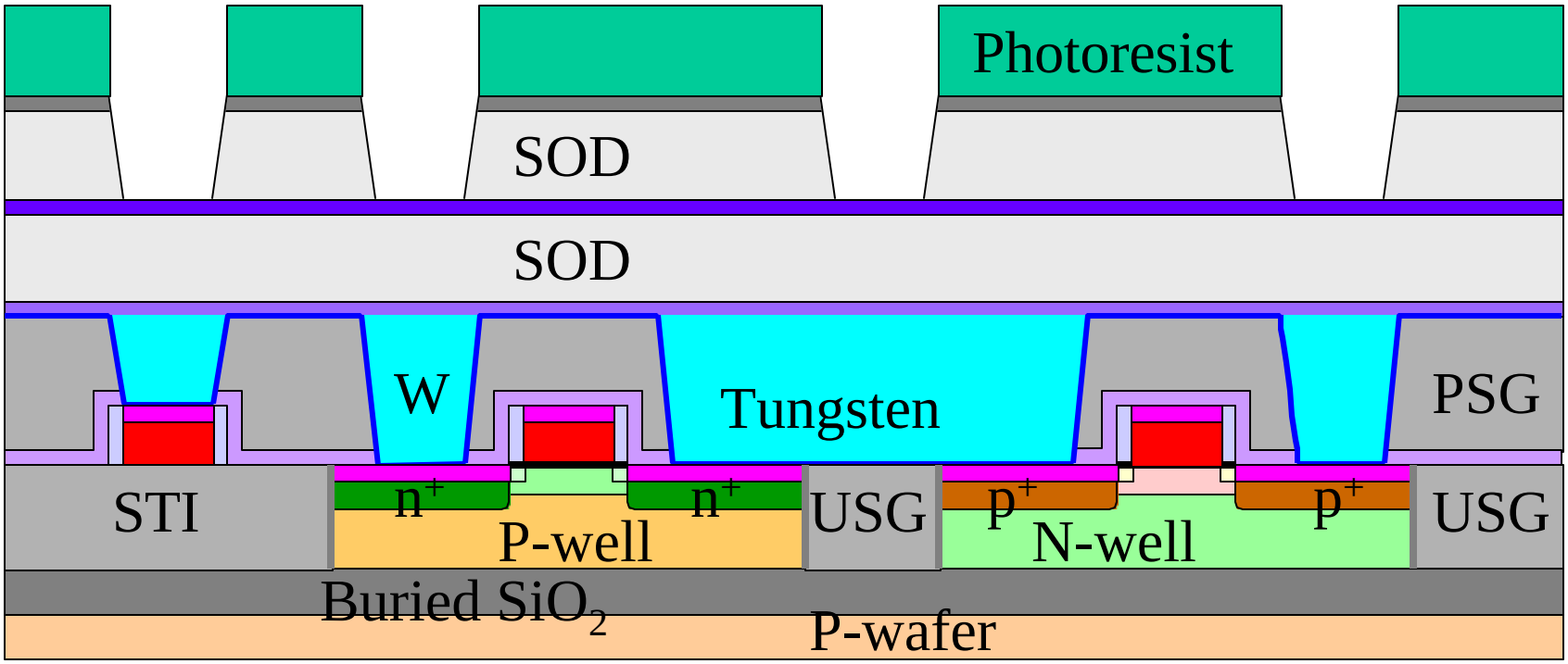
Mask 11, Metal Trench 1



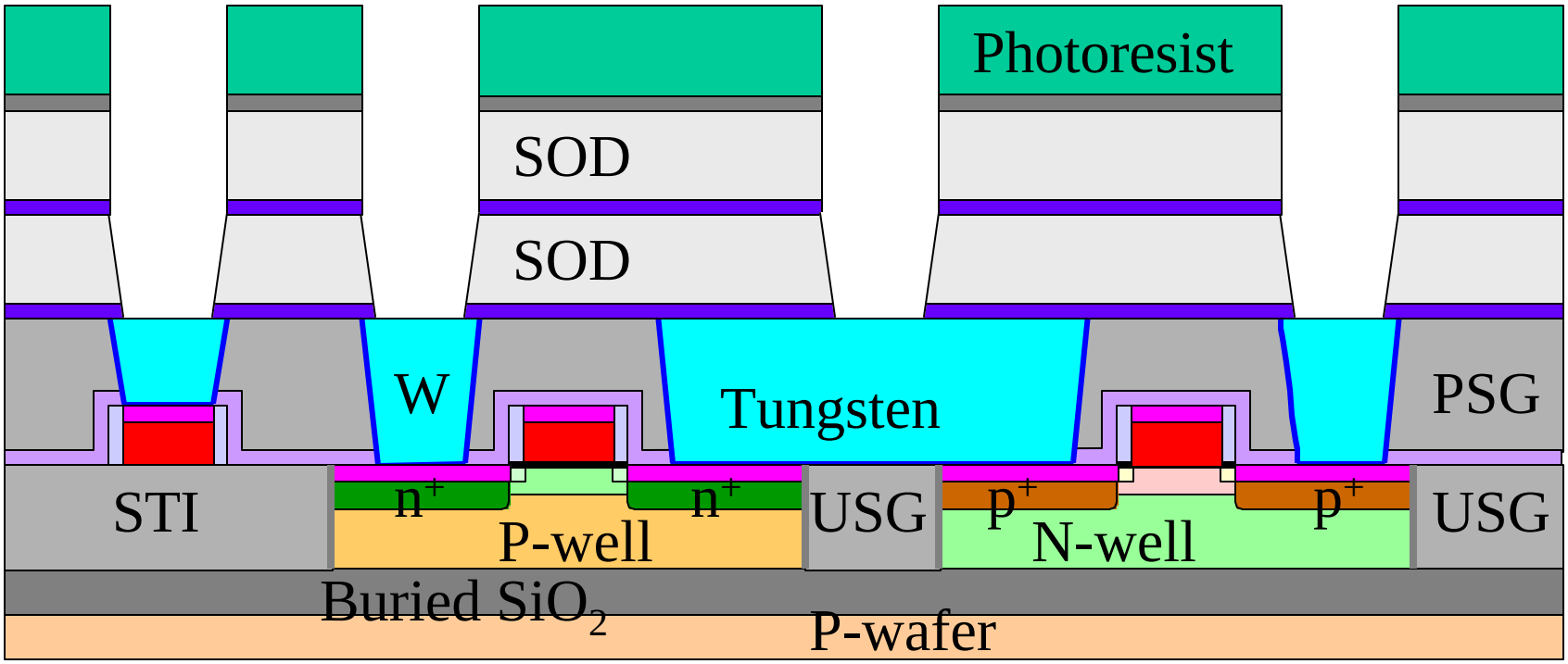
Alignment and Exposure



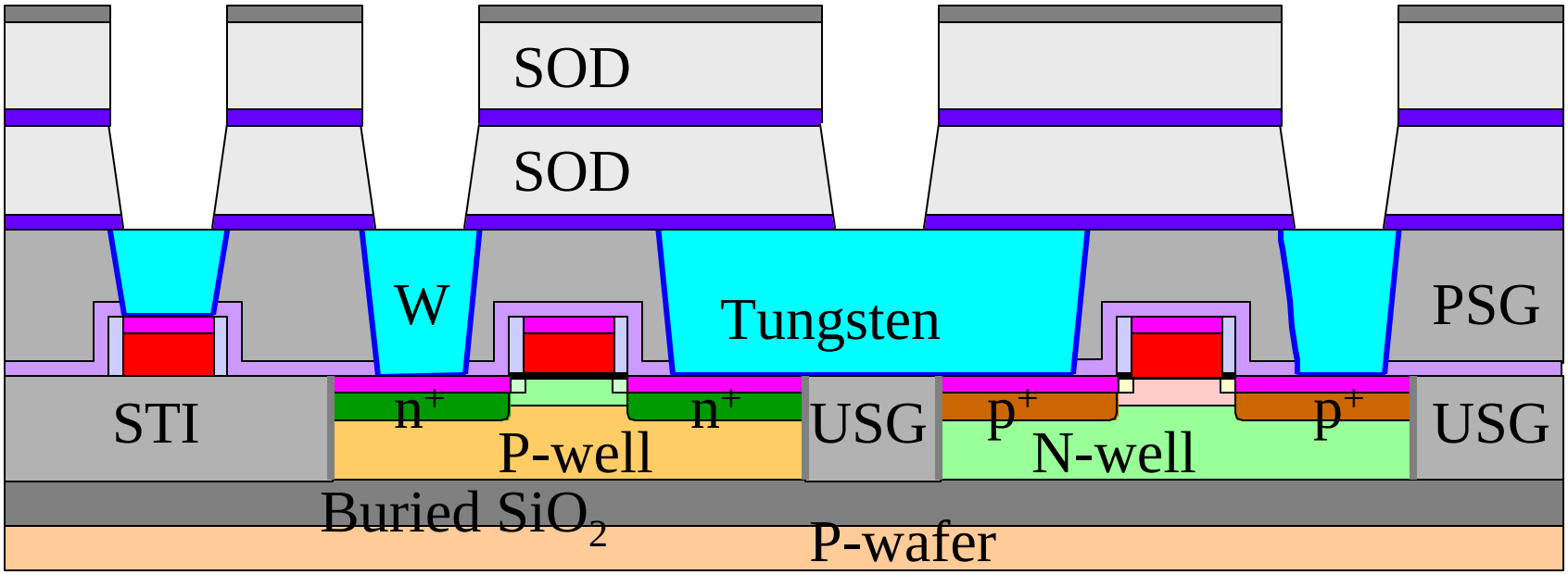
PEB, Development, and Inspection



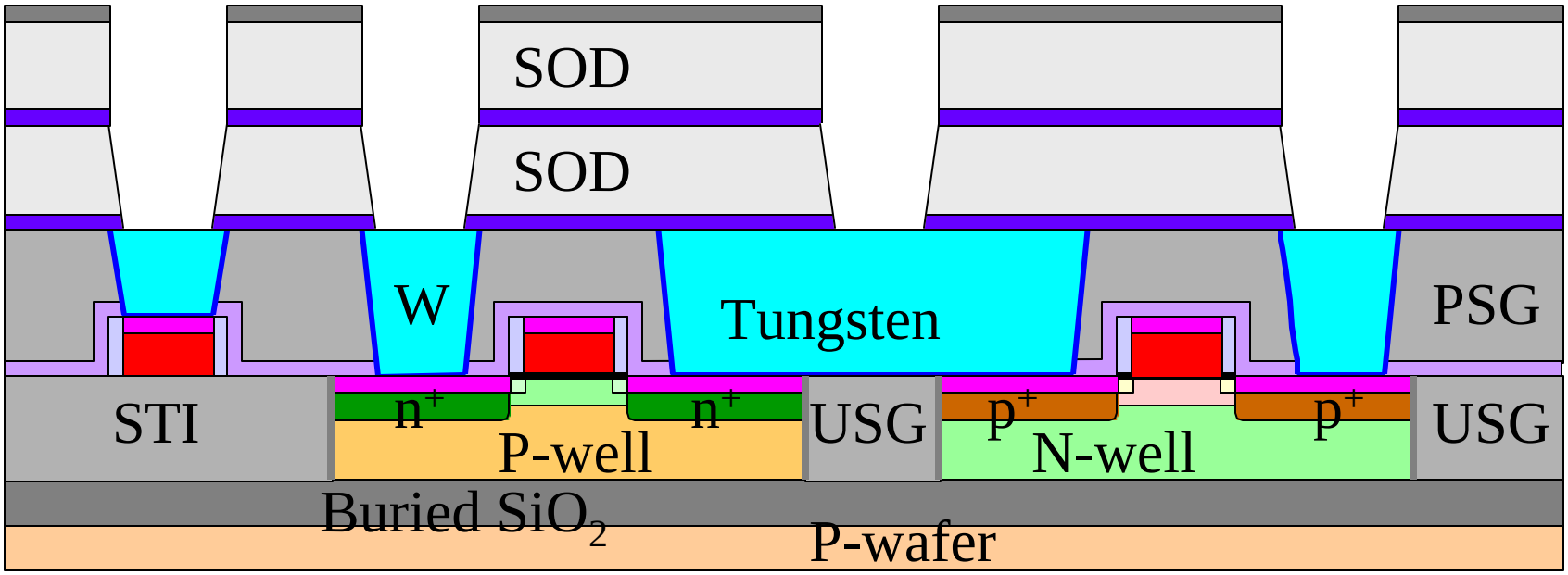
Etch Trench


Photoresist
SOD
SOD
W
Tungsten
PSG
STI
n+
n+
USG
p+
p+
USG
P-well
N-well
Buried SiO2
P-wafer

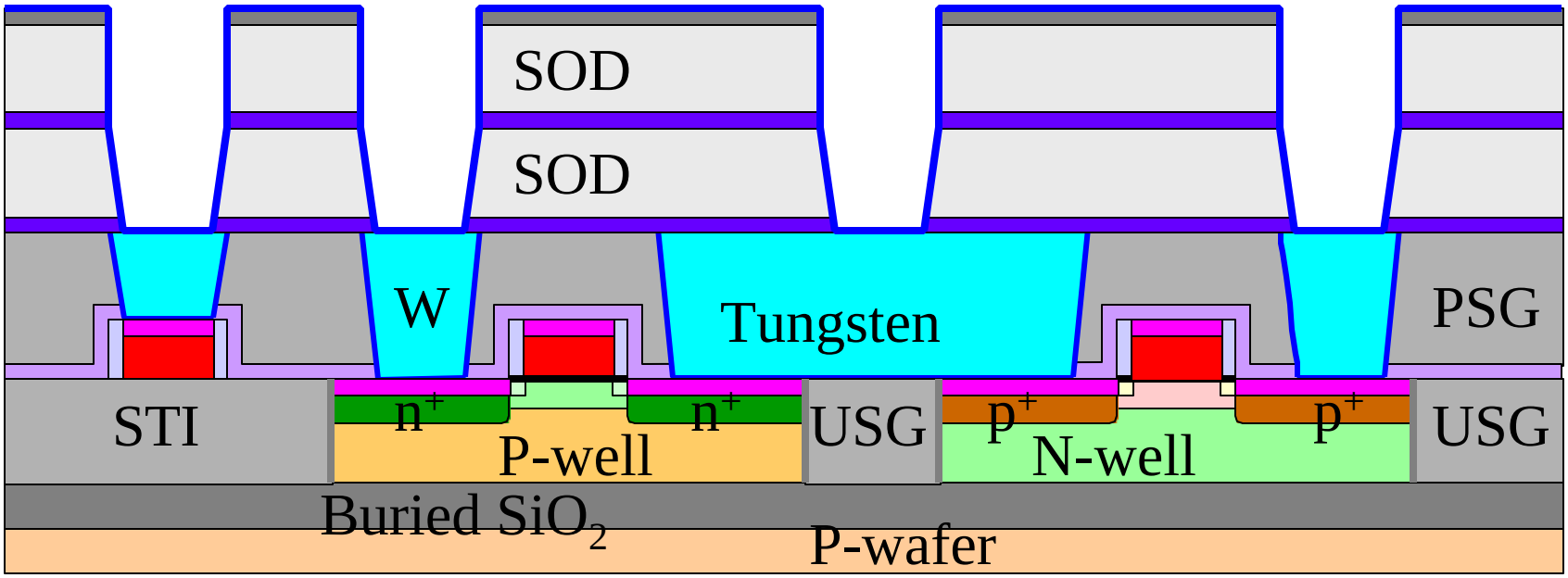
Strip Photoresist



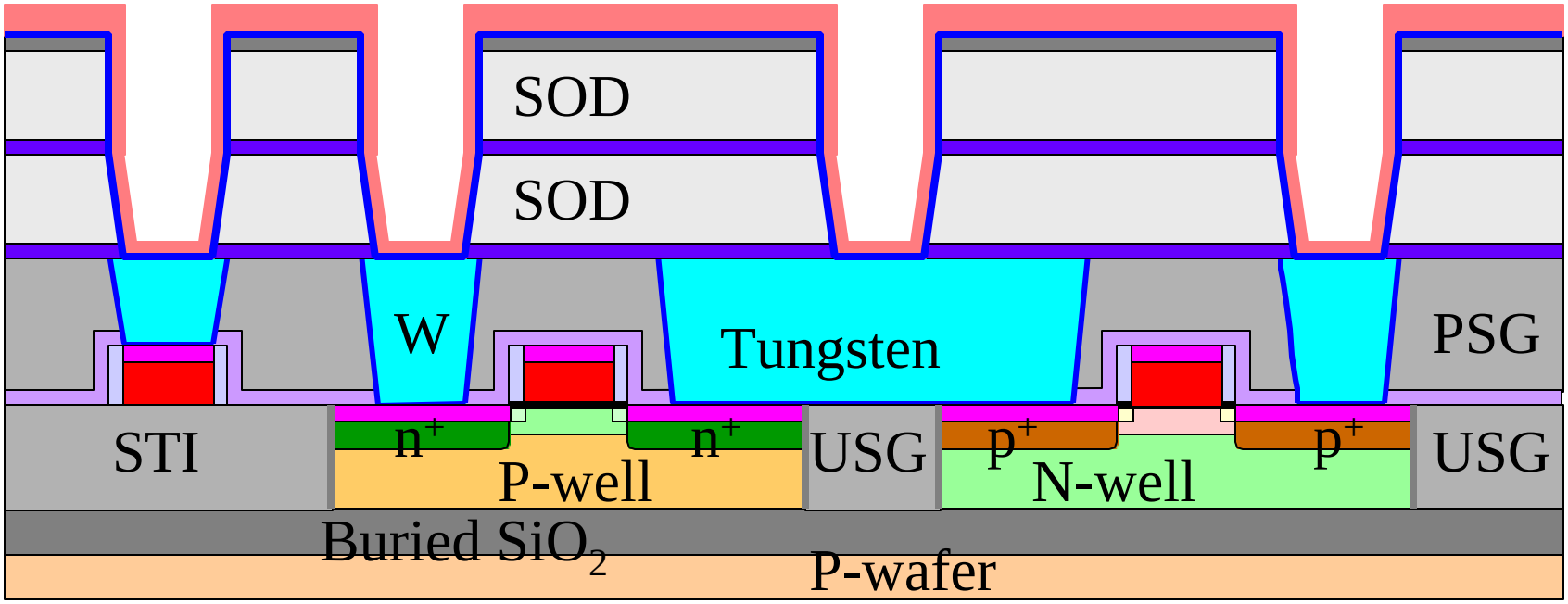
Argon Sputtering Clean



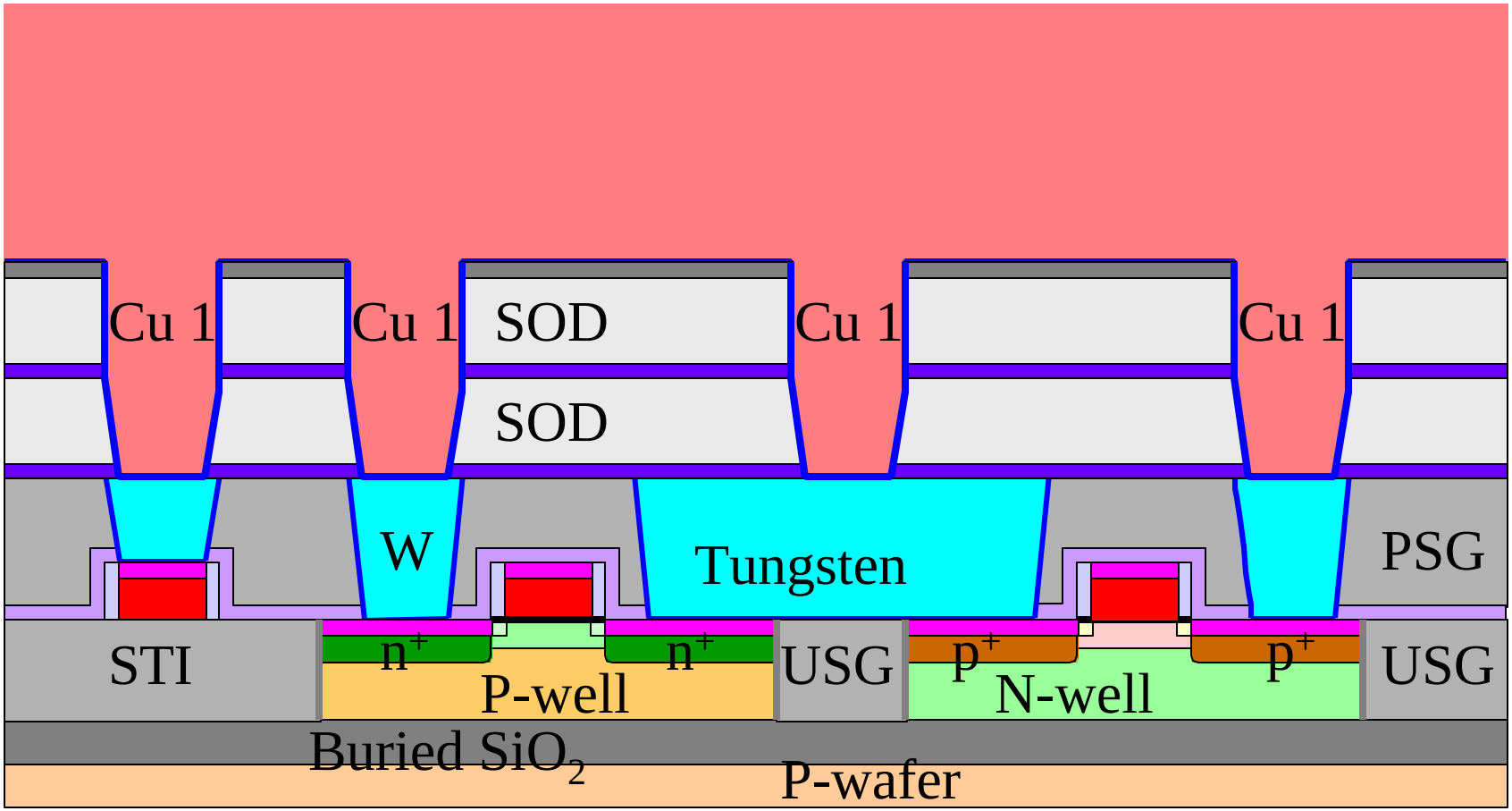
Ta and TaN Barrier Layer PVD



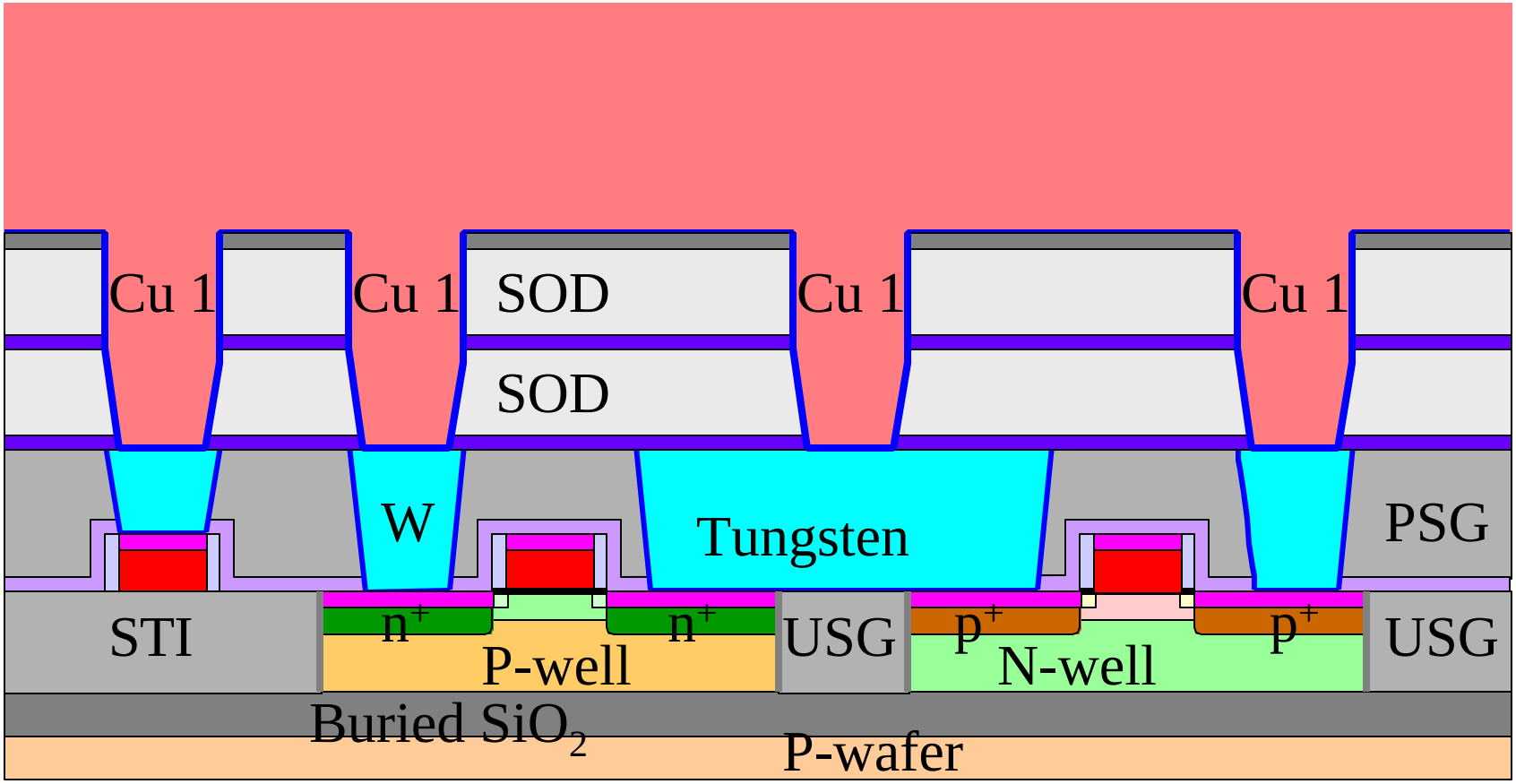
Cu Seed Layer PVD



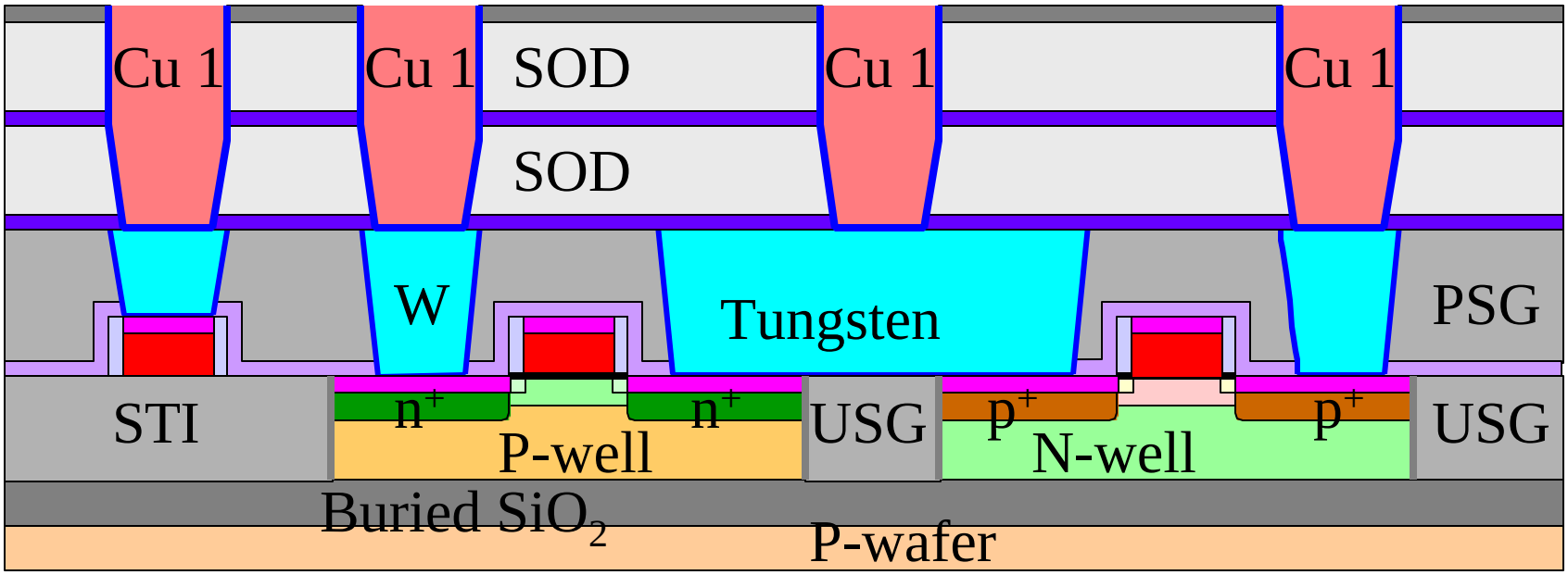
Bulk Copper Electrochemical Plating



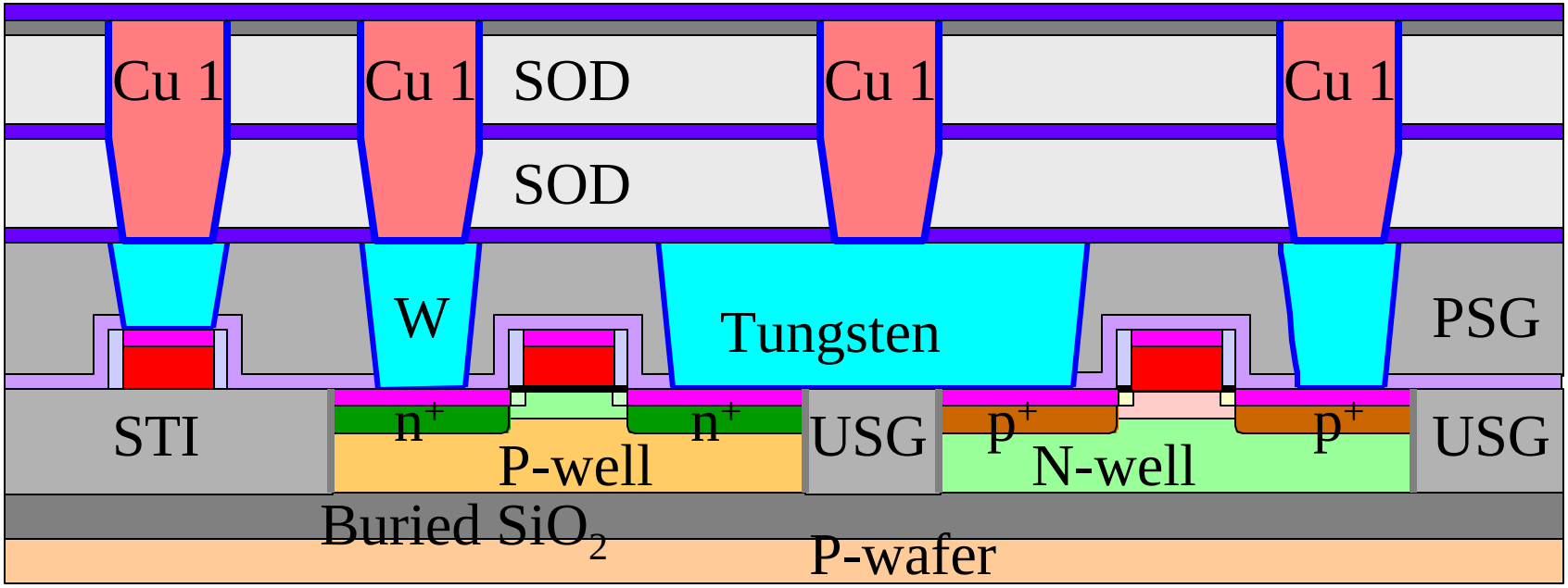
Copper Anneal



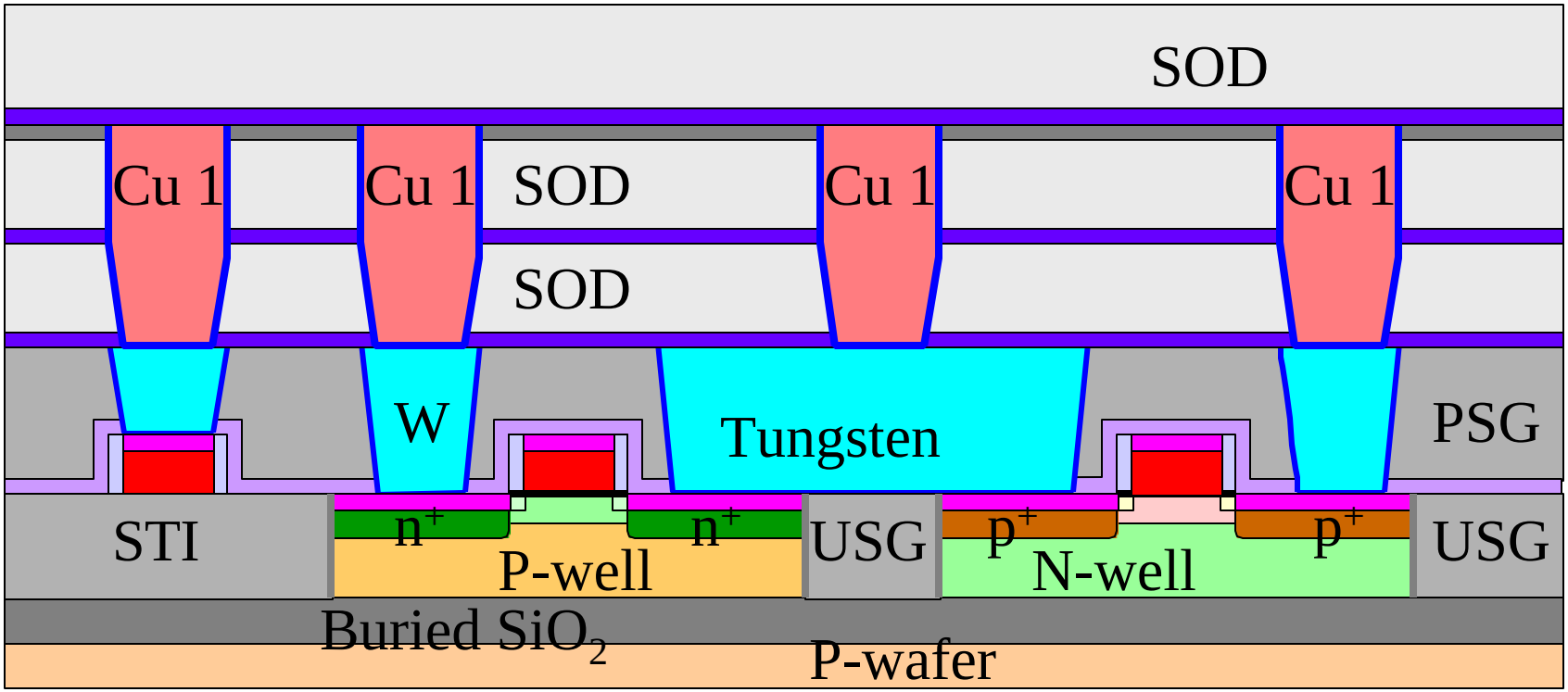
Cu, Ta, and TaN CMP



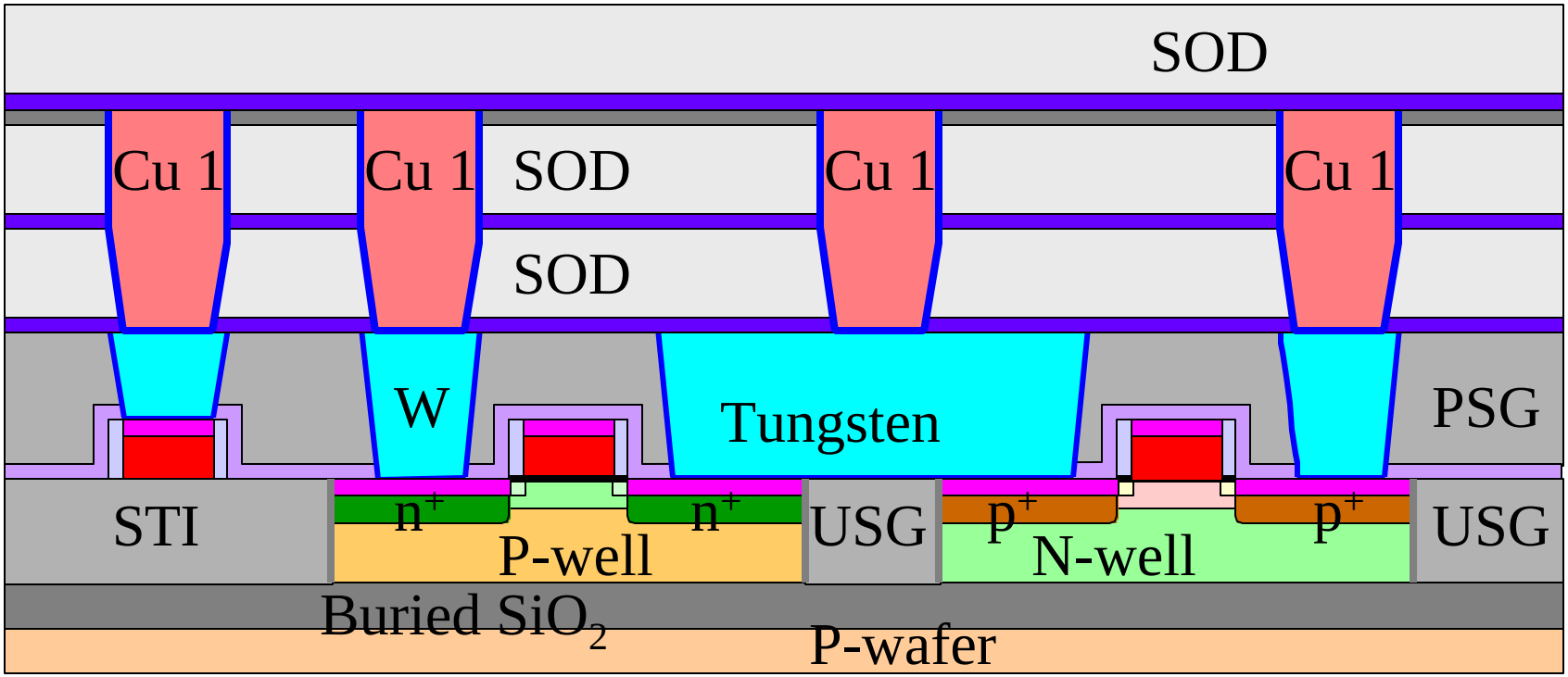
PECVD SiC Seal Layer



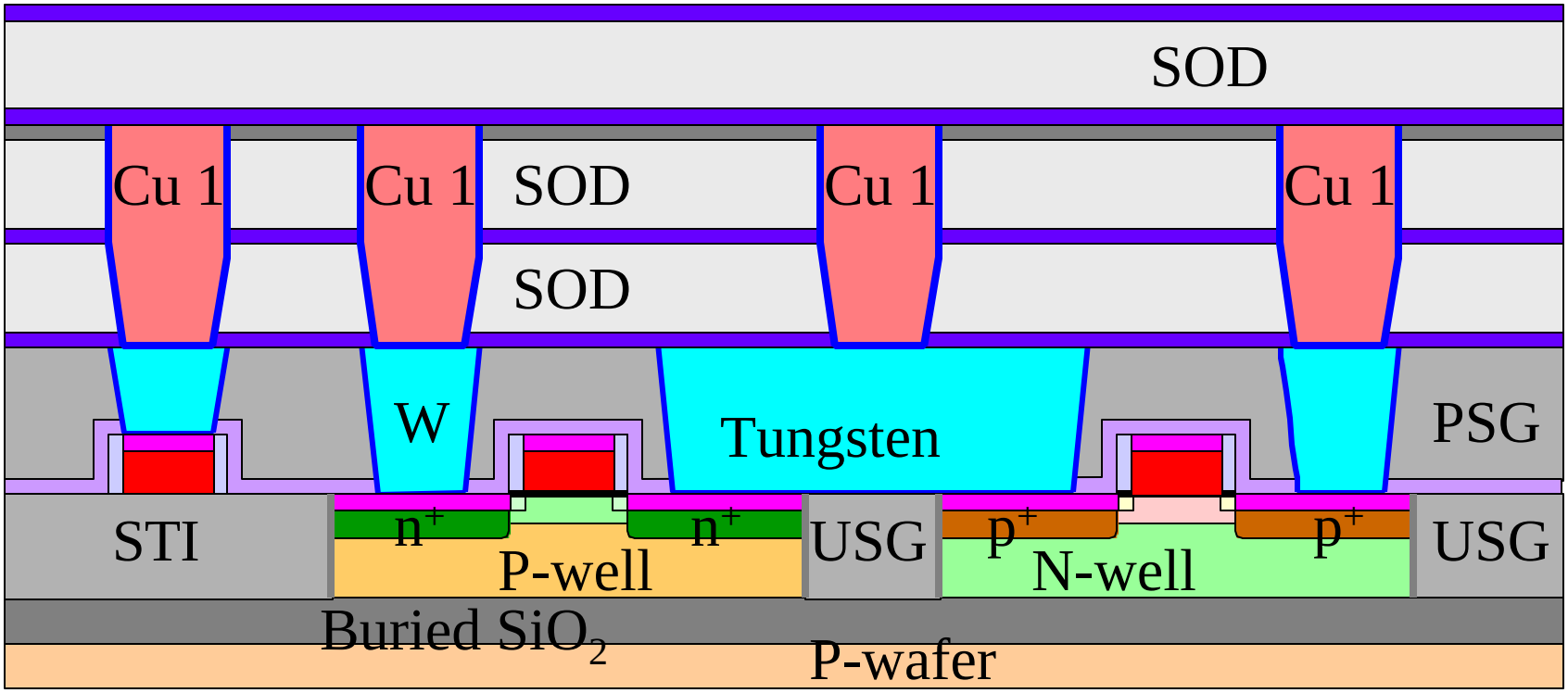
Spin-on Dielectric (SOD) Coating



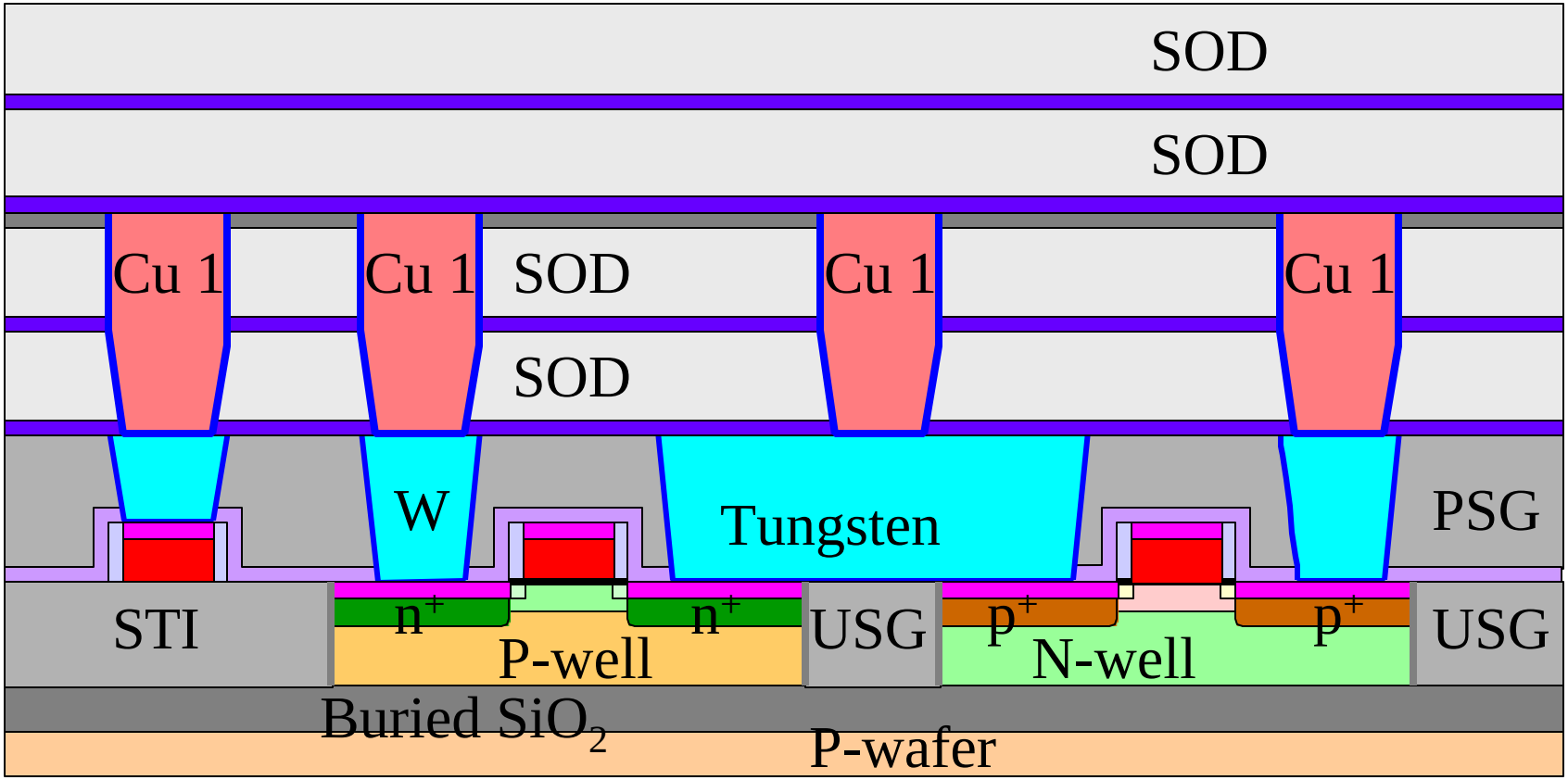
SOD Curing


SOD
Cu 1
Cu 1
SOD
Cu 1
Cu 1
SOD
W
Tungsten
PSG
STI
n+
n+
USG
p+
p+
USG
P-well
N-well
Buried SiO2
P-wafer

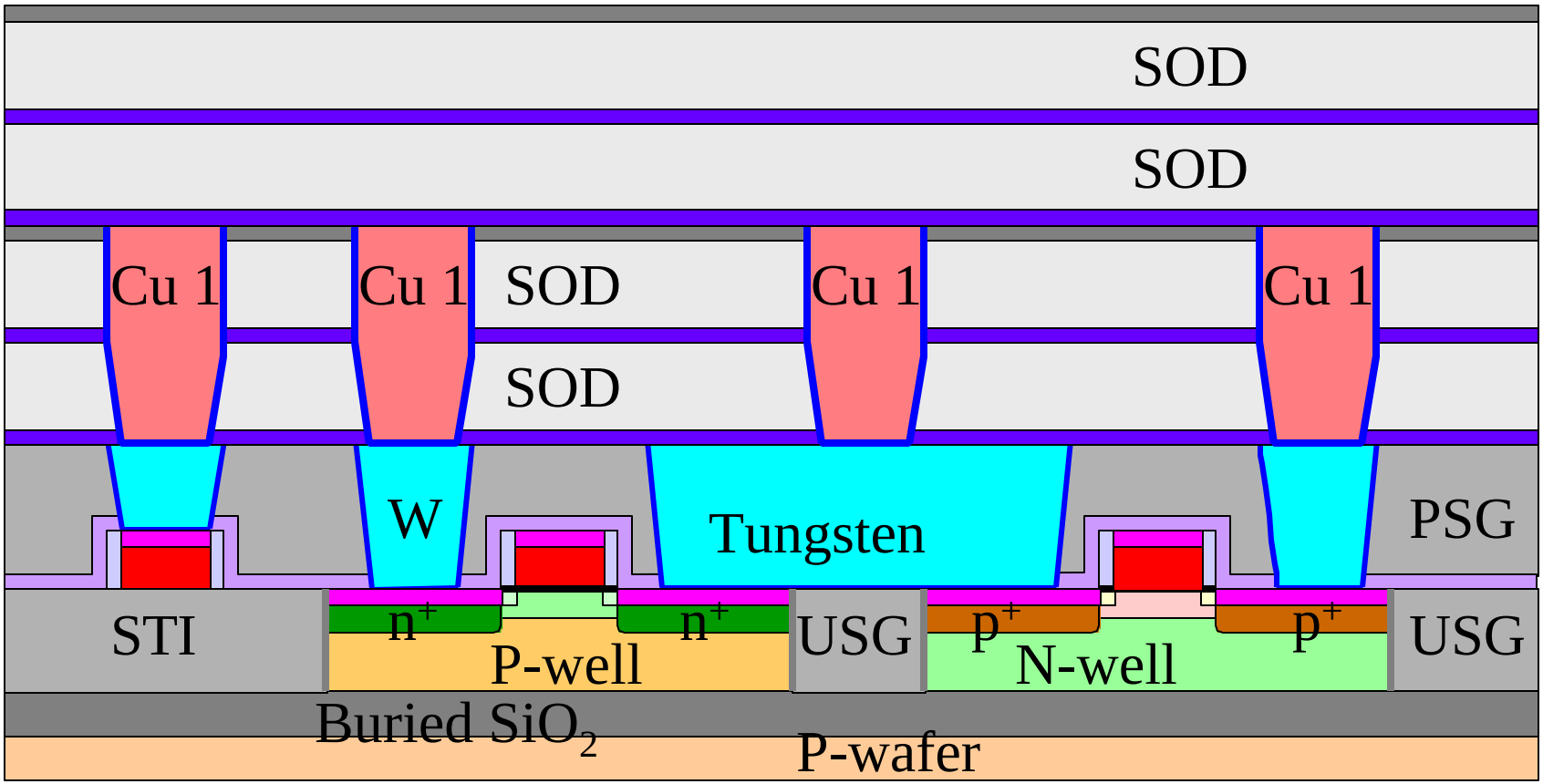
PECVD SiC Etch Stop Layer



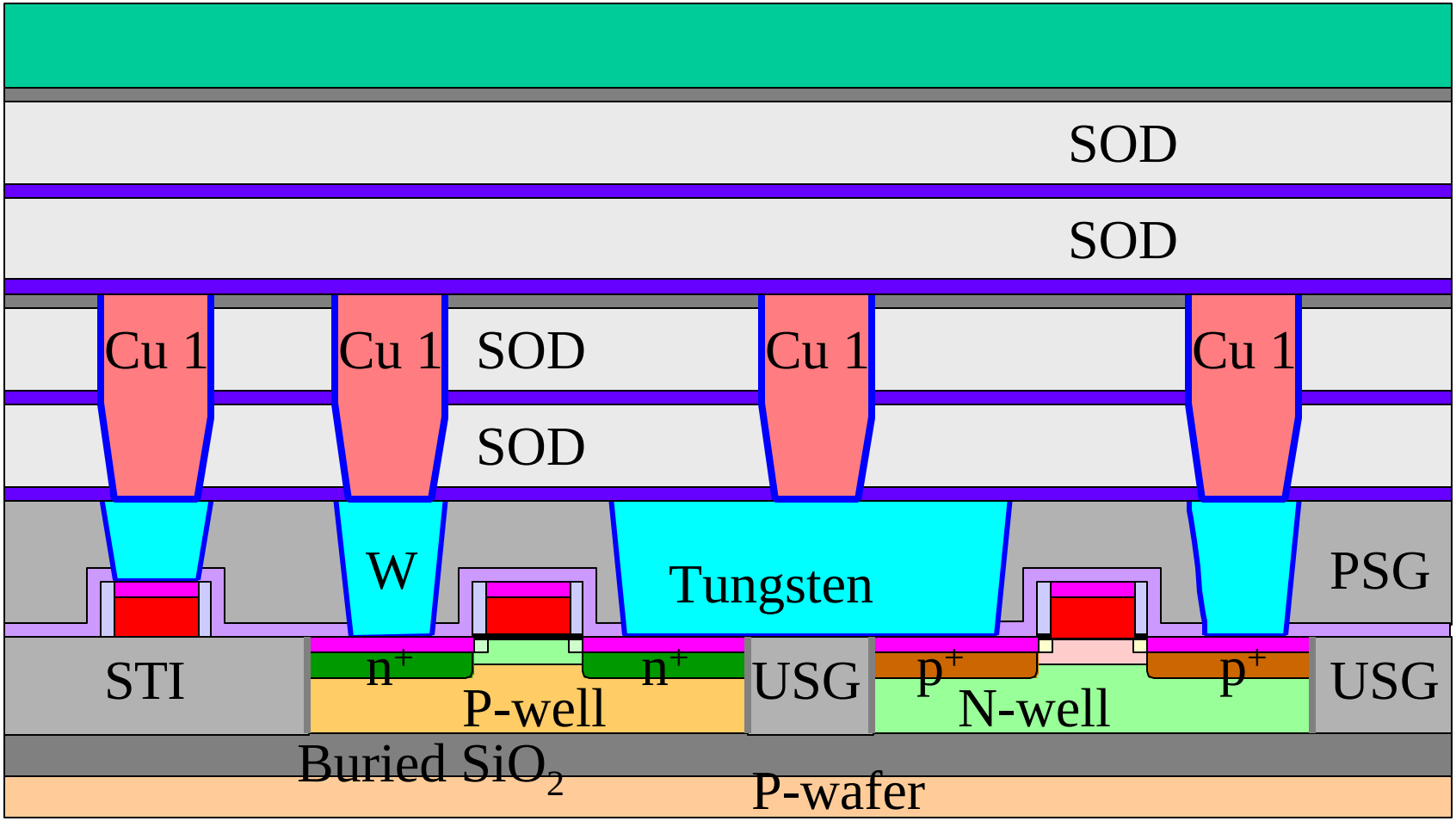
SOD Coating and Curing



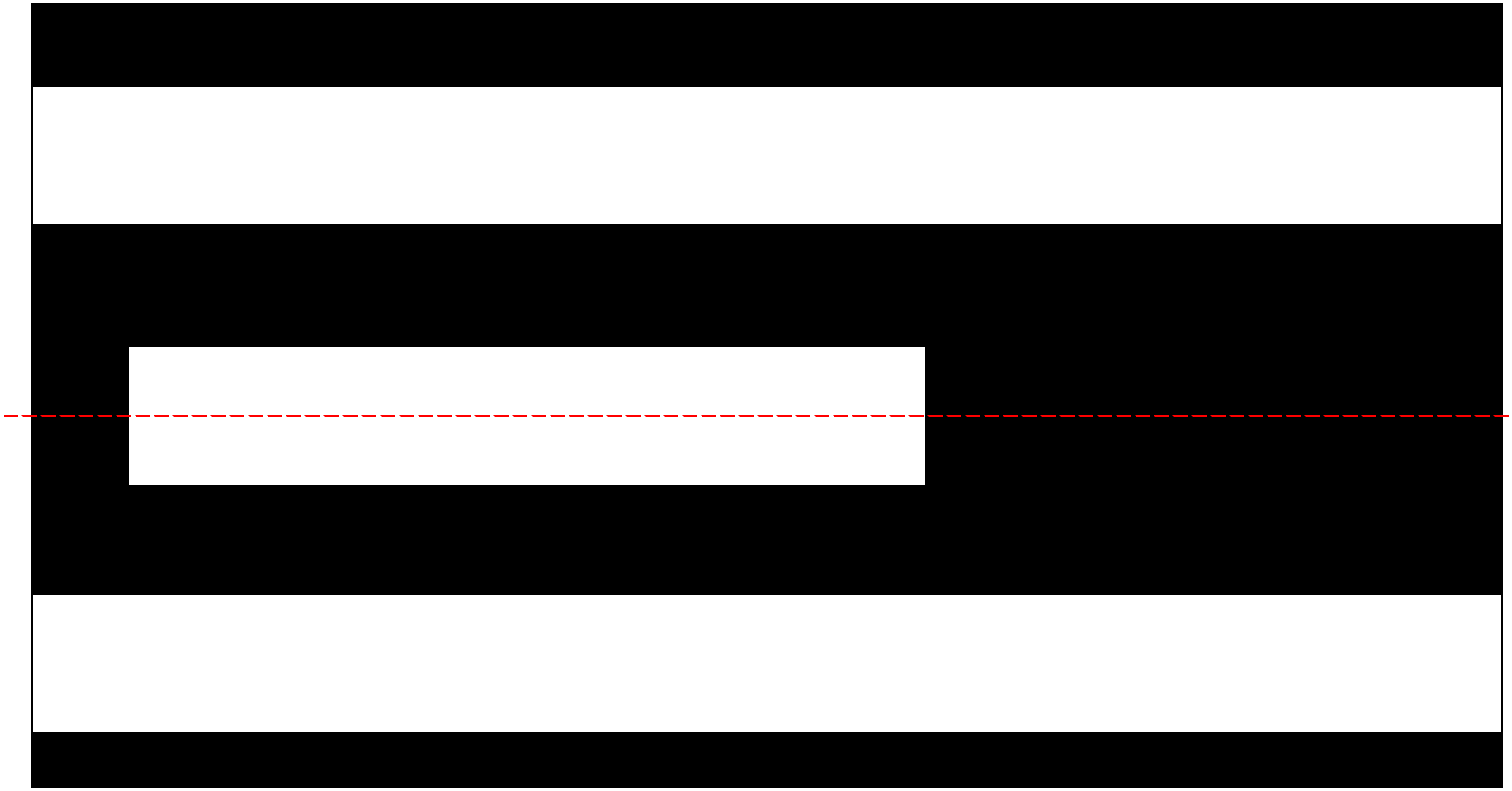
PE-TEOS Cap


SOD
SOD
Cu 1
Cu 1
SOD
Cu 1
Cu 1
SOD
W
Tungsten
PSG
STI
n+
n+
USG
p+
p+
USG
P-well
N-well
Buried SiO2
P-wafer

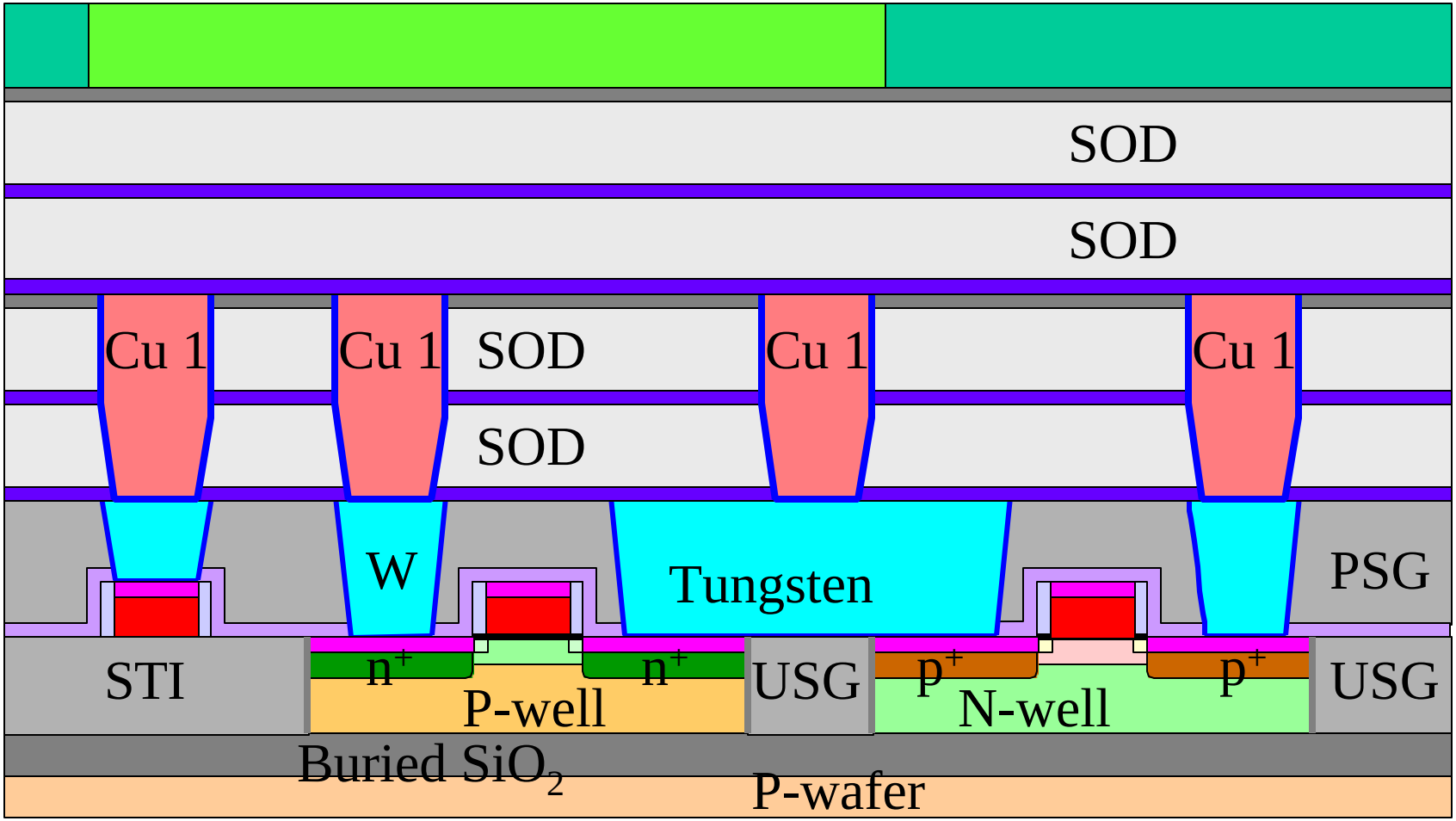
Photoresist Coating and Baking



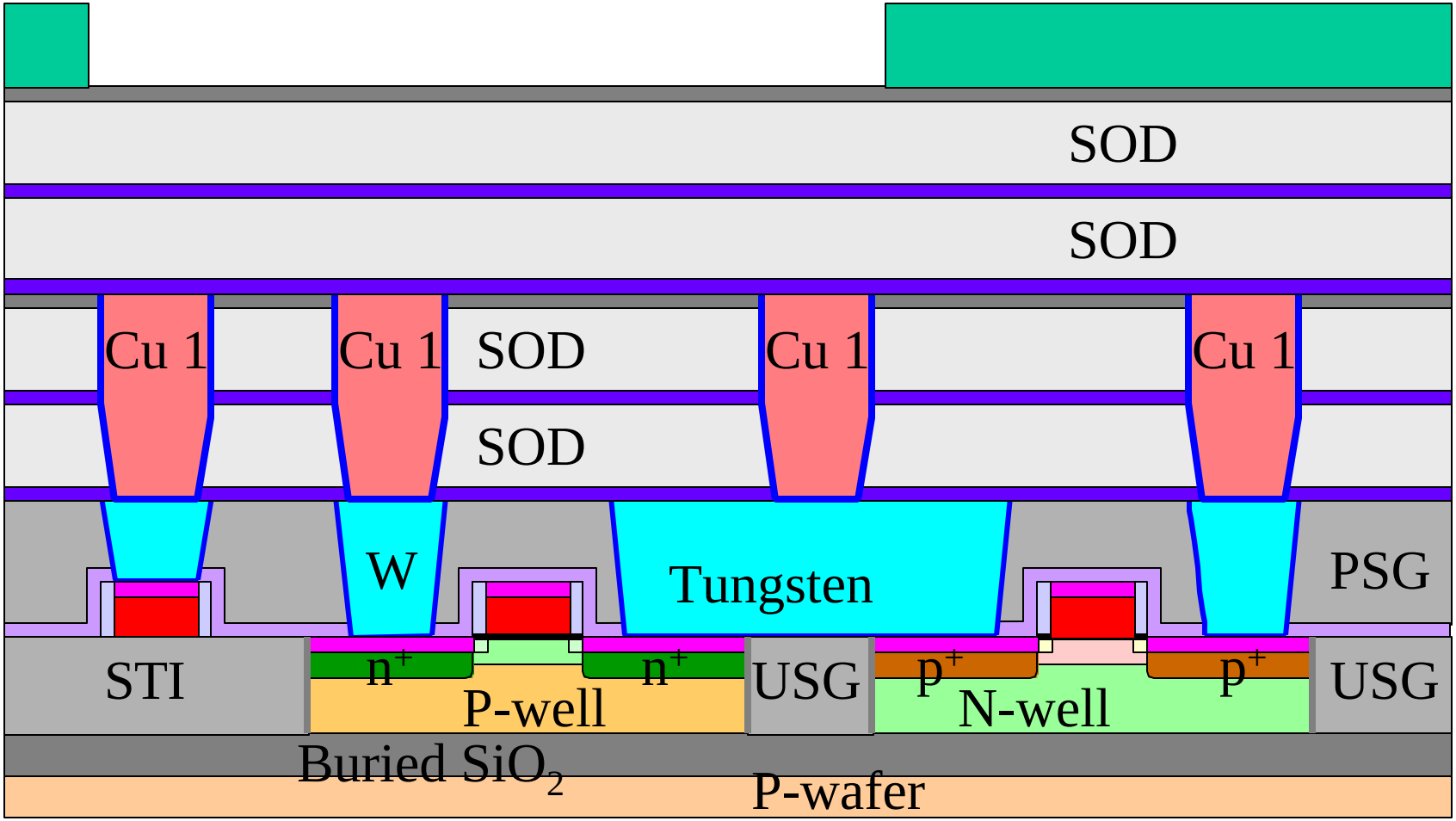
Mask 12, Metal Trench 2



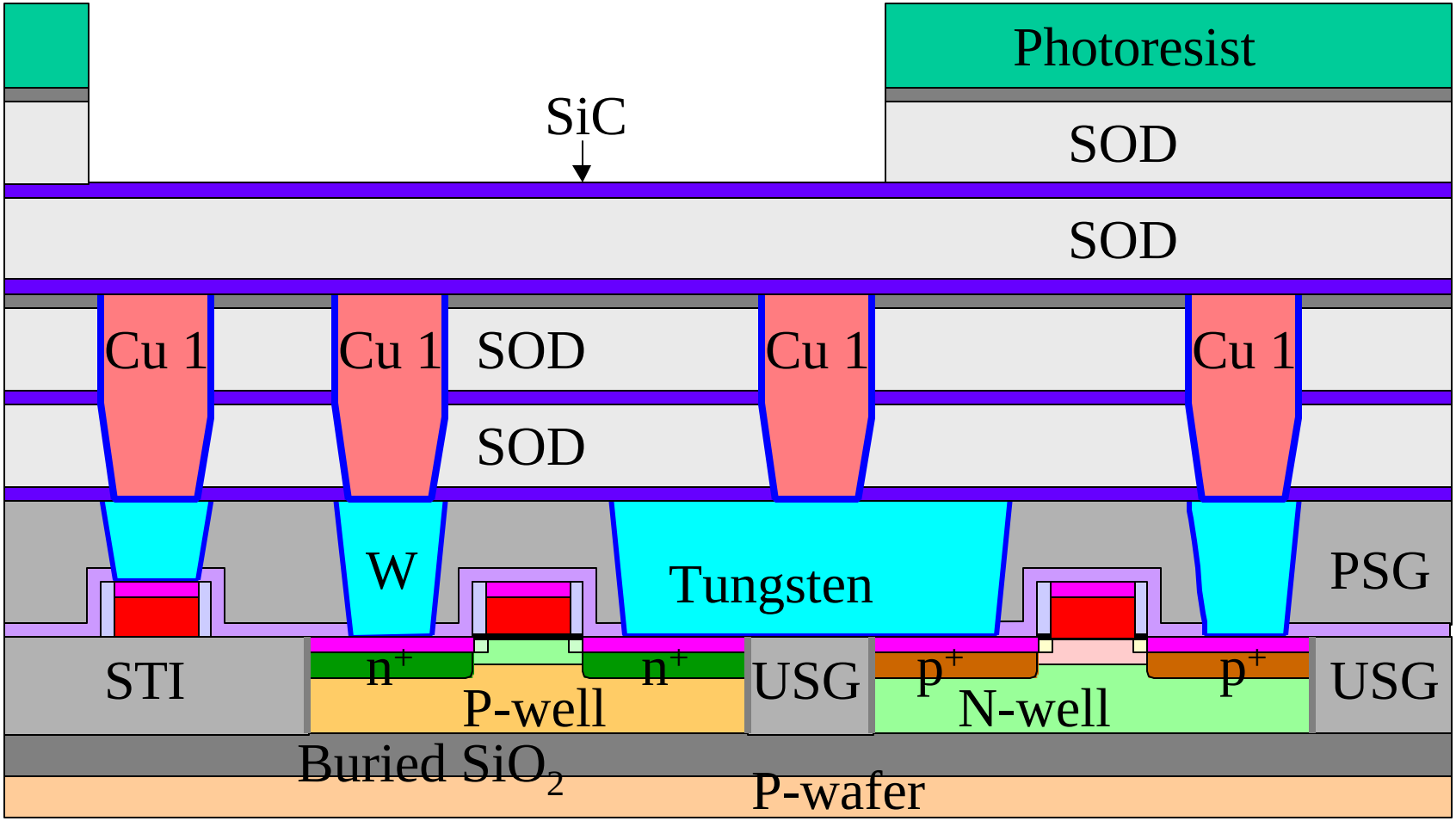
Alignment and Exposure



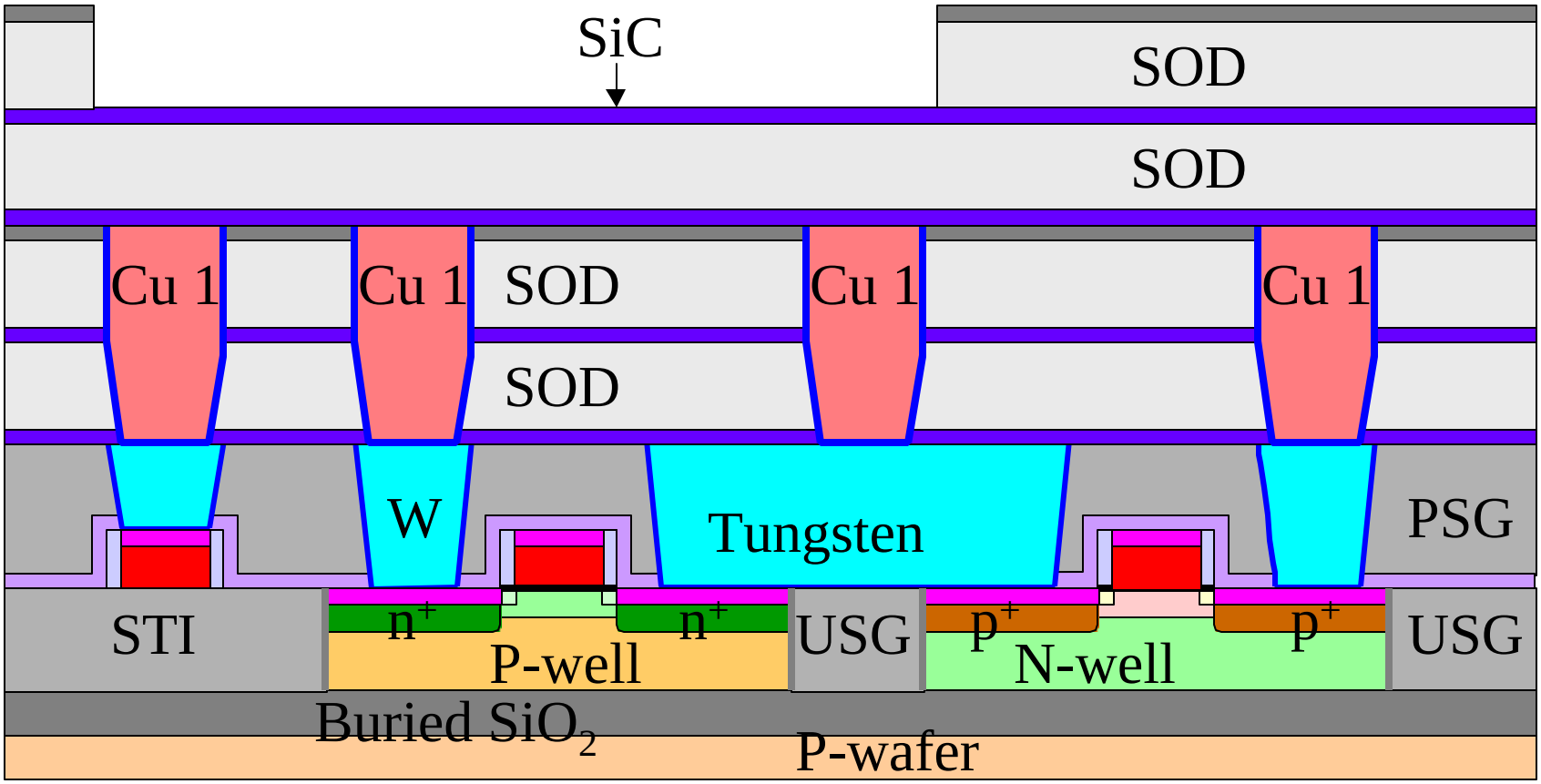
PEB, Development, and Inspection



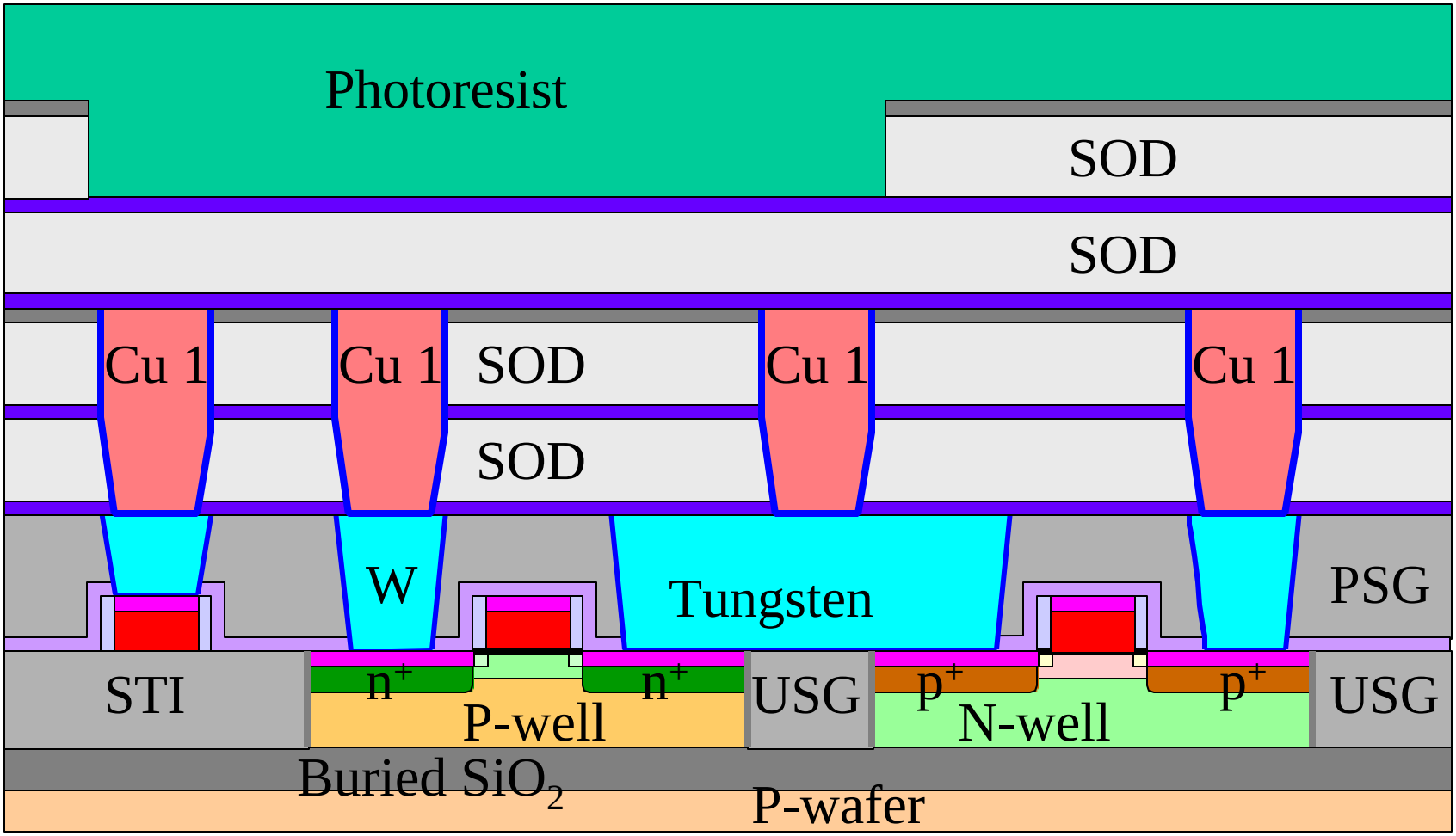
Etch Trench, Stop on SiC Layer



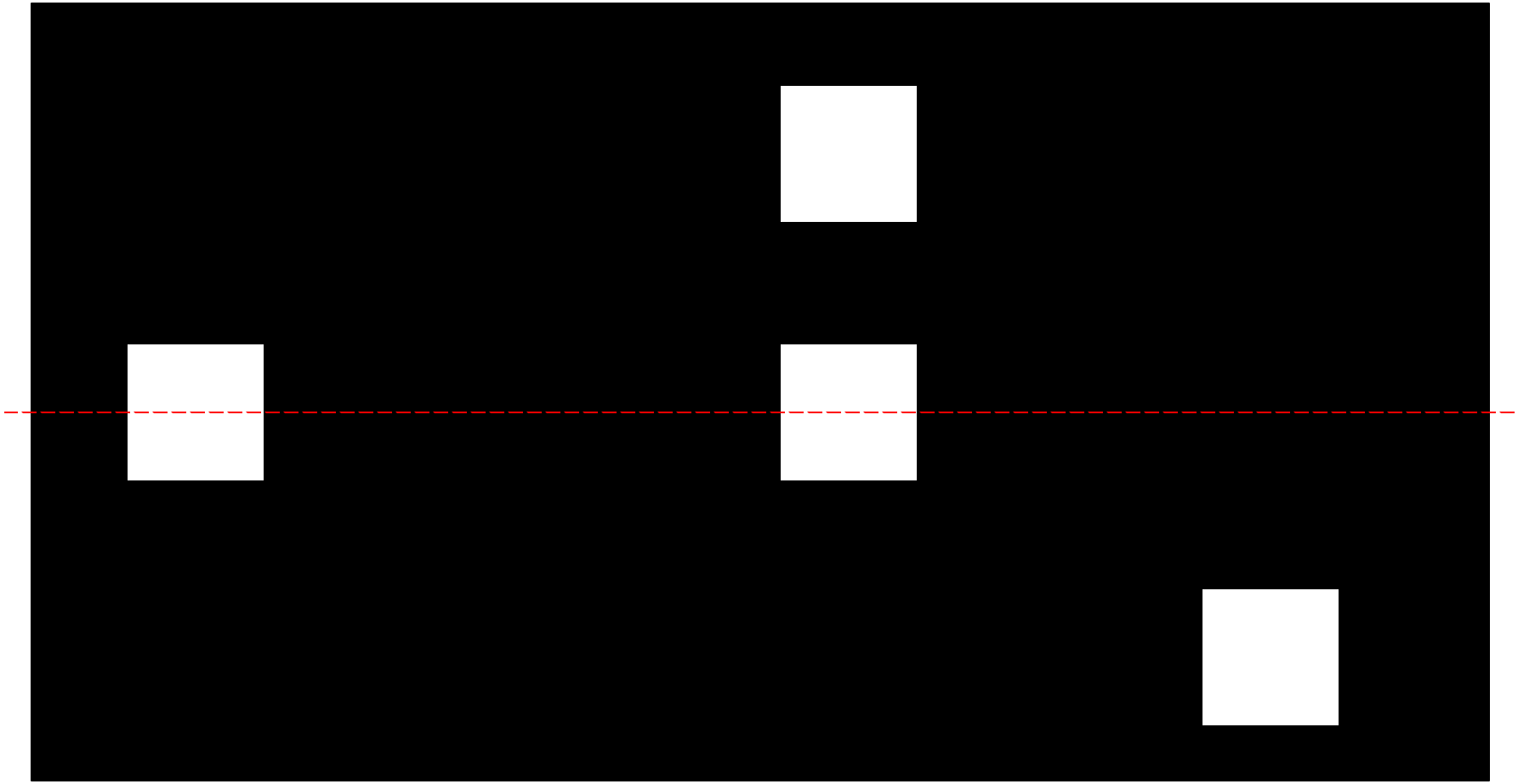
Strip Photoresist



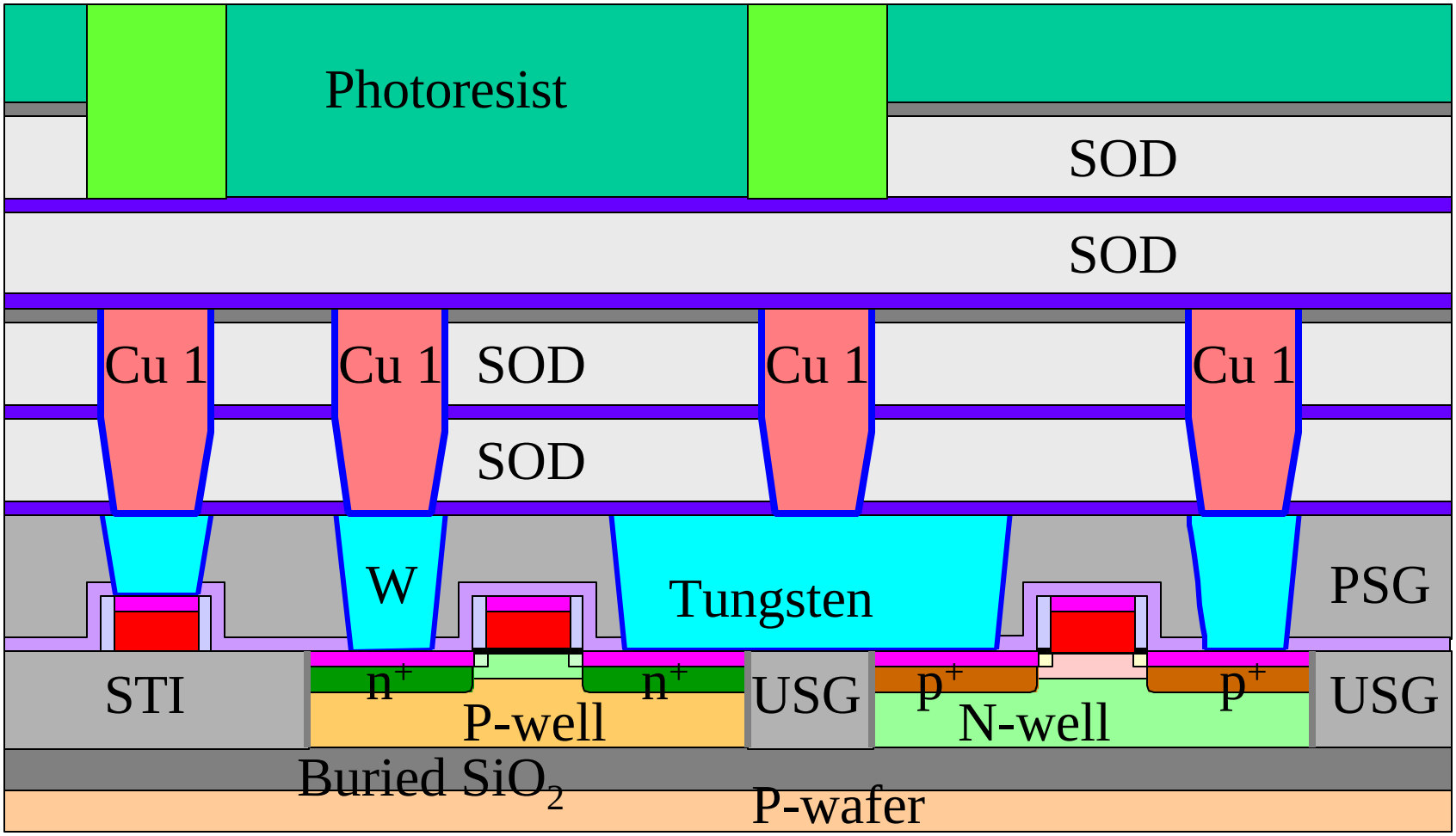
Photoresist Coating and Baking



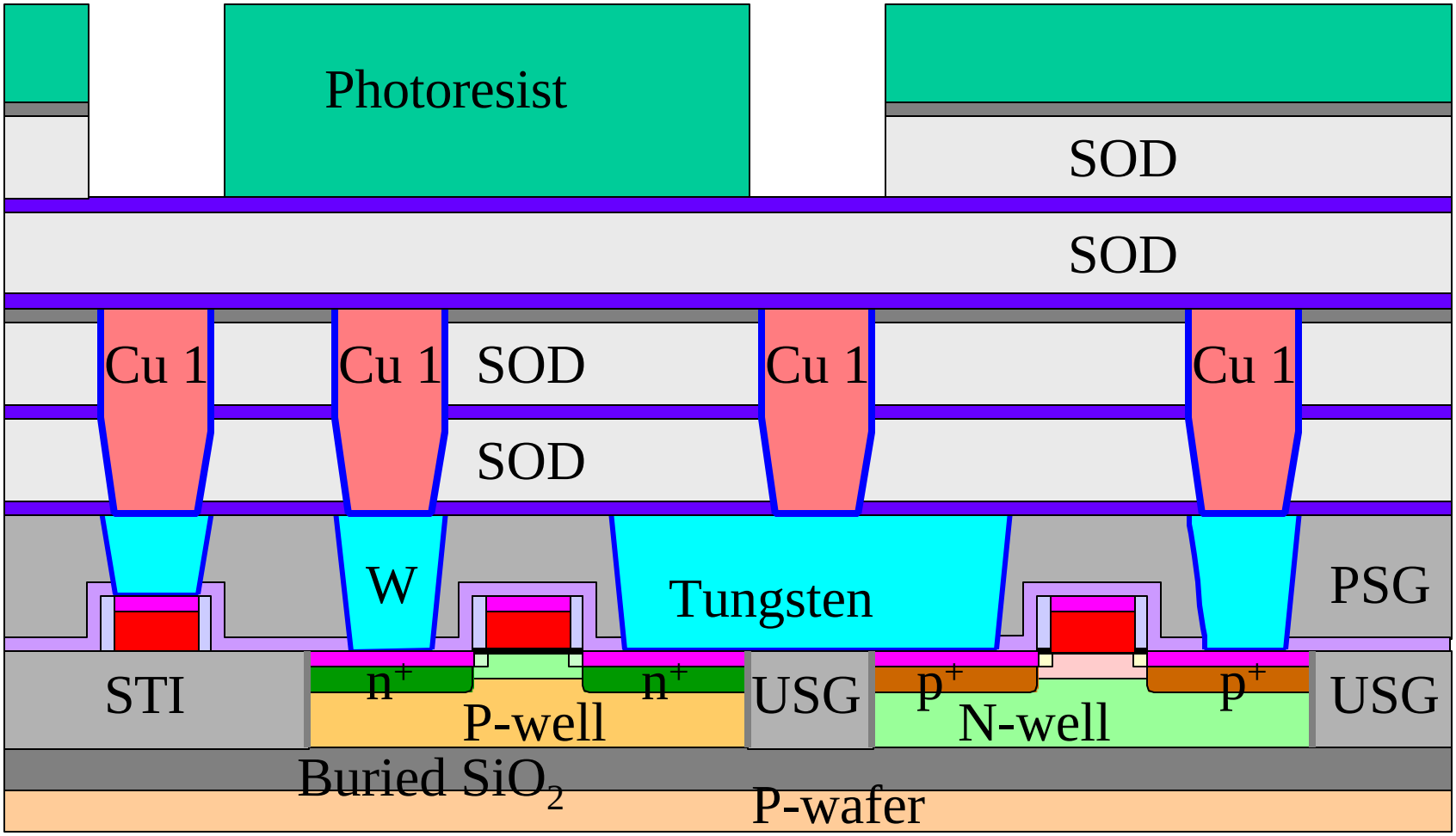
Mask 13, Via 2



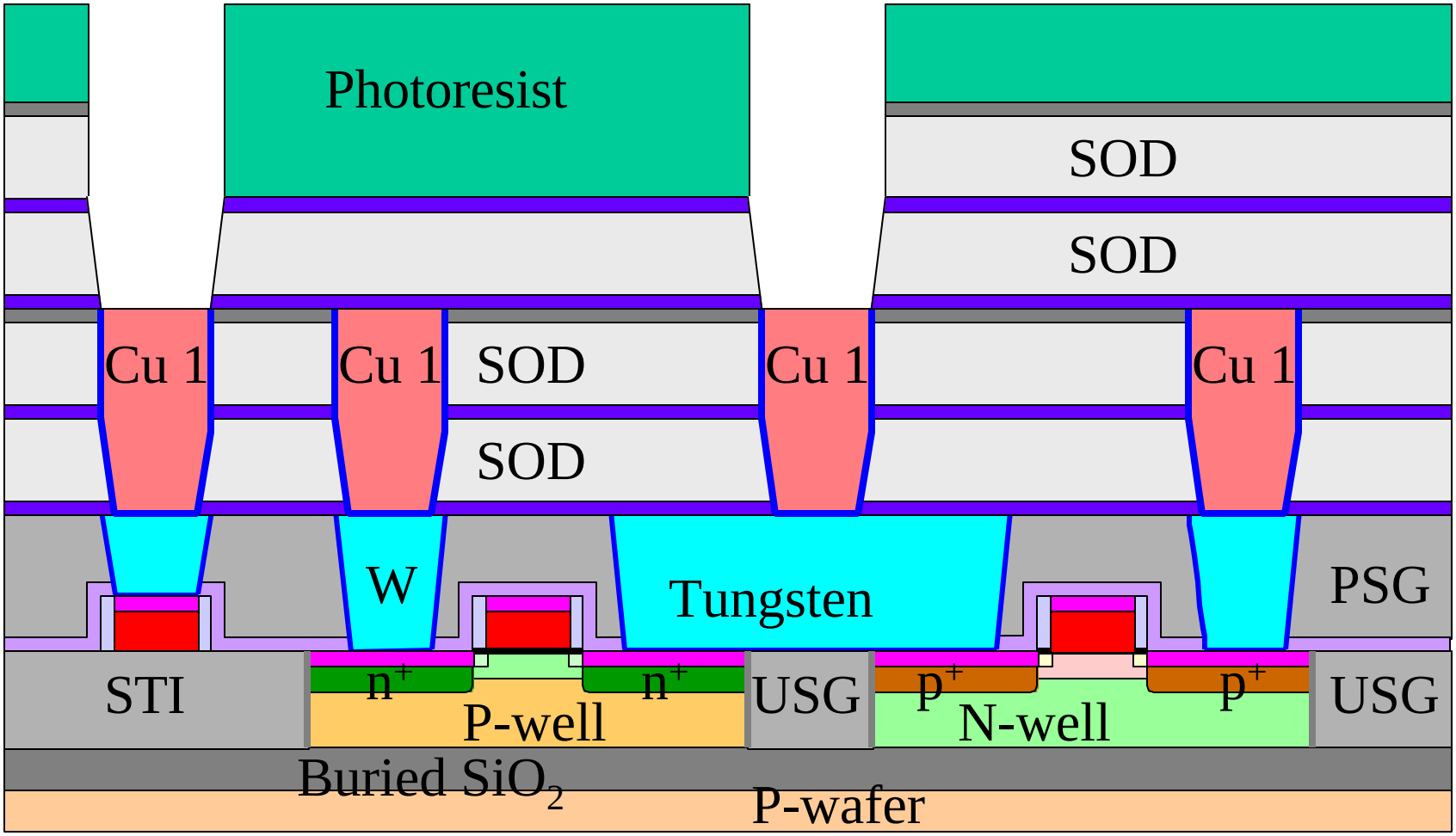
Alignment and Exposure



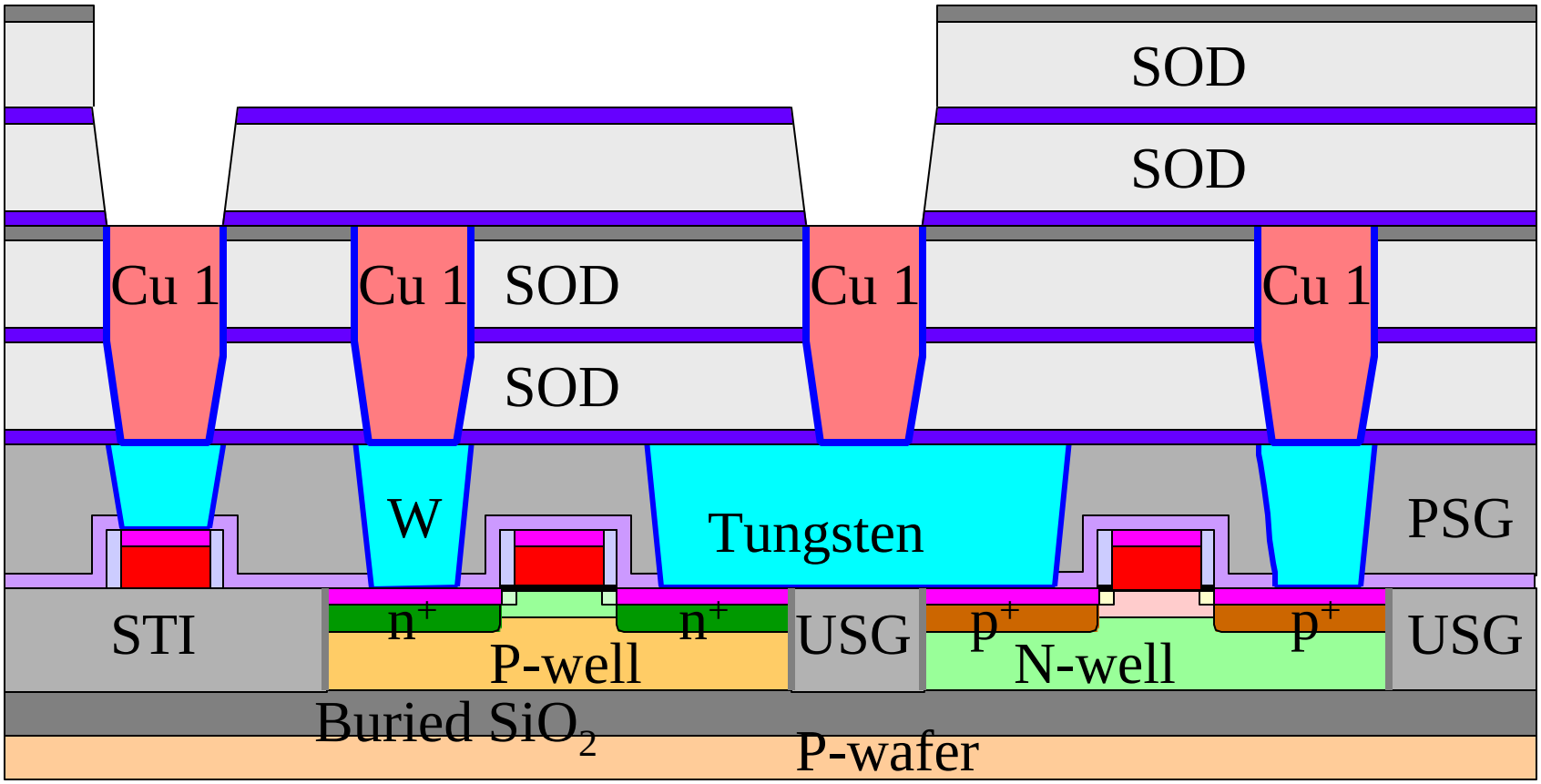
PEB, Development, and Inspection



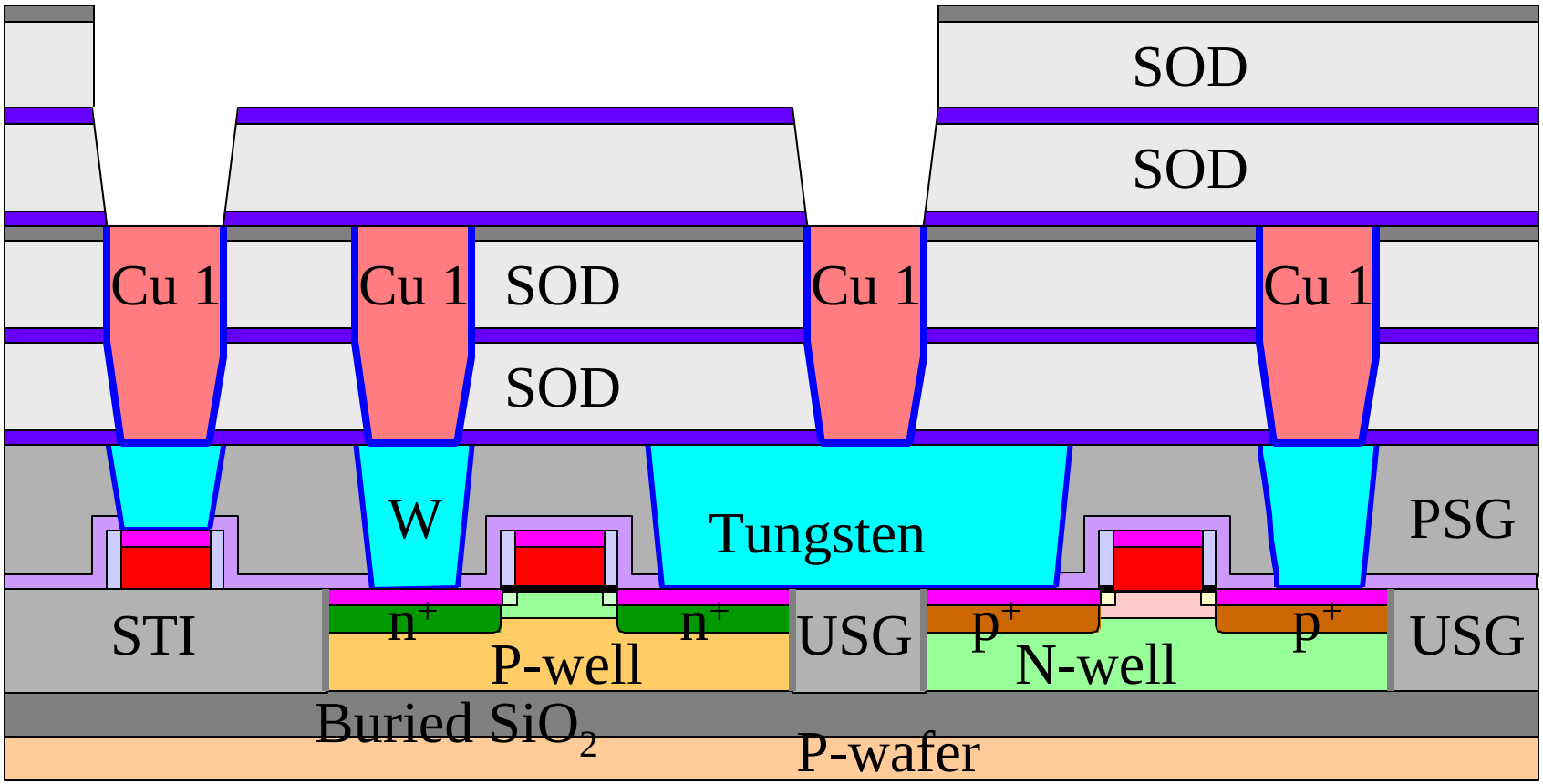
Via2 Etch


Photoresist
SOD
SOD
Cu 1
Cu 1
SOD
Cu 1
Cu 1
SOD
W
Tungsten
PSG
STI
n+
n+
USG
p+
p+
USG
P-well
N-well
Buried SiO2
P-wafer

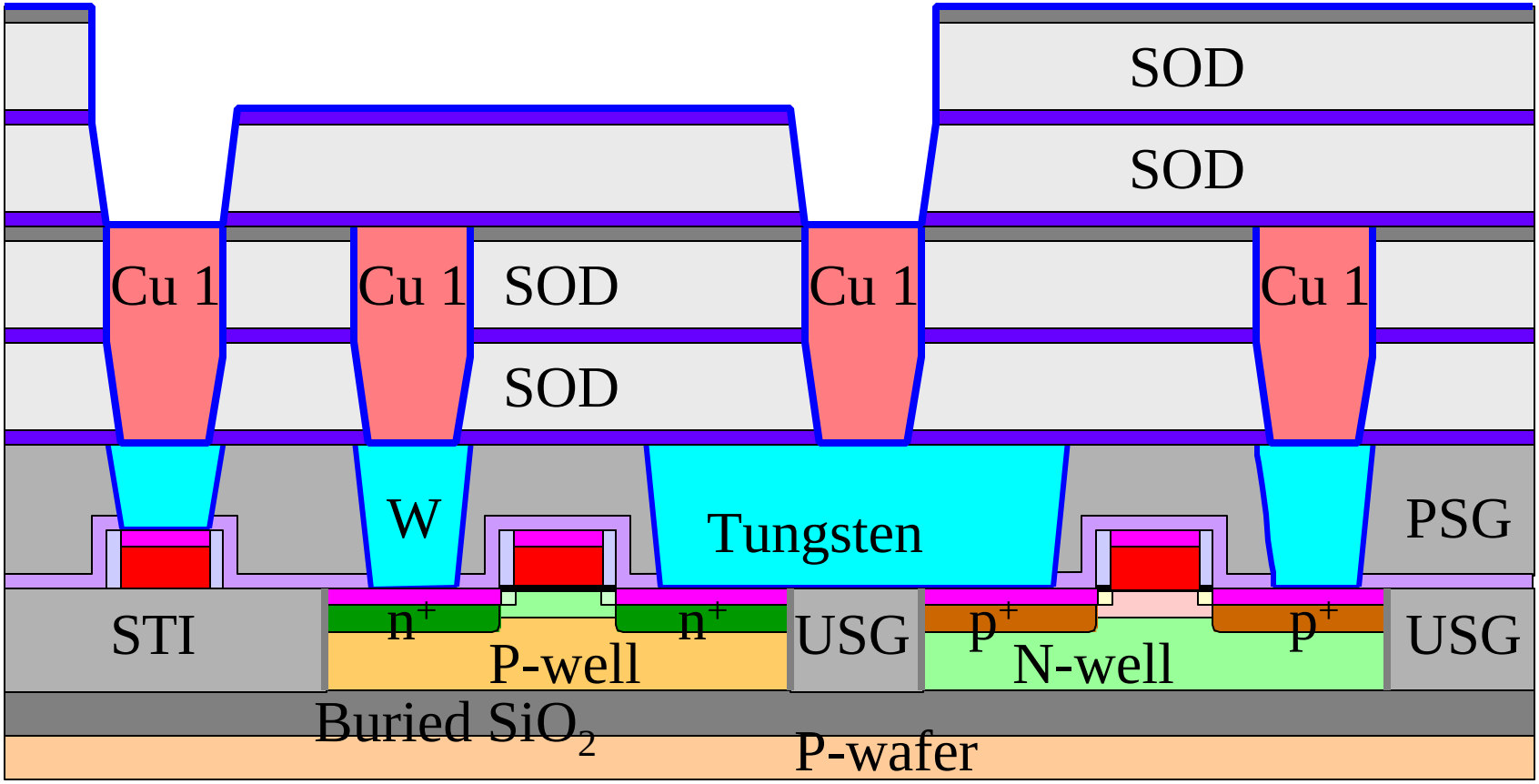
Strip Photoresist



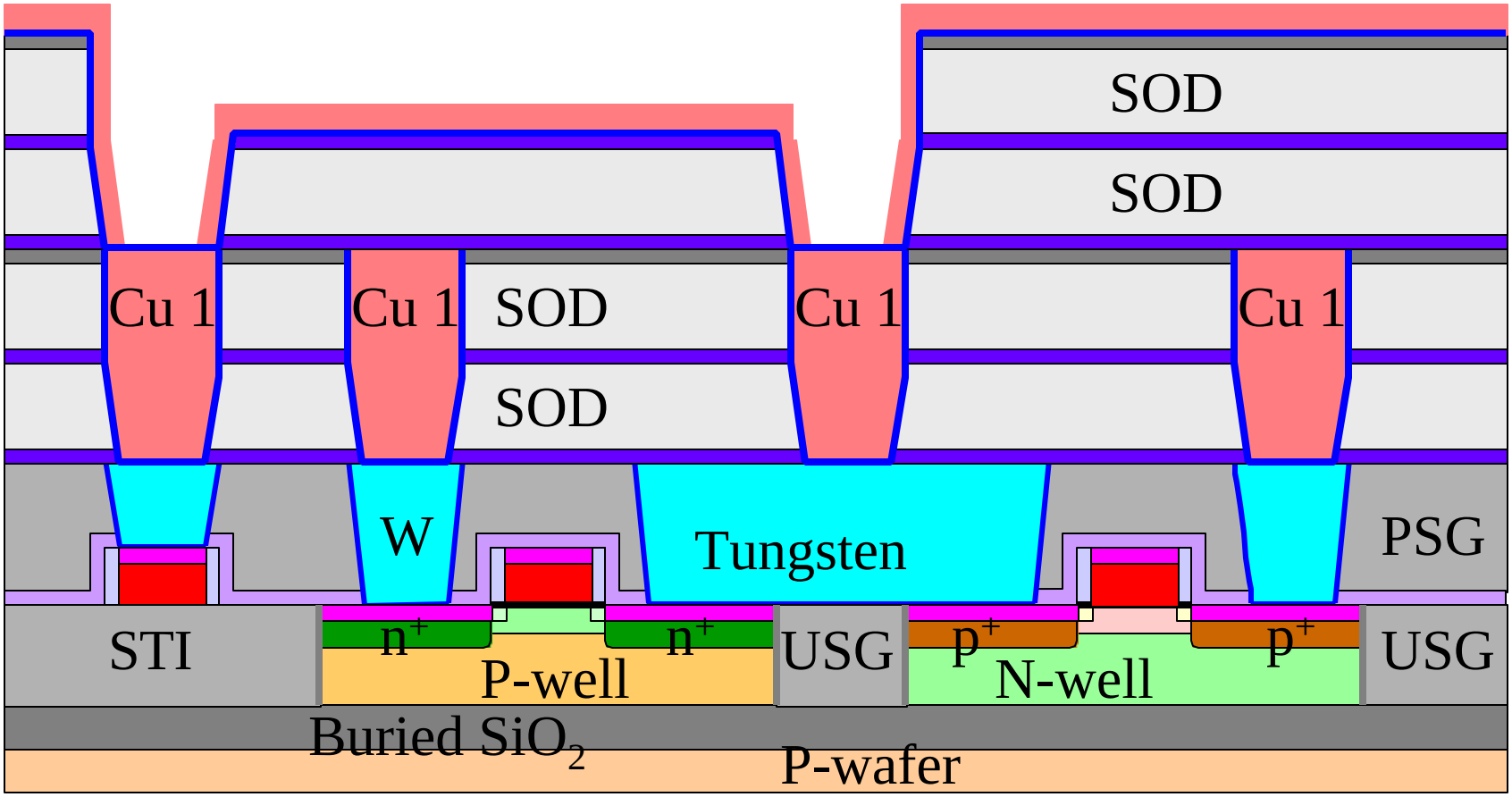
Hydrogen Plasma Clean



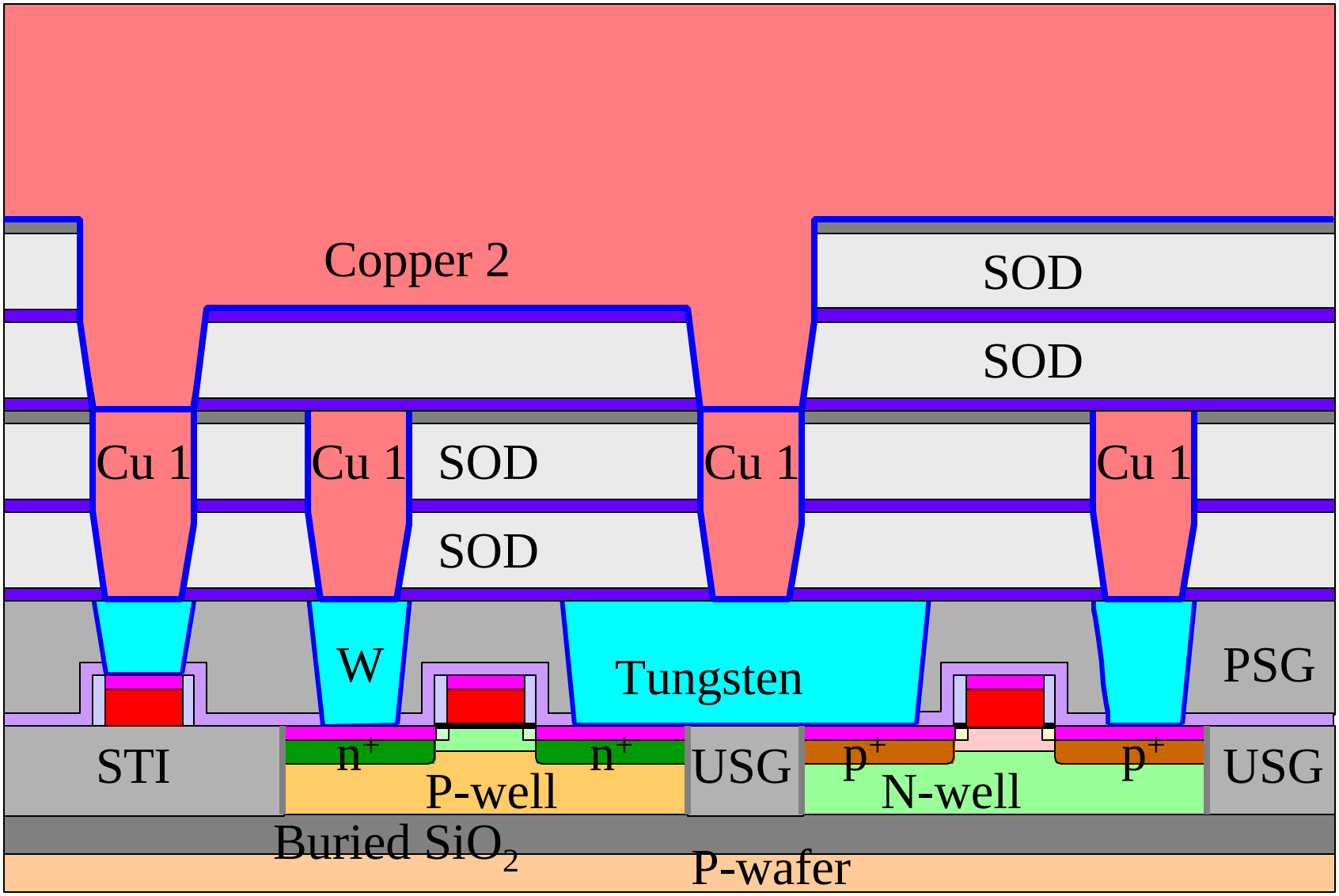
Ta and TaN Barrier Layer PVD



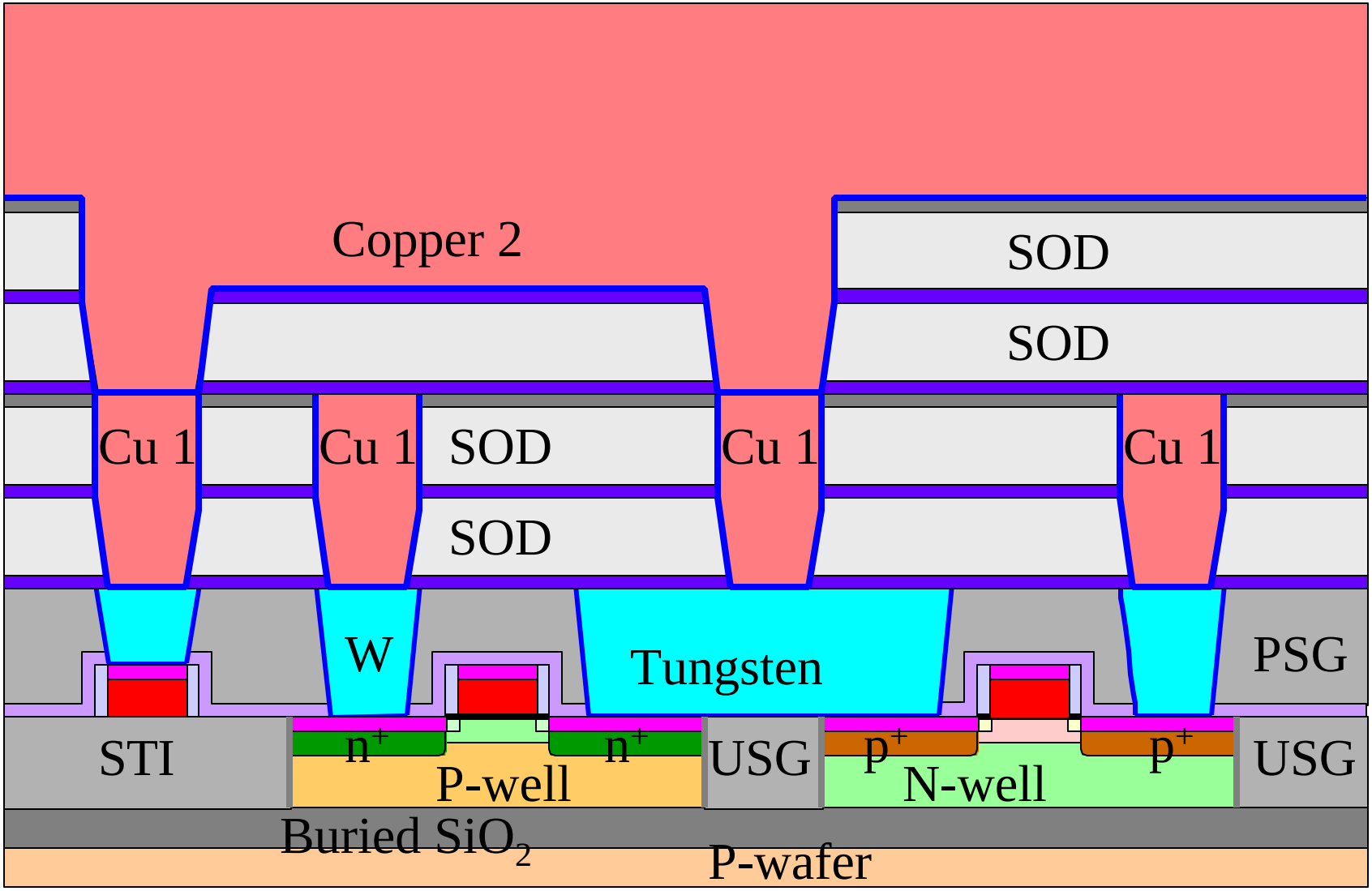
Cu Seed Layer PVD



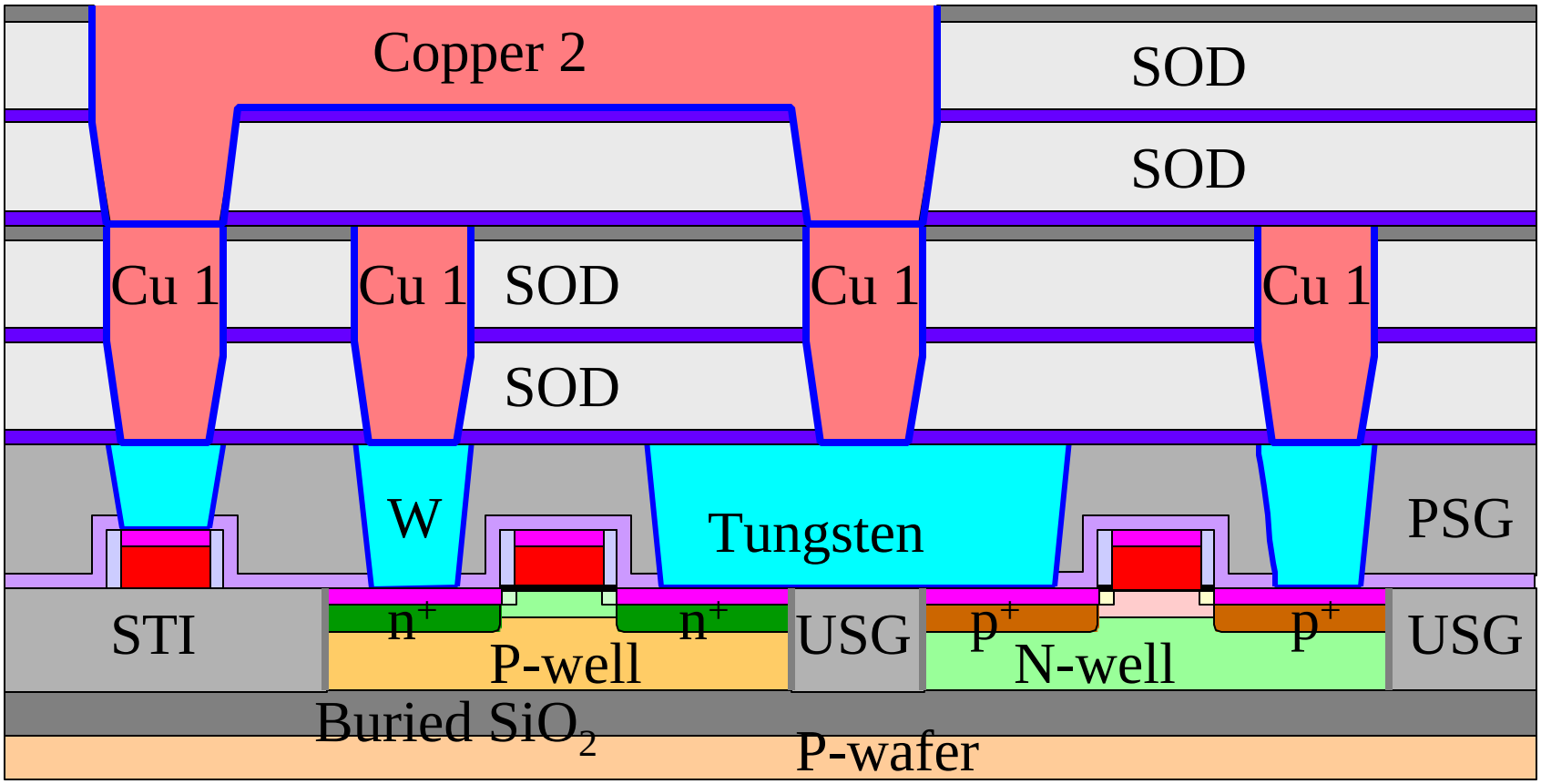
Bulk Cu ECP


Copper 2
SOD
SOD
Cu 1
Cu 1
SOD
Cu 1
Cu 1
SOD
W
Tungsten
PSG
STI
n+
n+
USG
p+
p+
USG
P-well
N-well
Buried SiO2
P-wafer

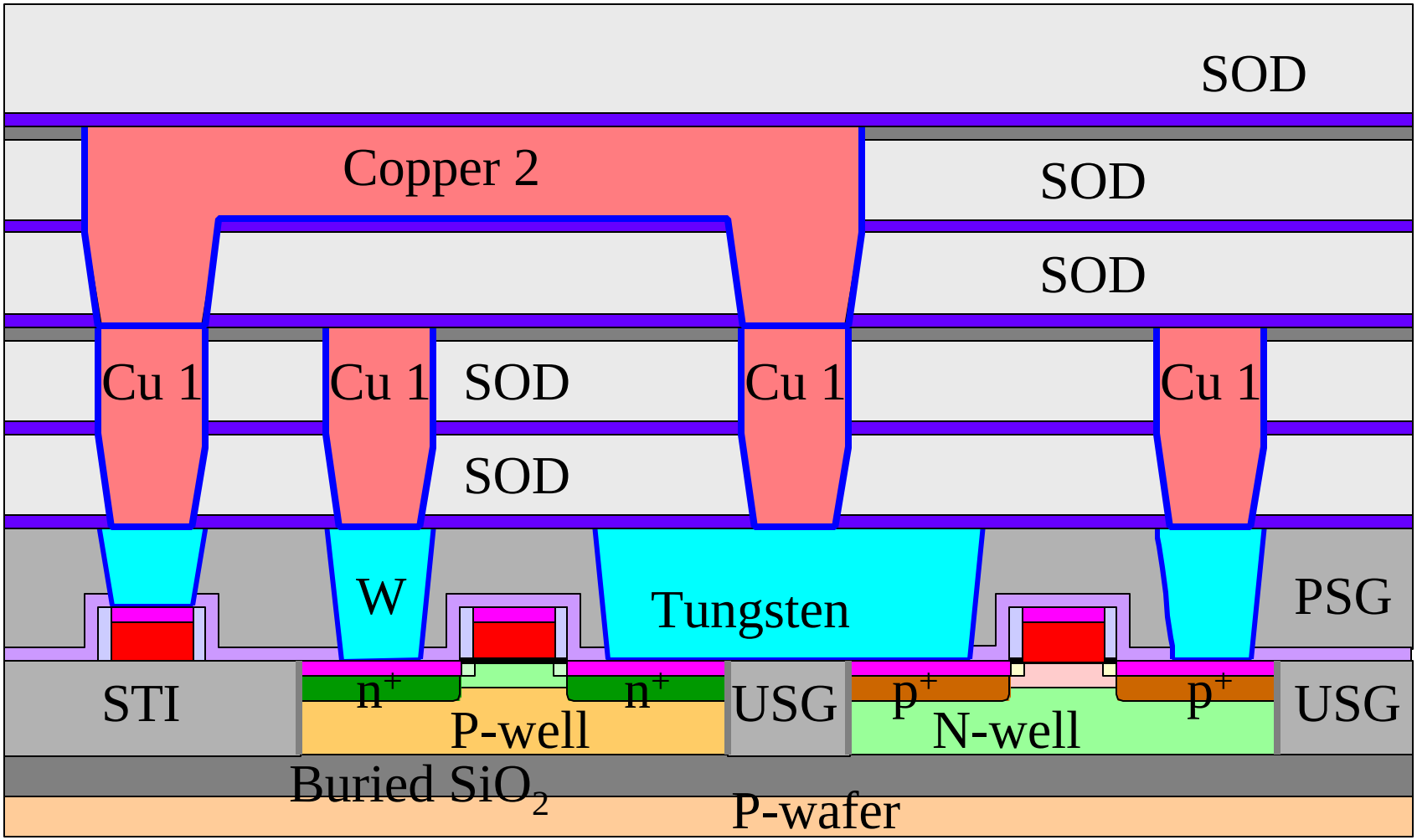
Copper Anneal



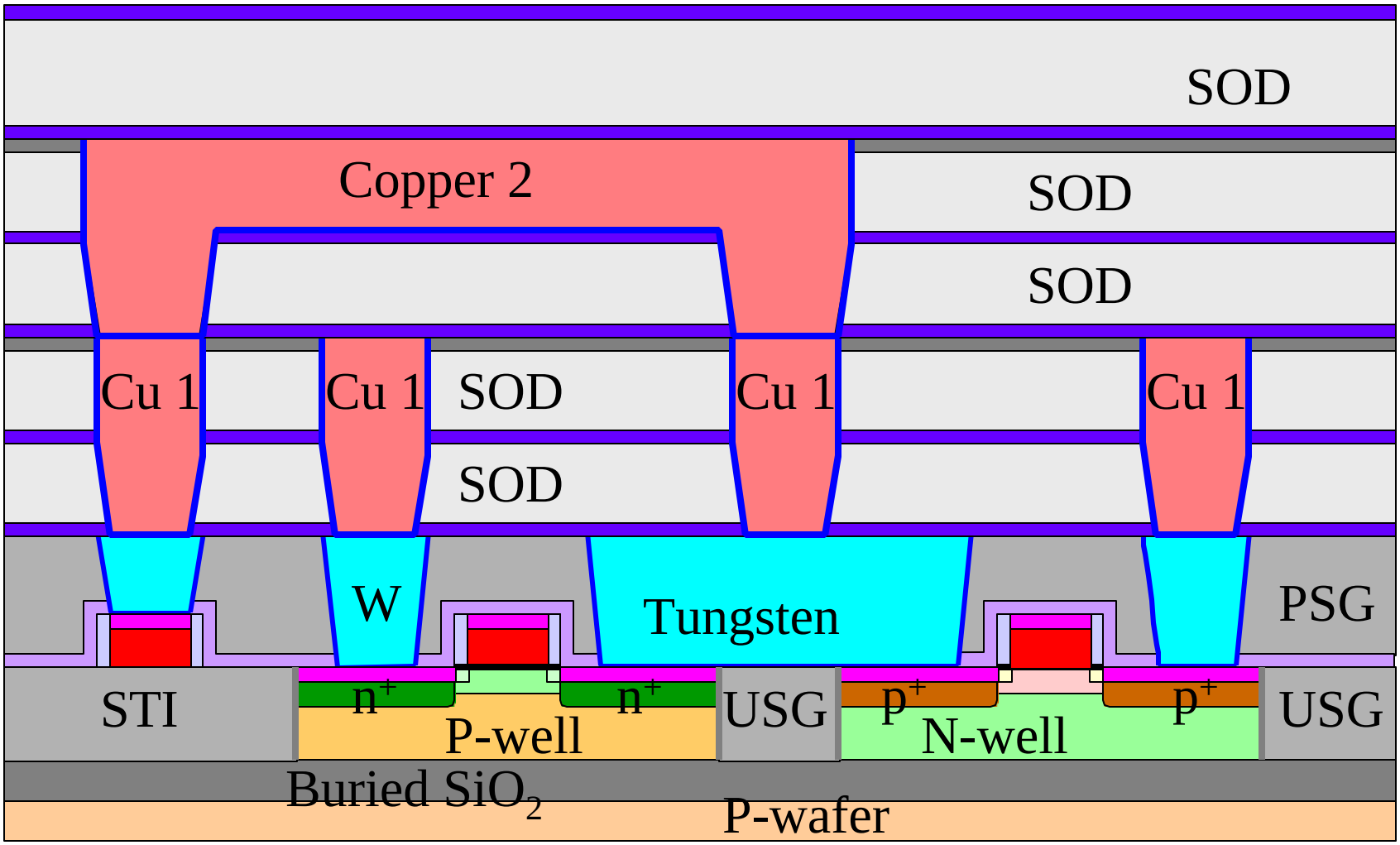
Cu, Ta, and TaN CMP



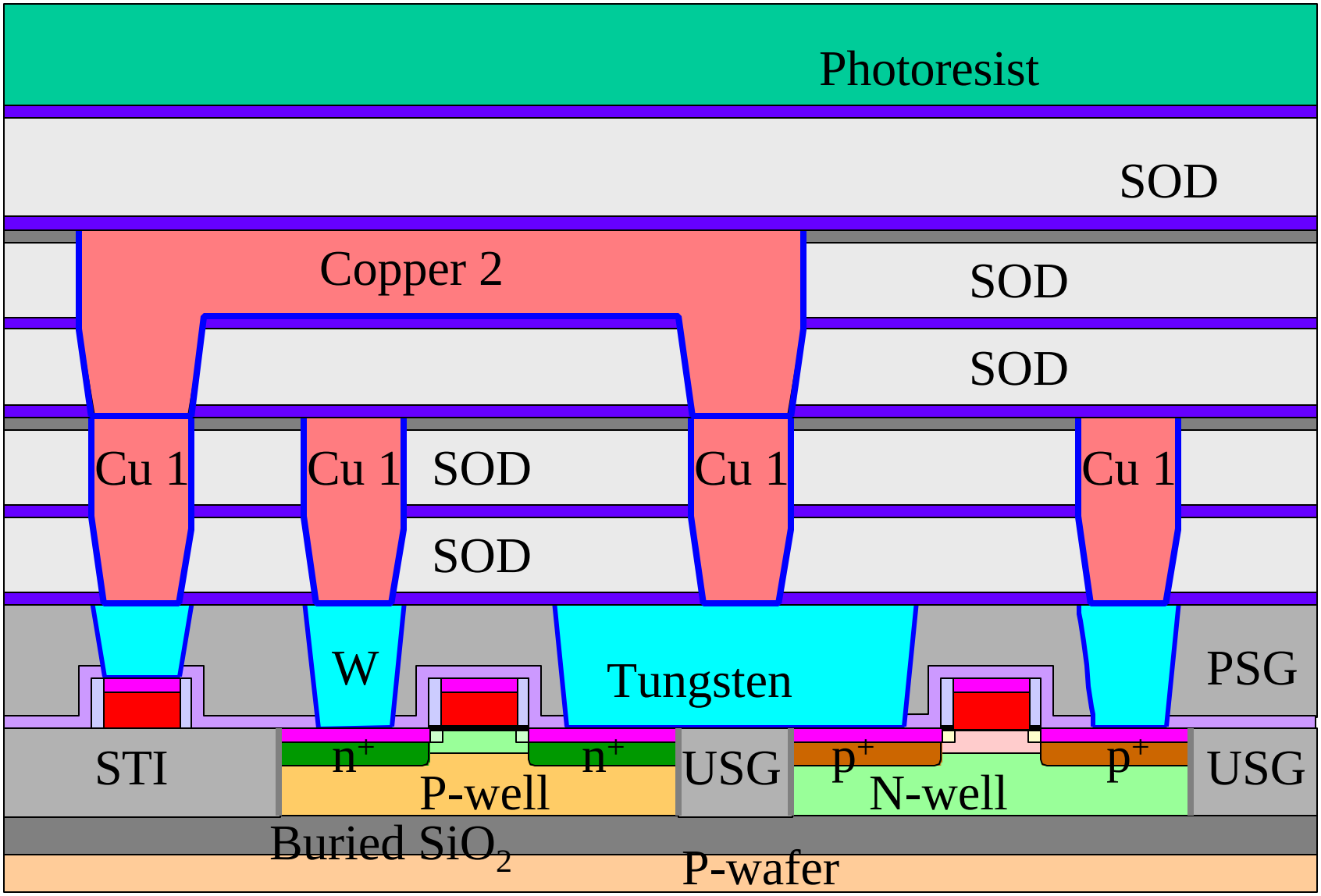
PECVD SiC, SOD Coating and Curing



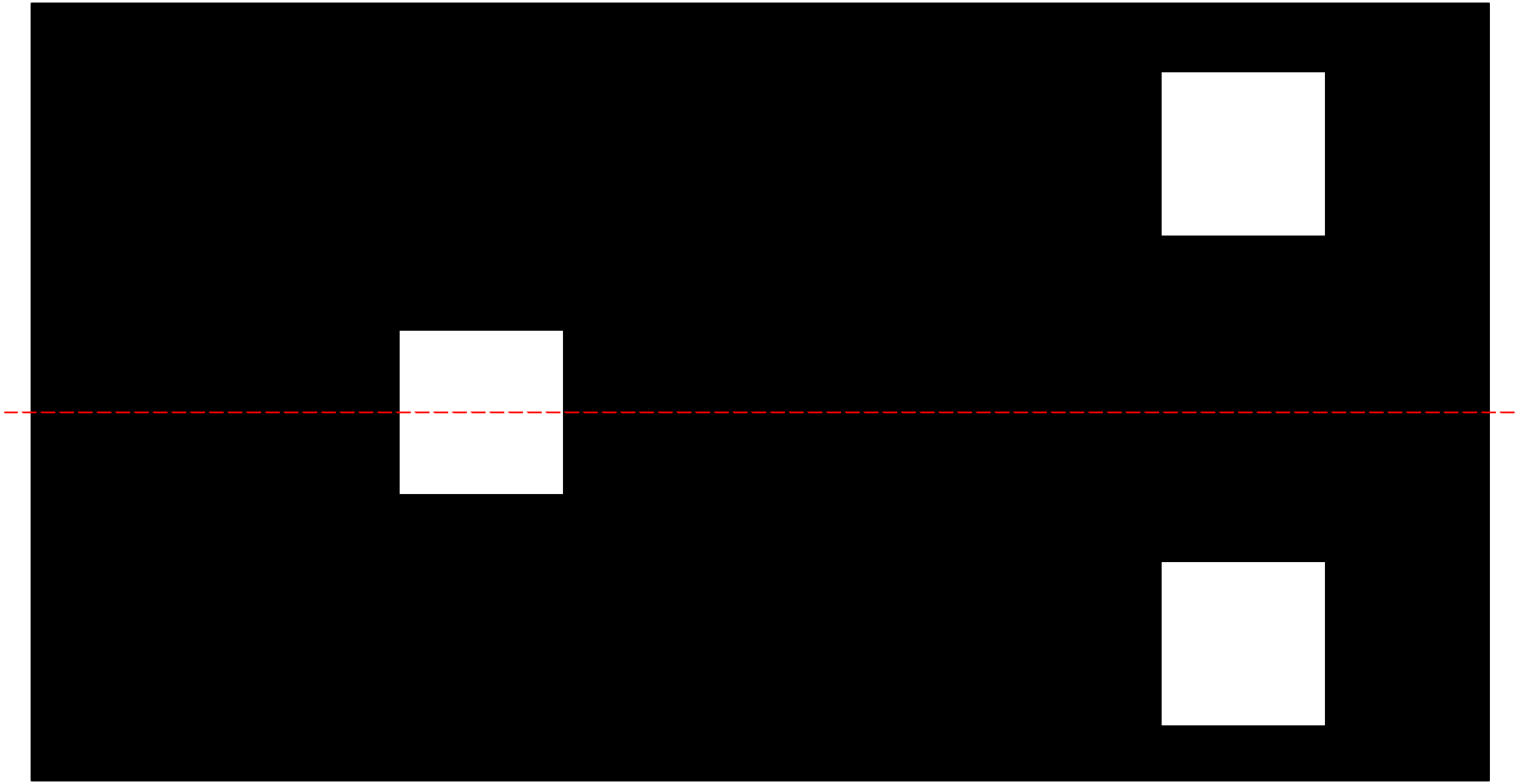
PECVD SiC Etch Stop Layer



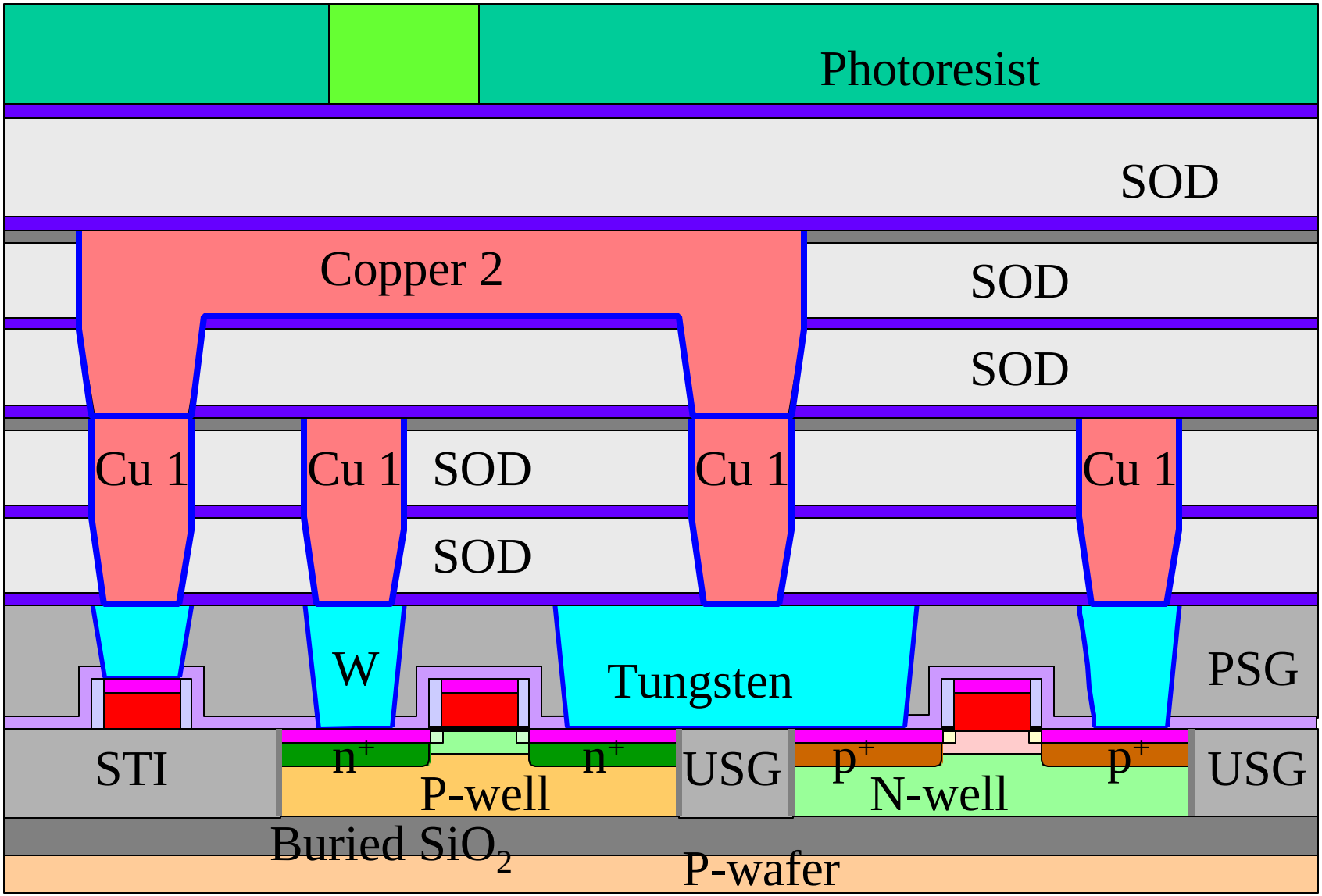
Photoresist Coating and Baking



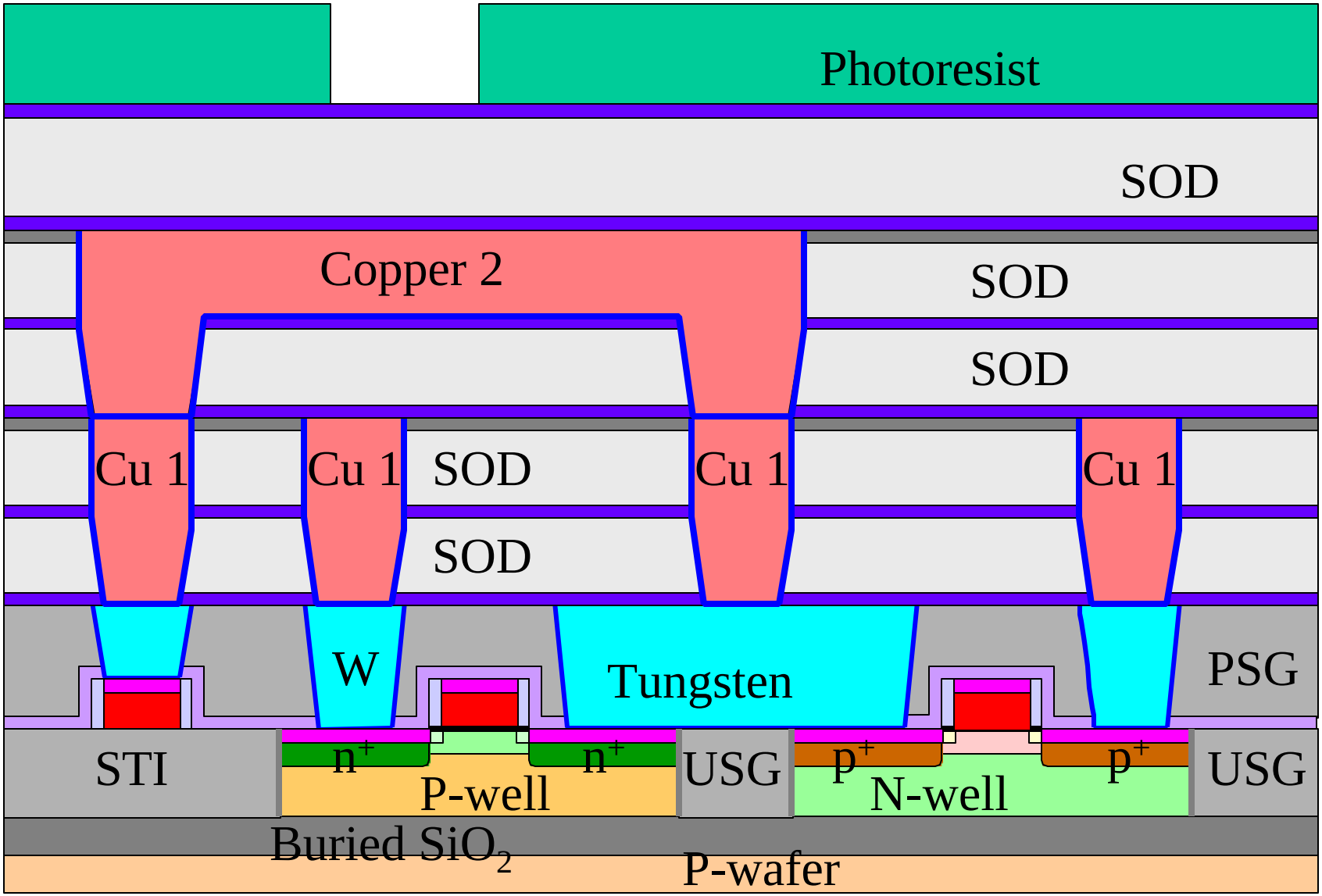
Mask 14, Via 3



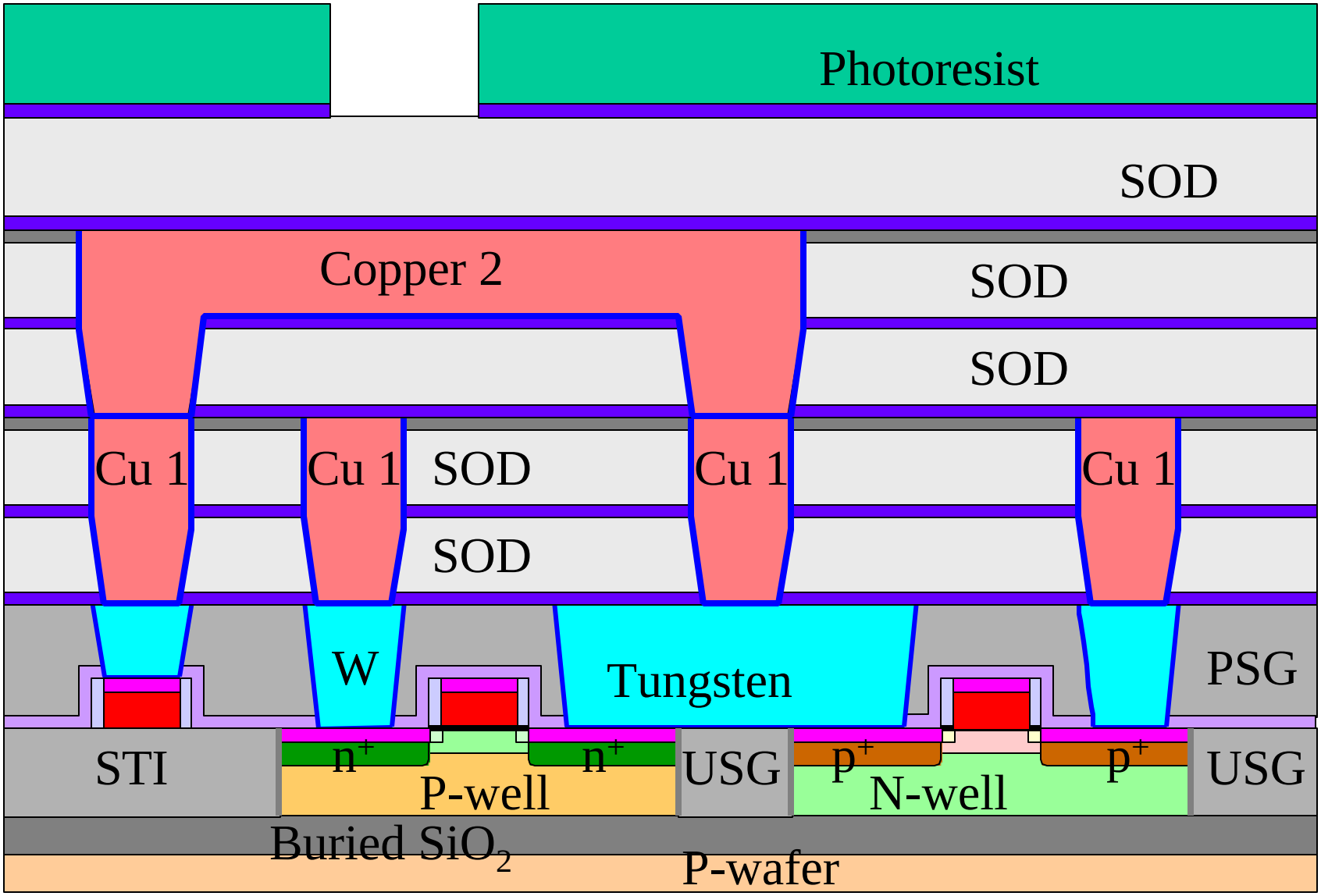
Alignment and Exposure



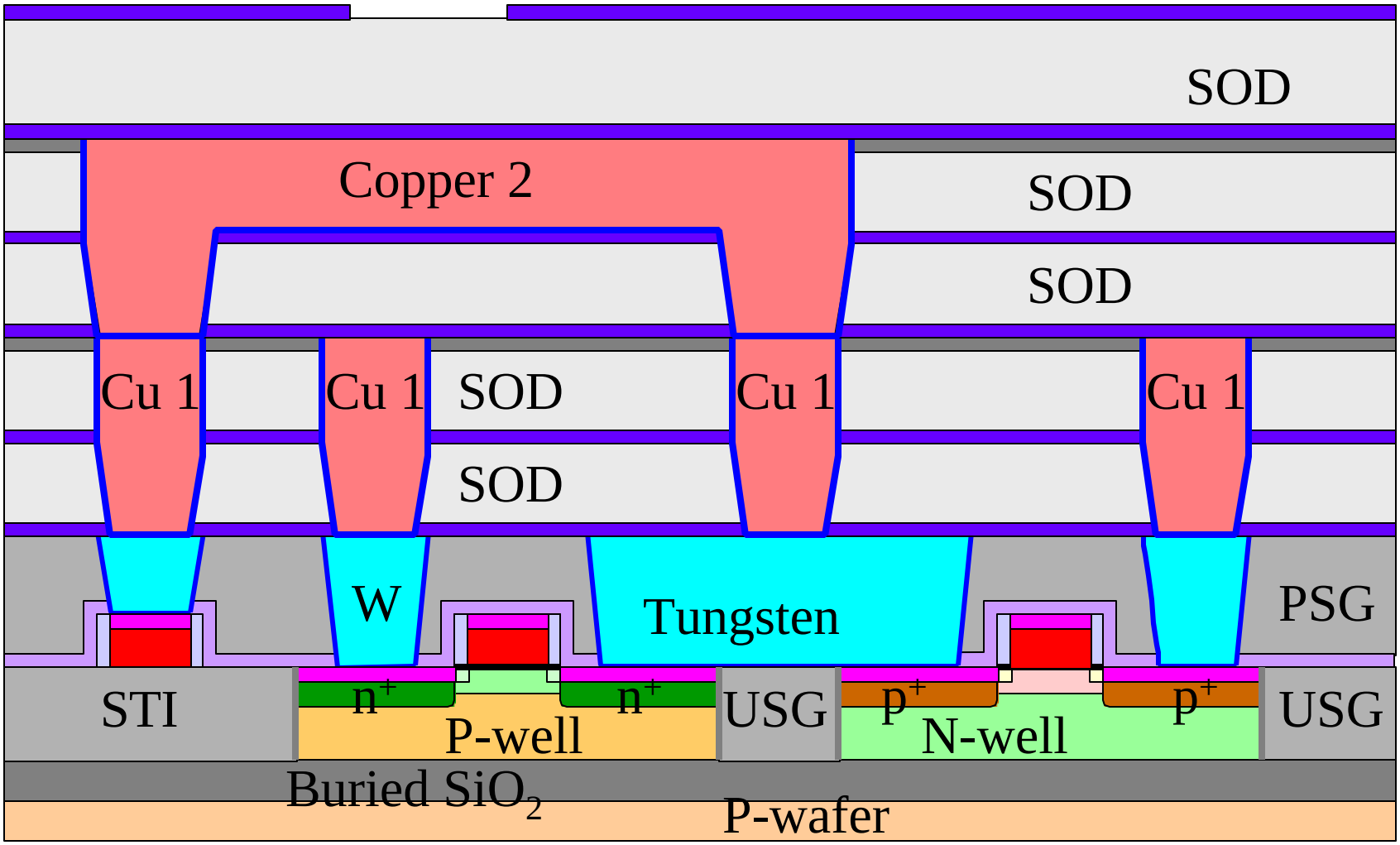
PEB, Development, and Inspection



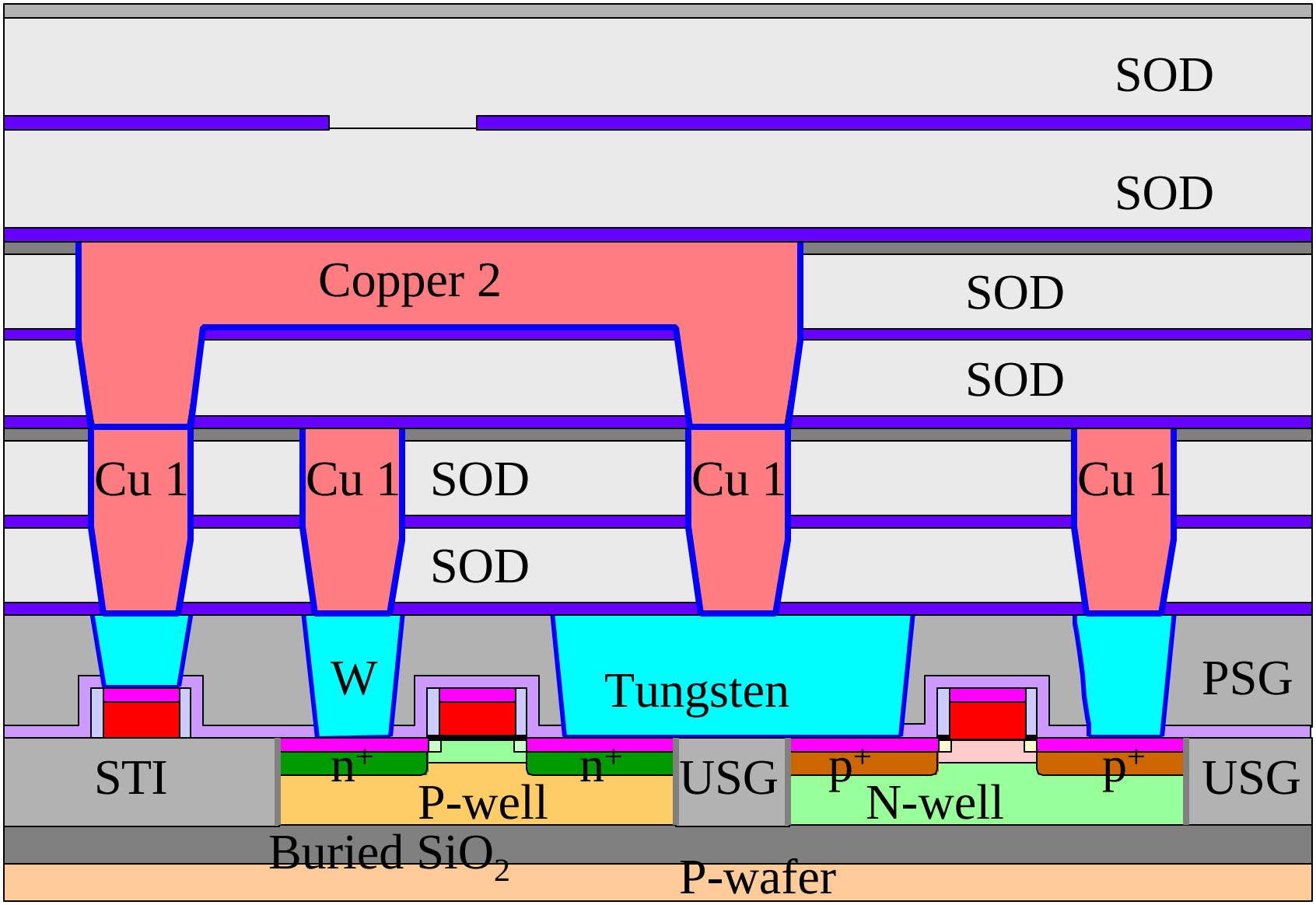
Etch SiC


Photoresist
SOD
Copper 2
SOD
SOD
Cu 1
Cu 1
SOD
Cu 1
Cu 1
SOD
W
Tungsten
PSG
STI
n+
n+
USG
p+
p+
USG
P-well
N-well
Buried SiO2
P-wafer

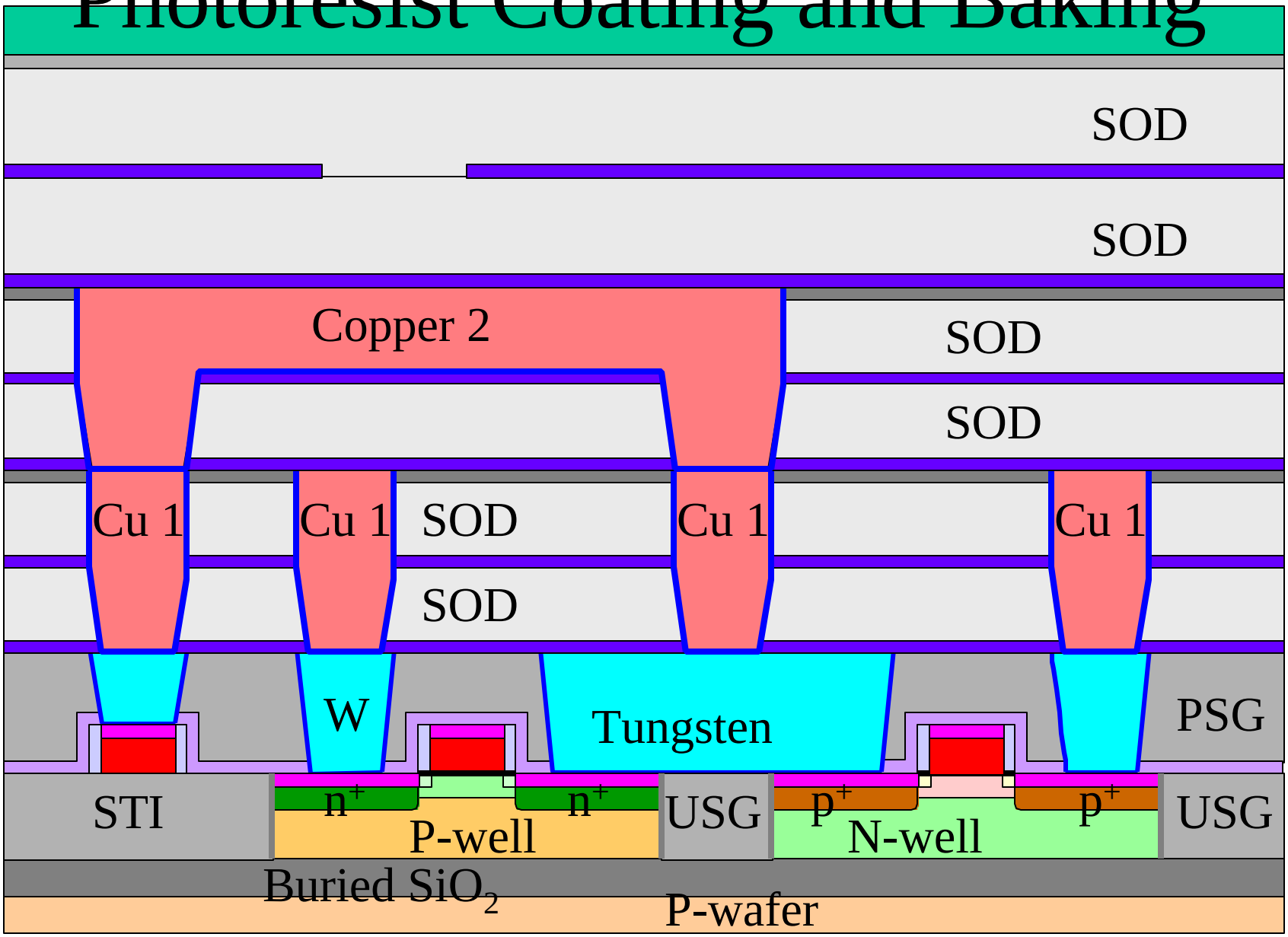
Strip Photoresist



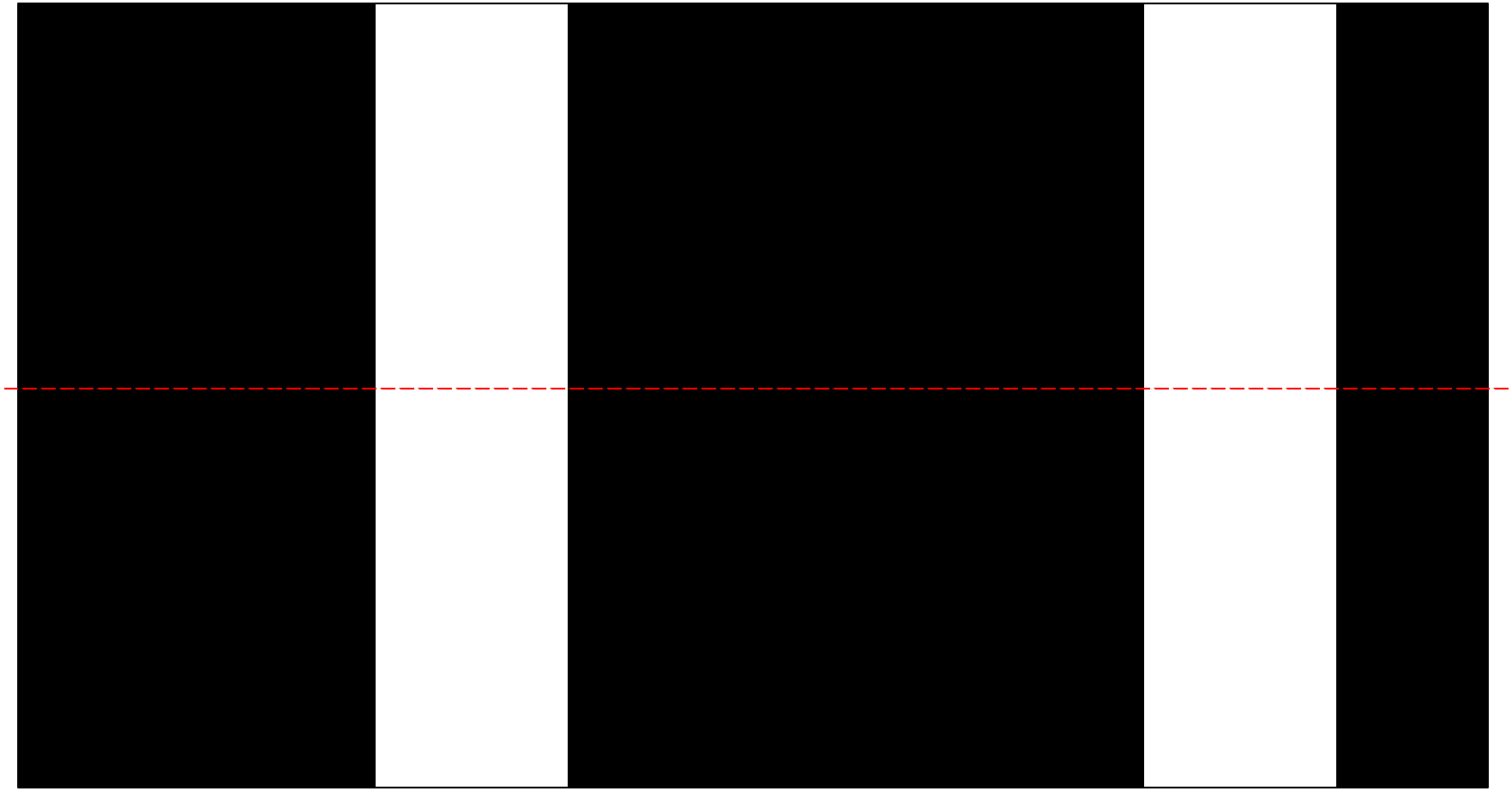
SOD Coating & Curing, PE-TEOS Cap



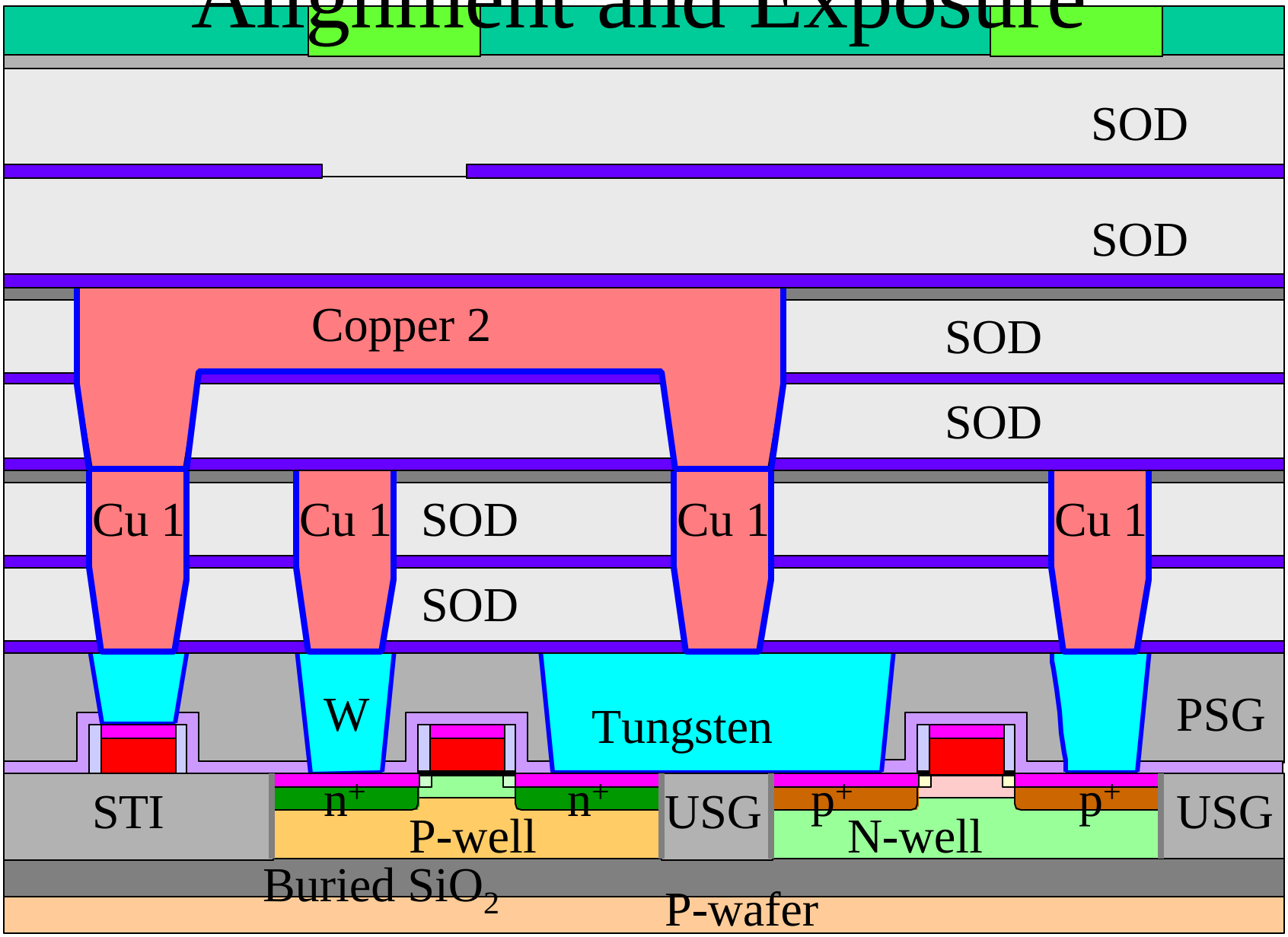
Photoresist Coating and Baking



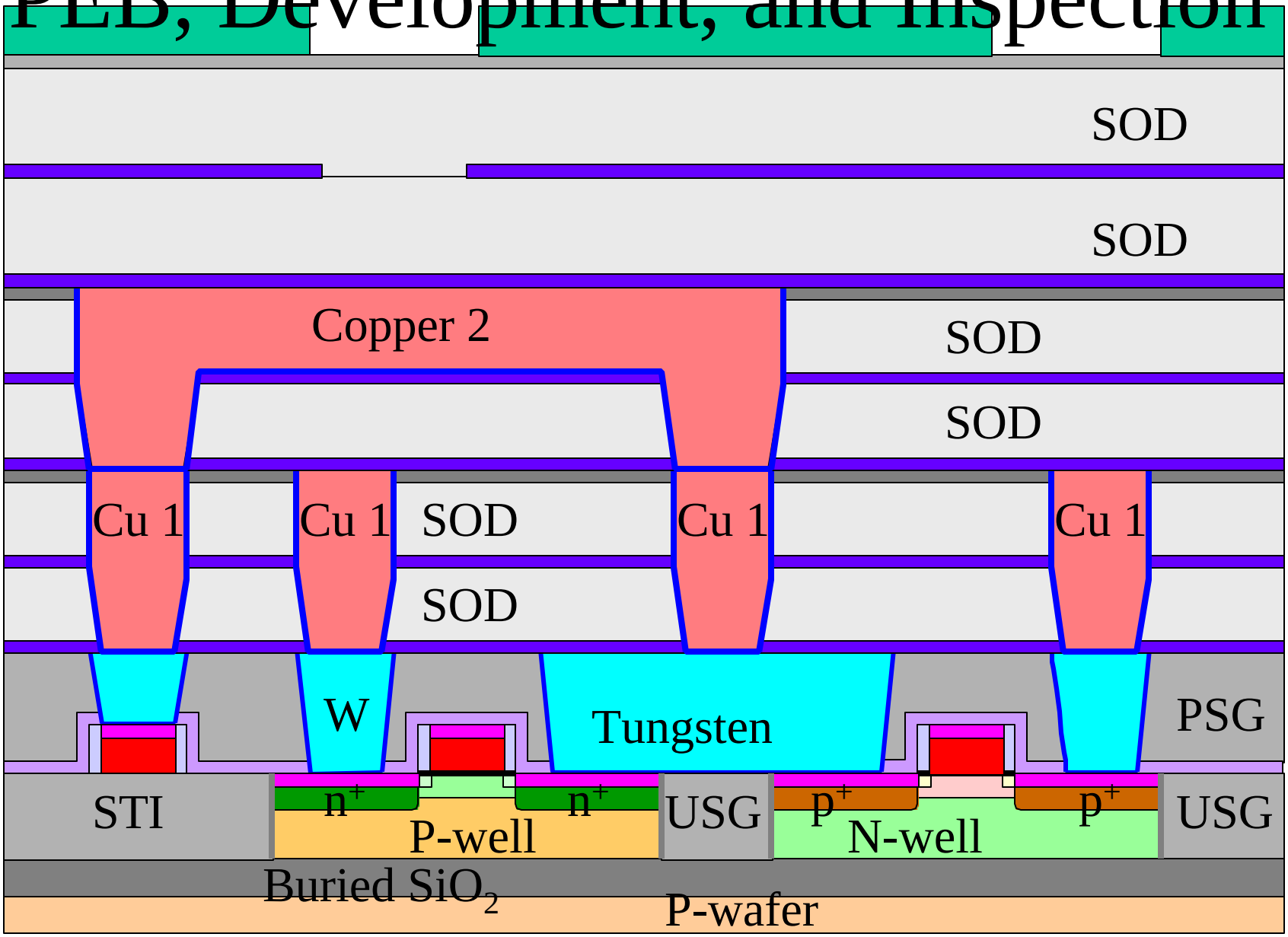
Mask 15, Metal Trench 3



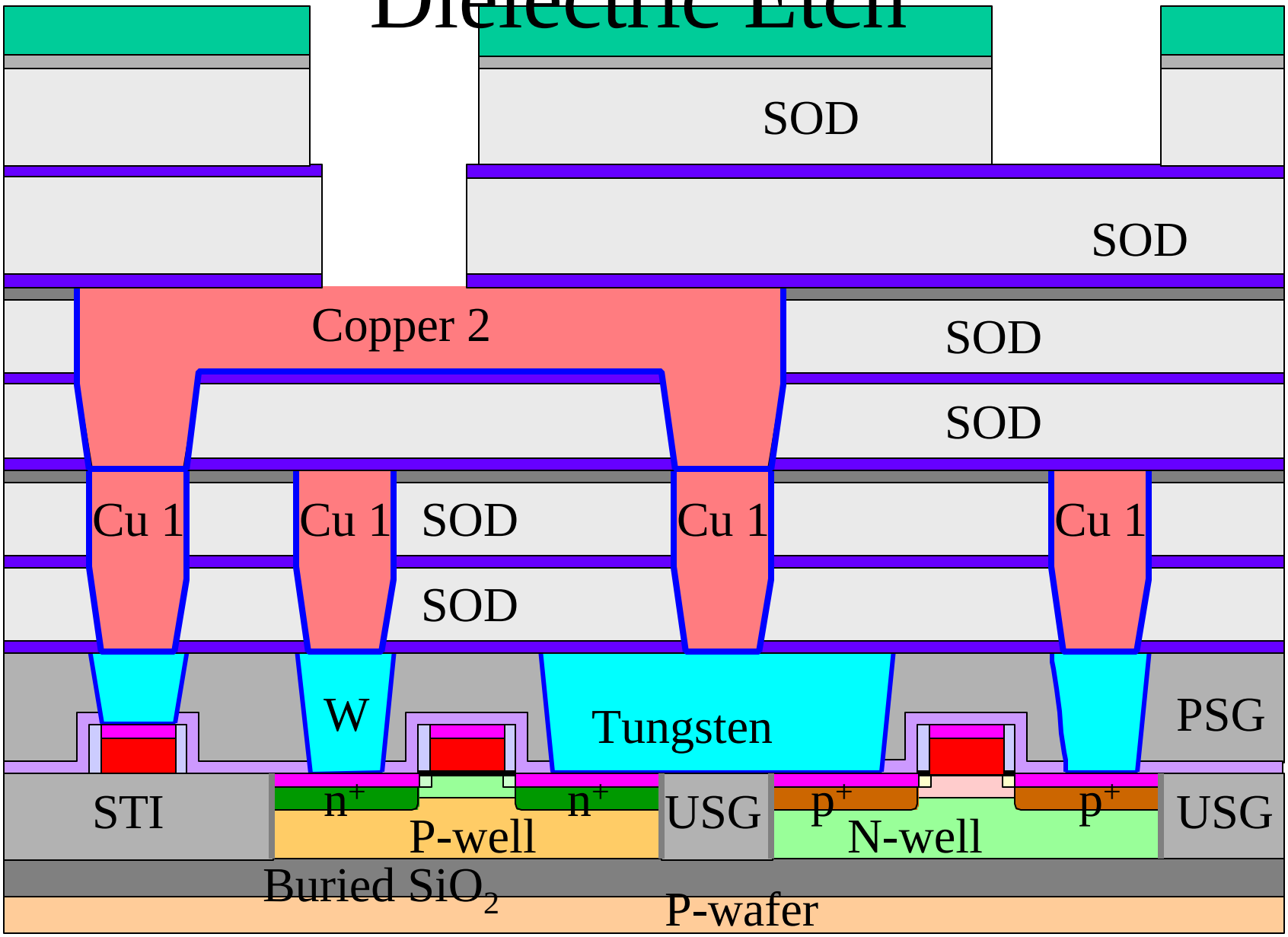
Alignment and Exposure



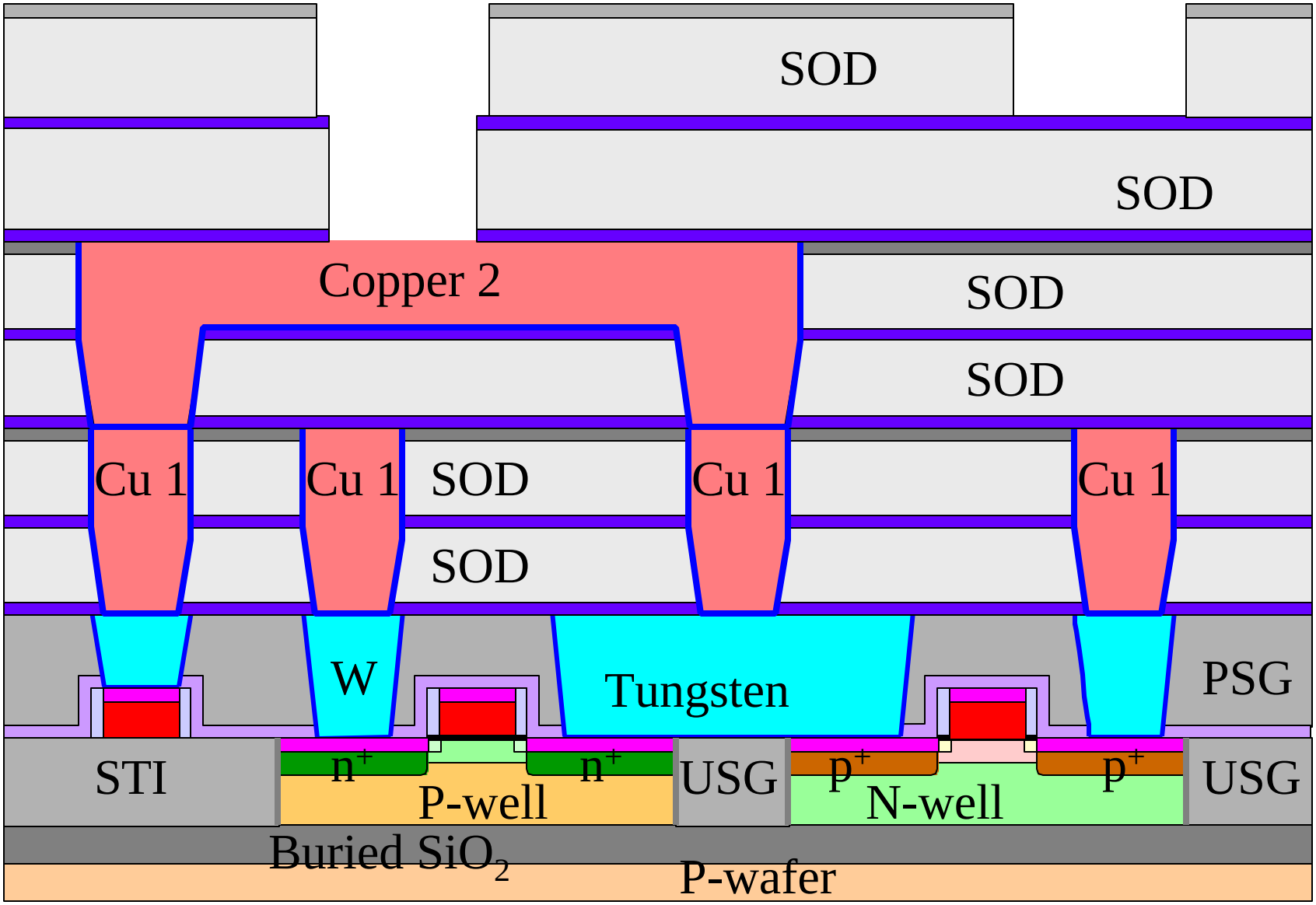
PEB, Development, and Inspection



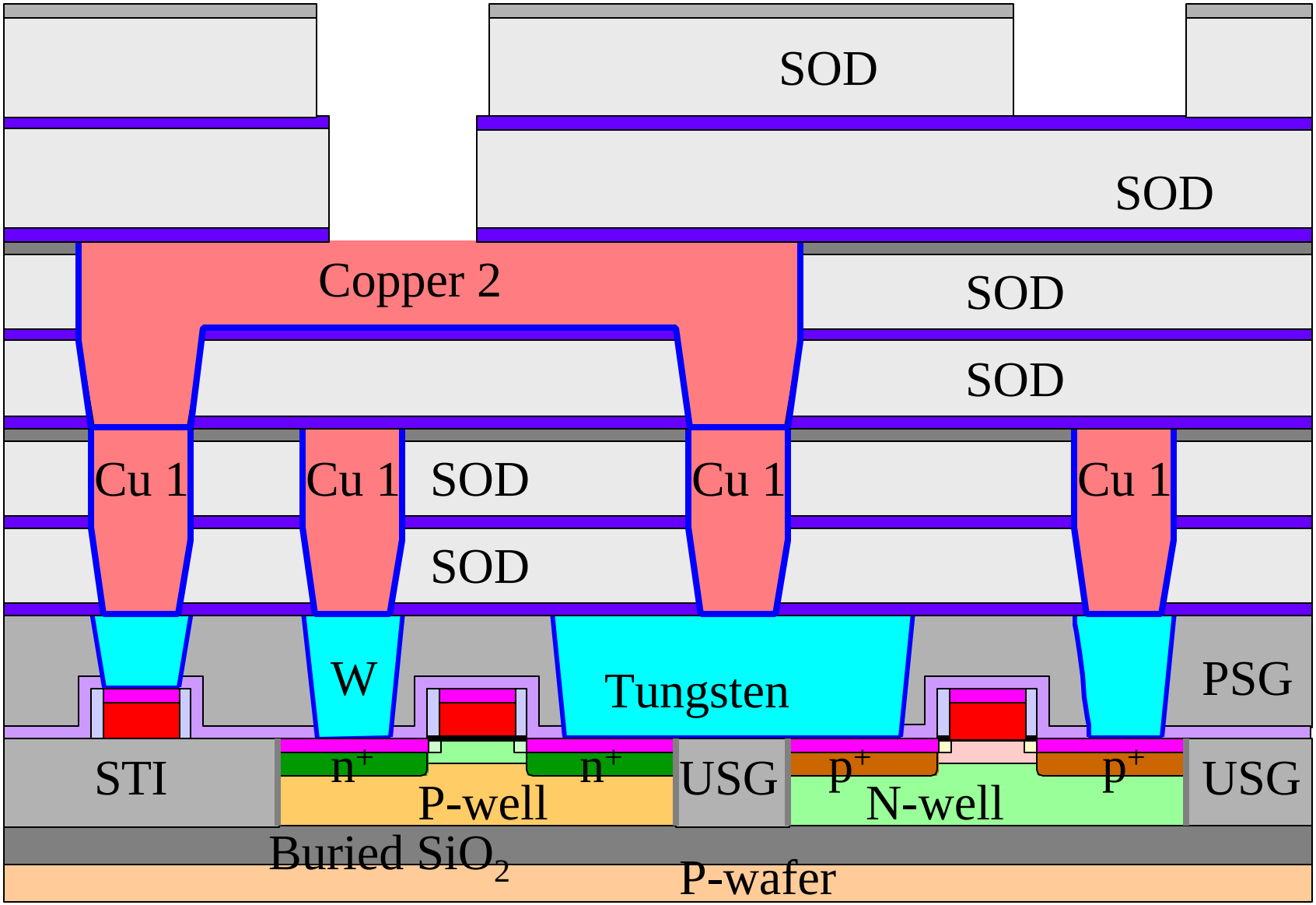
Dielectric Etch



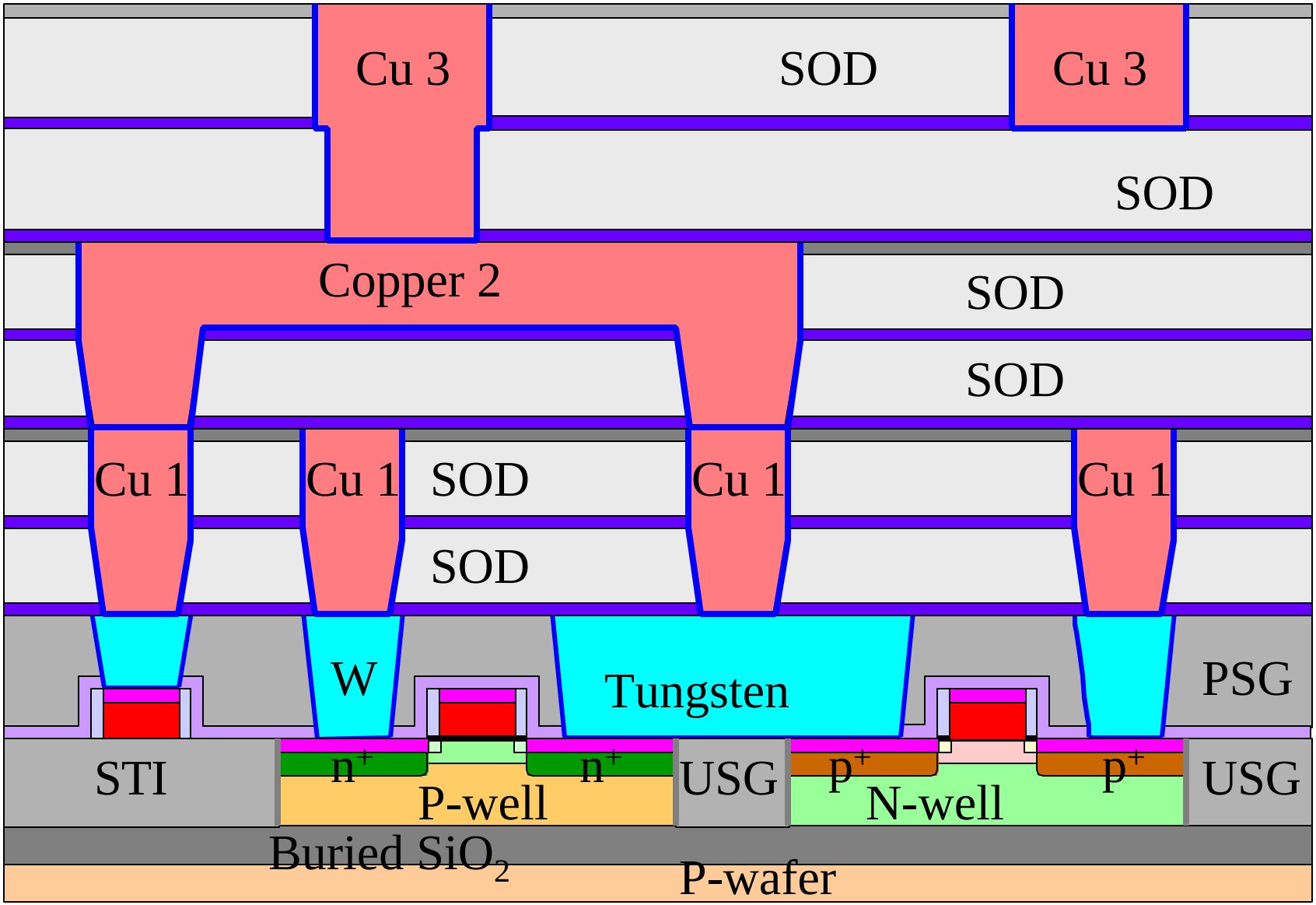
Strip Photoresist



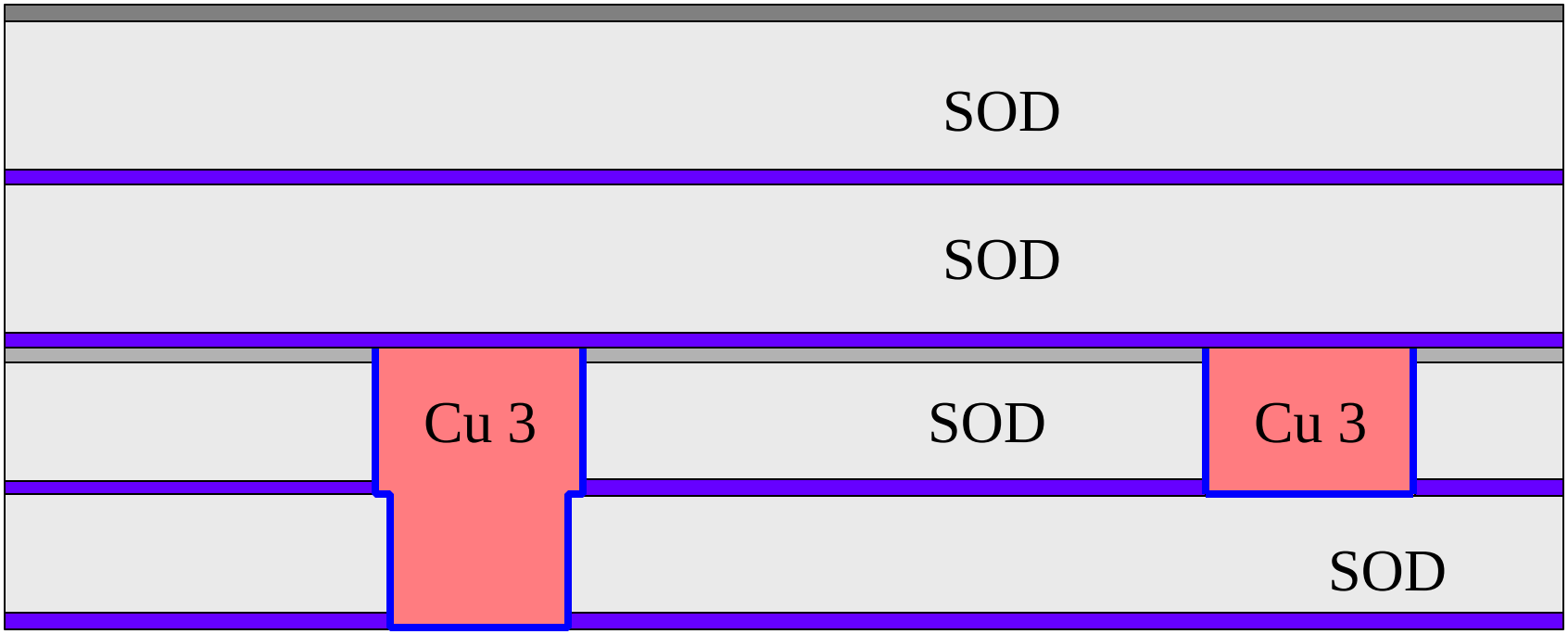
Hydrogen Plasma Clean



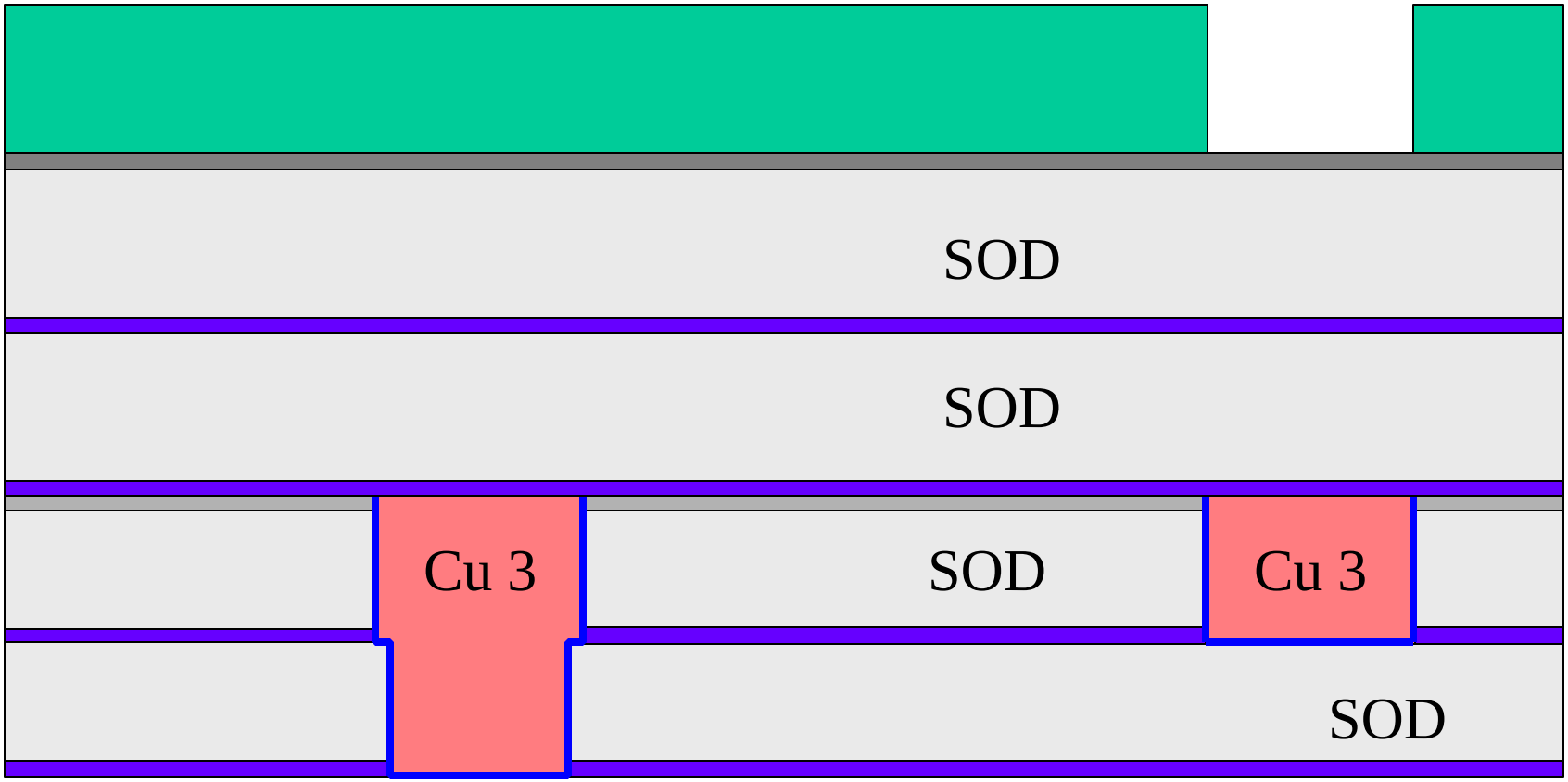
Cu, Ta, and TaN Deposition and CMP



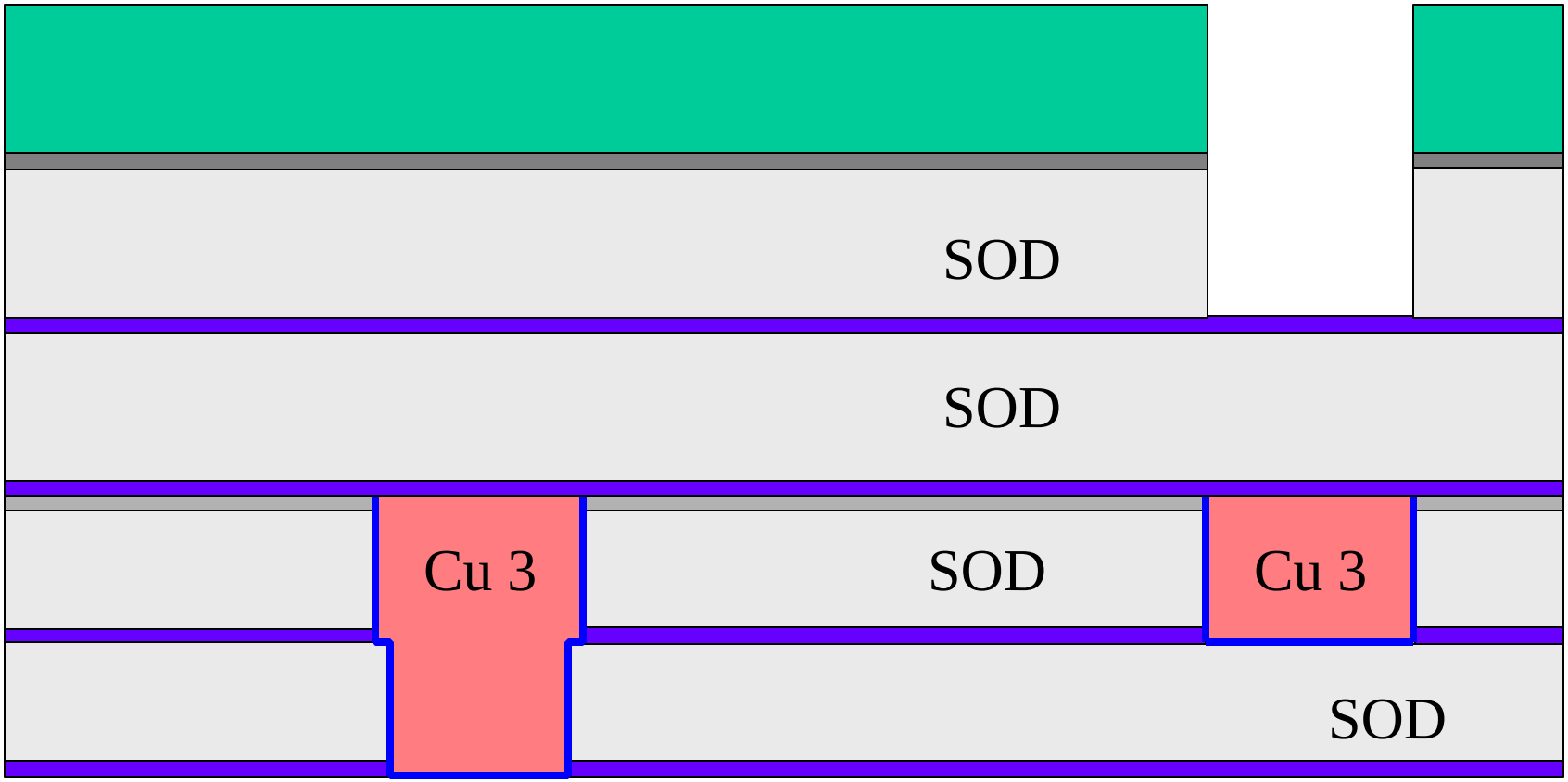
SiC, SOD, SiC, SOD, and PE-TEOS



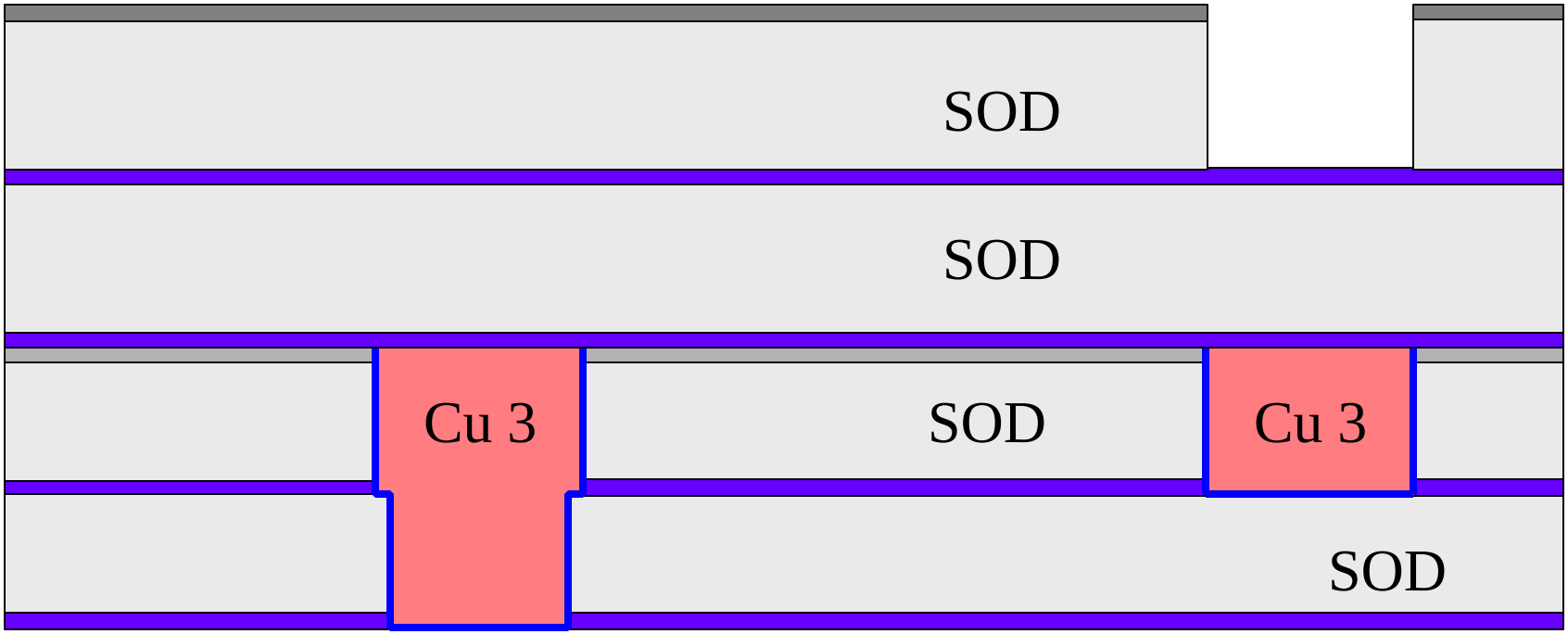
PR Coating, Alignment and Exposure, PEB, and Development



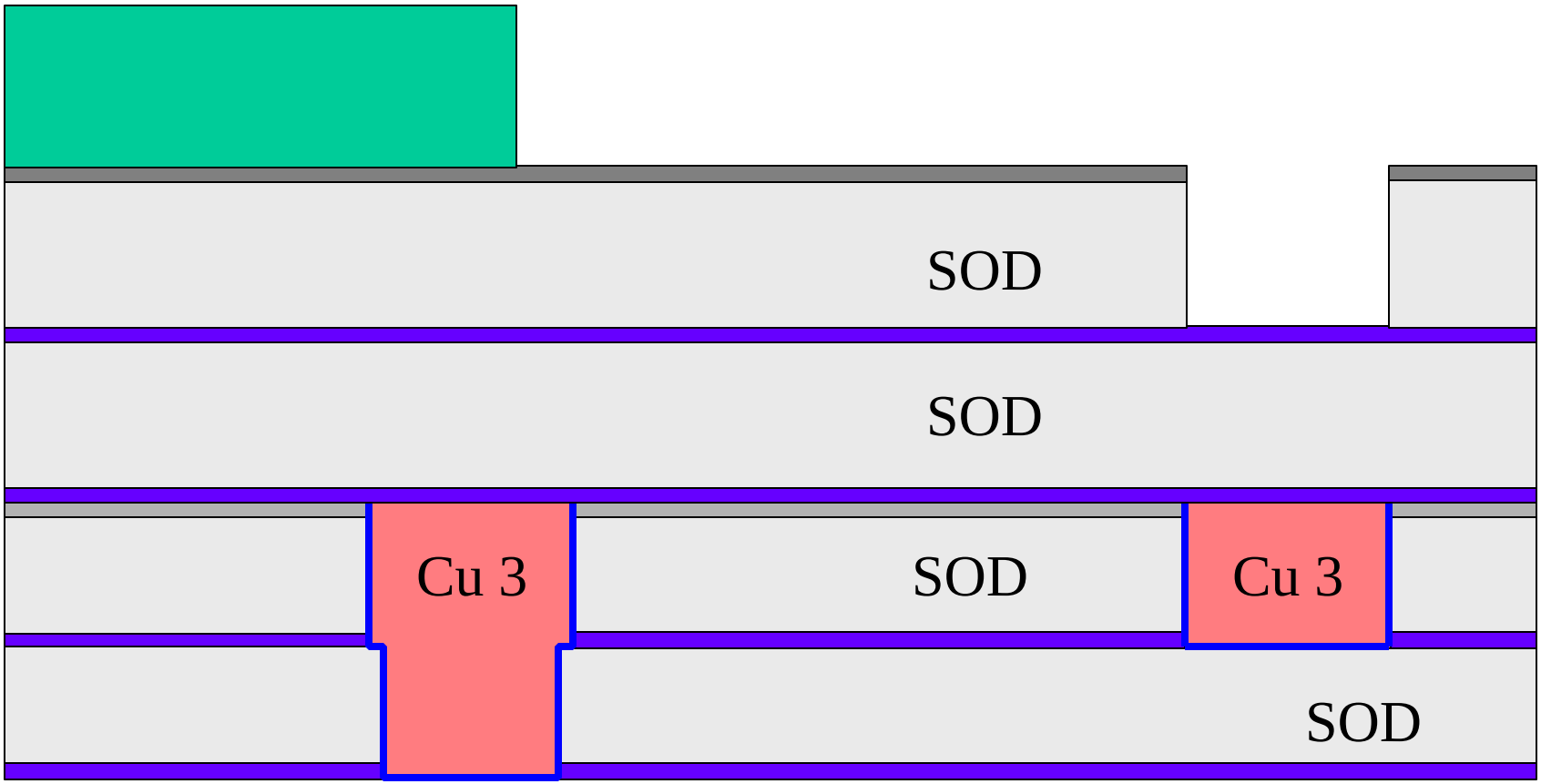
Via 4 Etch



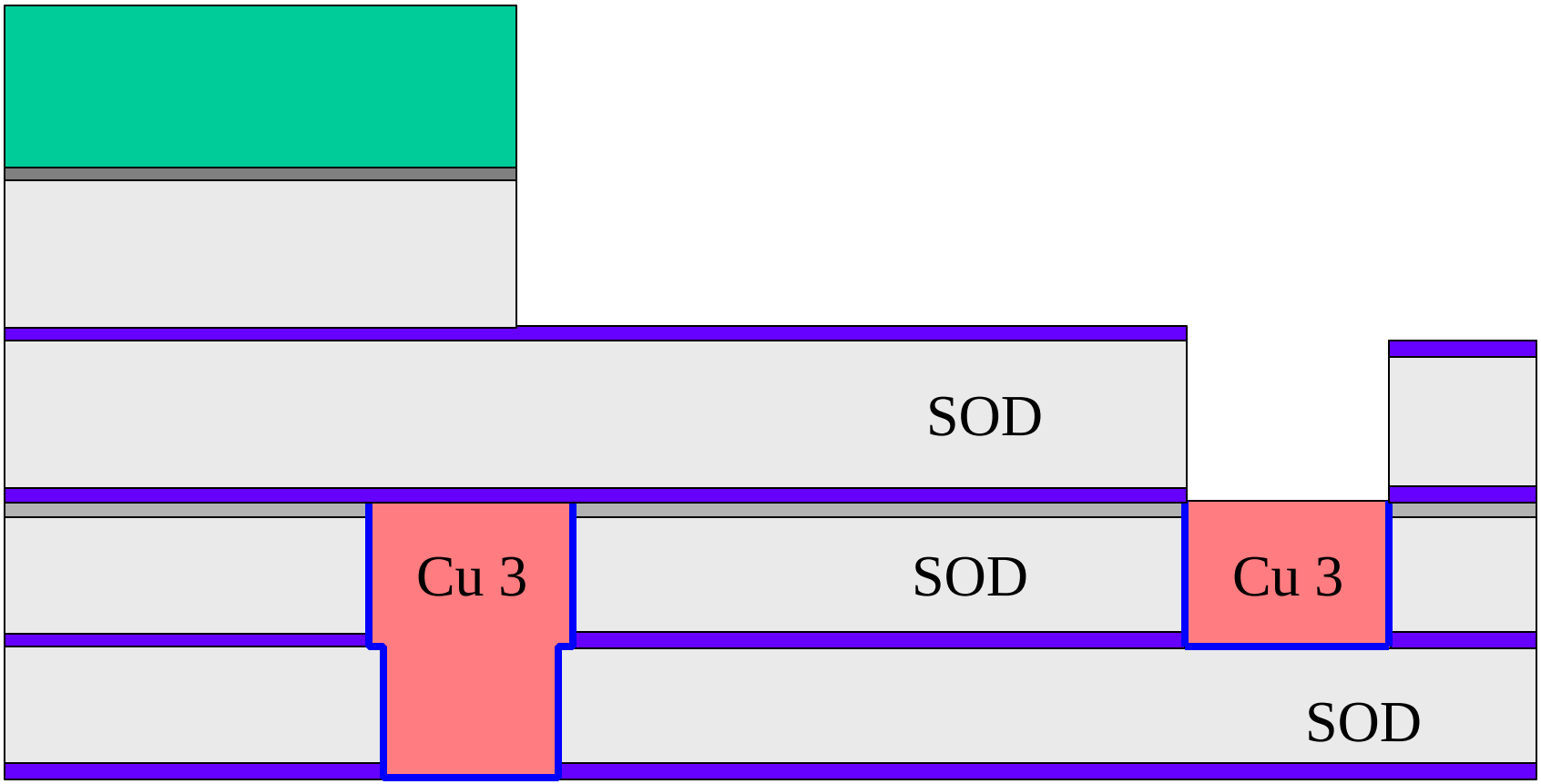
Strip Photoresist



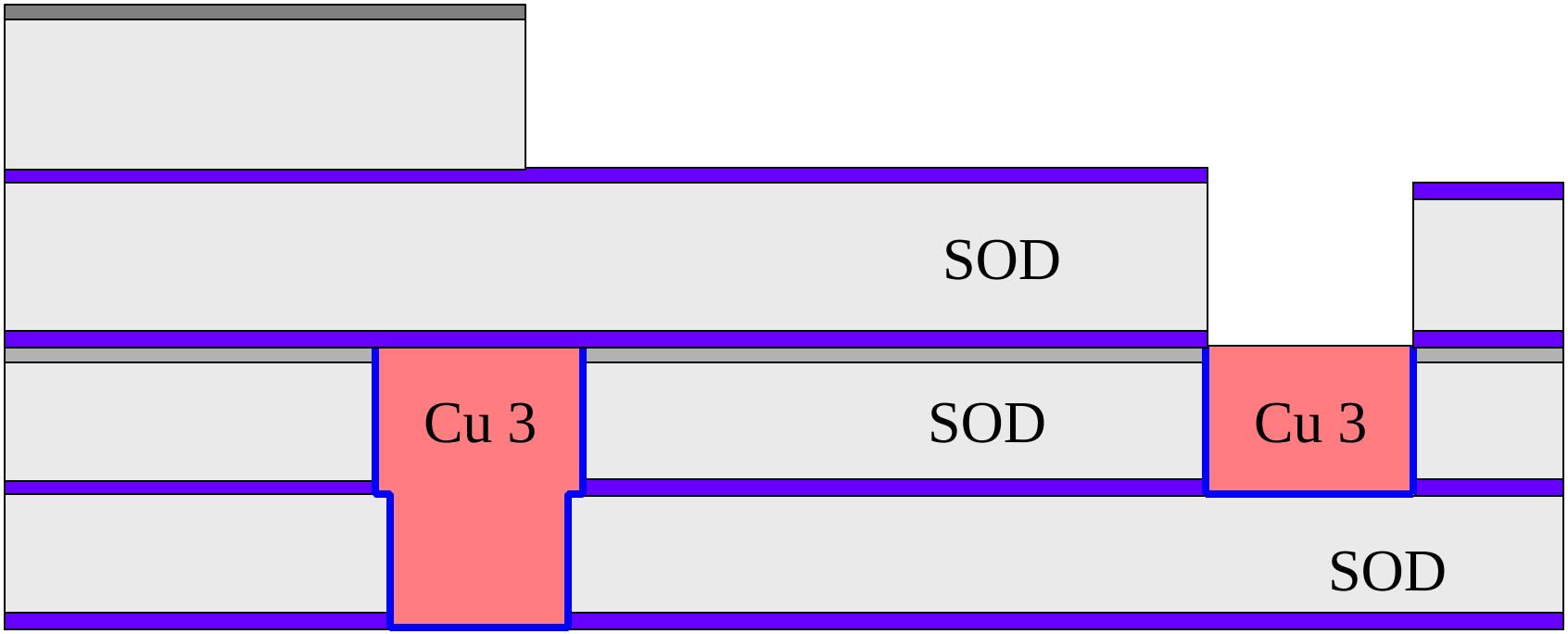
PR Coating, Alignment and Exposure, PEB, and Development



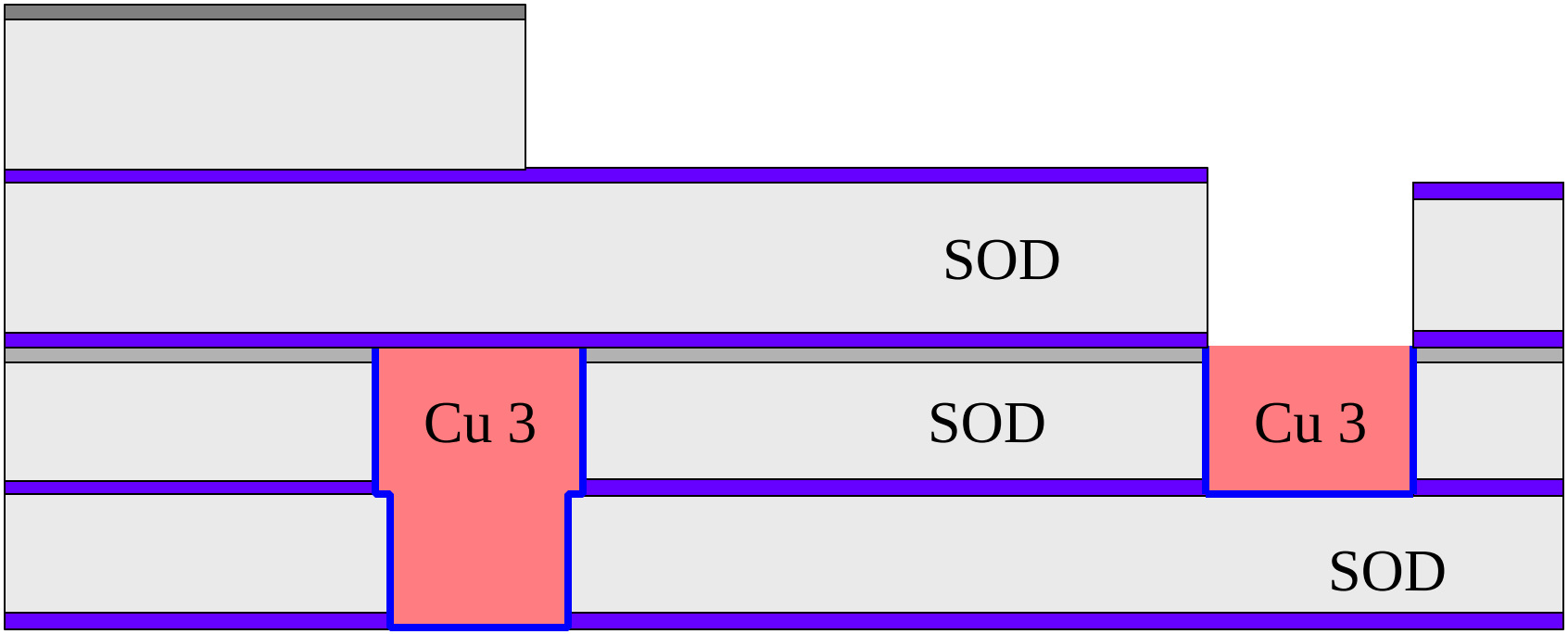
Etch Trench



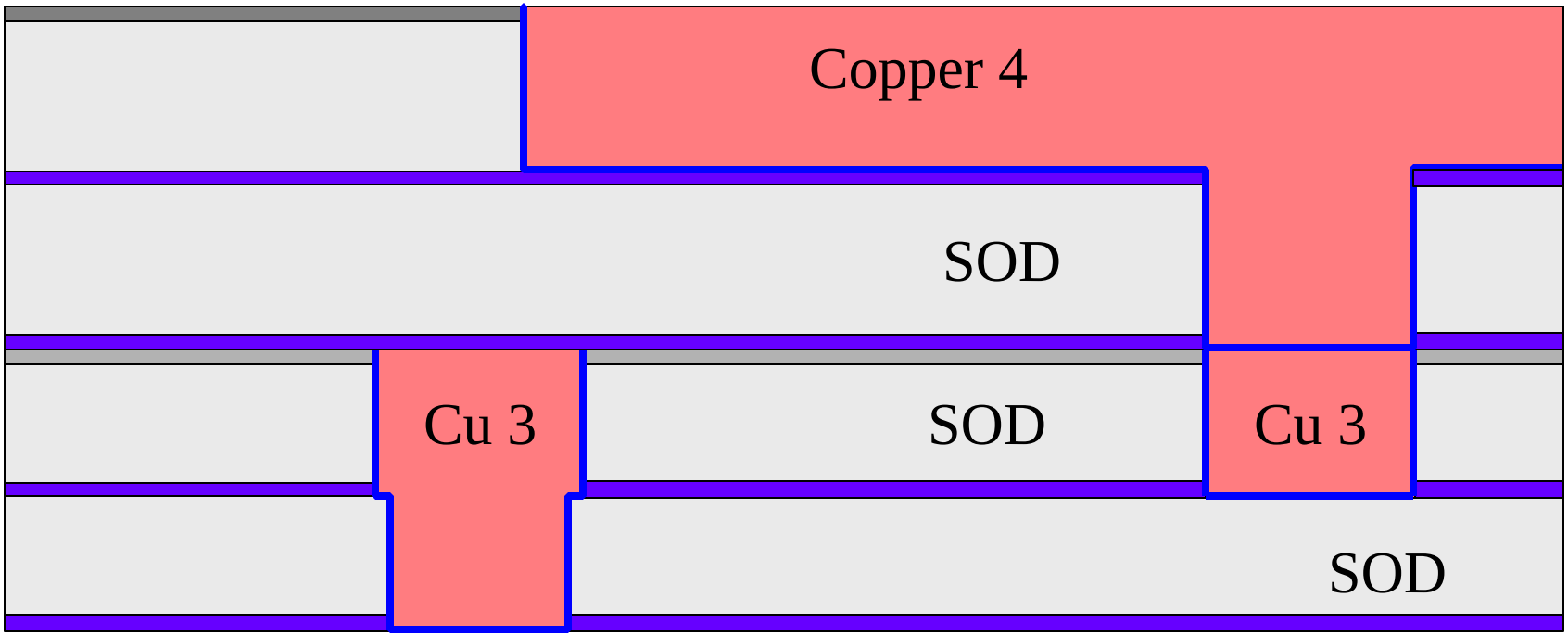
Strip Photoresist



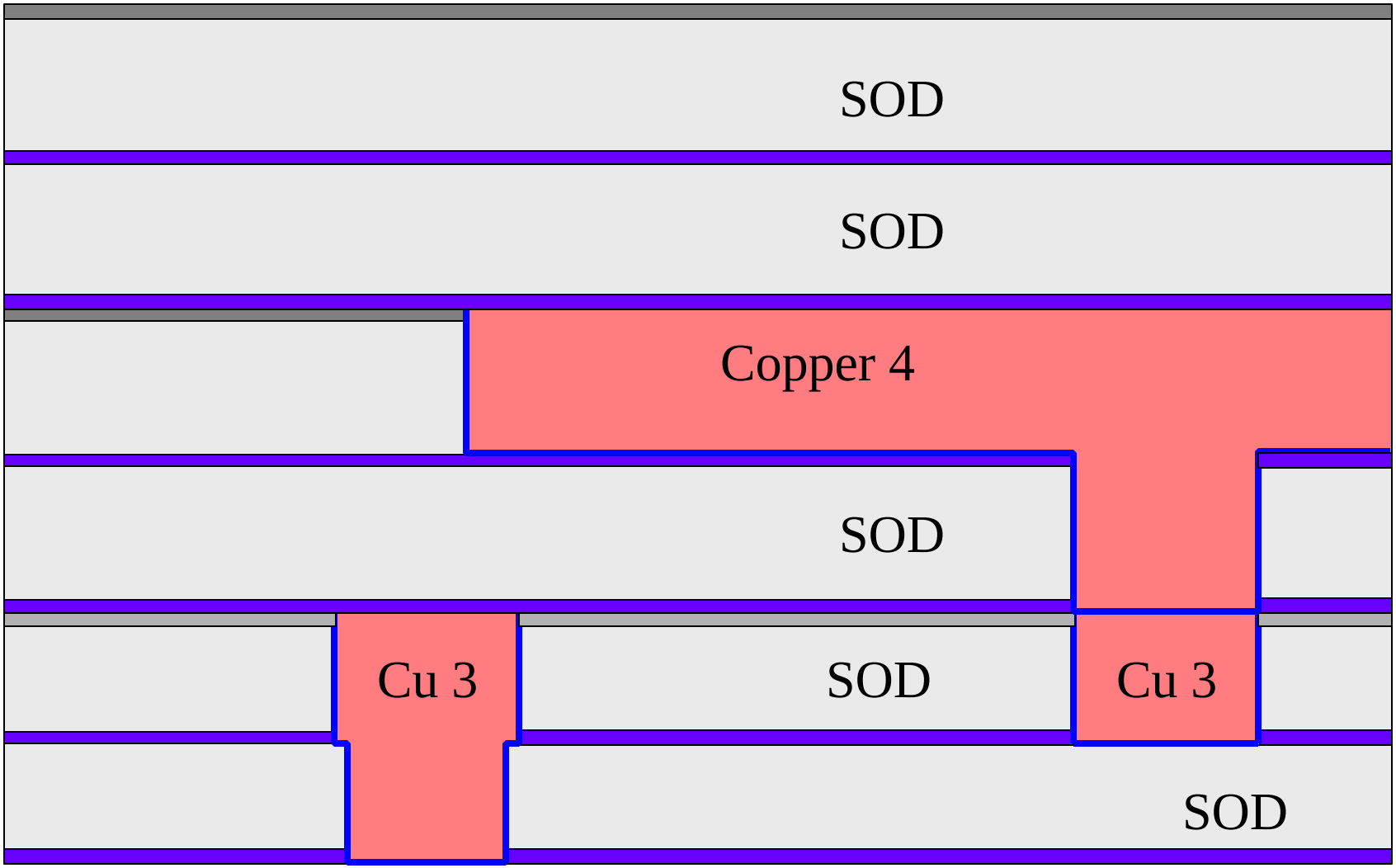
Hydrogen Plasma Clean



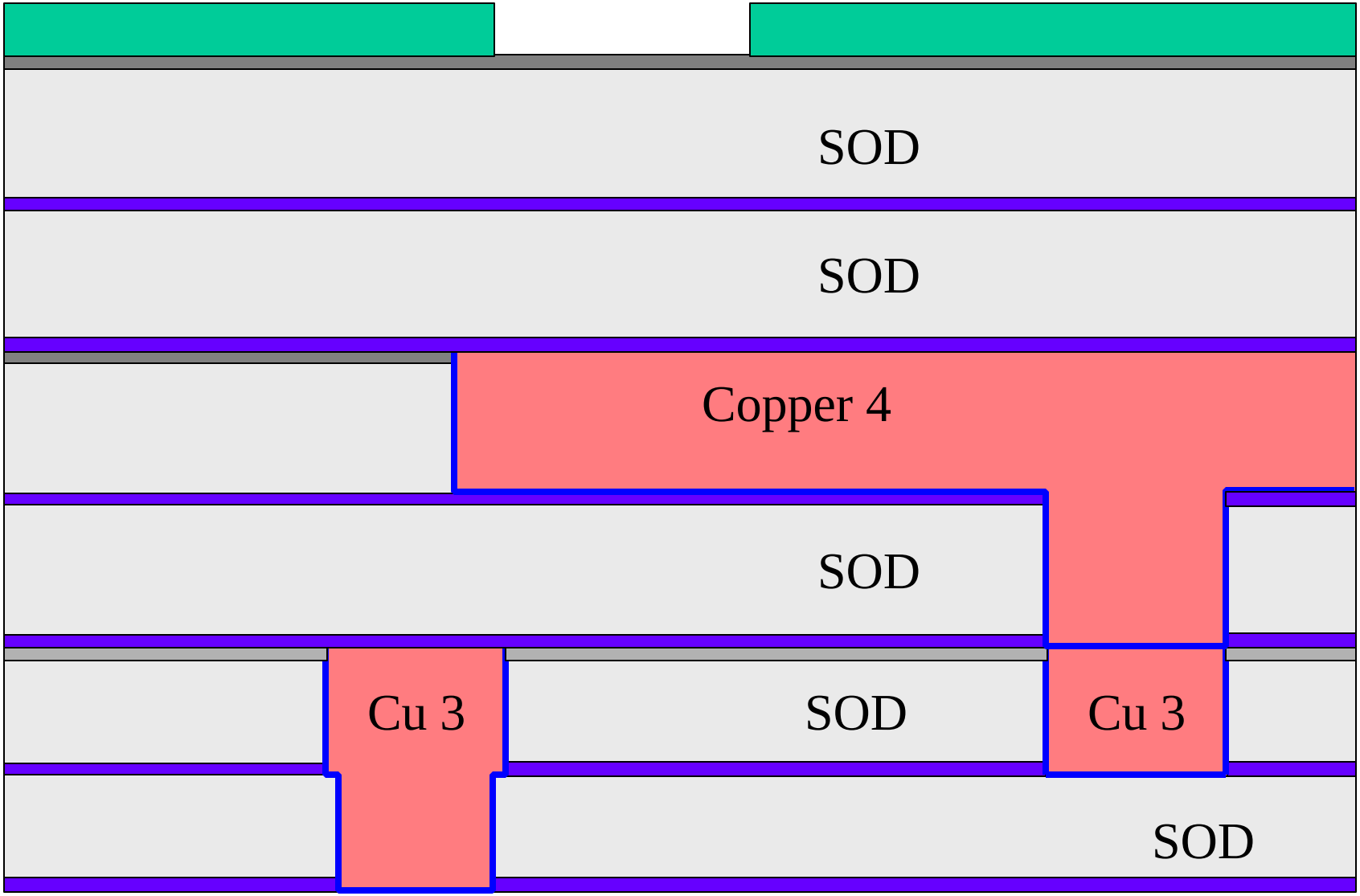
Cu, Ta, and TaN Deposition and CMP



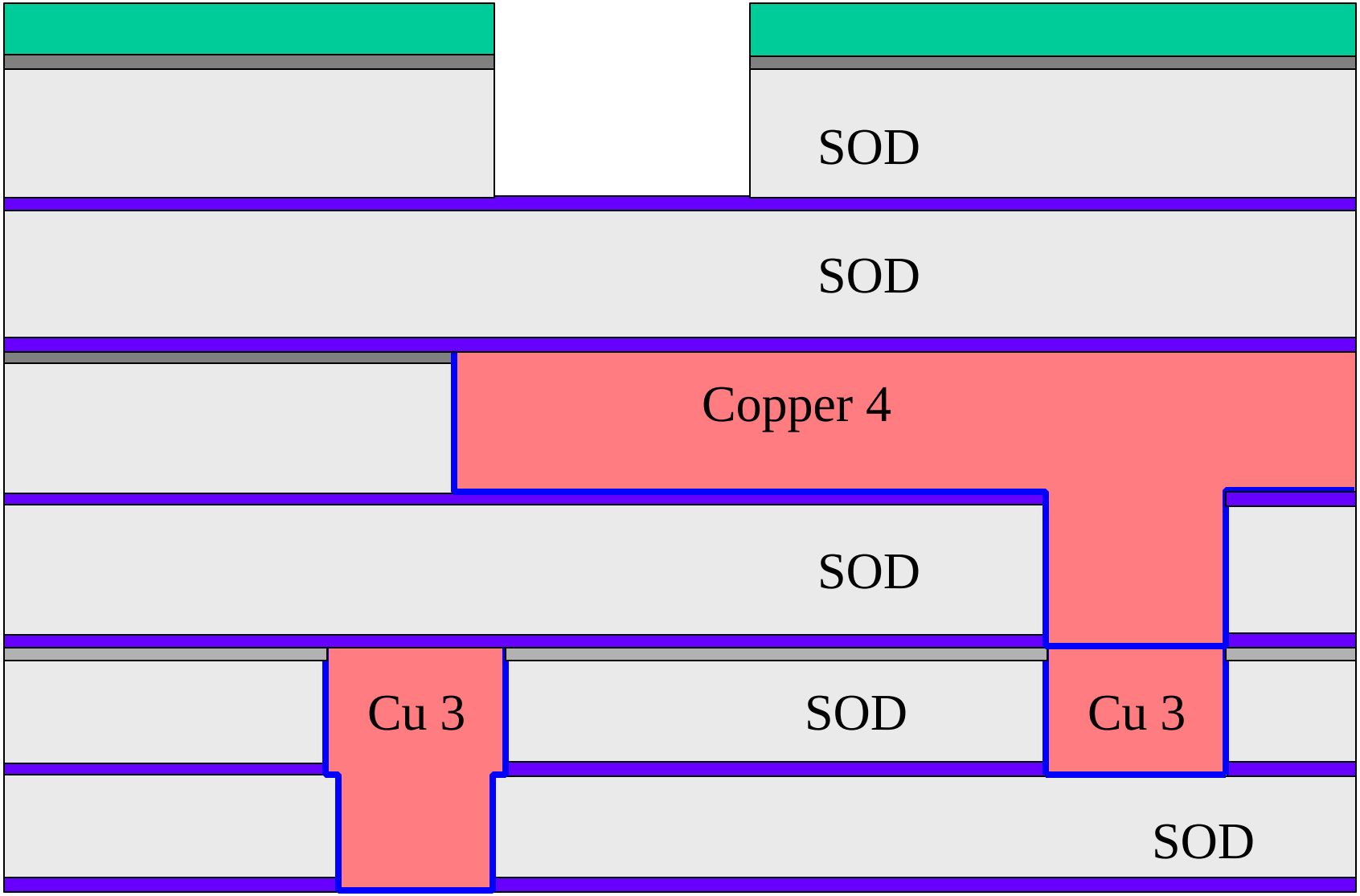
SiC, SOD, SiC, SOD, and PE-TEOS



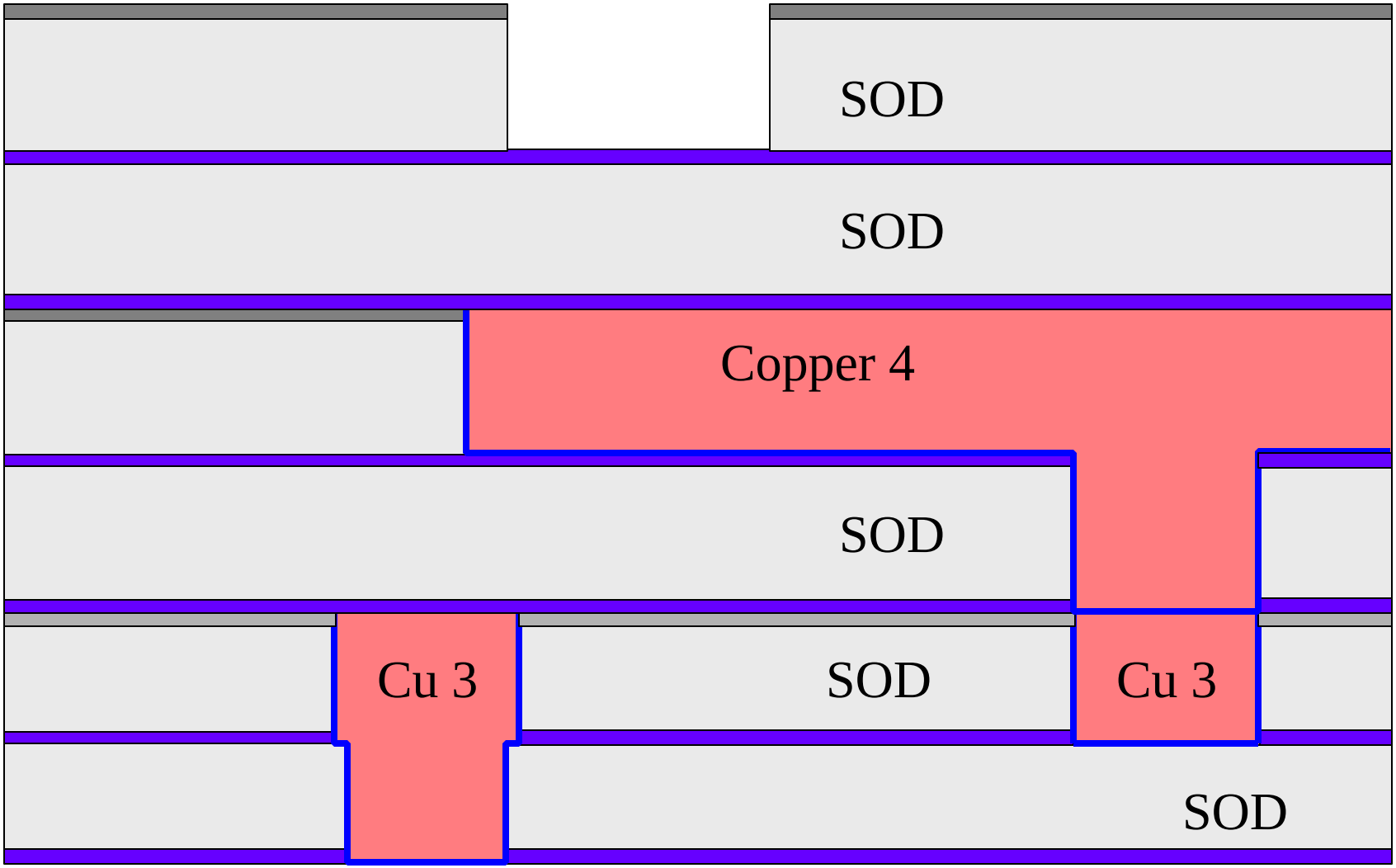
PR Coating, A&E, PEB, and Develop



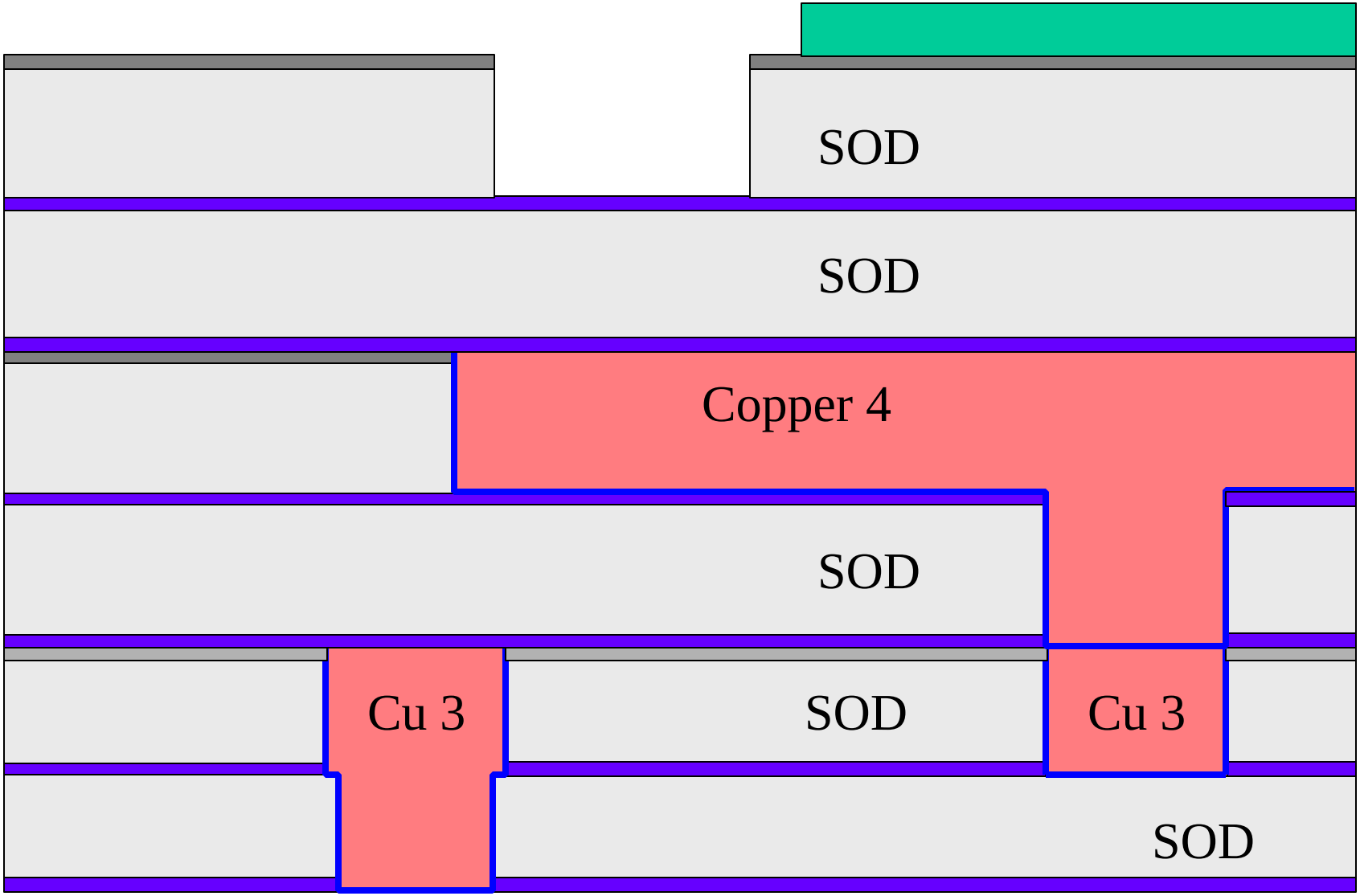
Etch Via5



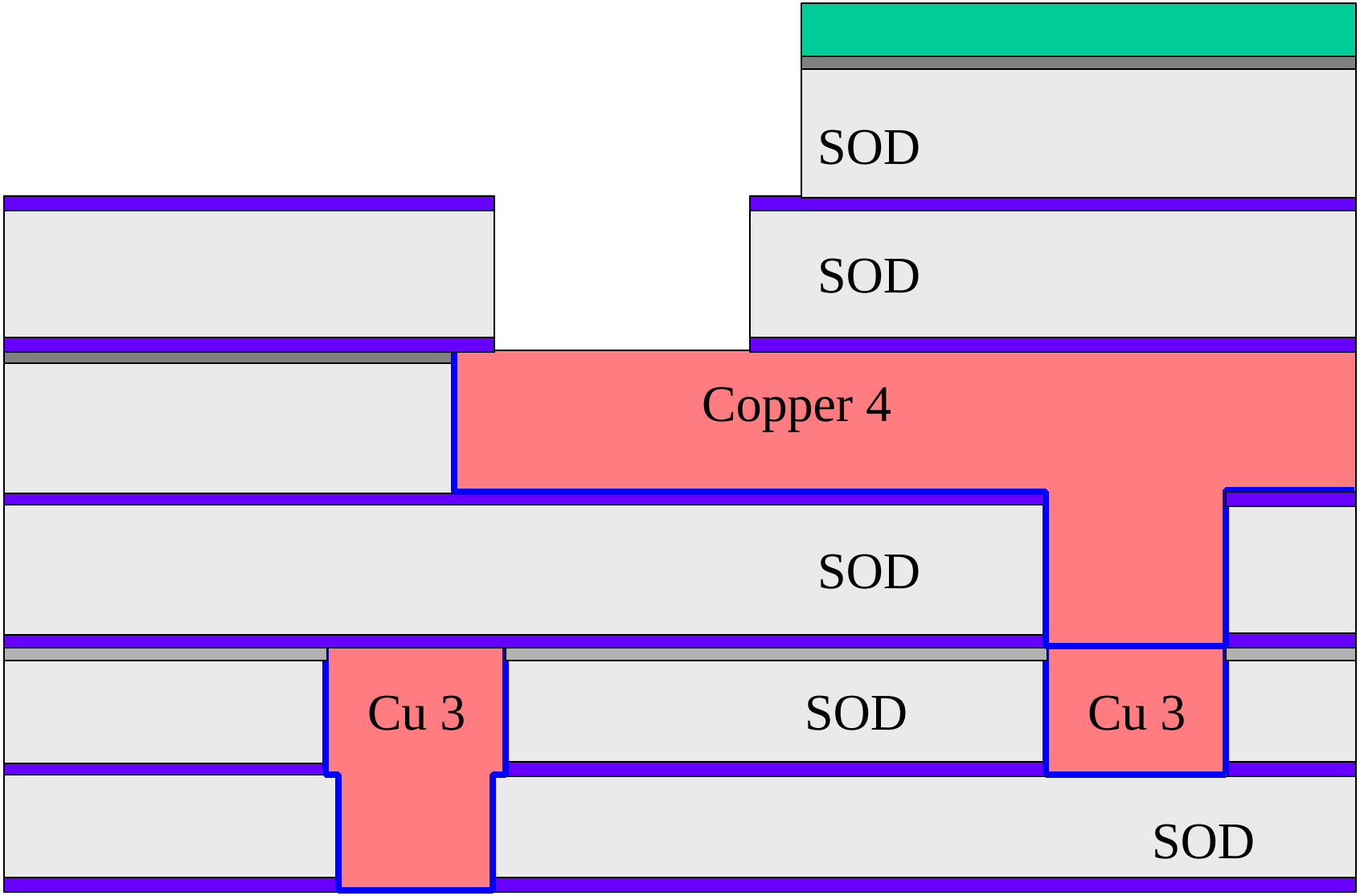
Strip Photoresist



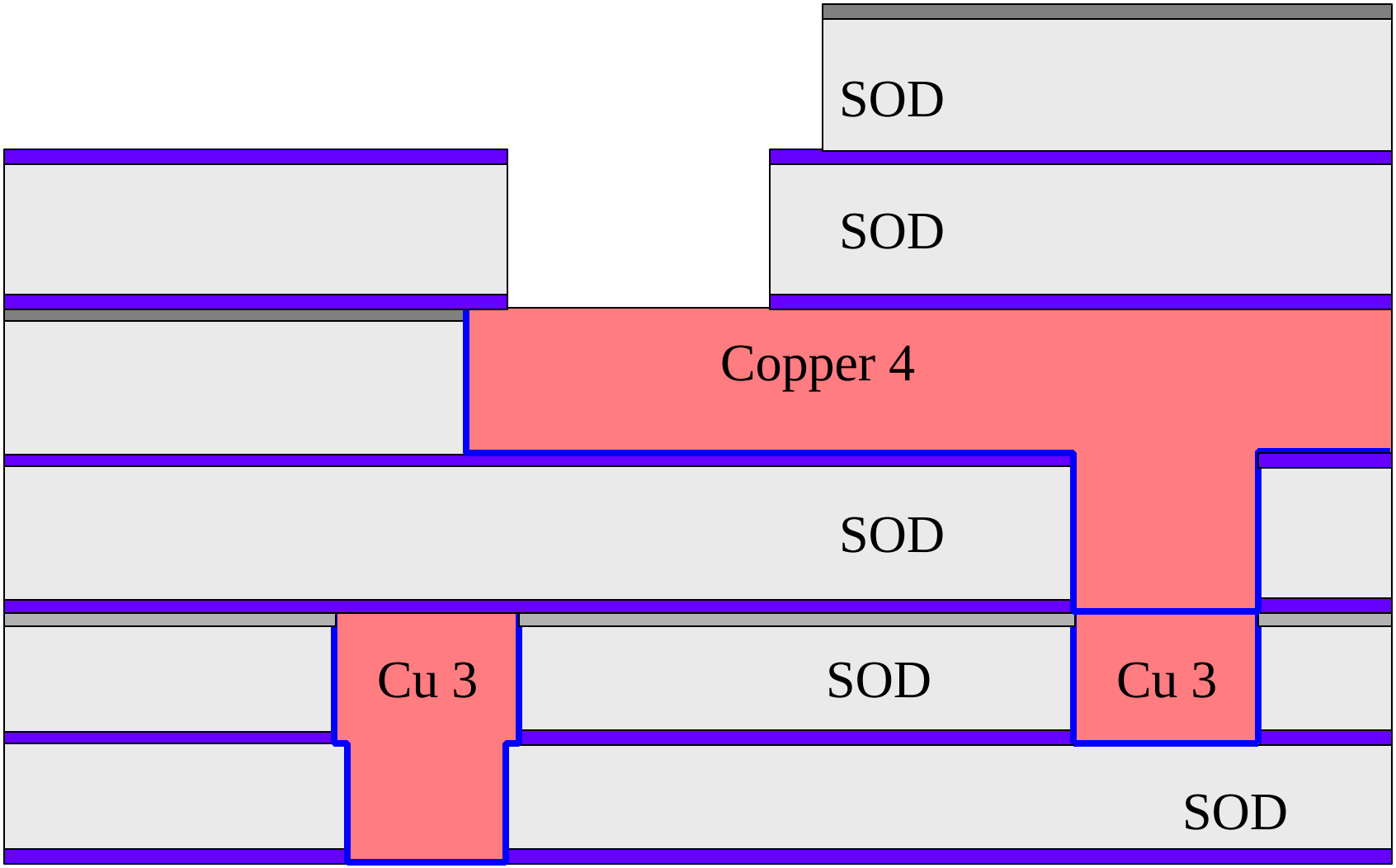
PR Coating, A&E, PEB, and Develop



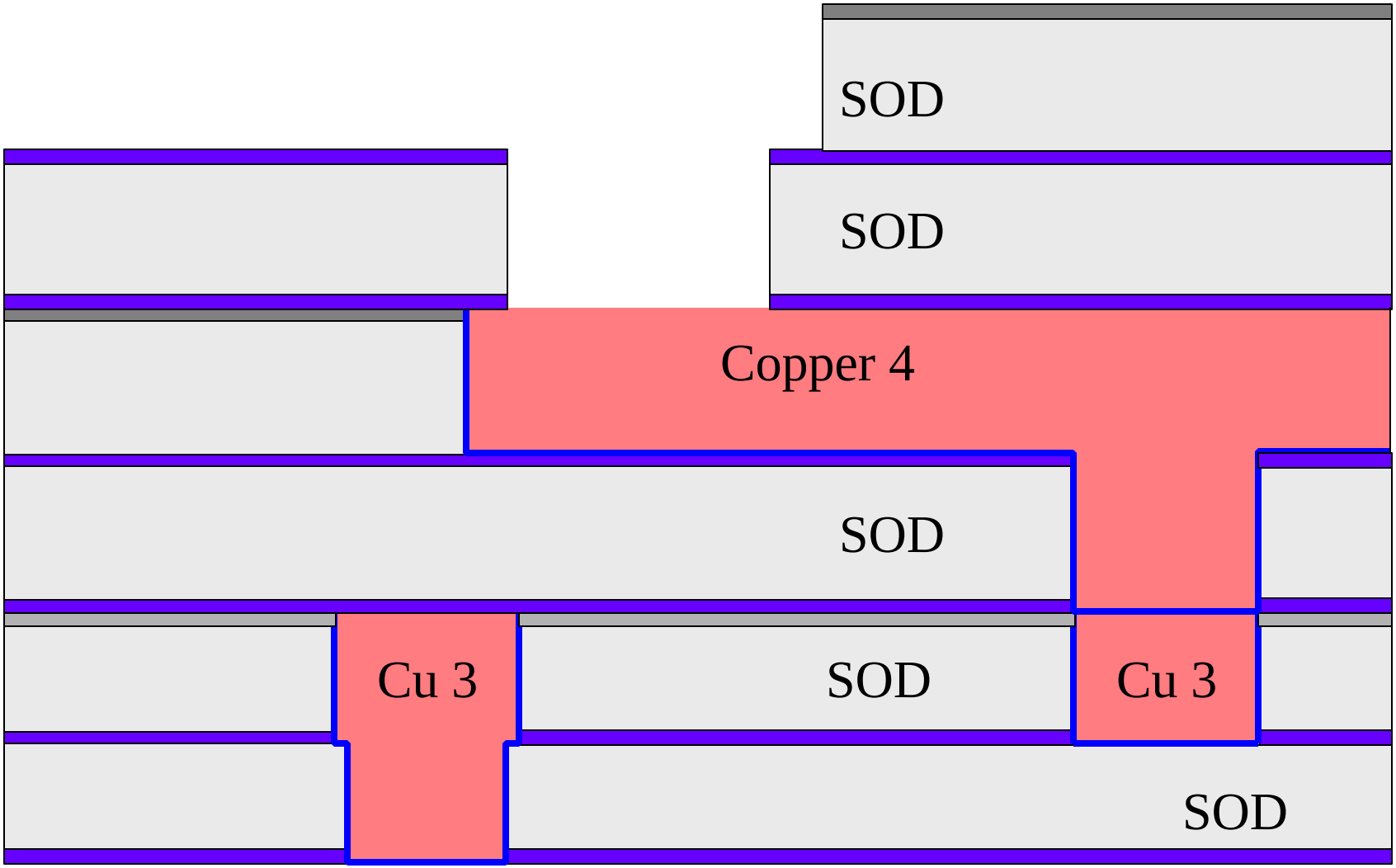
Dielectric Etch



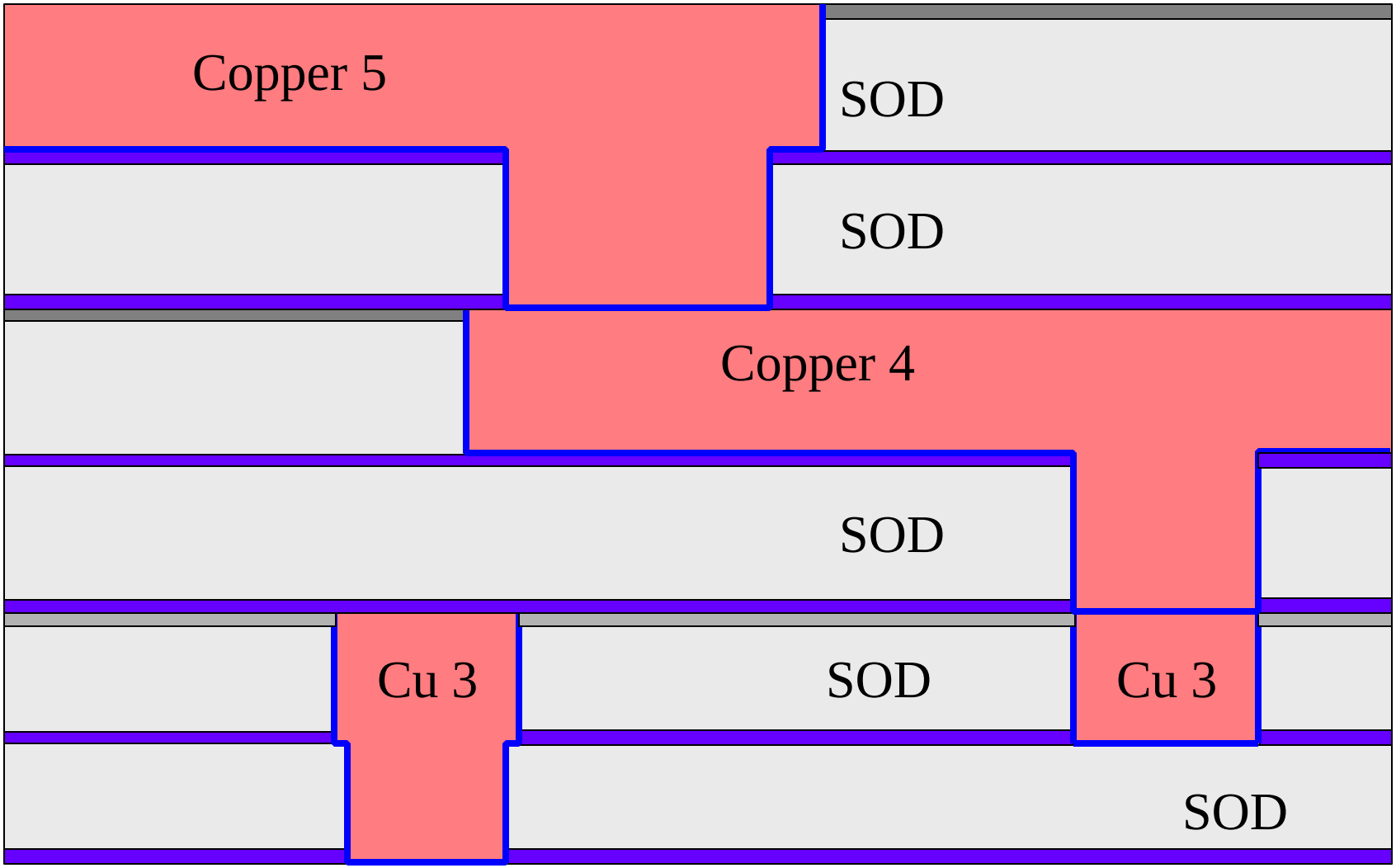
Strip Photoresist



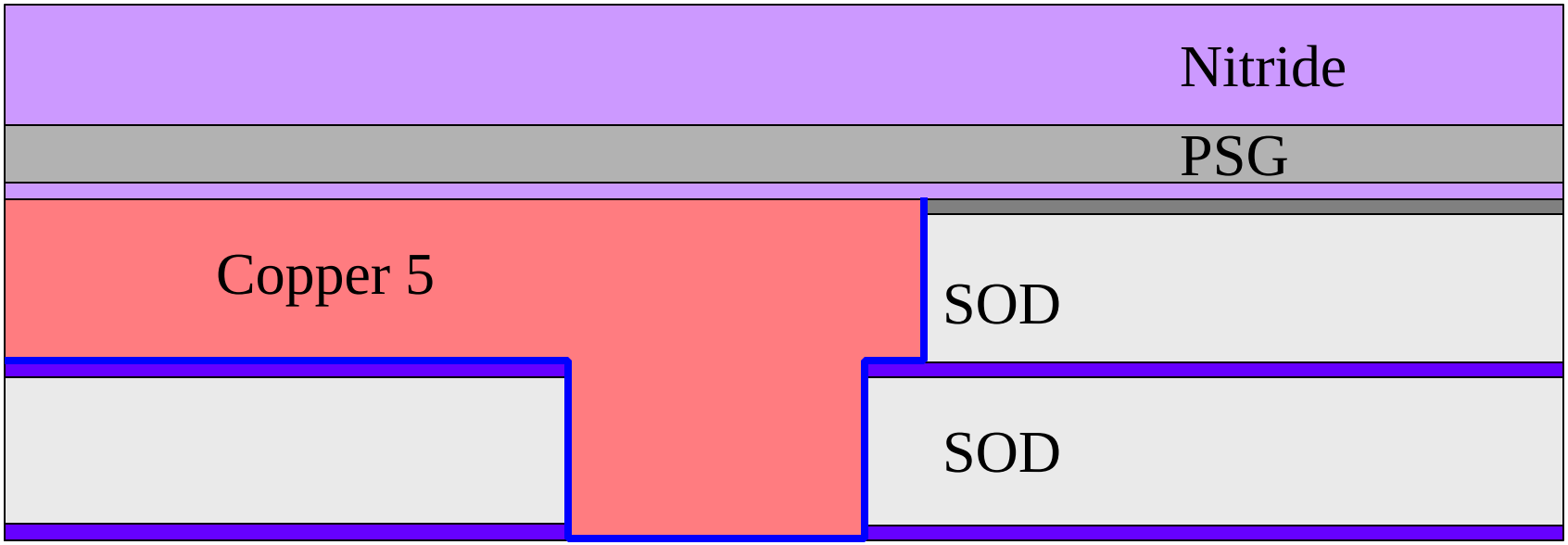
Hydrogen Plasma Clean



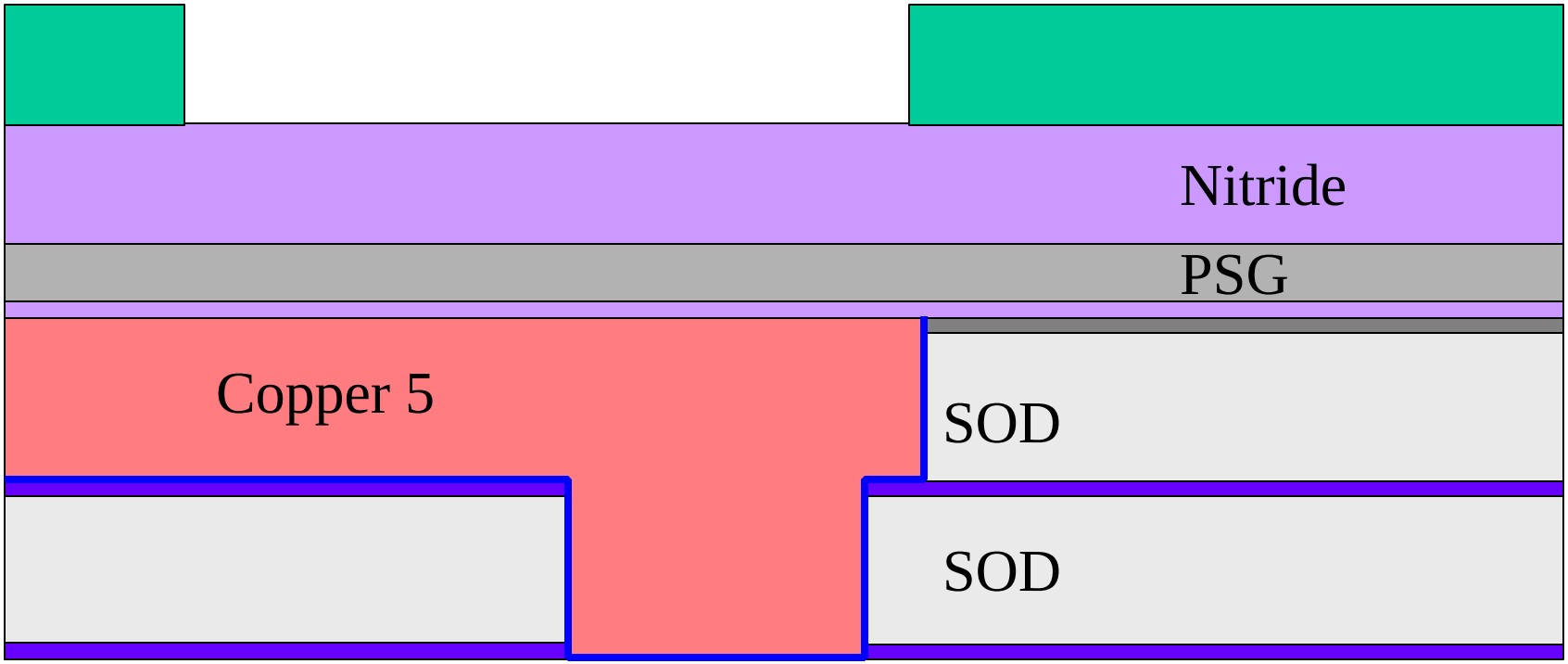
Cu, Ta, and TaN Deposition and CMP



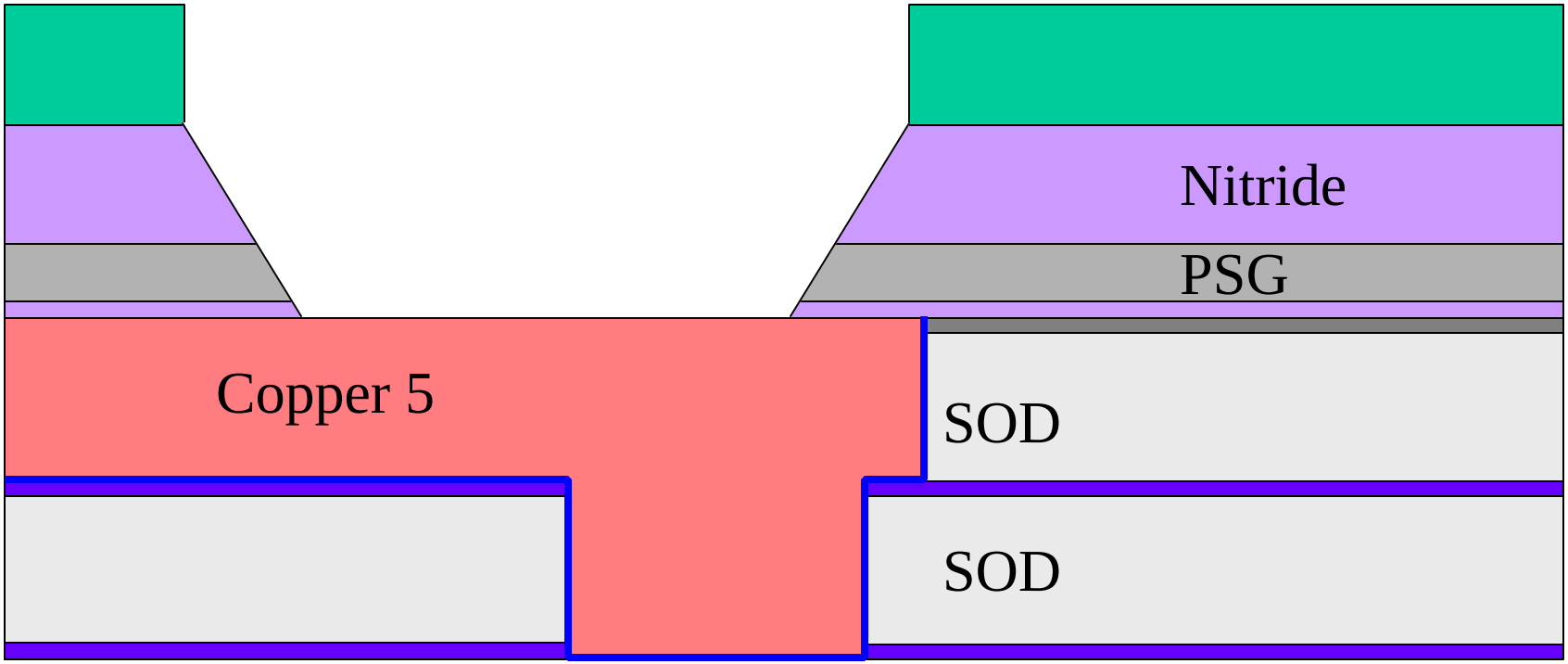
PECVD Passivation Layers: Nitride, PSG, and Nitride



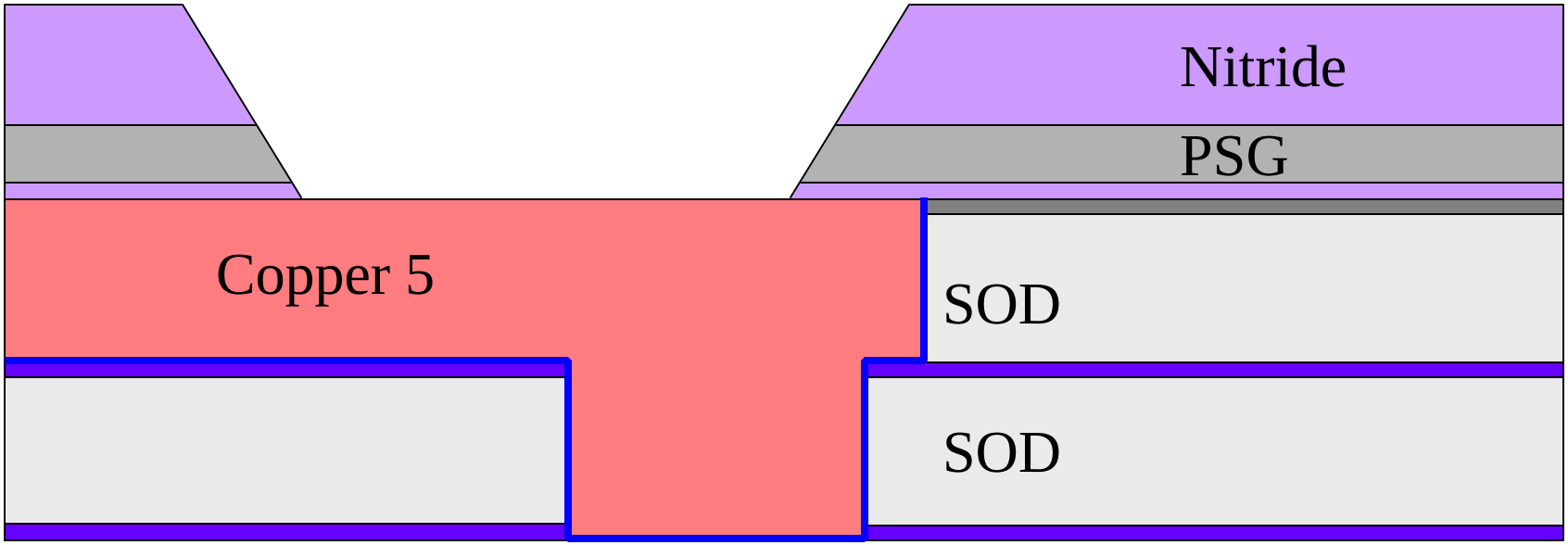
PR Coating, A&E, PEB, and Develop



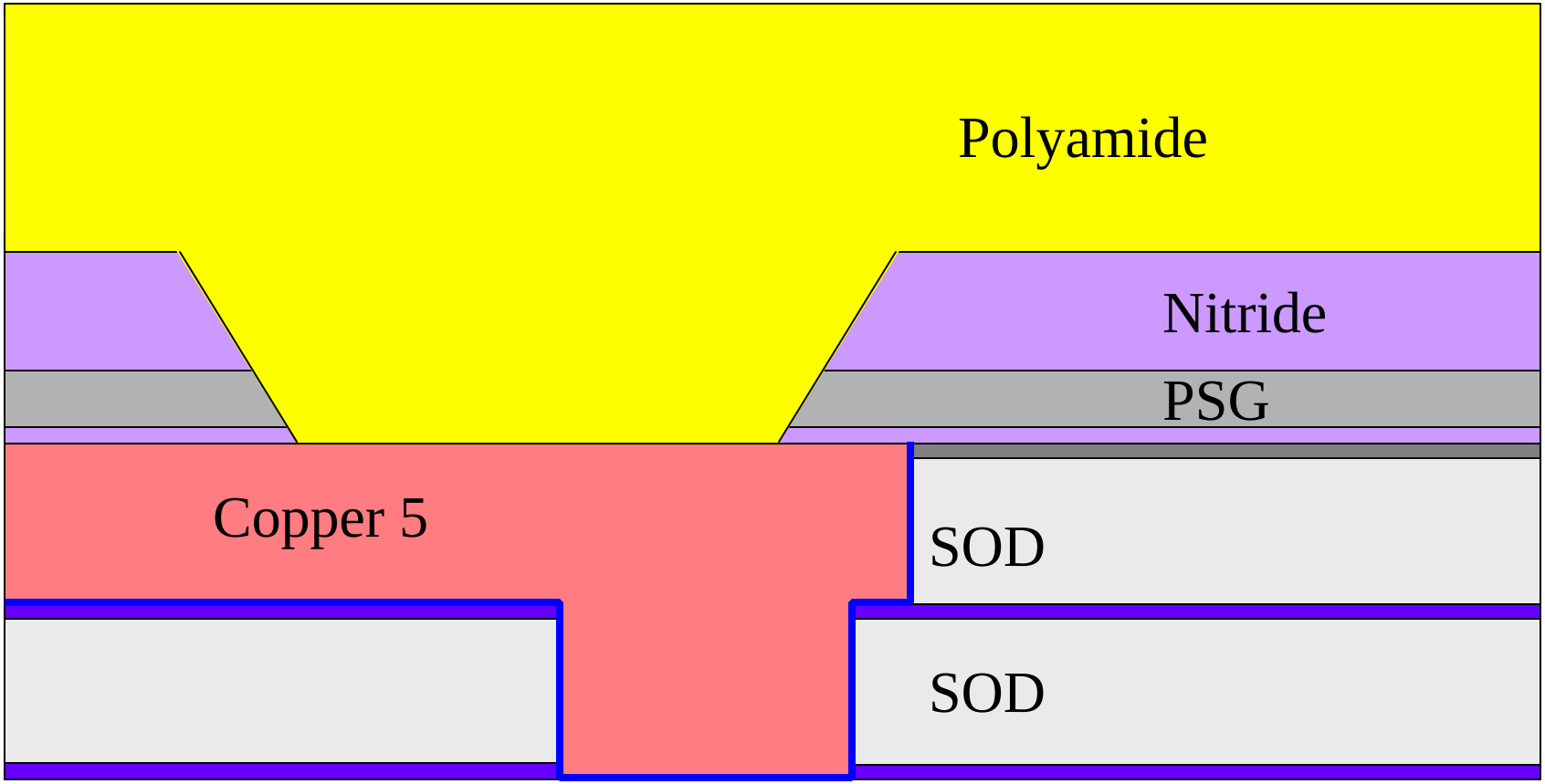
Etch Passivation Layers



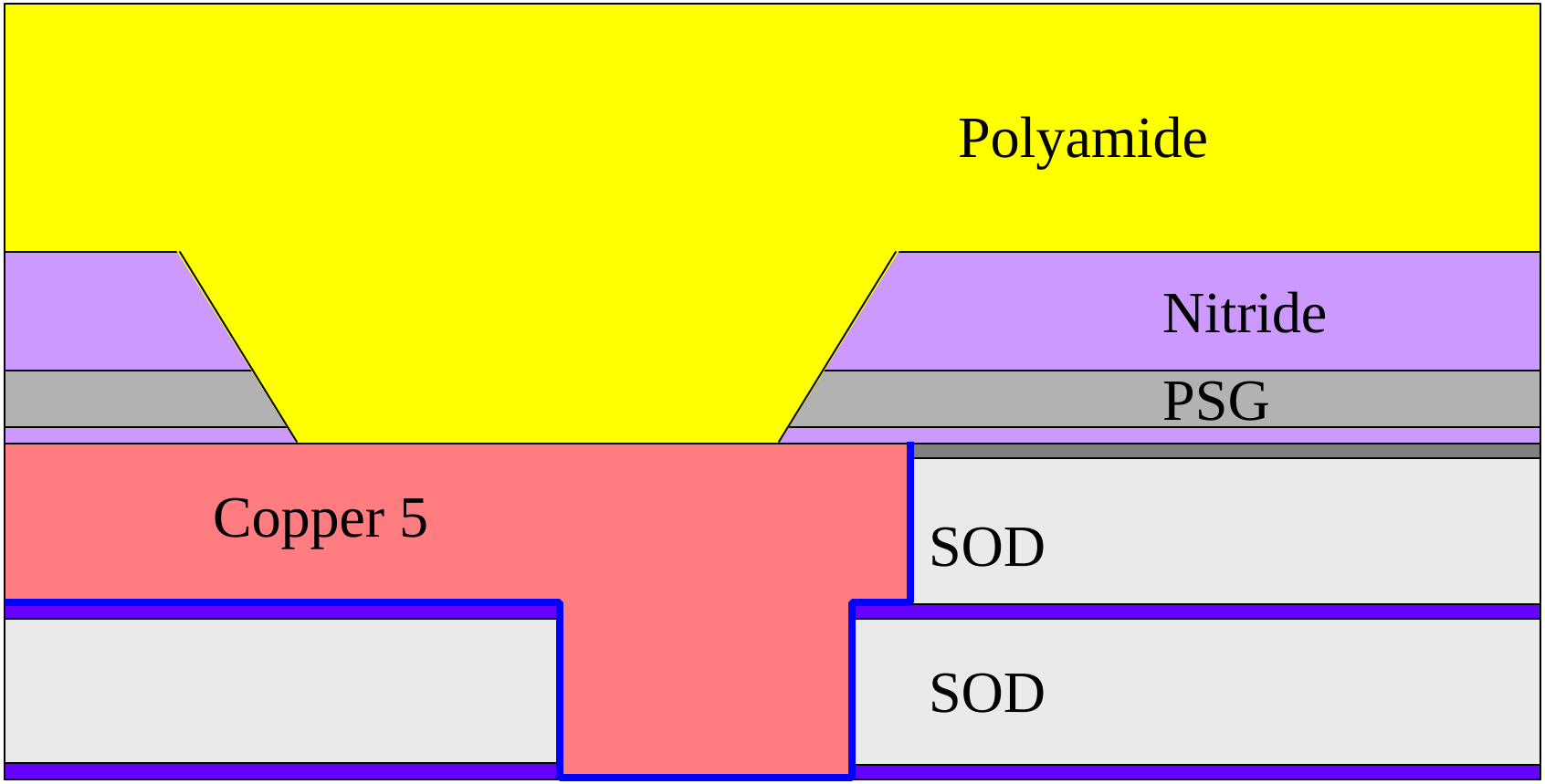
Strip Photoresist



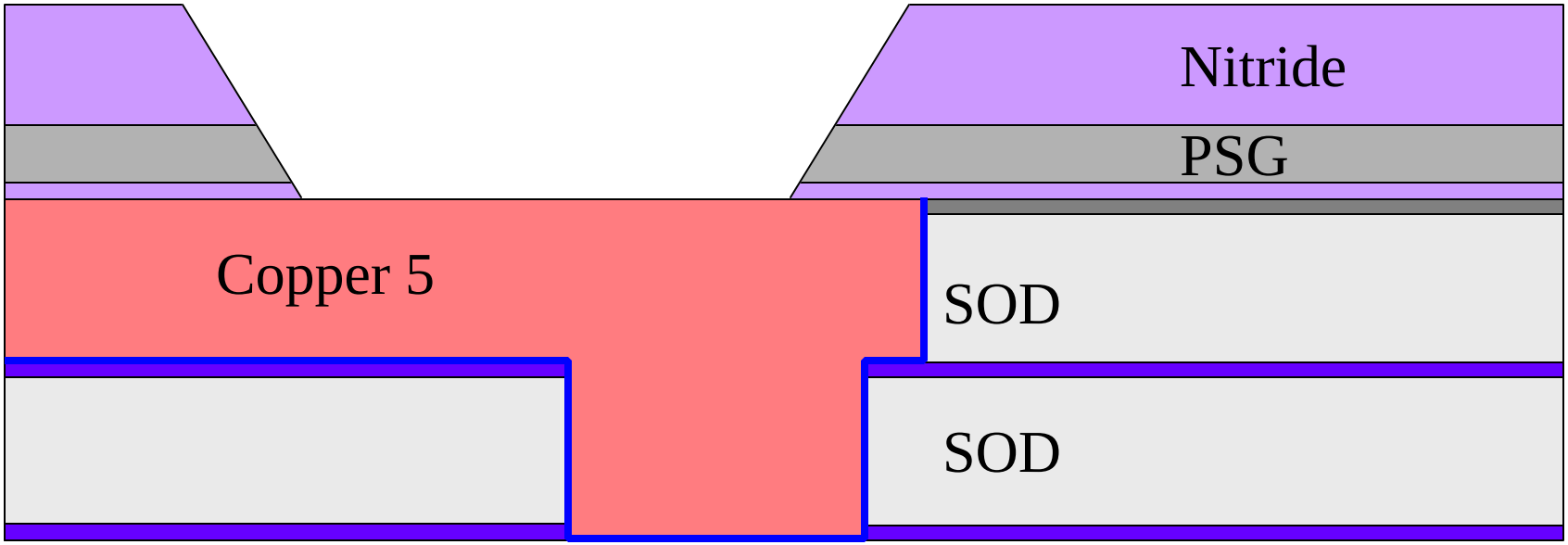
Polyamide Coating



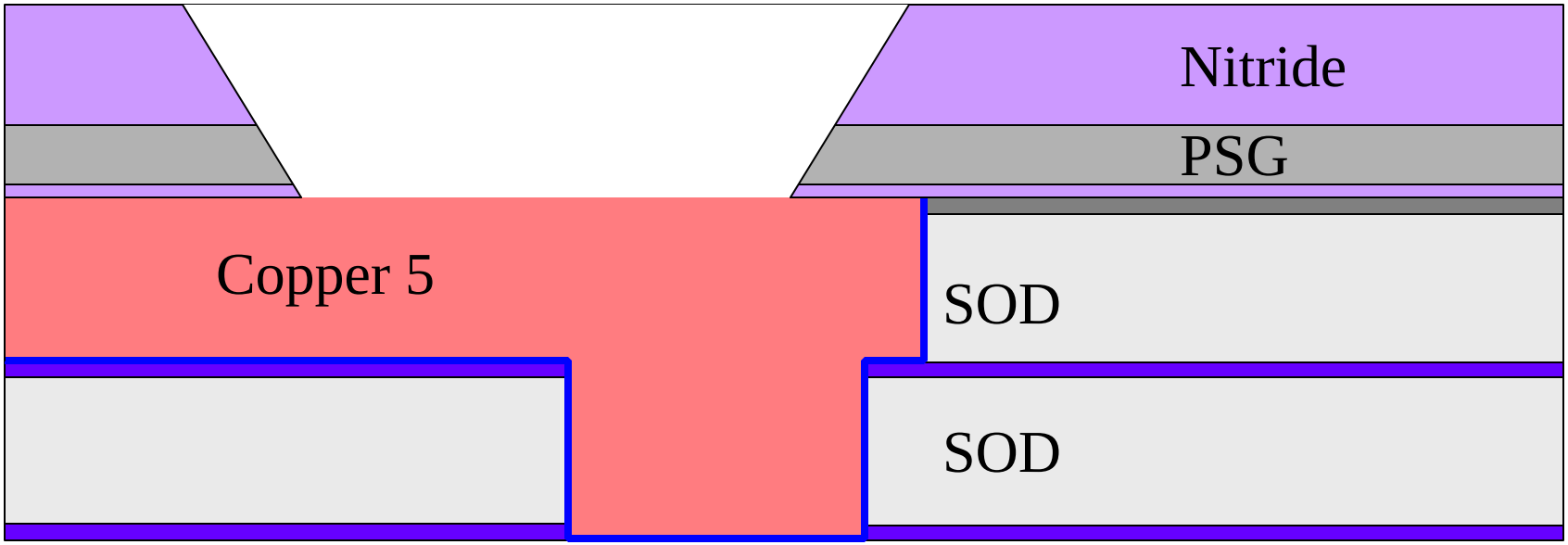
Ship to Test and Package



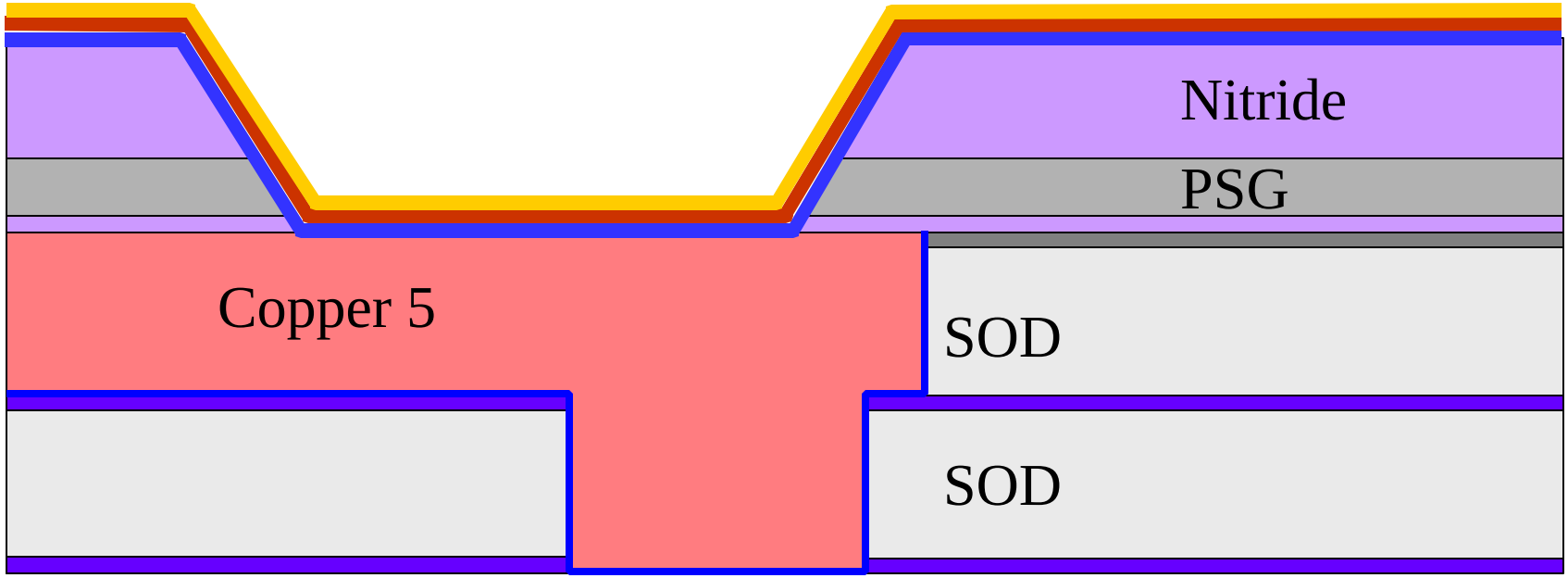
Strip Polyamide



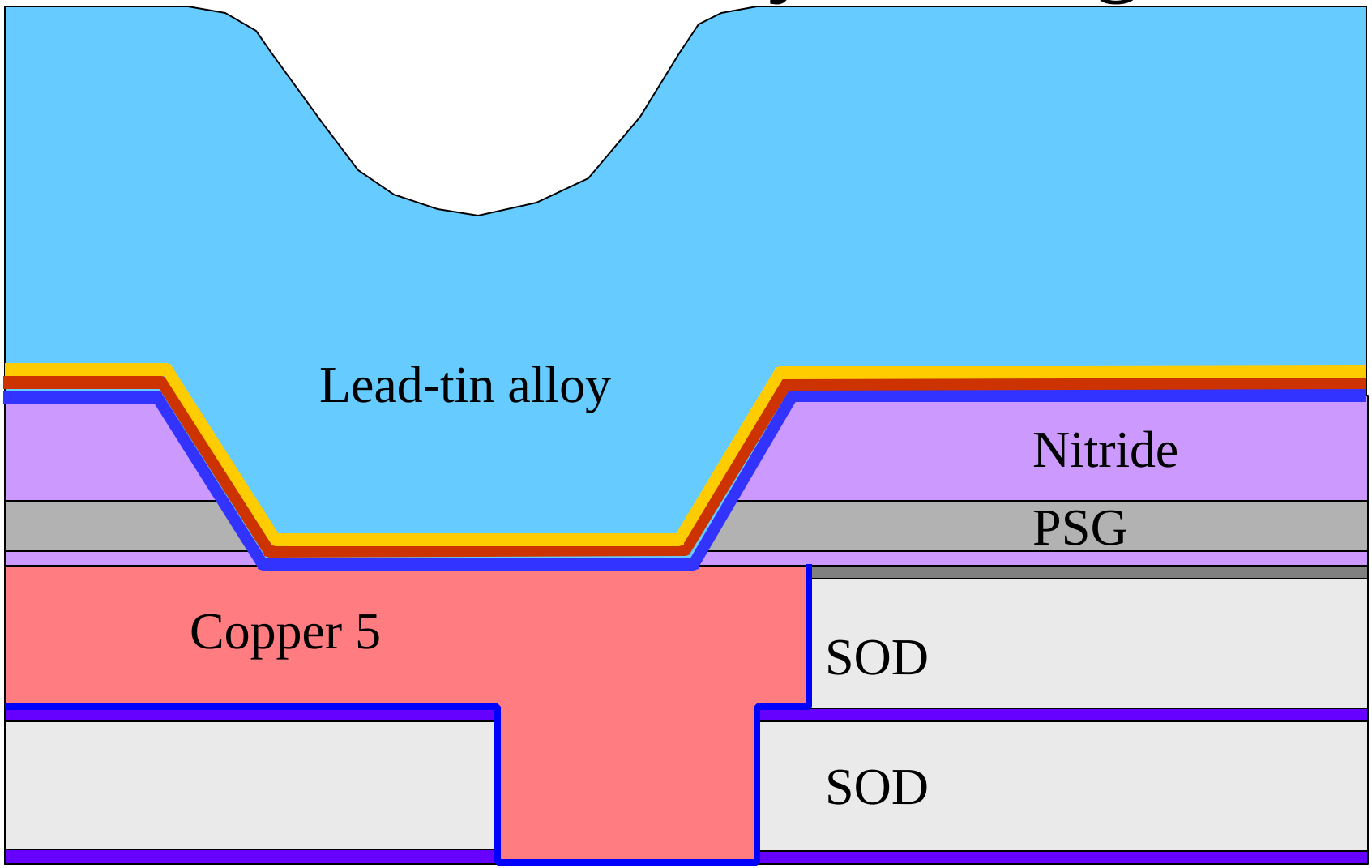
Argon Sputtering Etch



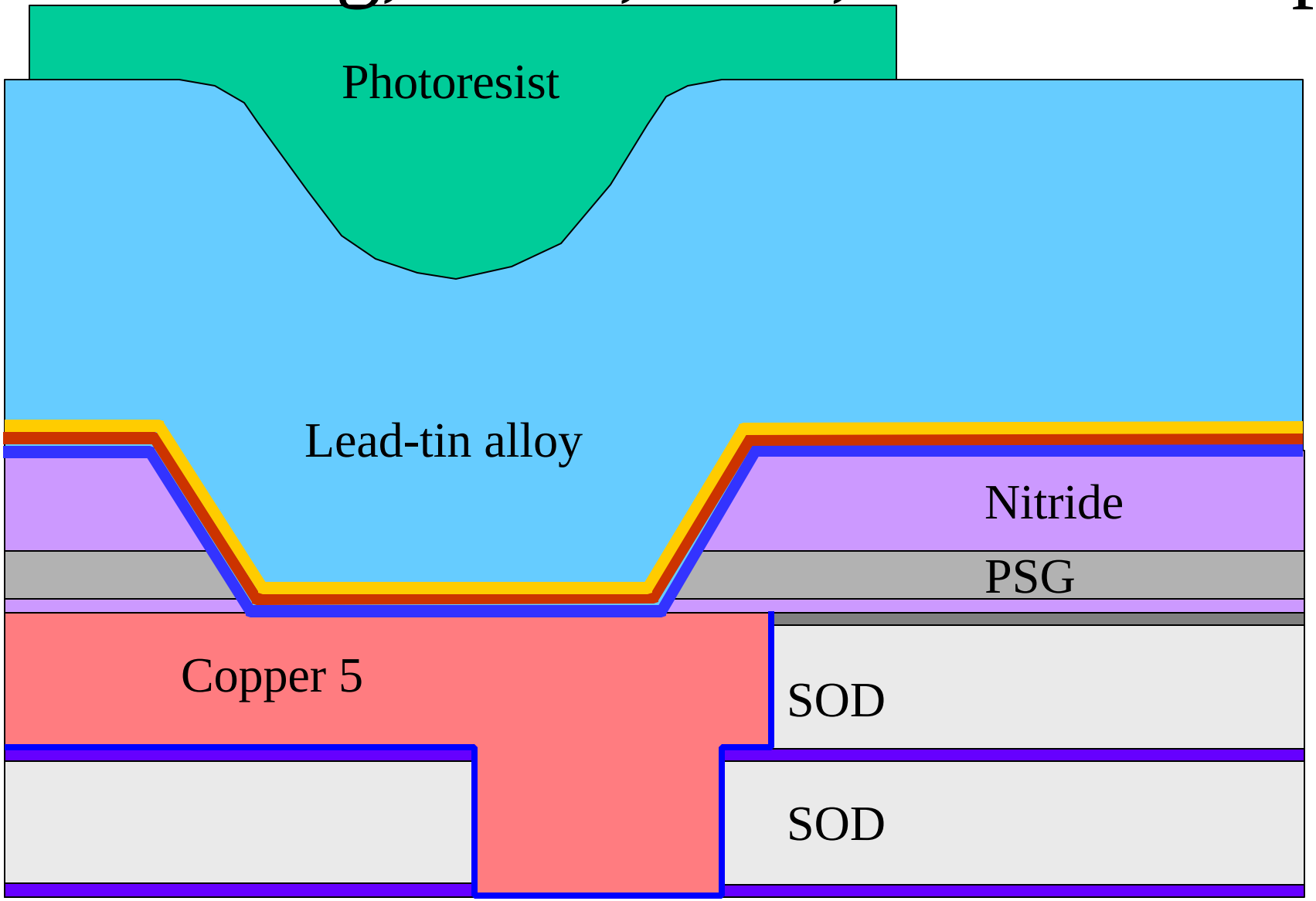
Cr, Cu, and Au Liner Coating



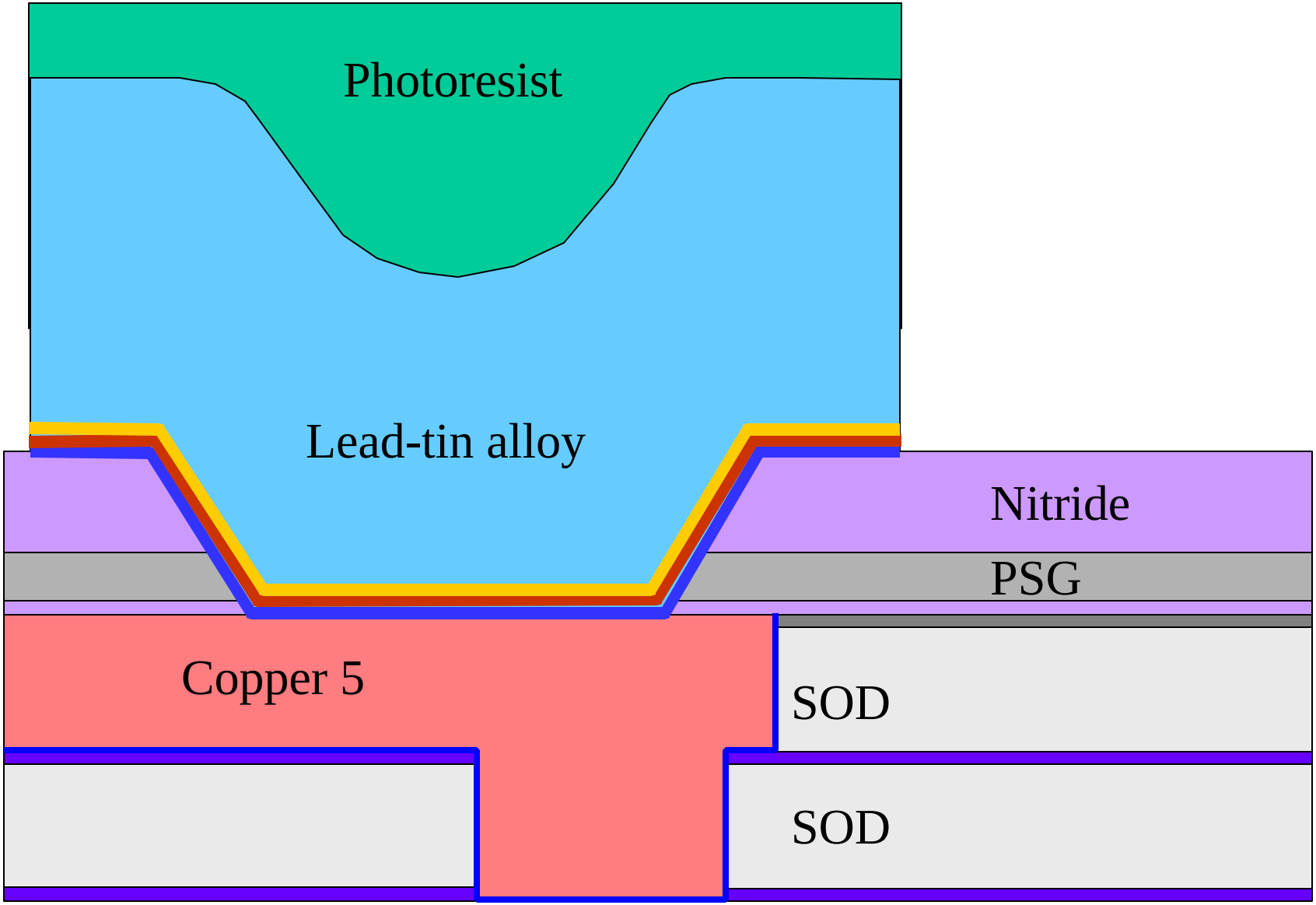
Lead-Tin Alloy Coating



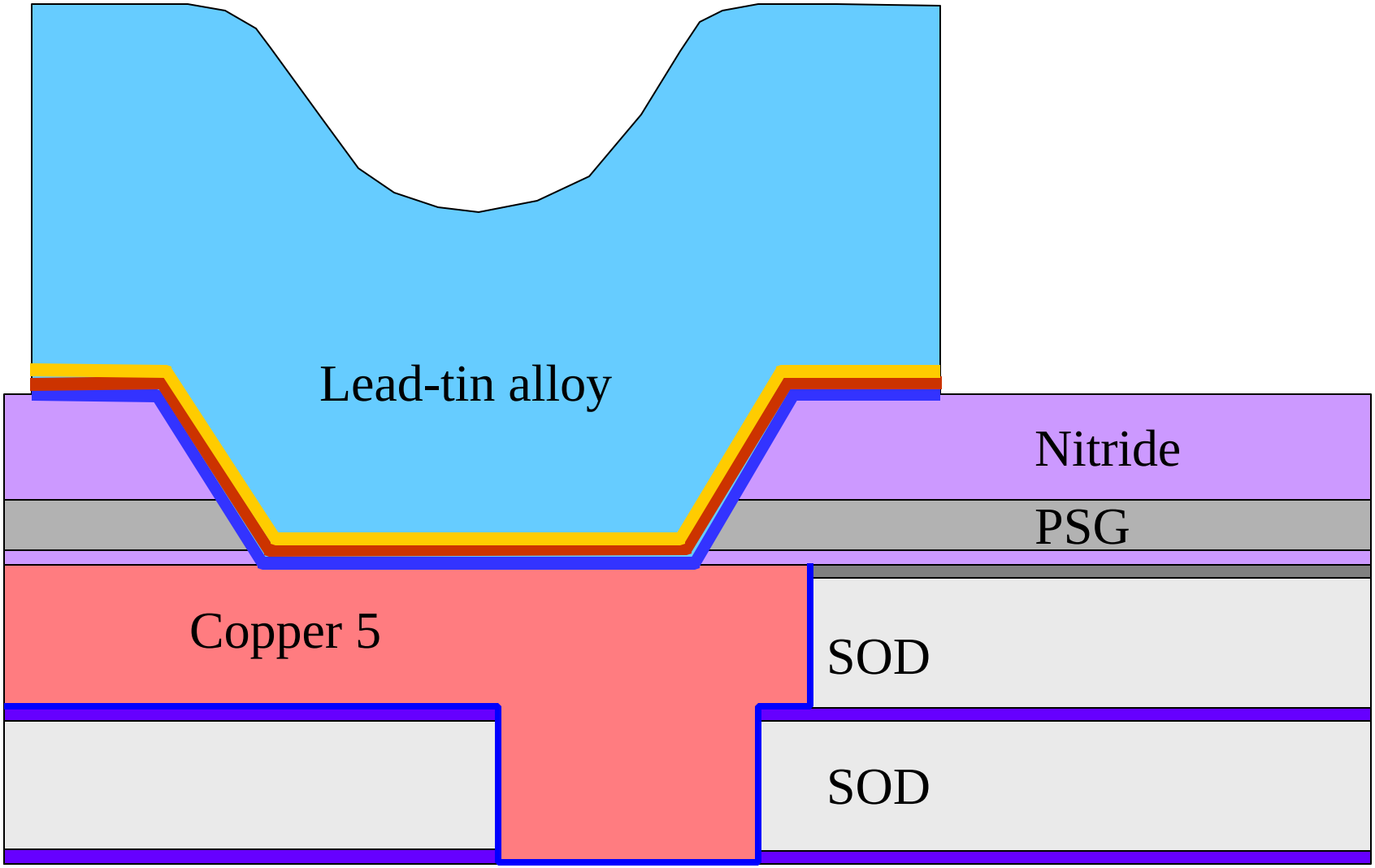
PR Coating, A&E, PEB, and Develop



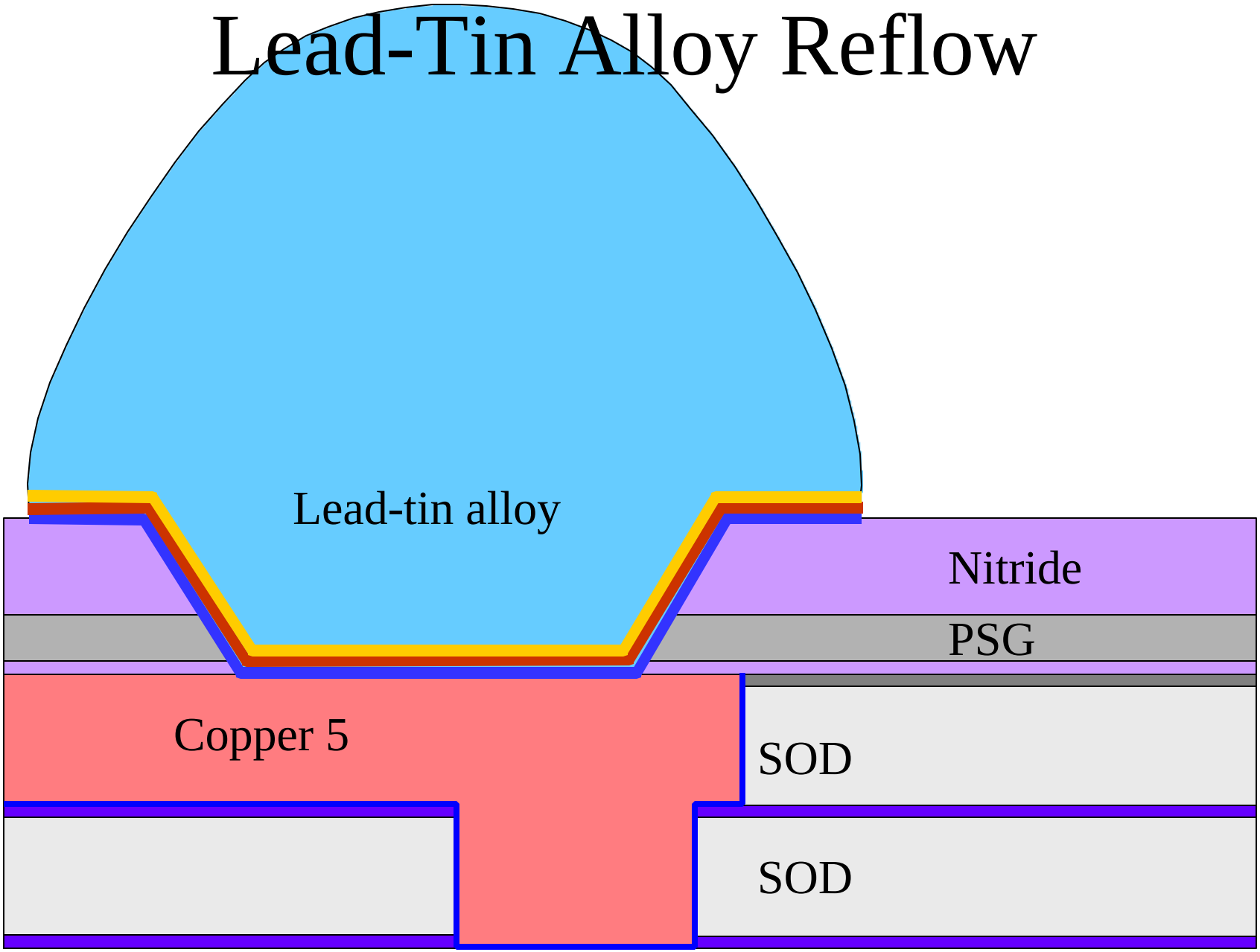
Metal Etch

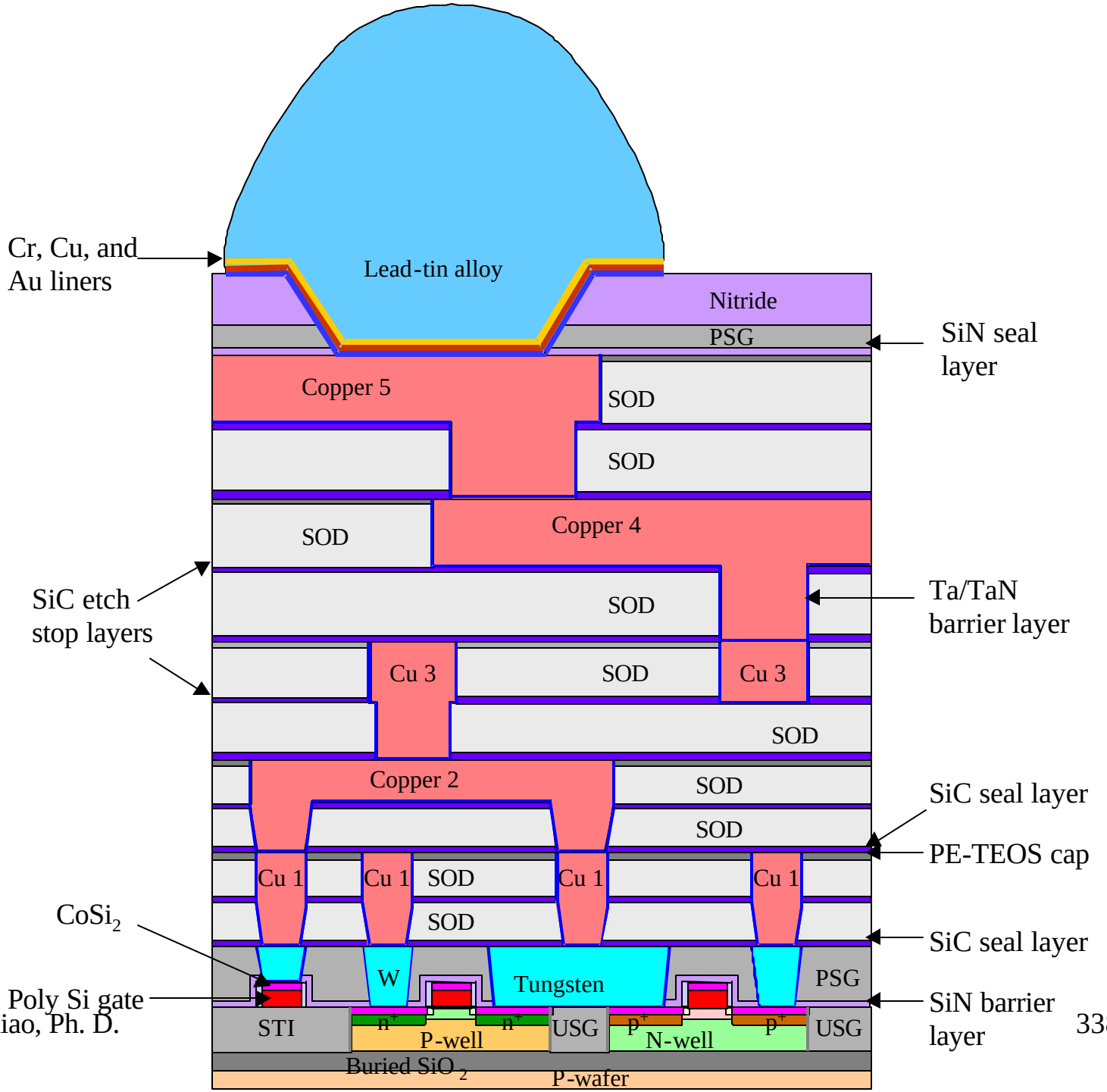


Strip Photoresist



Lead-Tin Alloy Reflow




Cr, Cu, and
Au liners
Lead-tin alloy
Nitride
PSG
SiN seal
layer
Copper 5
SOD
SOD
SOD
Copper 4
SiC etch
stop layers
SOD
Ta/TaN
barrier layer
Cu 3
SOD
Cu 3
SOD
Copper 2
SOD
SOD
SiC seal layer
PE-TEOS cap
Cu 1
Cu 1
SOD
Cu 1
Cu 1
SOD
CoSi2
SiC seal layer
W
Tungsten
PSG
Poly Si gate
SiN barrier
layer
STI
n+
n+
USG
p+
p+
USG
P-well
N-well
Buried SiO2
P-wafer

Summary

- CMOS IC chips dominate semiconductor industry
  - Demands for digital electronics, such as electronic watches, calculators, and personal computers

Summary

- In the 1980s
  - 3 micron to sub-micron
  - Multi-layer metallization
  - Tungsten CVD, dielectric CVD and metal sputtering
  - Sidewall spacer for LDD
  - Plasma etch gradually replaced wet etch in all patterning etch processes.
  - Steppers became popular for alignment and exposure while projection systems were widely used

Summary

- In the 1990s,
  - 0.8 micron to 0.18 micron
  - Silicides used for the gate and local interconnection
  - CMP widely used for tungsten polishing and dielectric planarization
  - RTP is widely used for anneal processes
  - HDP sources are used for etch, CVD, sputtering clean, and sputtering deposition
  - O_3-TEOS oxide CVD processes commonly used for STI, PMD and IMD depositions.
  - ECP is used for copper metallization process