Chapter 5
Thermal Processes

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Objective

- List four thermal processes
- Describe thermal process in IC fabrication
- Describe thermal oxidation process
- Explain the advantage of RTP over furnace
- Relate your job or products to the processes

Topics

- Introduction
- Hardware
- Oxidation
- Diffusion
- Annealing
  - Post-Implantation
  - Alloying
  - Reflow
- High Temp CVD
  - Epi
  - Poly
  - Silicon Nitride
- RTP
  - RTA
  - RTP
- Future Trends

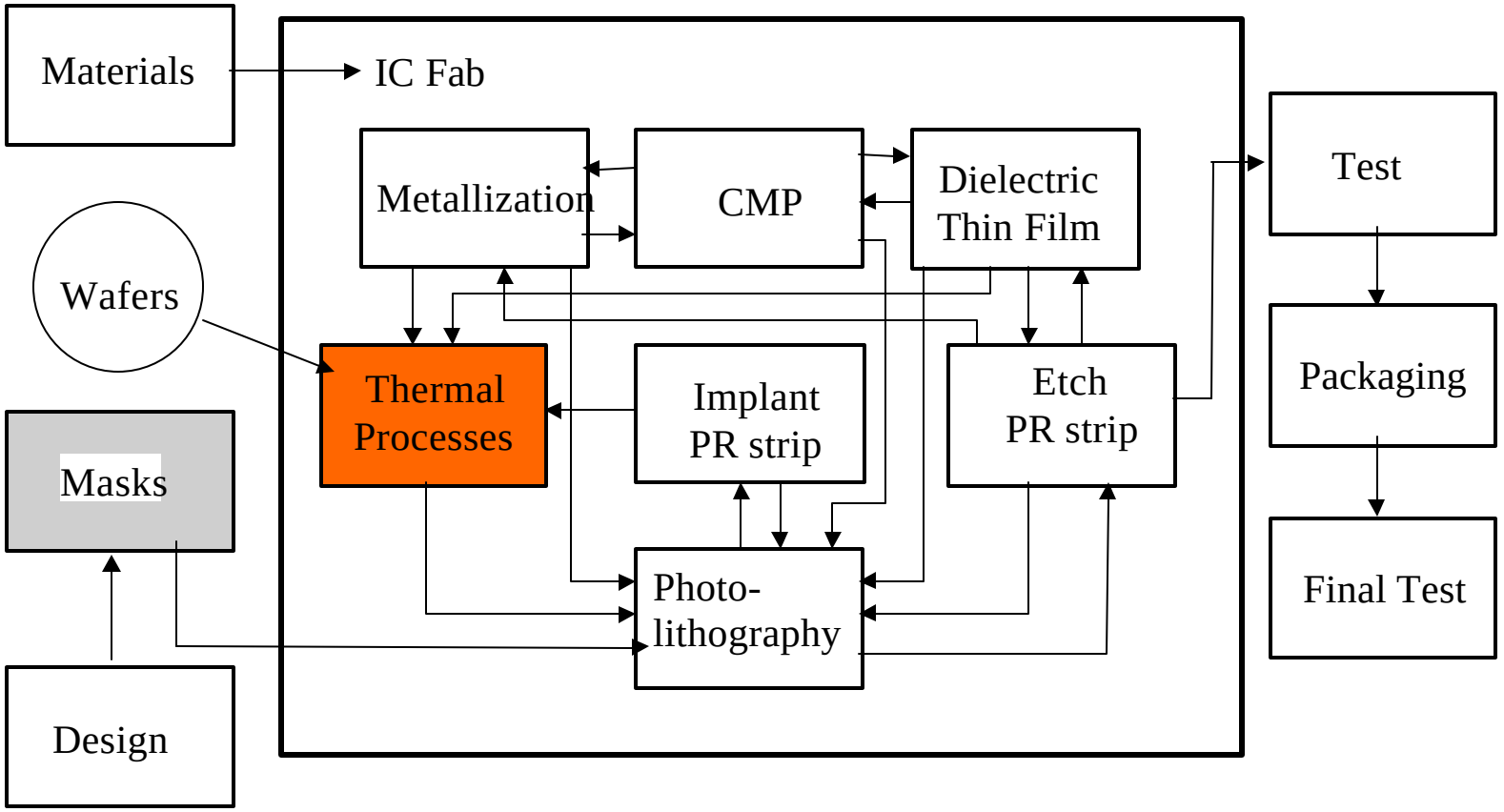
Definition

- Thermal processes are the processes operate at high temperature, which is usually higher than melting point of aluminum.
- They are performed in the front-end of the semiconductor process, usually in high temperature furnace commonly called diffusion furnace.

Introduction

- Advantages of Silicon
  - Abundant, cheap
  - Stable and useful oxide
- Oxidation and Diffusion are the backbone processes in early IC fabrications

Thermal Processes in IC Fabrication

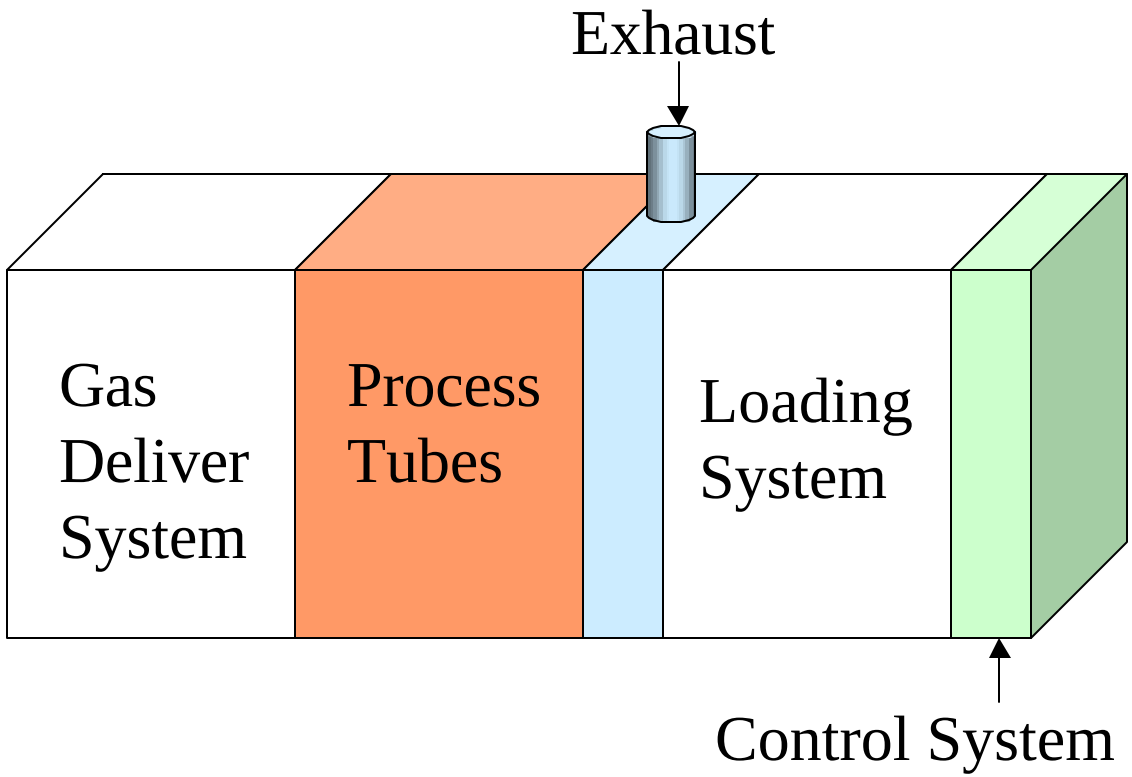


Hardware Overview

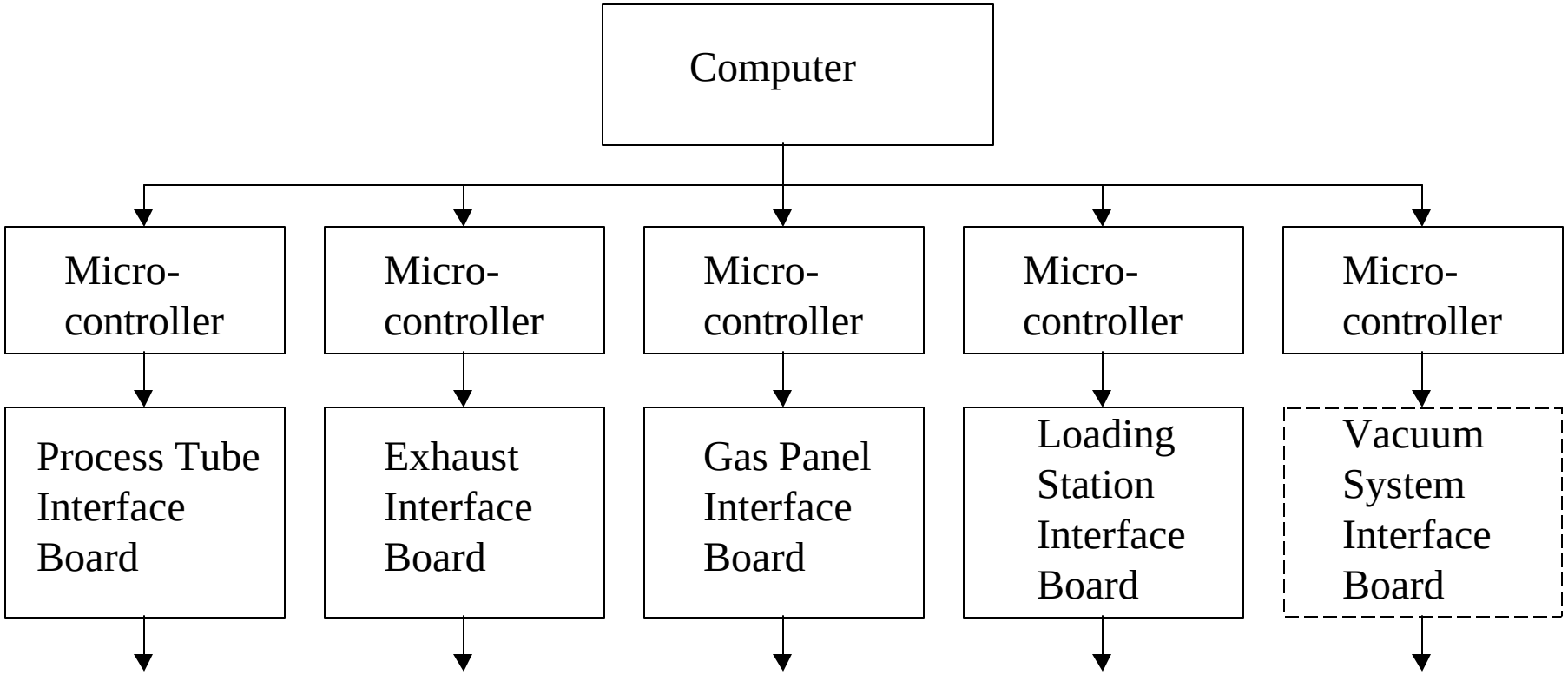
Horizontal Furnace

- Commonly used tool for thermal processes
- Often be called as *diffusion furnace*
- Quartz tube inside a ceramic liner called muffle
- Multi-tube system

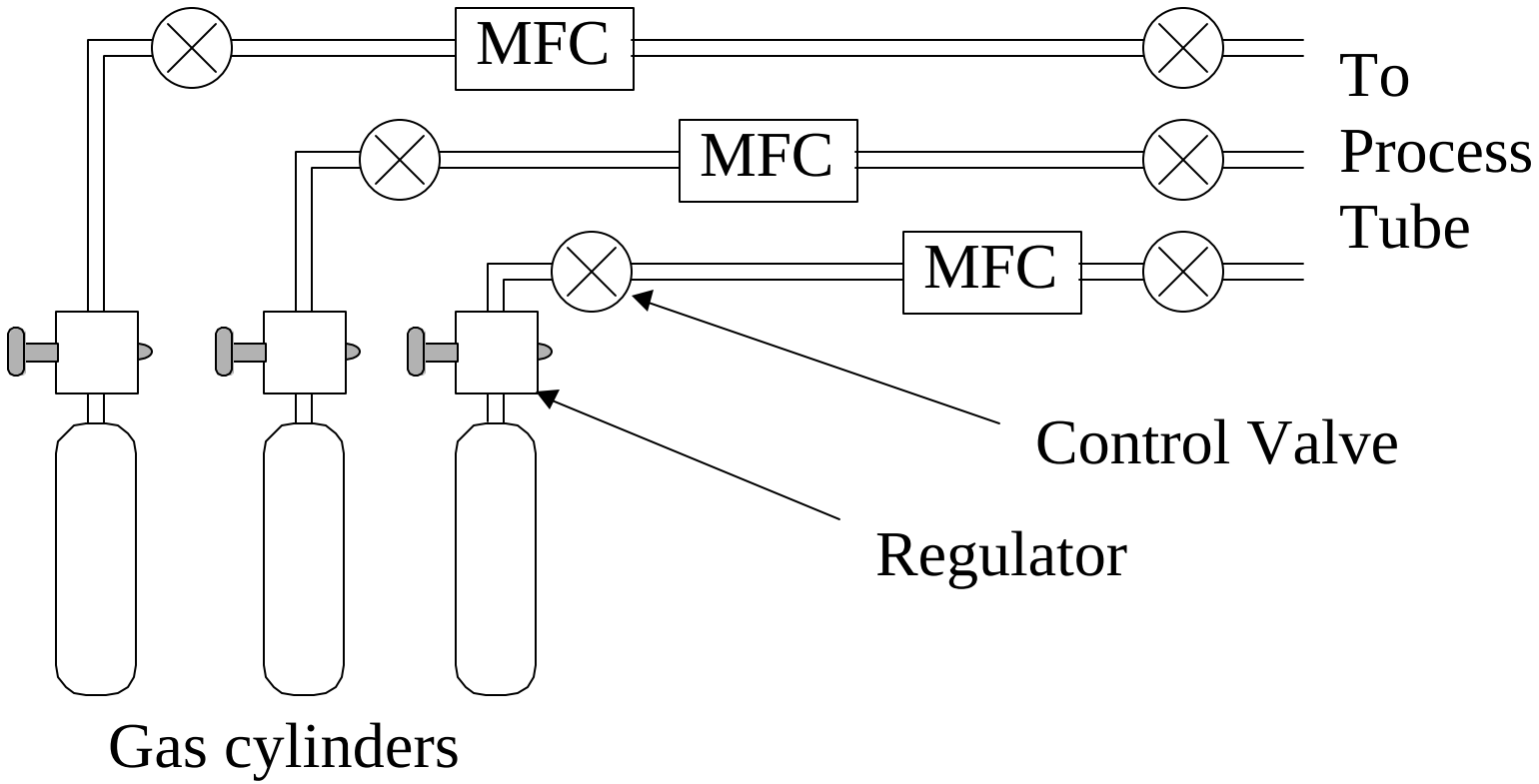
Layout of a Horizontal Furnace



Control System



Gas Deliver System



Source Cabinet

- Source Gases
  - Oxygen
  - Water Vapor
  - Nitrogen
  - Hydrogen
- Gas control panel
- Gas flow controller
- Gas flow meter

Oxidation Sources

- Dry Oxygen
- Water vapor sources
  - Bubblers
  - Flash systems
- Hydrogen and oxygen, $H_2 + O_2 \rightarrow H_2O$
- Chlorine sources, for minimized mobile ions in gate oxidation
  - Anhydrous hydrogen chloride HCl
  - Trichloroethylene (TCE), Trichloroethane (TCA)

Diffusion Sources

- P-type dopant
  - B_2H_6, burnt chocolate, sickly sweet odor
  - Poisonous, flammable, and explosive
- N-type dopants
  - PH_3, rotten fish smell
  - AsH_3, garlic smell
  - Poisonous, flammable, and explosive
- Purge gas
  - N_2

Deposition Sources

- Silicon source for poly and nitride deposition:
  - Silane, SiH_4, pyrophoric, toxic and explosive
  - DCS, SiH_2Cl_2, extremely flammable
- Nitrogen source for nitride deposition:
  - NH_3, pungent, irritating odor, corrosive
- Dopants for polysilicon deposition
  - B_2H_6, PH_3 and AsH_3
- Purge gas
  - N_2

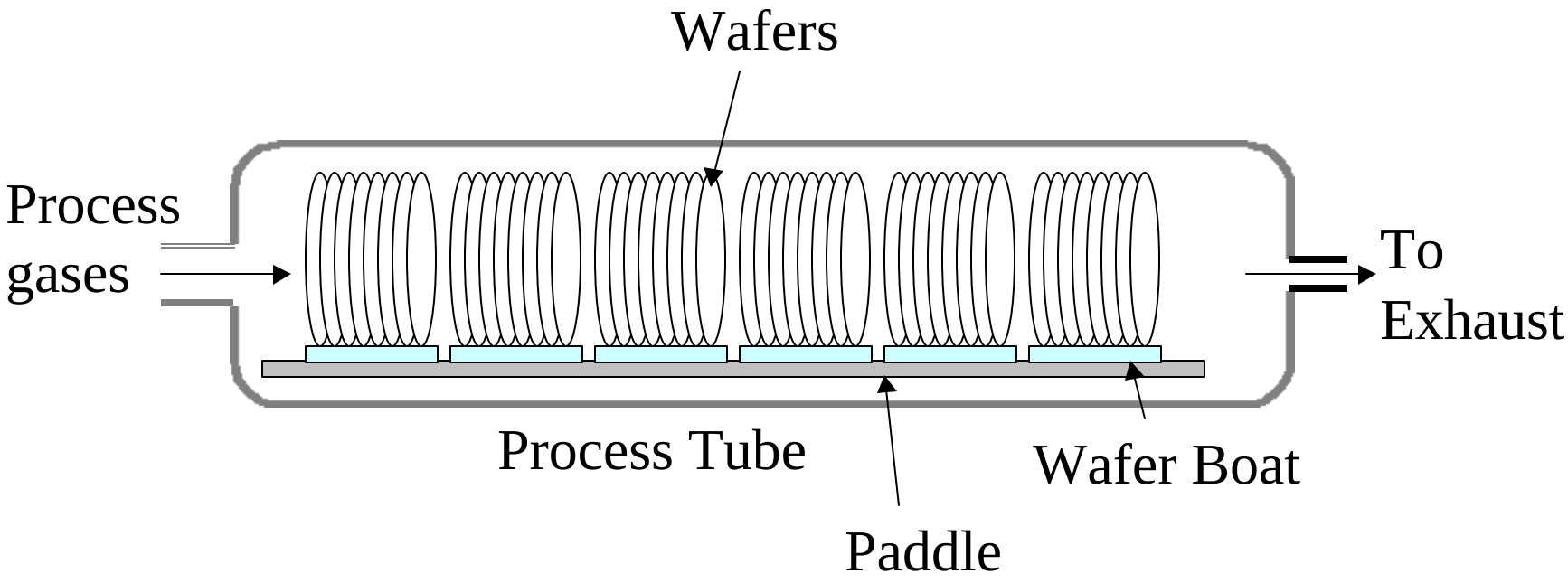
Anneal Sources

- High purity N_2, is used for most anneal processes.
- H_2O sometimes used as ambient for PSG or BPSG reflow.
- O_2 is used for USG anneal after USG CMP in STI formation process.
- Lower grade N_2 is used for idle purge.

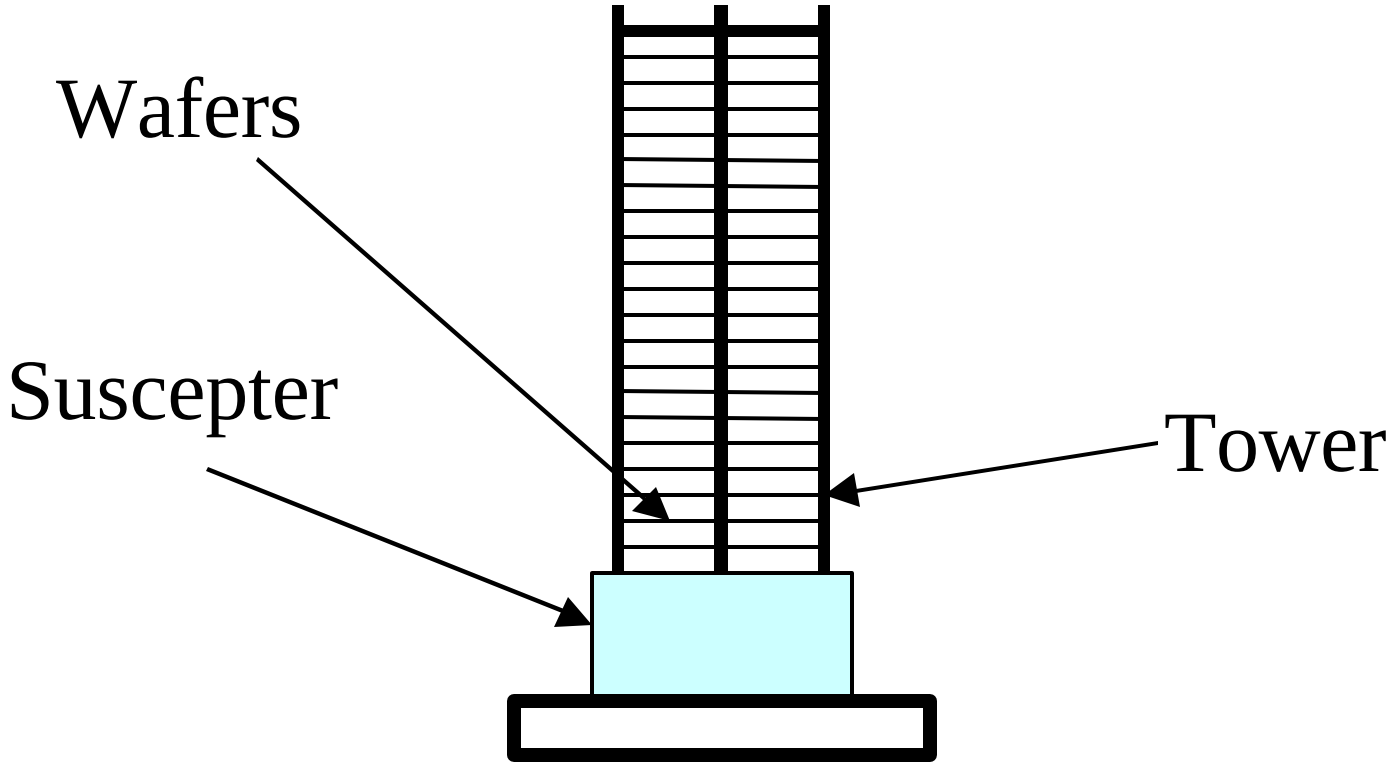
Exhaust System

- Removal of hazardous gases before release
- Poisonous, flammable, explosive and corrosive gases.
- Burn box removes most poisonous, flammable and explosive gases
- Scrubber removes burned oxide and corrosive gases with water.
- Treated gases exhaust to the atmosphere.

Wafer Loading, Horizontal System



Wafer Loading, Vertical System



Temperature Control

- Thermal processes are very sensitive to the temperature
- Precisely temperature control is vital
- ±0.5 °C at central zone
- ±0.05% at 1000 °C!

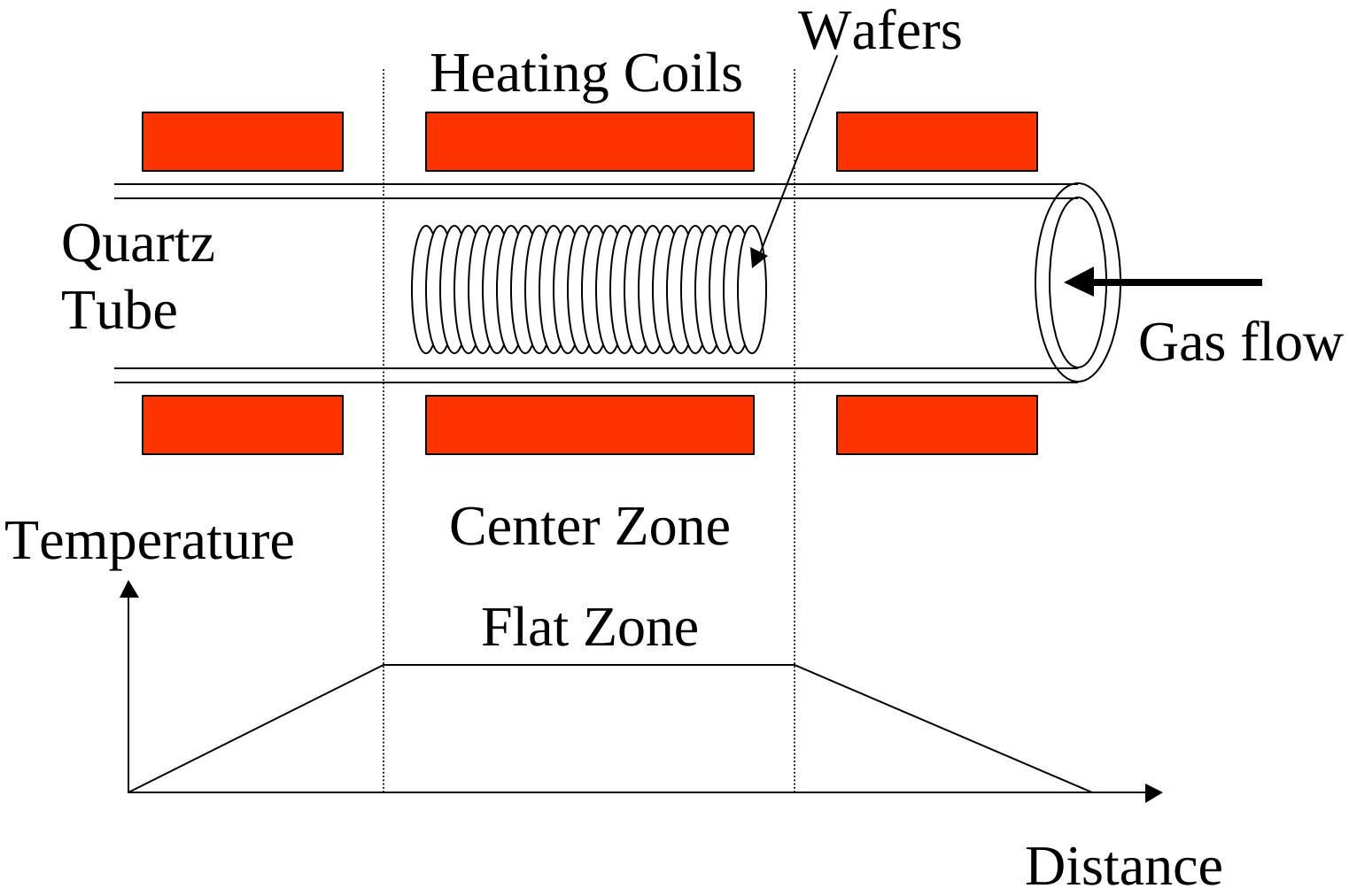
Temperature Control System

- Thermocouples touching the reaction tube
- Proportional band controllers feed the power to the heating coils
- The heating power is proportional to difference between setting point and measured value

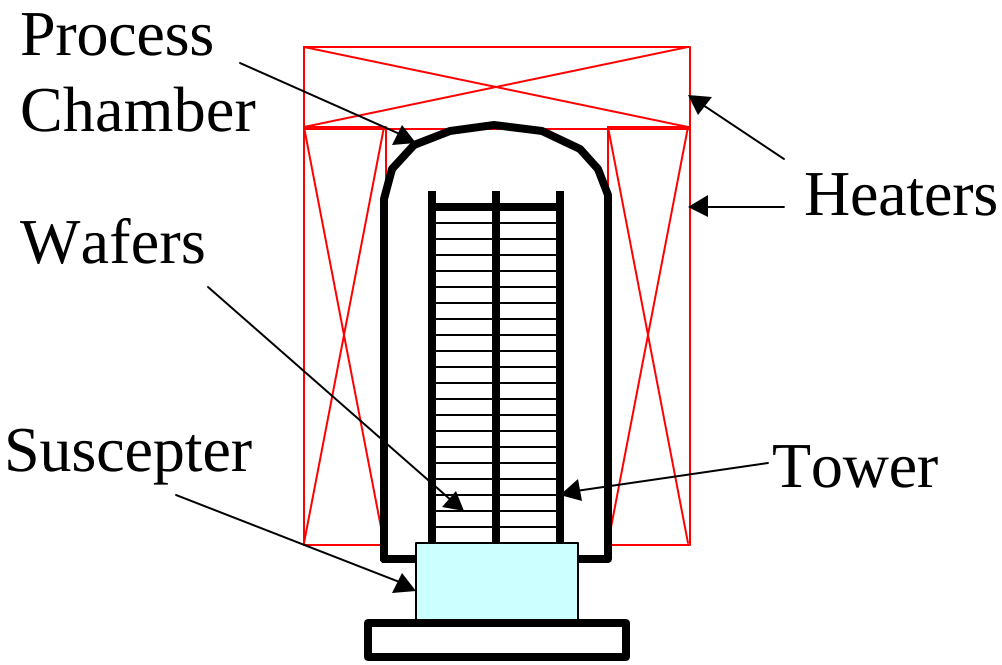
Reaction Chamber

- High-purity Quartz
  - Stability at high temperature
  - Basic Cleanliness
- Drawback
  - Fragility
  - Some metallic ions
  - Not a sodium barrier
  - Small flakes at > 1200 °C, *devitrification*

Horizontal Furnace



Vertical Furnace, Process Position



Quartz Tube

- Electric Fused
- Flame Fused
- Both of them as trace amount of metals
- Flame-fused tubes produced devices have better characteristics.

Quartz Tube Clean

- Very important especially for deposition furnace to prevent particle contamination
- Out side fab, ex-situ
  - Hydrofluoric acid (HF) tank
  - Remove a thin layer of quartz every time
  - limited tube lifetime
- In-situ clean
  - Plasma generator inside tube
  - Free fluorine from NF_3 etch away contaminant

Silicon Carbide Tube

- Pro
  - Higher thermal stability
  - Better metallic ion barrier
- Con
  - Heavier
  - More expensive

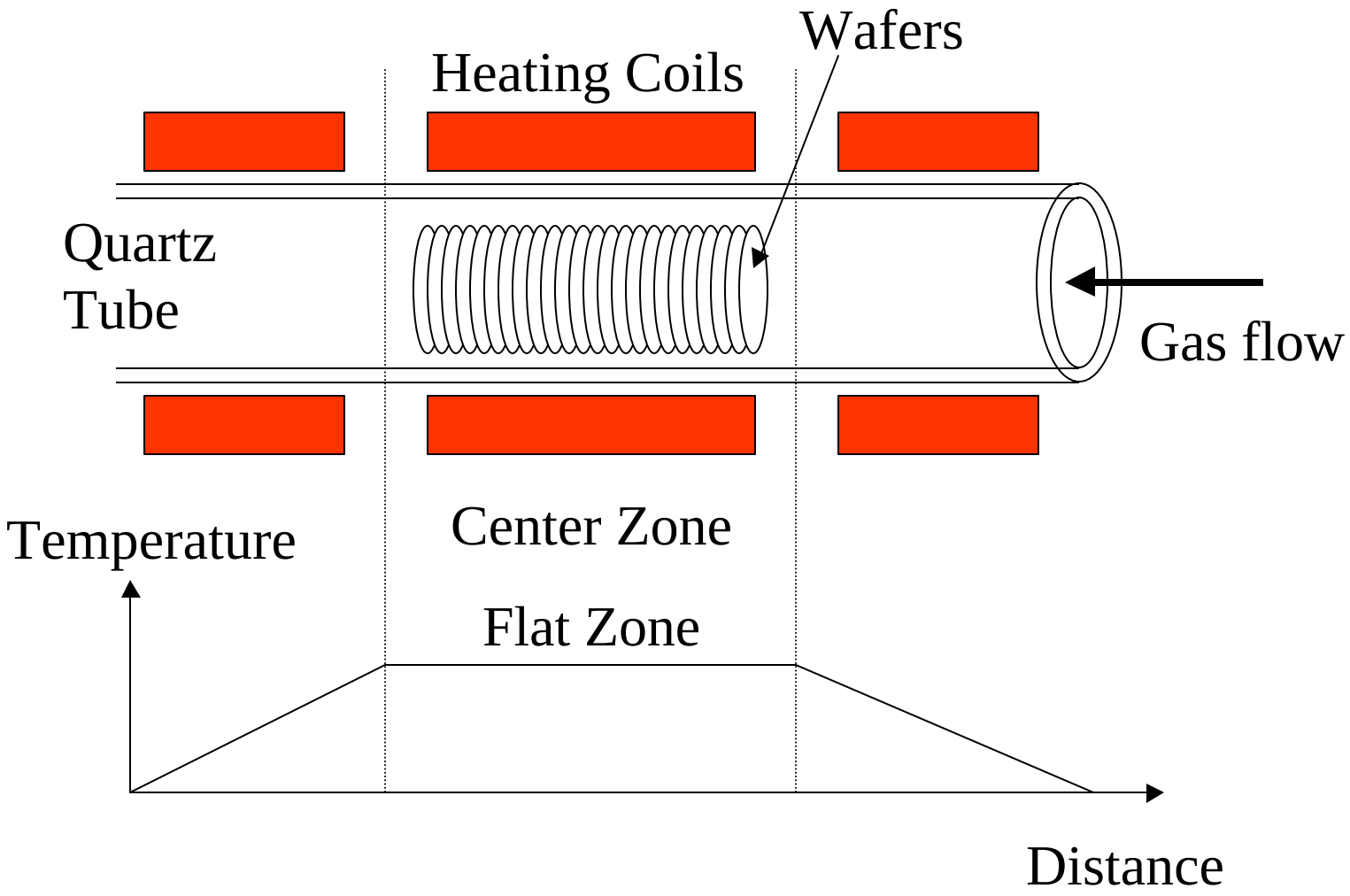
Temperature Control
Anti-Warp Methods

- Ramping
  - Load wafer slowly at a lower temperature (idle temperature, ~ 800 °C)
  - Ramp temperature to process point after a short stabilization period
- Slow loading
  - 1 inch/min
  - thermal capacity of 200 six-inch wafers can drop temperature as much as 50 °C

Horizontal Furnace

- Contain 3 or 4 tubes (reaction chambers)
- Separate temperature control system for each tube

Horizontal Furnace



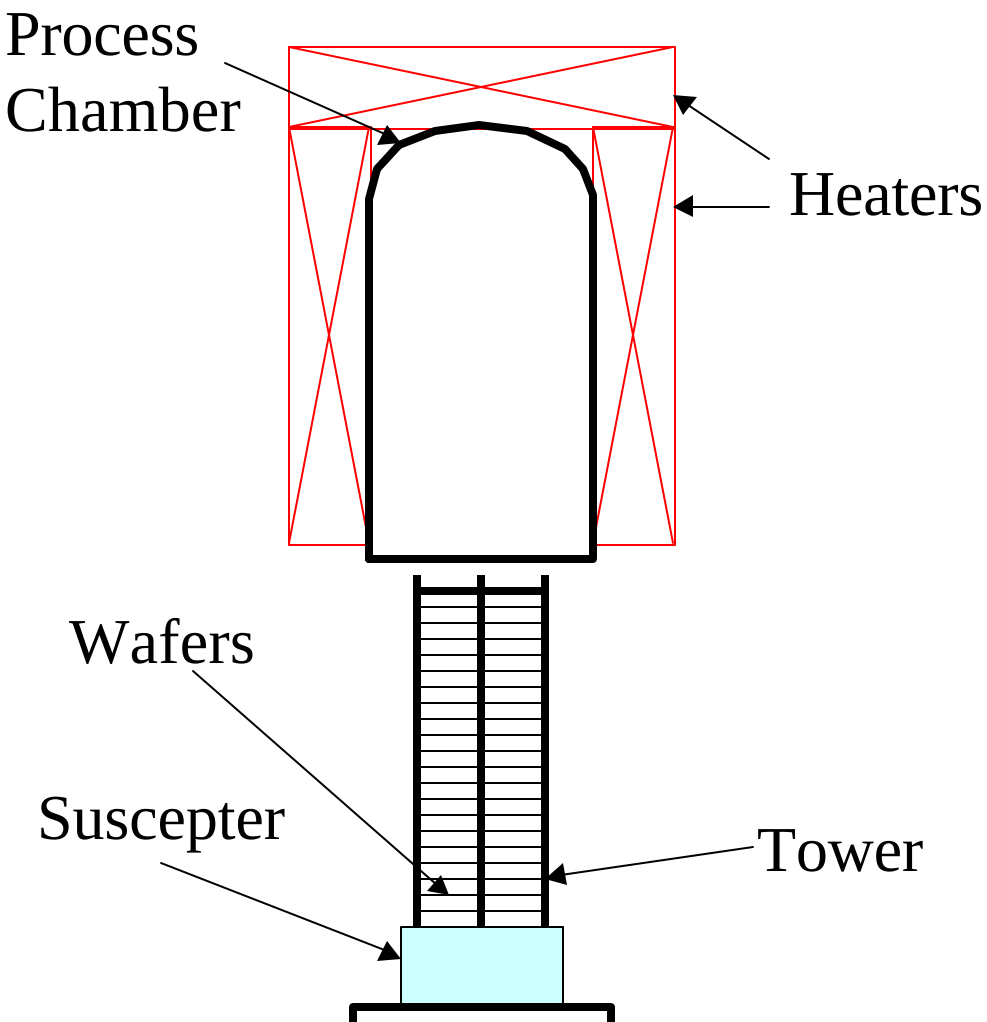
Furnace

- Wafer Clean Station
- Wafer Loading Station
  - Manual wafer loading
  - Automatic wafer loading
- Oxidation Process Automation

Vertical Furnaces

- Place the process tube in vertical direction
- Smaller footprint
- Better contamination control
- Better wafer handling
- Lower maintenance cost and higher uptime

Vertical Furnace, Loading and Unloading Position



Smaller Footprint

- Clean room footage becomes very expensive
- Small footprint reduces cost of ownership (COO)

Better Contamination Control

- Gas flow from top to bottom
- Better uniformity for Laminar gas flow control
- Particles has less chance to fall at the center of the wafers

Better Wafer Handling

- High torque on paddle of horizontal when it handle large amount of large diameter wafers
- Zero torque for wafer tower in vertical system

Summery of Hardware

- Furnaces are commonly used in thermal processes
- Furnaces usually consist with control system, gas delivery system, process tube or chamber, wafer loading system, and exhaust system.
- Vertical furnace is more widely used due to it smaller footprint, better contamination control, and lower maintenance.
- Precise temperature and its uniformity is vital for the success of the thermal processes.

Oxidation

Oxidation

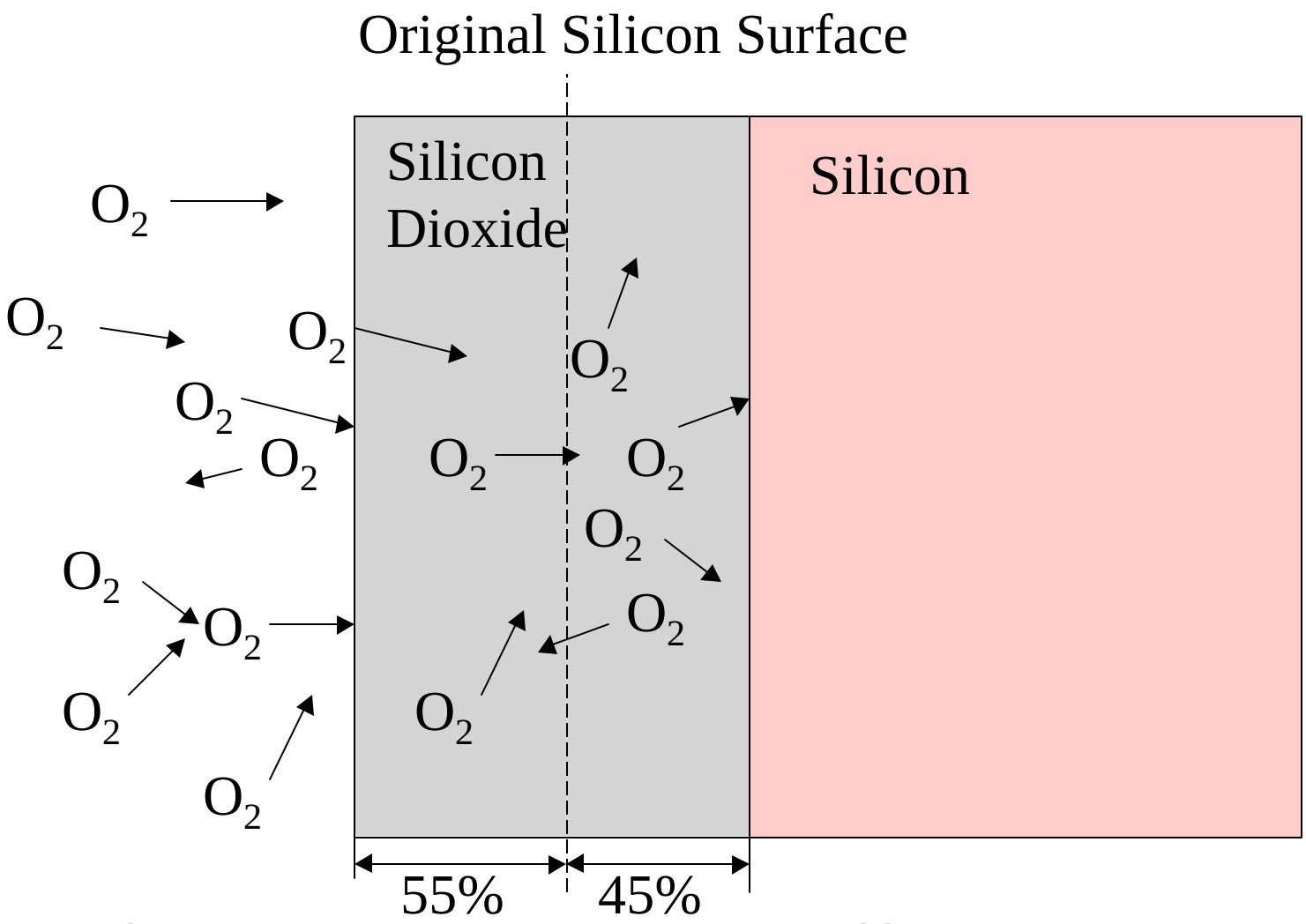
- Introduction
- Applications
- Mechanism
- Process
- System
- RTO

Introduction

- Silicon reacts with oxygen
- Stable oxide compound
- Widely used in IC manufacturing

$$Si + O_2 \rightarrow SiO_2$$

Oxidation



Some Facts About Silicon

Name	Silicon
Symbol	Si
Atomic number	14
Atomic weight	28.0855
Discoverer	Jöns Jacob Berzelius
Discovered at	Sweden
Discovery date	1824
Origin of name	From the Latin word "silicis" meaning "flint"
Bond length in single crystal Si	2.352 Å
Density of solid	2.33 g/cm^3
Molar volume	12.06 cm^3
Velocity of sound	2200 m/sec
Hardness	6.5
Electrical resistivity	100,000 μΩ·cm
Reflectivity	28%
Melting point	1414 °C
Boiling point	2900 °C
Thermal conductivity	150 $W\ m^{-1}\ K^{-1}$
Coefficient of linear thermal expansion	$2.6\times10^{-6}\ K^{-1}$
Etchants (wet)	HNO_4 and HF, KOH, etc.
Etchants (dry)	HBr, Cl_2, NF_3, etc.
CVD Precursor	SiH_4, SiH_2Cl_2, $SiHCl_3$, and $SiCl_4$

Fact About Oxygen

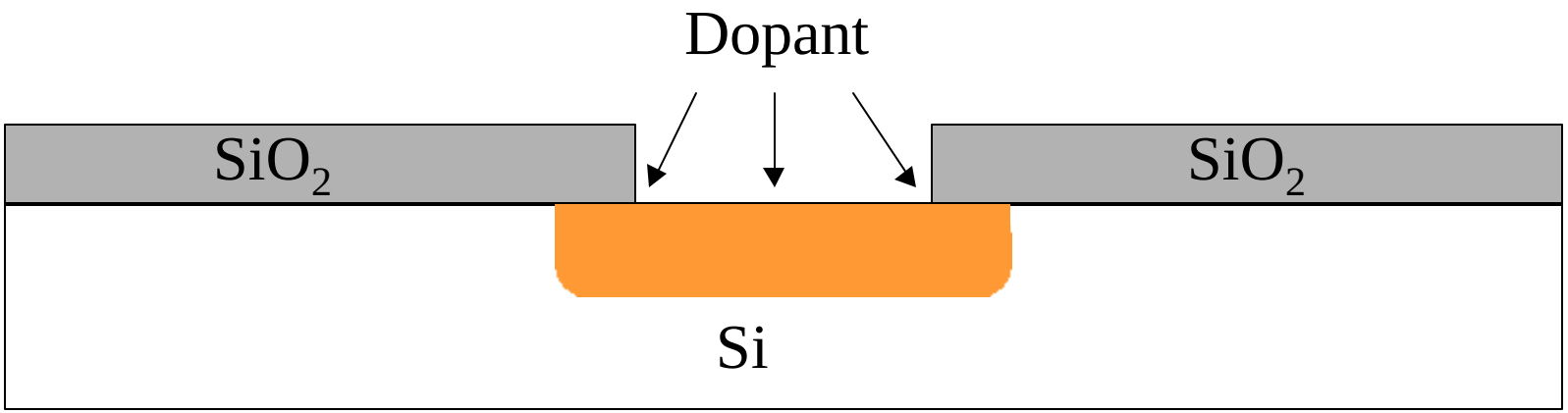
Name	Oxygen
Symbol	O
Atomic number	8
Atomic weight	15.9994
Discoverer	Joseph Priestley, Carl Scheele
Discovered at	England, Sweden
Discovery date	1774
Origin of name	From the Greek words "oxy genes" meaning "acid" (sharp) and "forming" (acid former)
Molar volume	17.36 cm^3
Velocity of sound	317.5 m/sec
Refractivity	1.000271
Melting point	54.8 K = -218.35 °C
Boiling point	90.2 K = -182.95 °C
Thermal conductivity	0.02658 W m^{-1} K^{-1}
Applications	Thermal oxidation, oxide CVD, reactive sputtering and photoresist stripping
Main sources	O_2, H_2O, N_2O, O_3

Application of Oxidation

- Diffusion Masking Layer
- Surface Passivation
  - Screen oxide, pad oxide, barrier oxide
- Isolation
  - Field oxide and LOCOS
- Gate oxide

Diffusion Barrier

- Much lower B and P diffusion rates in SiO_2 than that in Si
- SiO_2 can be used as diffusion mask



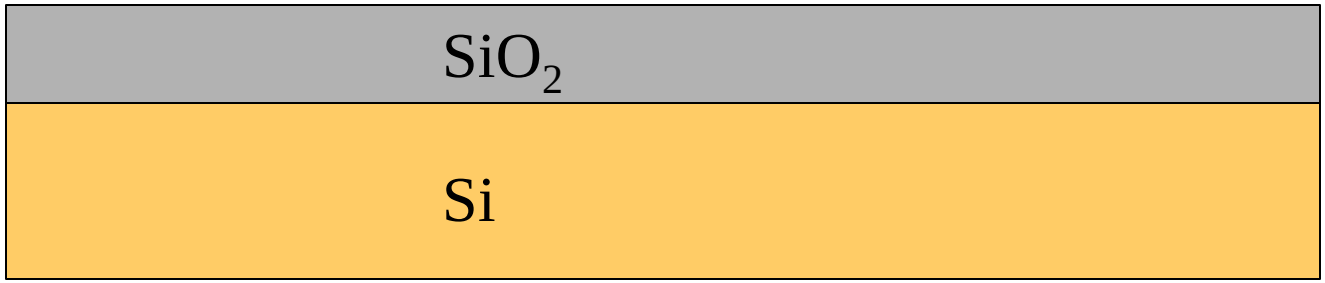
Application, Surface Passivation

Pad Oxide

Screen Oxide

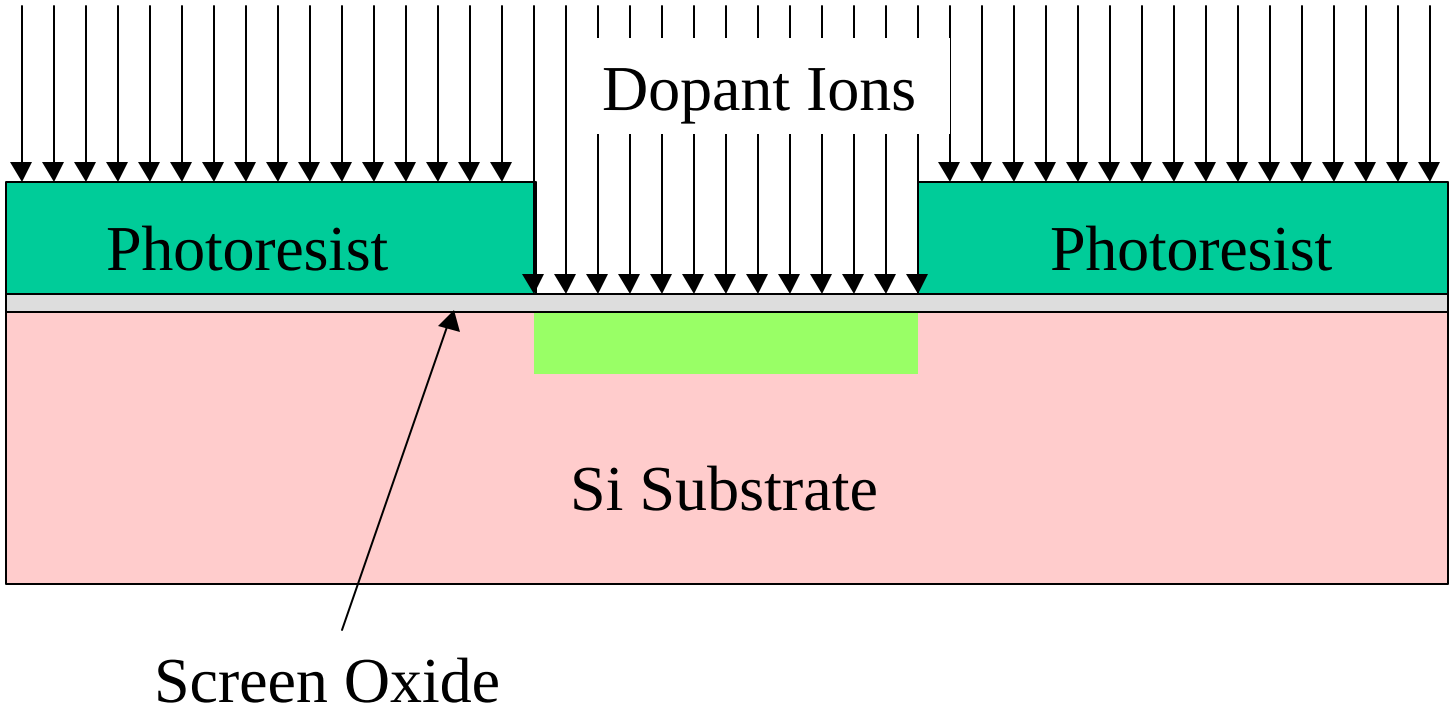
Sacrificial Oxide

Barrier Oxide

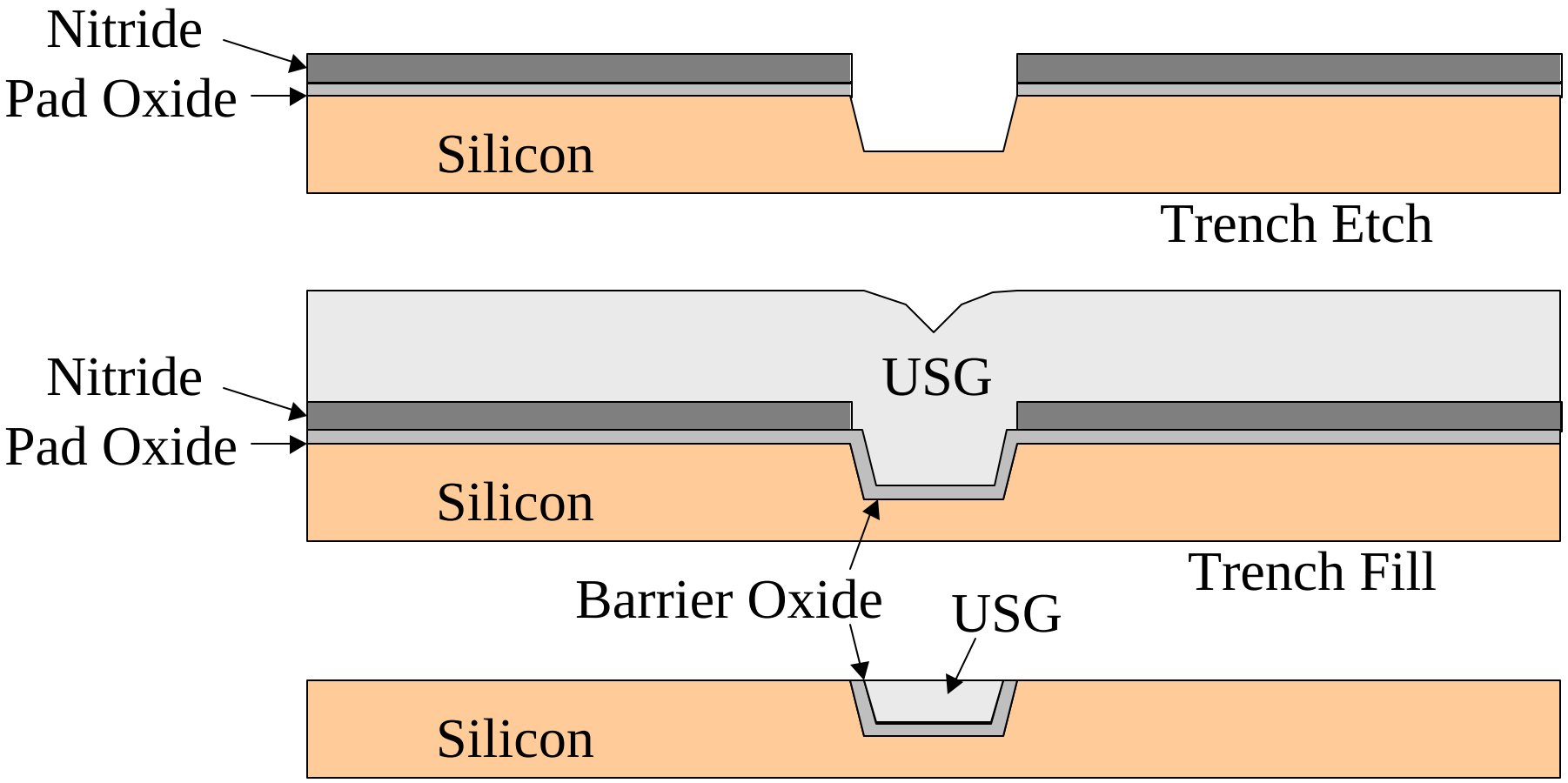


Normally thin oxide layer (~150Å) to protect silicon defects from contamination and over-stress.

Screen Oxide

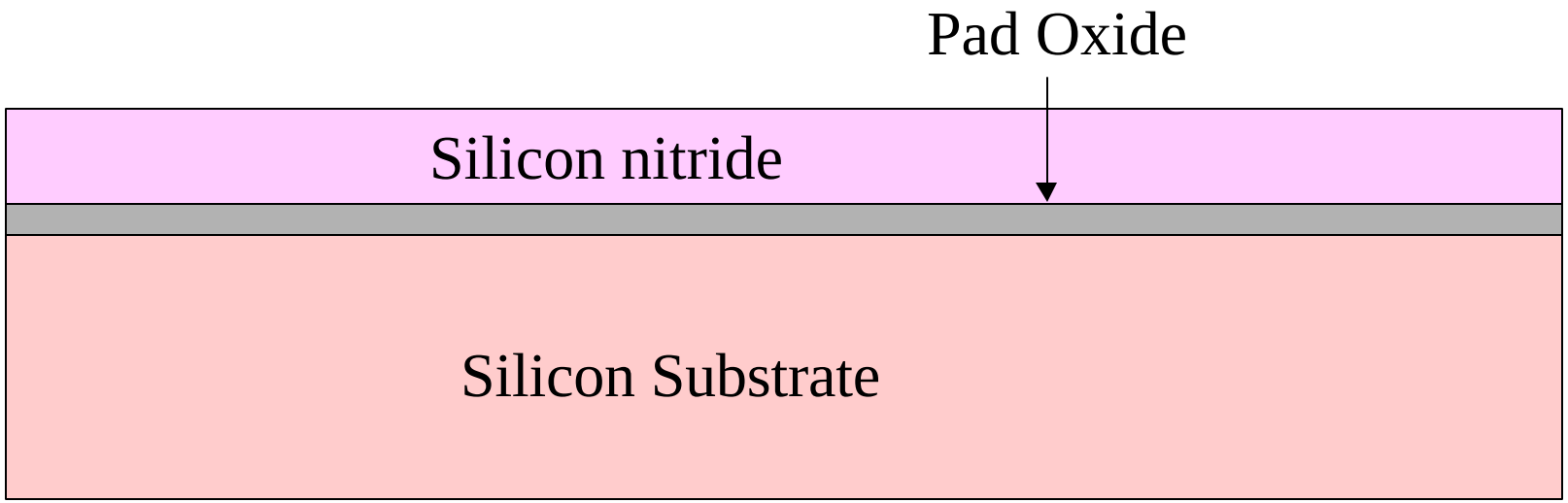


Pad and Barrier Oxides in STI Process



Application, Pad Oxide

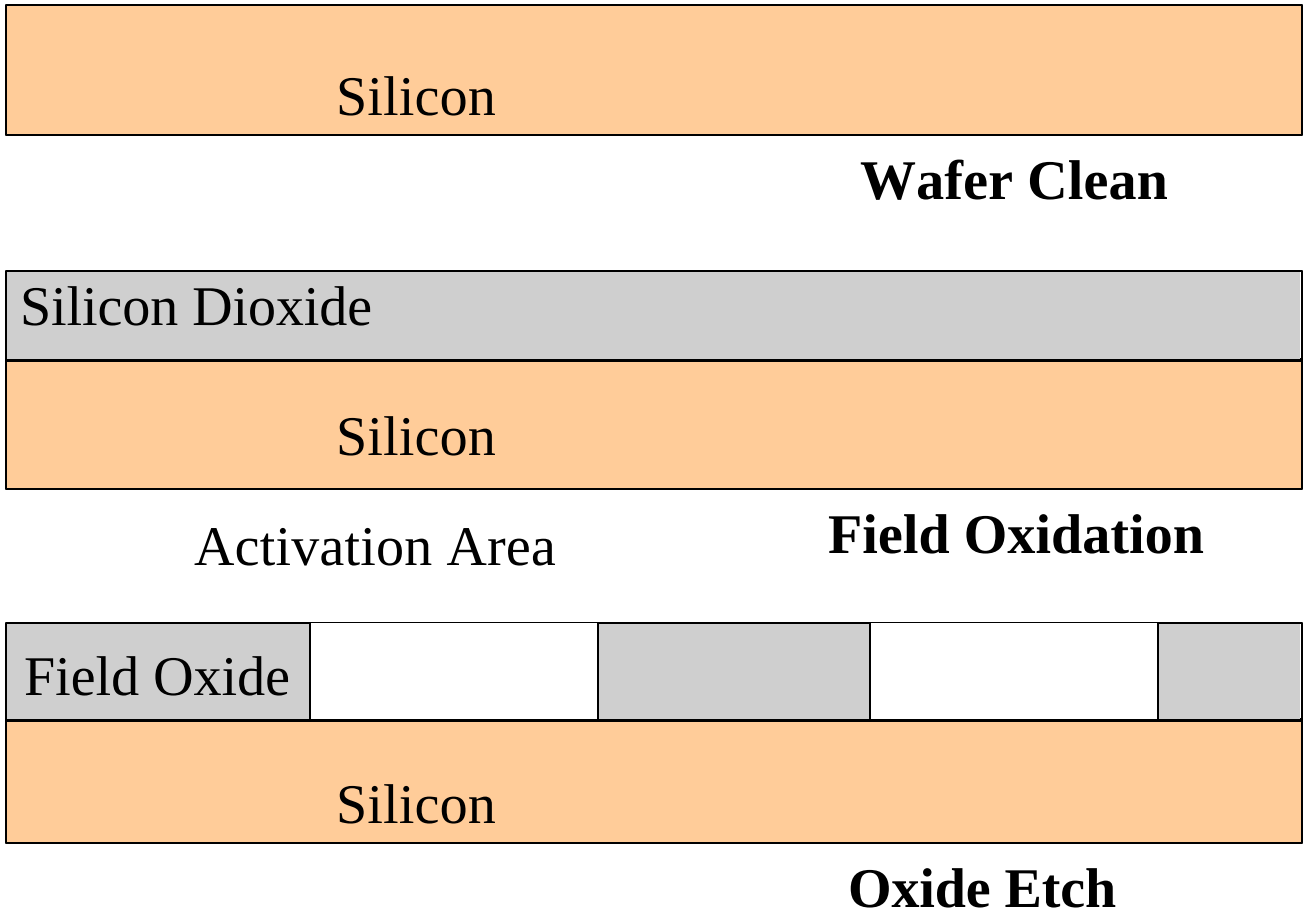
- Relieve strong tensile stress of the nitride
- Prevent stress induced silicon defects



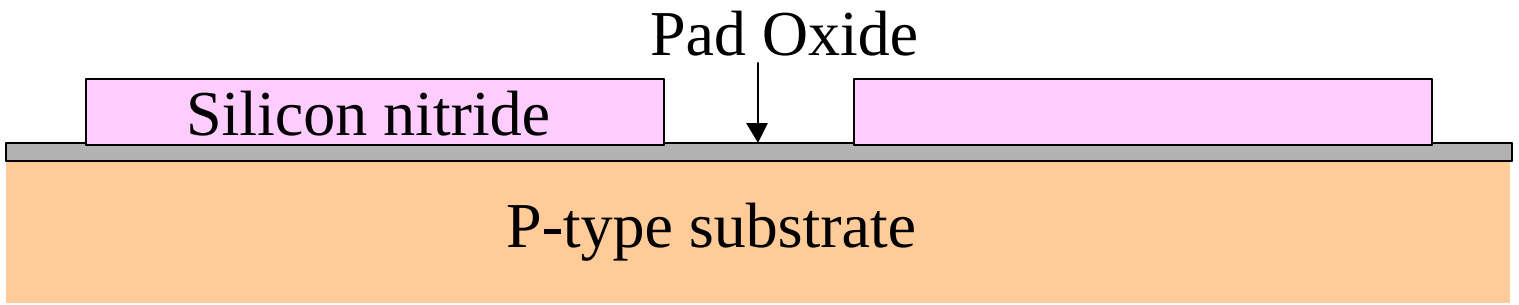
Application, Device Isolation

- Electronic isolation of neighboring devices
- Blanket field oxide
- Local oxidation of silicon (LOCOS)
- Thick oxide, usually 3,000 to 10,000 Å

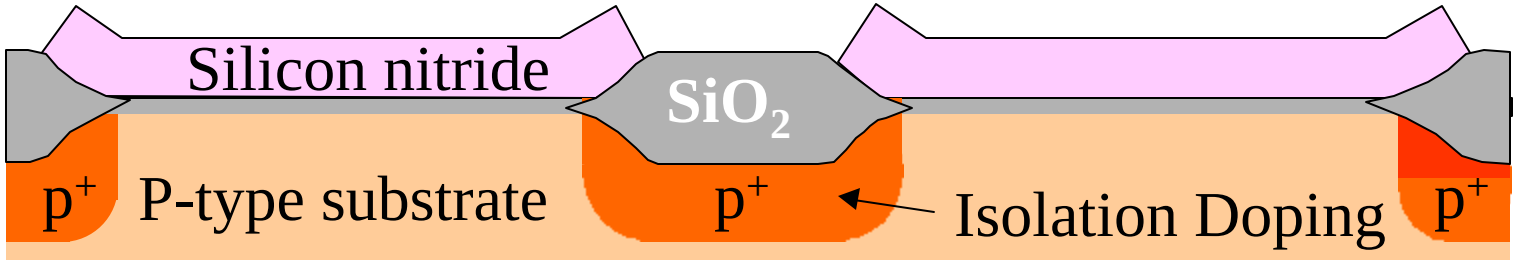
Blanket Field Oxide Isolation



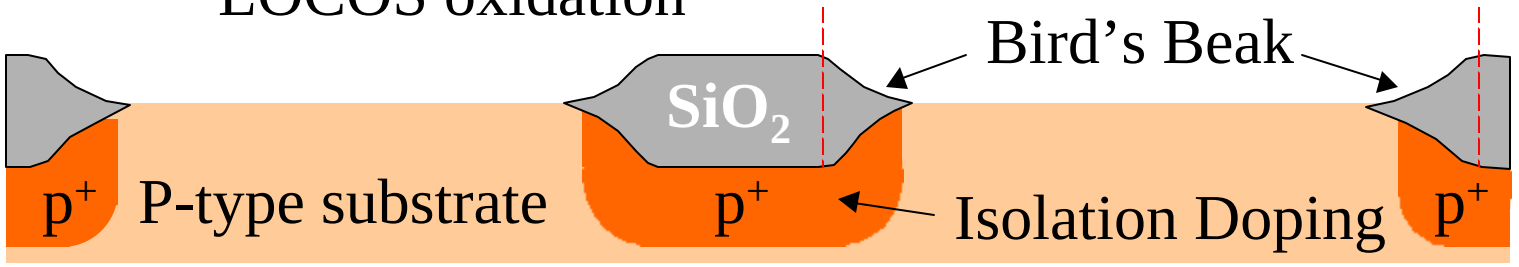
LOCOS Process



Pad oxidation, nitride deposition and patterning



LOCOS oxidation



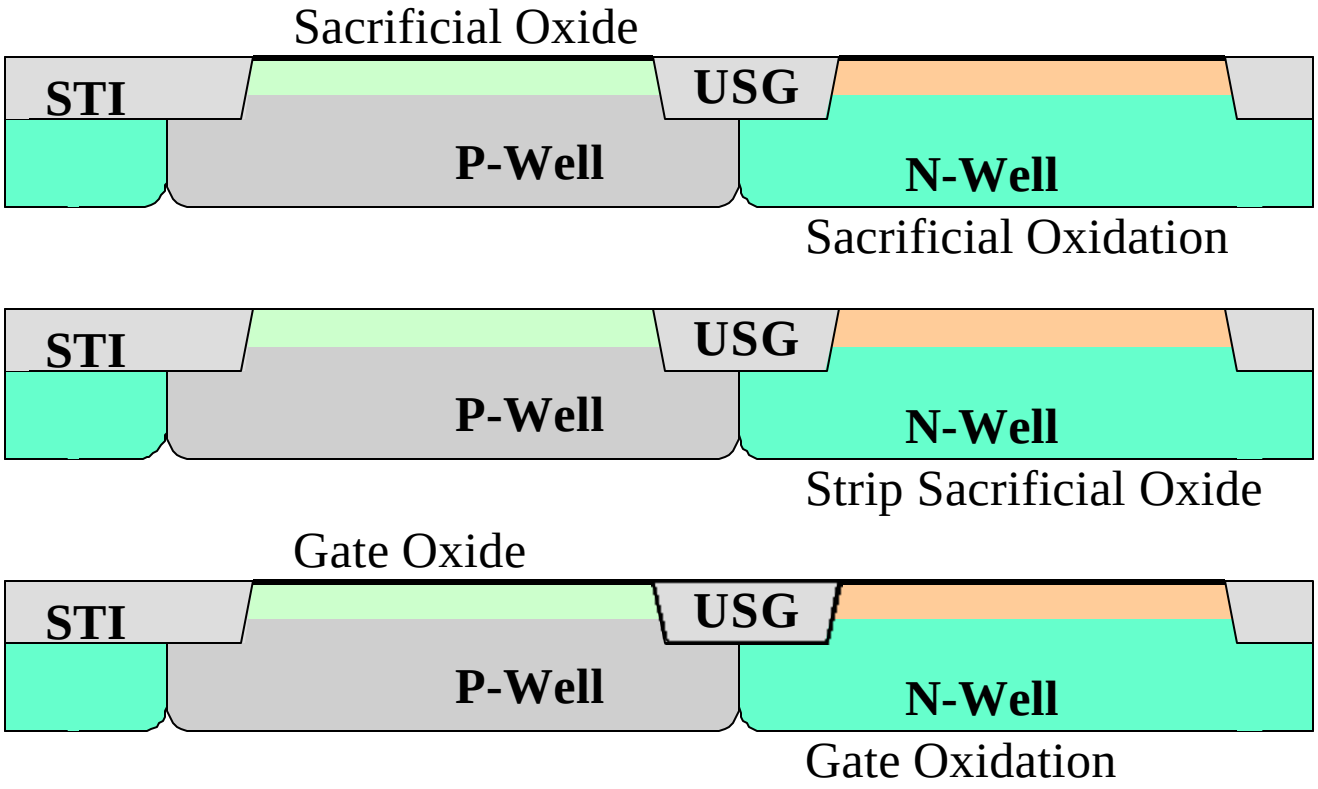
Nitride and pad oxide strip

LOCOS

- Compare with blanket field oxide
  - Better isolation
  - Lower step height
  - Less steep sidewall
- Disadvantage
  - rough surface topography
  - Bird’s beak
- Replacing by shallow trench isolation (STI)

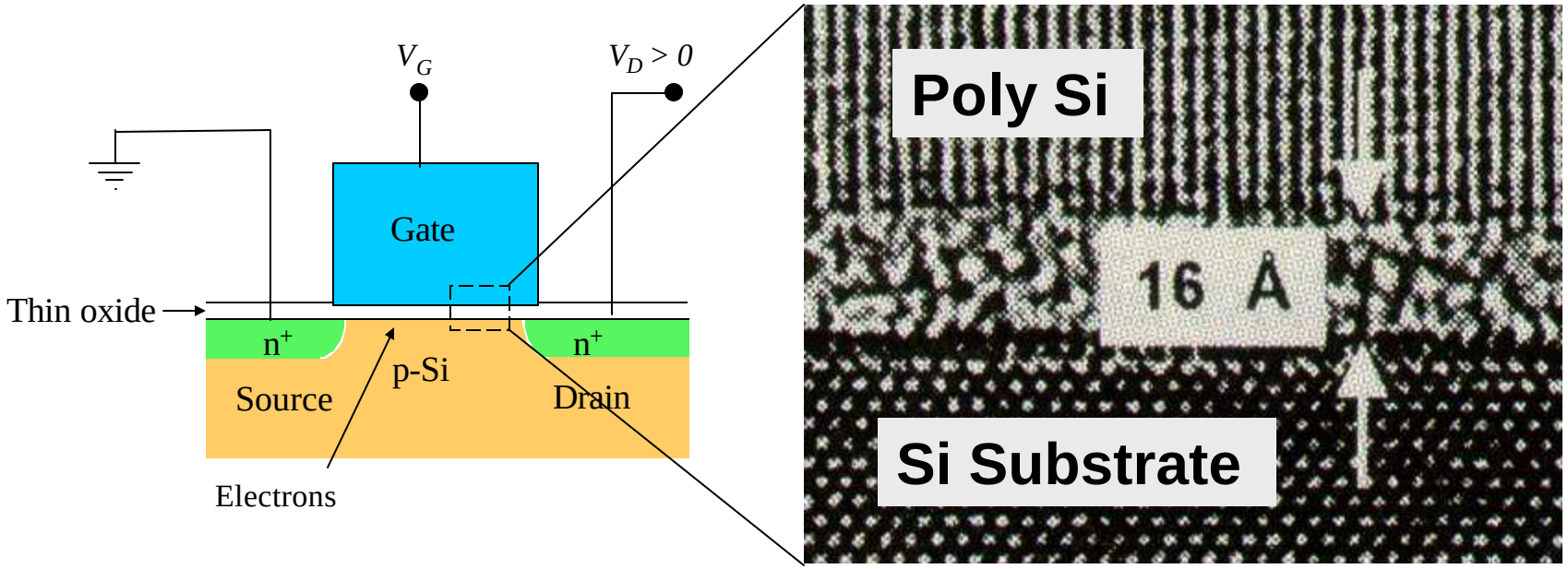
Application, Sacrificial Oxide

- Defects removal from silicon surface



Application, Device Dielectric

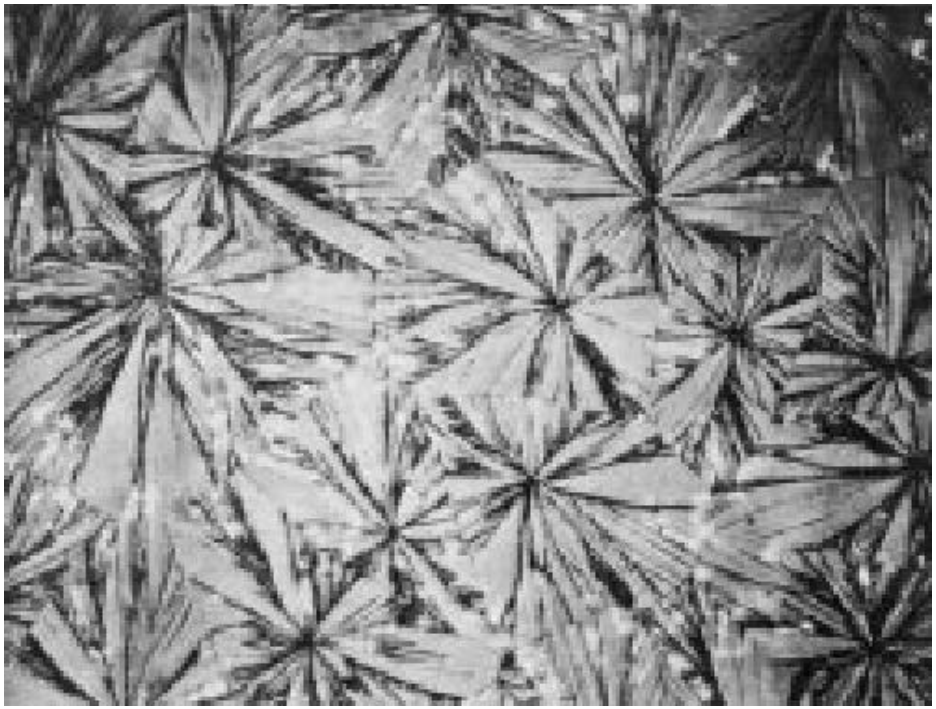
- Gate oxide: thinnest and most critical layer
- Capacitor dielectric



Oxide and Applications

Name of the Oxide	Thickness	Application	Time in application
Native	15 - 20 Å	undesirable	-
Screen	~ 200 Å	Implantation	Mid-70s to present
Masking	~ 5000 Å	Diffusion	1960s to mid-1970s
Field and LOCOS	3000 - 5000 Å	Isolation	1960s to 1990s
Pad	100 - 200 Å	Nitride stress buffer	1960s to present
Sacrificial	<1000 Å	Defect removal	1970s to present
Gate	30 - 120 Å	Gate dielectric	1960s to present
Barrier	100 - 200 Å	STI	1980s to present

Silicon Dioxide Grown on Improperly Cleaned Silicon Surface



Pre-oxidation Wafer Clean

- Particulates
- Organic residues
- Inorganic residues
- Native oxide layers

RCA Clean

- Developed by Kern and Puotinen in 1960 at RCA
- Most commonly used clean processes in IC fabs
- SC-1-- NH_4OH:H_2O_2:H_2O with 1:1:5 to 1:2:7 ratio at 70 to 80 °C to remove organic contaminants.
- SC-2-- HCl:H_2O_2:$H_2O$with 1:1:6 to 1:2:8 ratio at 70 to 80 °C to remove inorganic contaminates.
- DI water rinse
- HF dip or HF vapor etch to remove native oxide.

Pre-oxidation Wafer Clean Particulate Removal

- High purity deionized (DI) water or H_2SO_4:H_2O_2 followed by DI H_2O rinse.
- High pressure scrub or immersion in heated dunk tank followed by rinse, spin dry and/or dry bake (100 to 125 °C).

Pre-oxidation Wafer Clean Organic Removal

- Strong oxidants remove organic residues.
- H_2SO_4:H_2O_2 or NH_3OH:H_2O_2 followed by DI H_2O rinse.
- High pressure scrub or immersion in heated dunk tank followed by rinse, spin dry and/or dry bake (100 to 125 °C).

Pre-oxidation Wafer Clean Inorganic Removal

- $HCl:H_2O$.
- Immersion in dunk tank followed by rinse, spin dry and/or dry bake (100 to 125 °C).

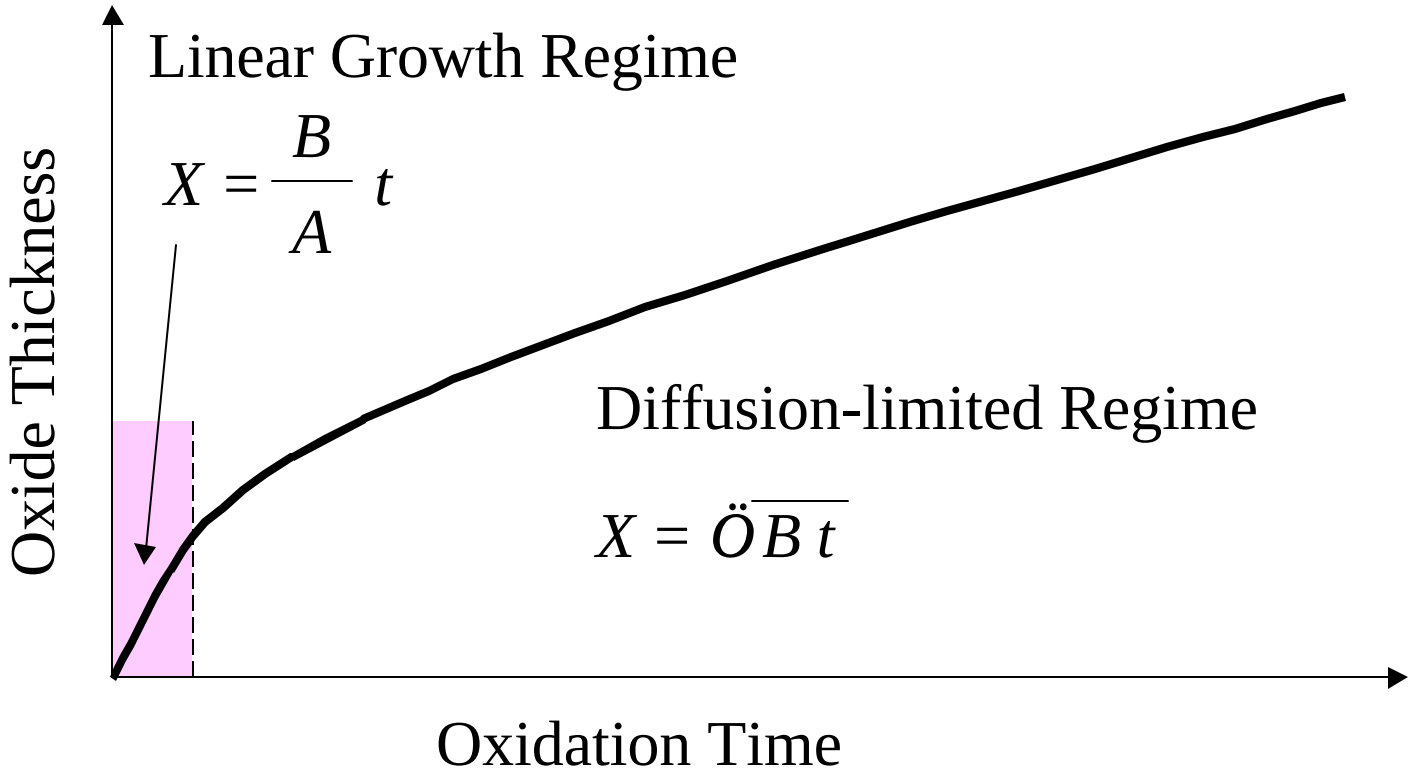
Pre-oxidation Wafer Clean
Native Oxide Removal

- HF:H_2O.
- Immersion in dunk tank or single wafer vapor etcher followed by rinse, spin dry and/or dry bake (100 to 125 °C).

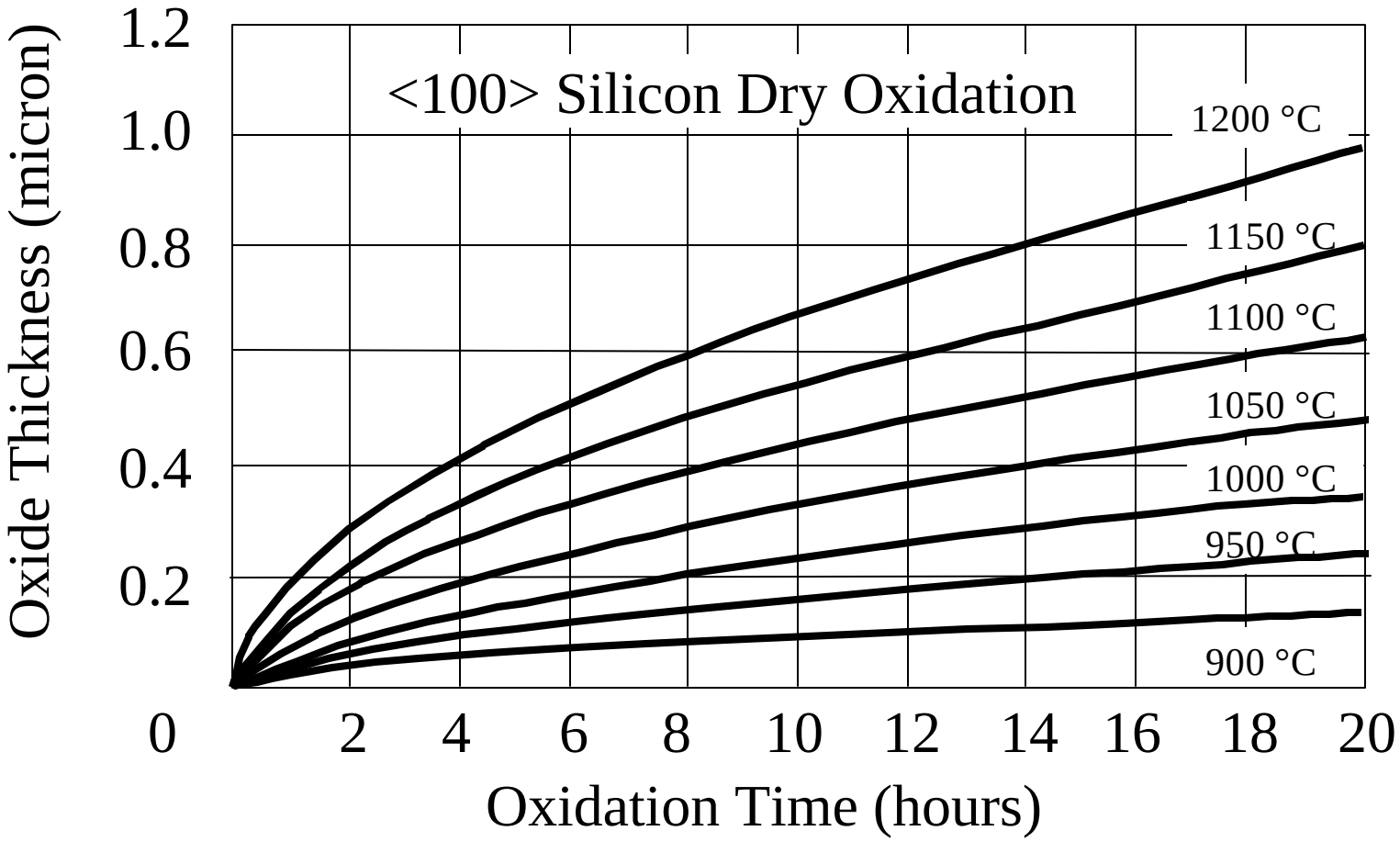
Oxidation Mechanism

- $Si + O_2 \longrightarrow SiO_2$
- Oxygen comes from gas
- Silicon comes from substrate
- Oxygen diffuse cross existing silicon dioxide layer and react with silicon
- The thicker of the film, the lower of the growth rate

Oxide Growth Rate Regime



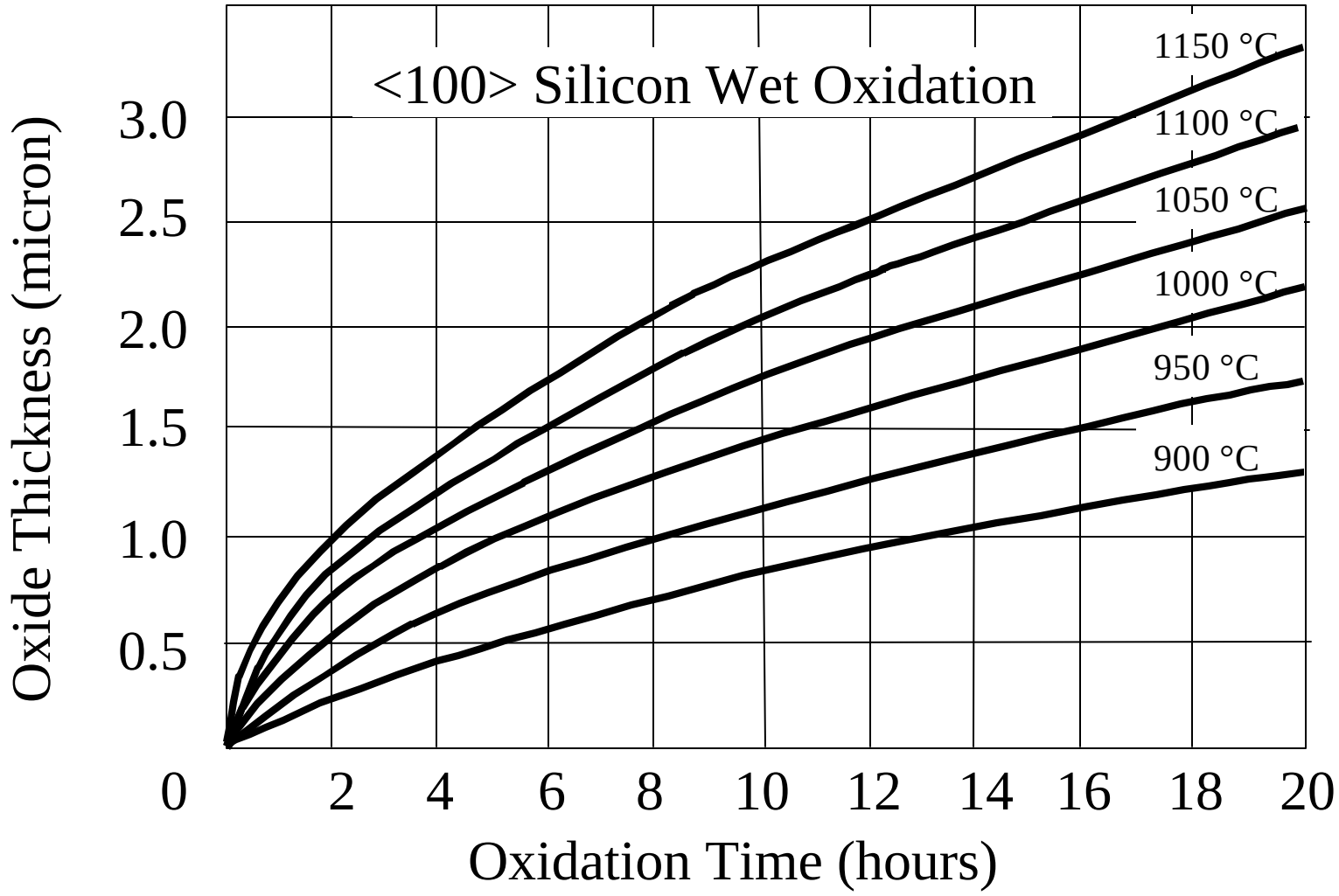
<100> Silicon Dry Oxidation



Wet (Steam) Oxidation

- $Si + 2H_2O \longrightarrow SiO_2 + 2H_2$
- At high temperature H_2O is dissociated to H and H-O
- H-O diffuses faster in SiO_2 than O_2
- Wet oxidation has higher growth rate than dry oxidation.

<100> Silicon Wet Oxidation Rate



Oxidation Rate

- Temperature
- Chemistry, wet or dry oxidation
- Thickness
- Pressure
- Wafer orientation (<100> vs. <111>)
- Silicon dopant

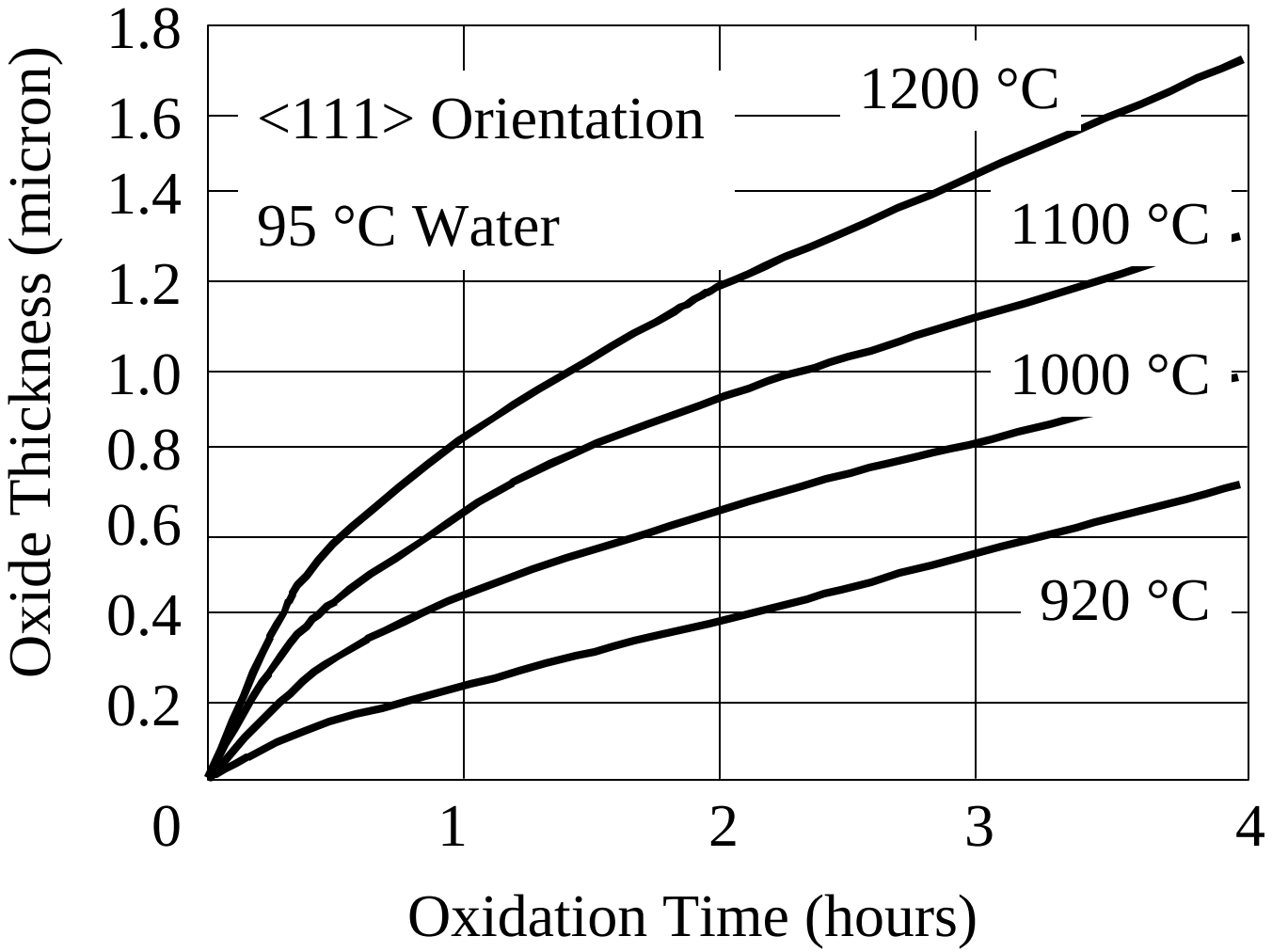
Oxidation Rate Temperature

- Oxidation rate is very sensitive (exponentially related) to temperature
- Higher temperature will have much higher oxidation rate.
- The higher of temperature is, the higher of the chemical reaction rate between oxygen and silicon is and the higher diffusion rate of oxygen in silicon dioxide is.

Oxidation Rate
Wafer Orientation

- <111> surface has higher oxidation rate than <100> surface.
- More silicon atoms on the surface.

Wet Oxidation Rate



Oxidation Rate
Dopant Concentration

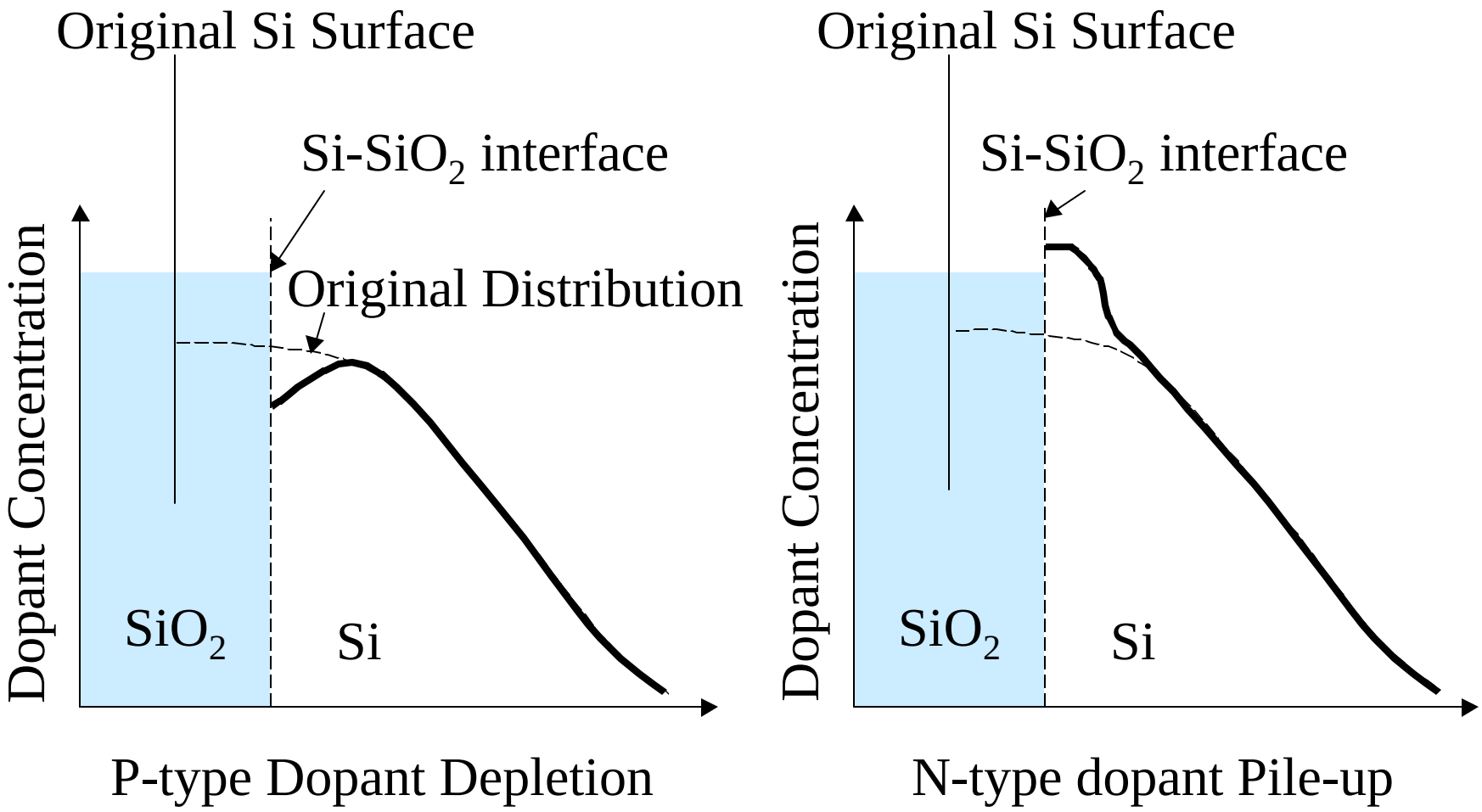
- Dopant elements and concentration
- Highly phosphorus doped silicon has higher growth rate, less dense film and etch faster.
- Generally highly doped region has higher grow rate than lightly doped region.
- More pronounced in the linear stage (thin oxides) of oxidation.

Oxidation: Dopants
Pile-up and Depletion Effects

- N-type dopants (P, As, Sb) have higher solubility in Si than in SiO_2, when SiO_2 grow they move into silicon, it is call pile-up or snowplow effect.

- Boron tends to go to SiO_2, it is called depletion effect.

Depletion and Pile-up Effects



Oxidation Rate
Doped oxidation (HCl)

- HCl is used to reduce mobile ion contamination.
- Widely used for gate oxidation process.
- Growth rate can increase from 1 to 5 percent.

Oxidation Rate
Differential Oxidation

- The thicker of the oxide film is, the slower of the oxidation rate is.
- Oxygen need more time to diffuse cross the existing oxide layer to react with substrate silicon.

Pre-oxidation Clean

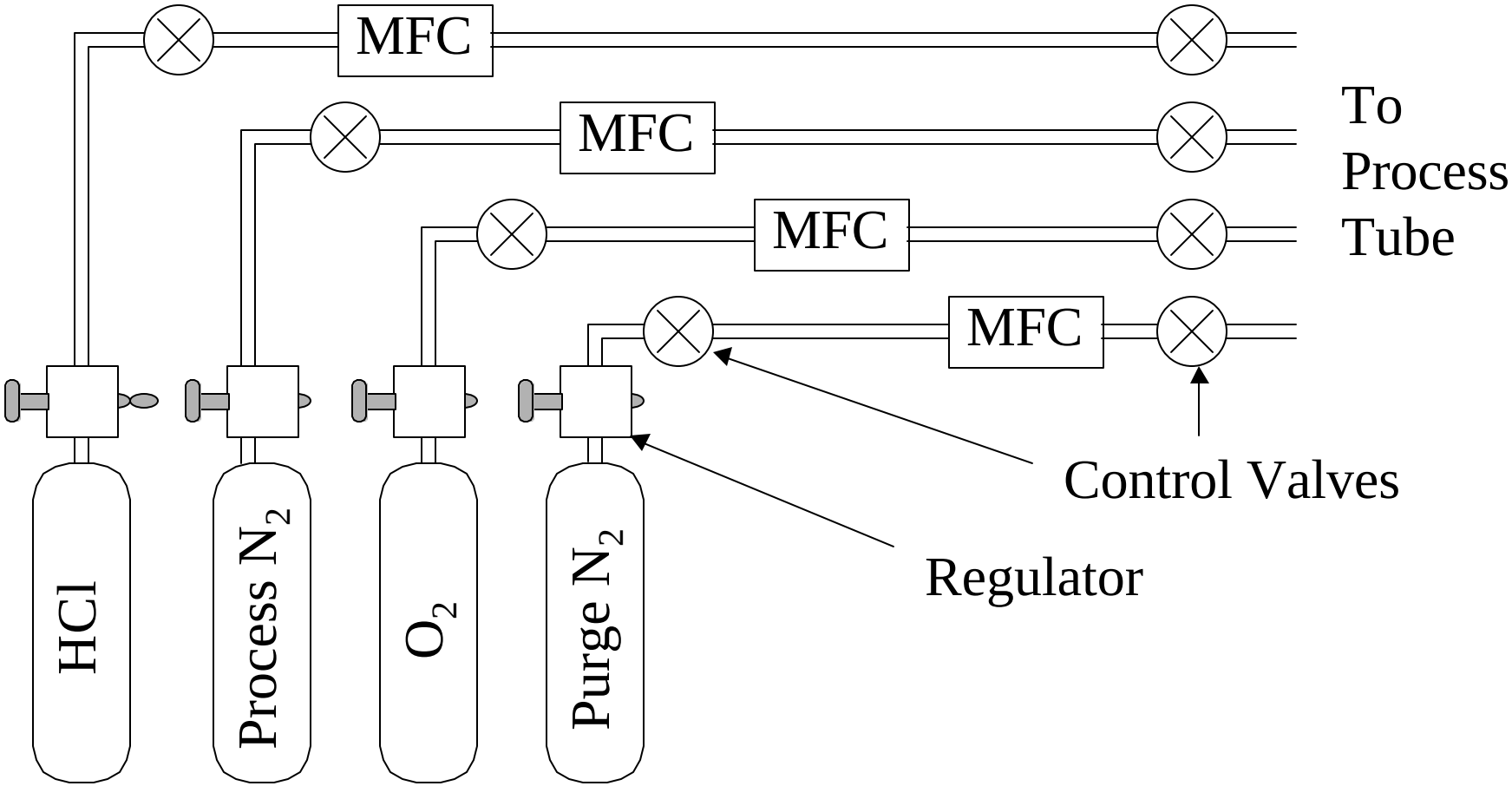
- Thermally grown SiO_2 is amorphous.
- Tends to cross-link to form a crystal
- In nature, SiO_2 exists as quartz and sand
- Defects and particles can be the nucleation sites
- Crystallized SiO_2 with poor barrier capability.

- Need clean silicon surface before oxidation.

Oxidation Process

- Dry Oxidation, thin oxide
  - Gate oxide
  - Pad oxide, screen oxide, sacrificial oxide, etc.
- Wet Oxidation, thick oxide
  - Field oxide
  - Diffusion masking oxide

Dry Oxidation System



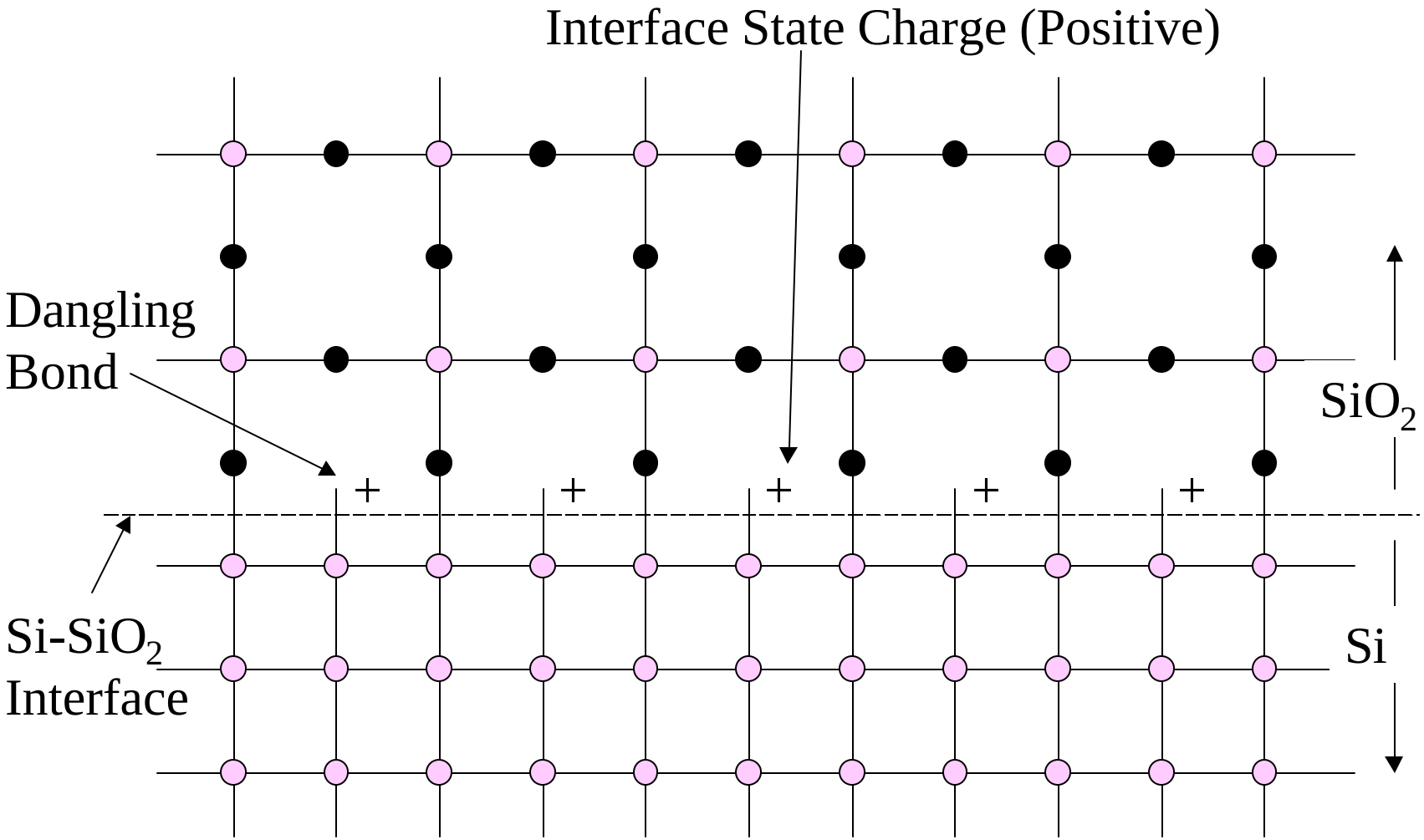
Dry Oxidation

- Dry O_2 as the main process gas
- HCl is used to remove mobile ions for gate oxidation
- High purity N_2 as process purge gas
- Lower grade N_2 as idle purge gas

Gate Oxidation Steps

- Idle with purge N_2 flow
- Idle with process N_2 flow
- Wafer boats push-in with process N_2 flow
- Temperature ramp-up with process N_2 flow
- Temperature stabilization with process N_2 flow
- Oxidation with O_2, HCl, stop N_2 flow

Dangling Bonds and Interface Charge



Gate Oxidation Steps, Continue

- Oxide annealing, stop O_2, start process flow N_2
- Temperature cool-down with process N_2 flow
- Wafer boats pull-out with process N_2 flow
- Idle with process N_2 flow
- Next boats and repeat process
- Idle with purge N_2 flow

Wet Oxidation Process

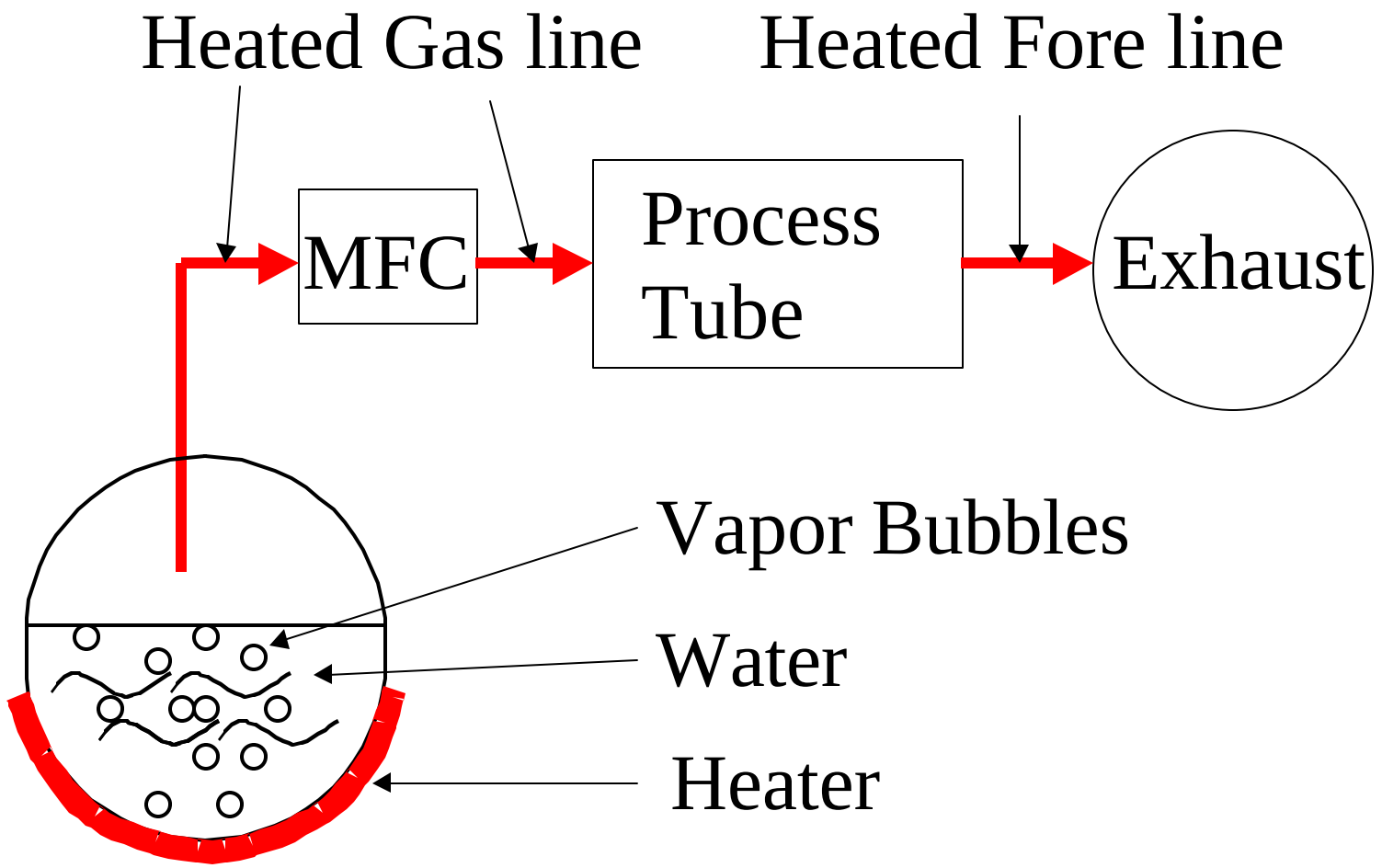
- Faster, higher throughput
- Thick oxide, such as LOCOS
- Dry oxide has better quality

Process	Temperature	Film Thickness	Oxidation Time
Dry oxidation	1000 °C	1000 Å	~ 2 hours
Wet oxidation	1000 °C	1000 Å	~ 12 minutes

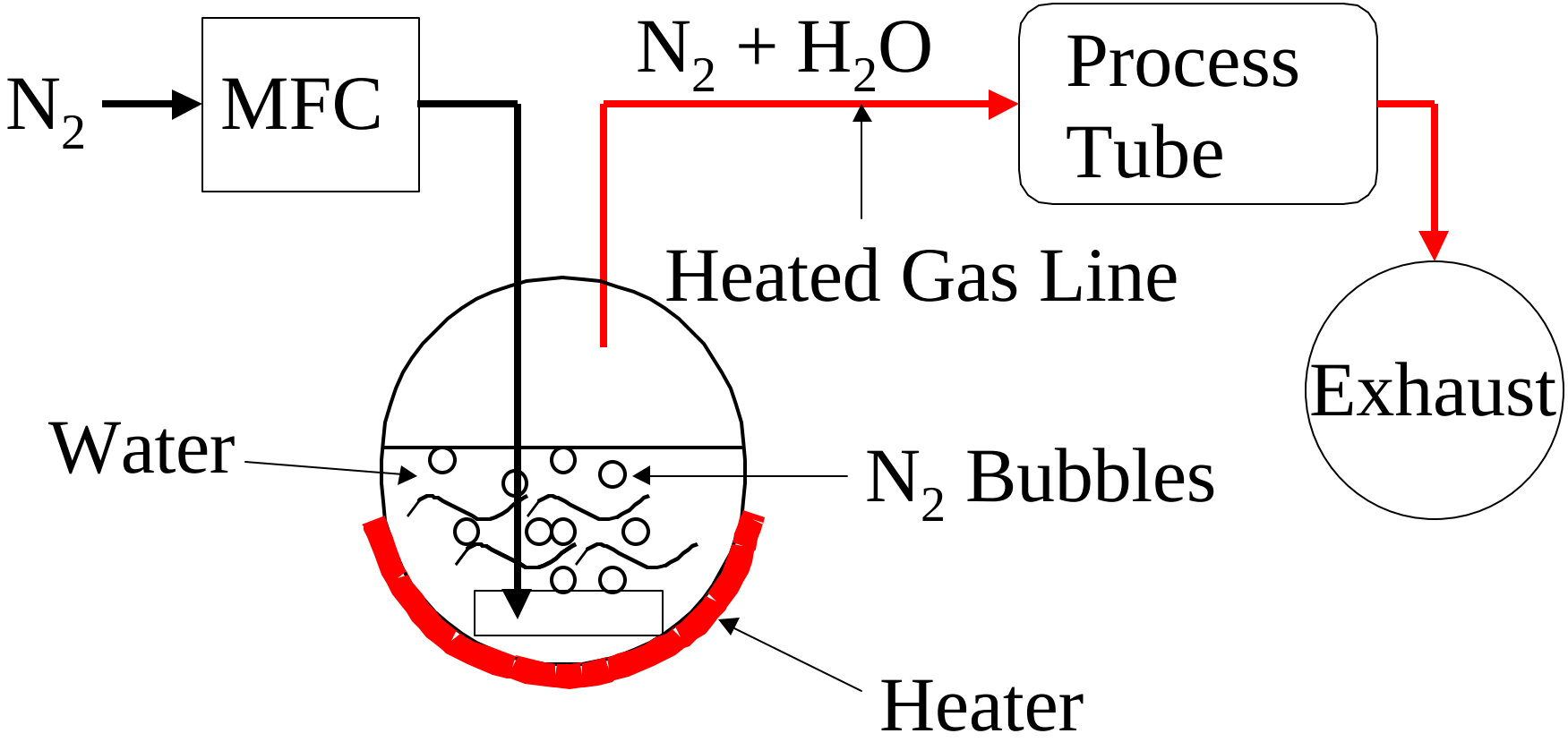
Water Vapor Sources

- Boiler
- Bubbler
- Flush
- Pyrogenic

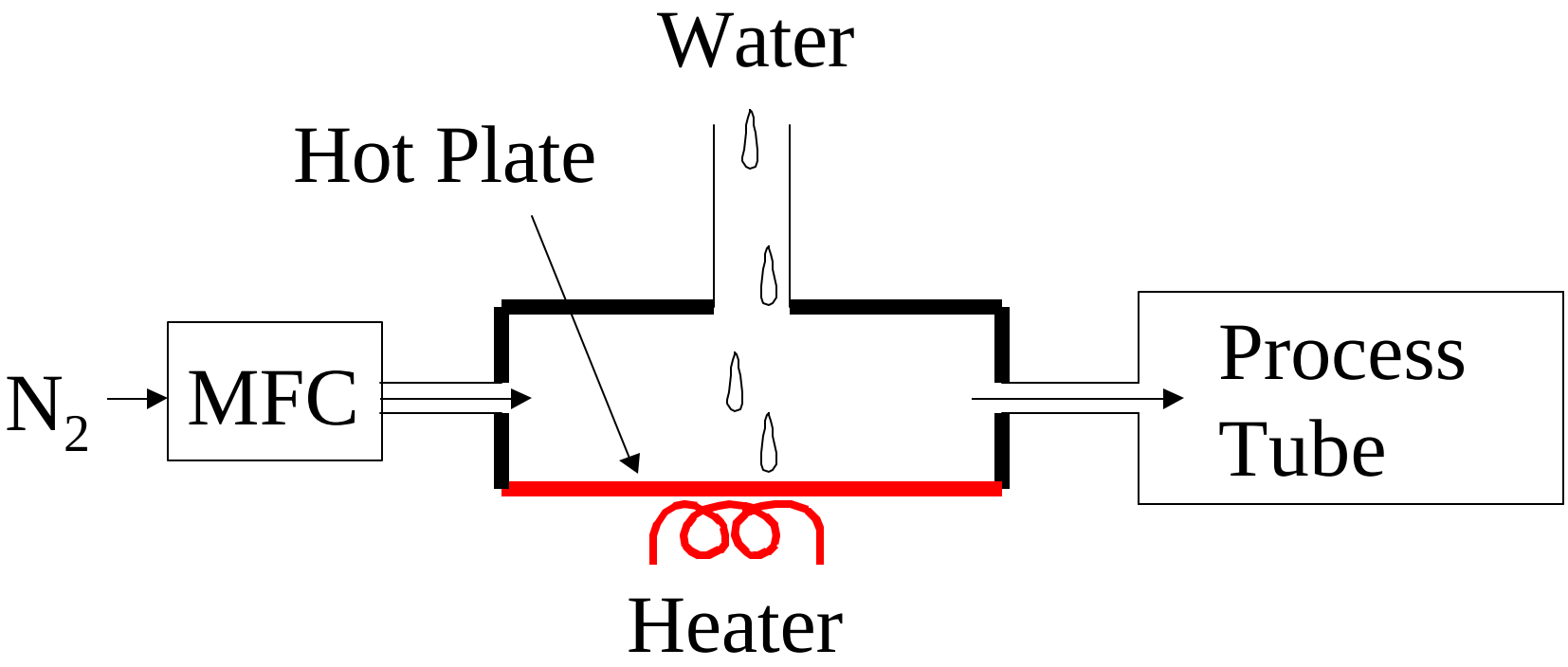
Boiler System



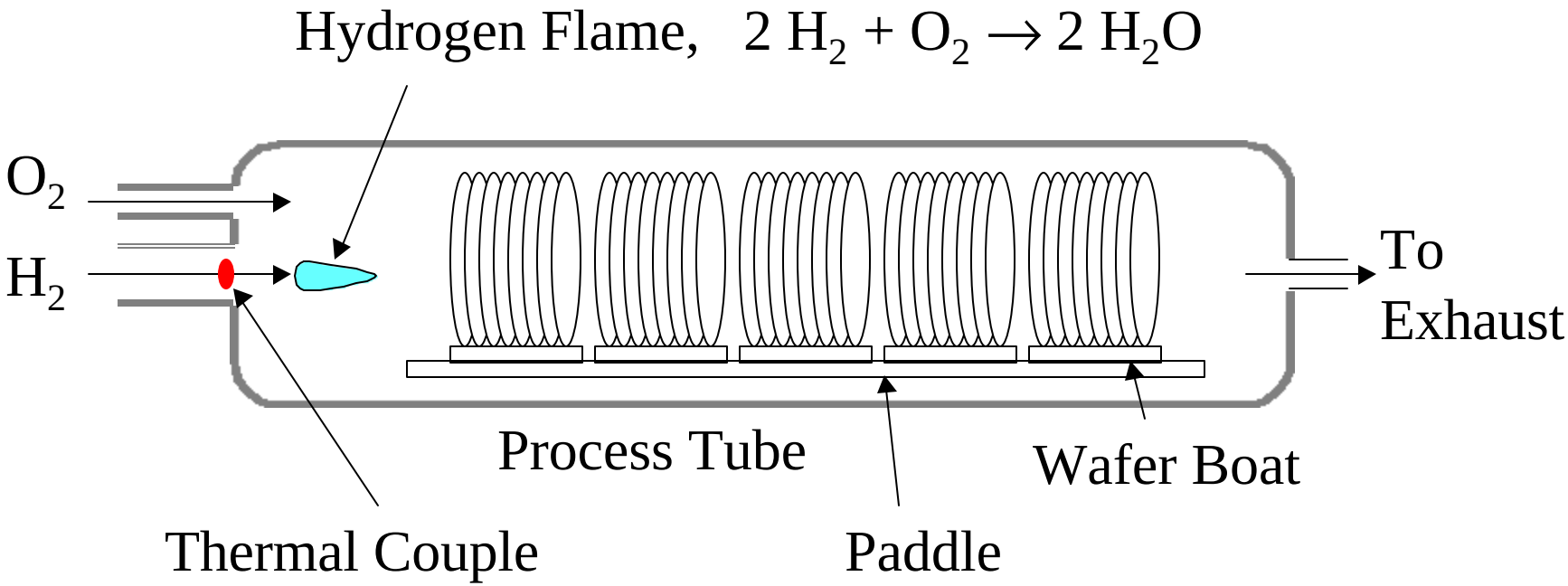
Bubbler System



Flush System



Pyrogenic Steam System

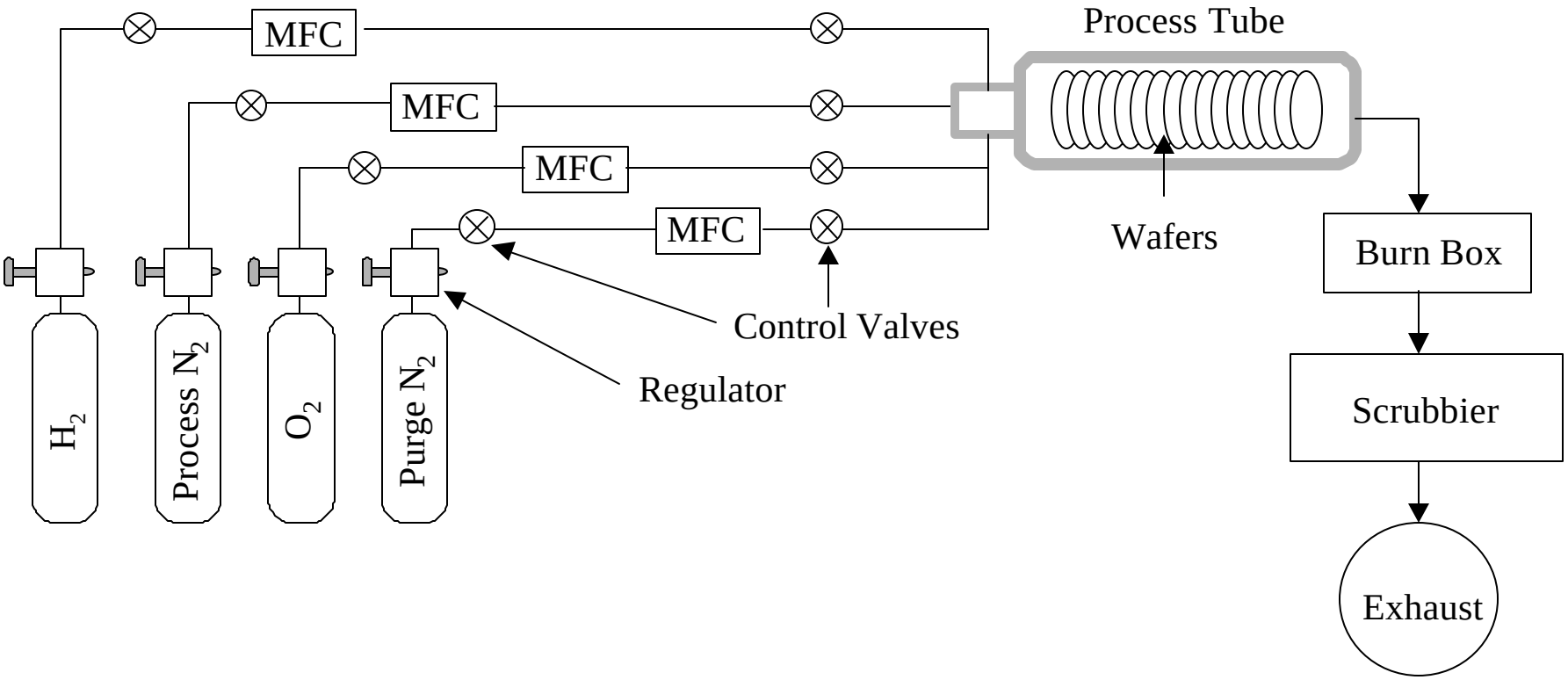


Pyrogenic System

- Advantage
  - All gas system
  - Precisely control of flow rate
- Disadvantage
  - Introducing of flammable, explosive hydrogen

- Typical H_2:O_2 ratio is between 1.8:1 to 1.9:1.

Pyrogenic Wet Oxidation System



Wet Oxidation Process Steps

- Idle with purge N_2 flow
- Idle with process N_2 flow
- Ramp O_2 with process N_2 flow
- Wafer boat push-in with process N_2 and O_2 flows
- Temperature ramp-up with process N_2 and O_2 flows
- Temperature stabilization with process N_2 and O_2 flows
- Ramp O_2, turn-off N_2 flow
- Stabilize the O_2 flow

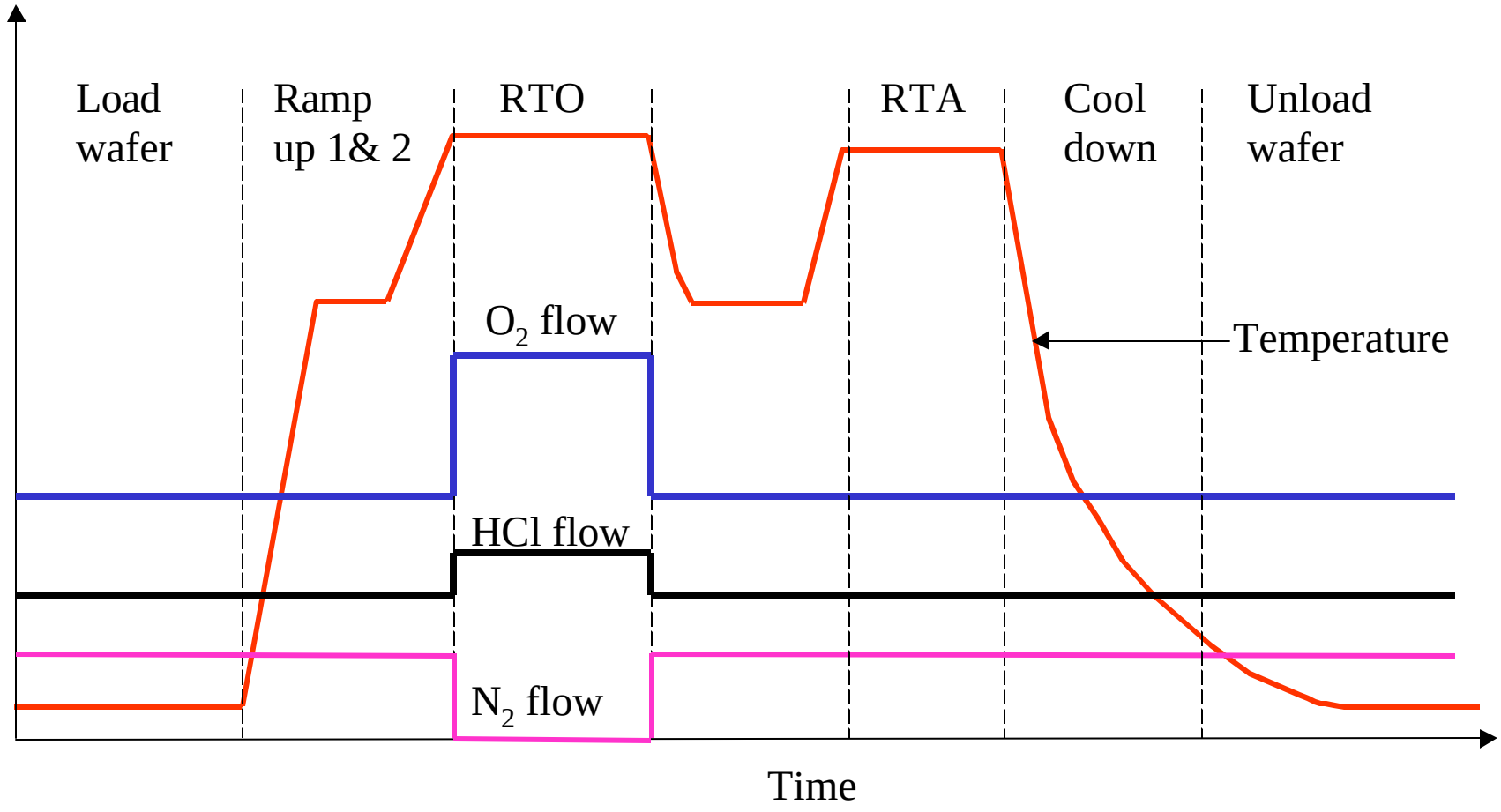
Wet Oxidation Process Steps

- Turn-on H_2 flow, ignition and H_2 flow stabilization
- Steam oxidation with O_2 and H_2 flow
- Hydrogen termination, turn-off H_2 while keeping O_2 flow
- Oxygen termination, turn-off O_2 start process N_2 flow
- Temperature ramp-down with process N_2 flow
- Wafer boat pull-out with process N_2 flow
- Idle with process N_2 flow
- Next boats and repeat process
- Idle with purge N_2 flow

Rapid Thermal Oxidation

- For gate oxidation of deep sub-micron device
- Very thin oxide film, < 30 Å
- Need very good control of temperature uniformity, WIW and WTW.
- RTO will be used to achieve the device requirement.

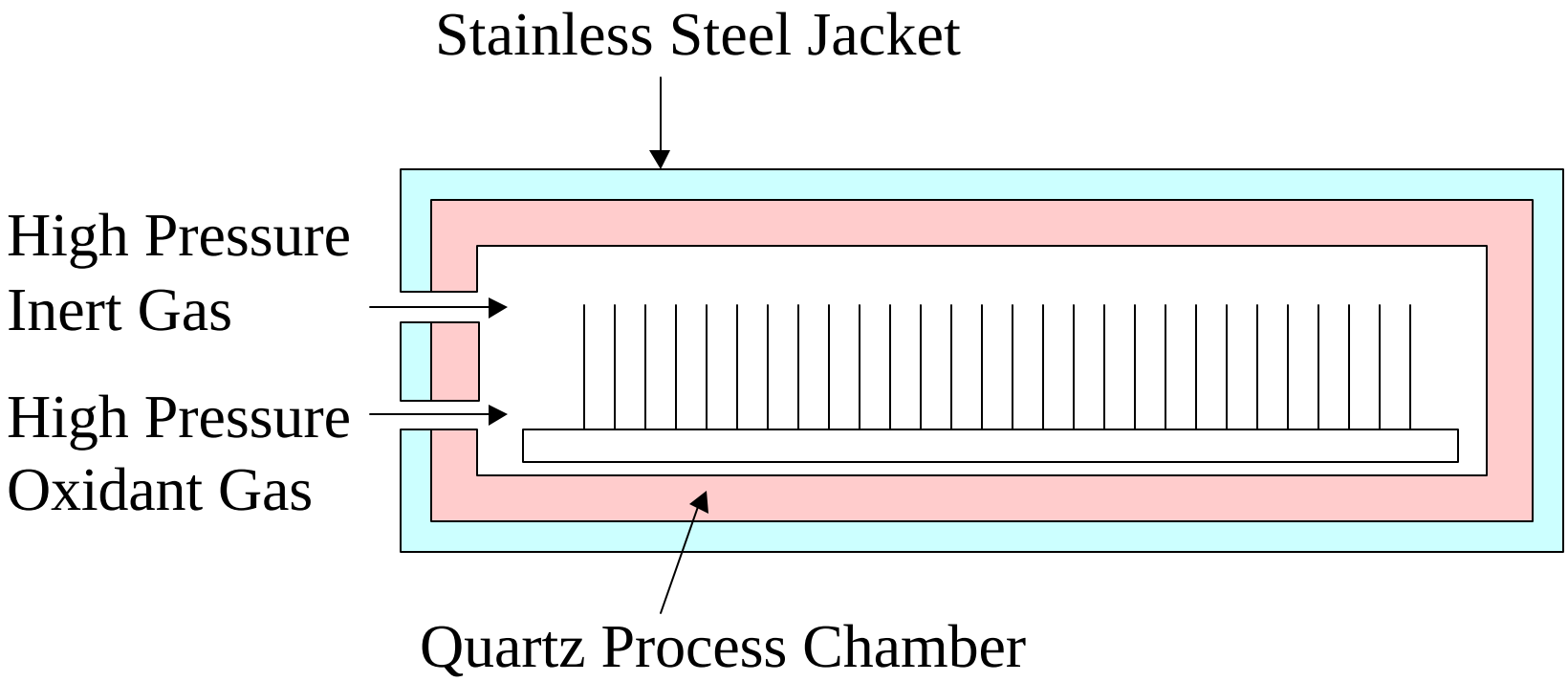
RTP Process Diagram



High Pressure Oxidation

- Faster growth rate
- Reducing oxidation temperature:
  - 1 amt. = –30 °C
- Higher dielectric strength

High Pressure Oxidation



High Pressure Oxidation

Oxidation time to grow 10,000 Å wet oxide

Temperature	Pressure	Time
1000 °C	1 atmosphere	5 hours
	5 atmosphere	1 hour
	25 atmosphere	12 minutes

High Pressure Oxidation

Oxidation temperature to grow 10,000 Å wet oxide in 5 hours

Time	Pressure	Temperature
5 hours	1 atmosphere	1000 °C
	10 atmosphere	700 °C

High Pressure Oxidation

- Complex system
- Safety issues

- Not widely used in IC production

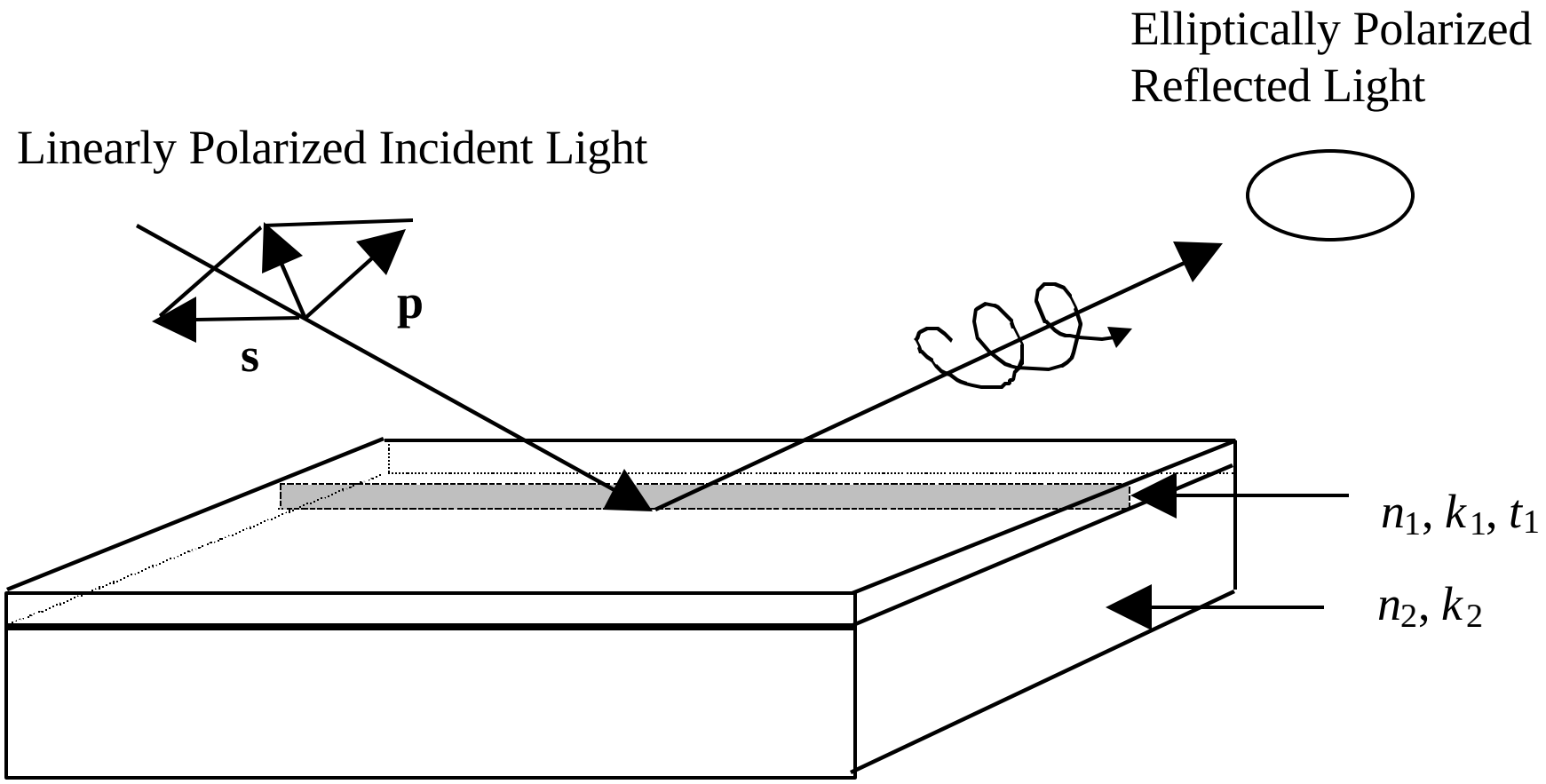
Oxide Measurement

- Thickness
- Uniformity

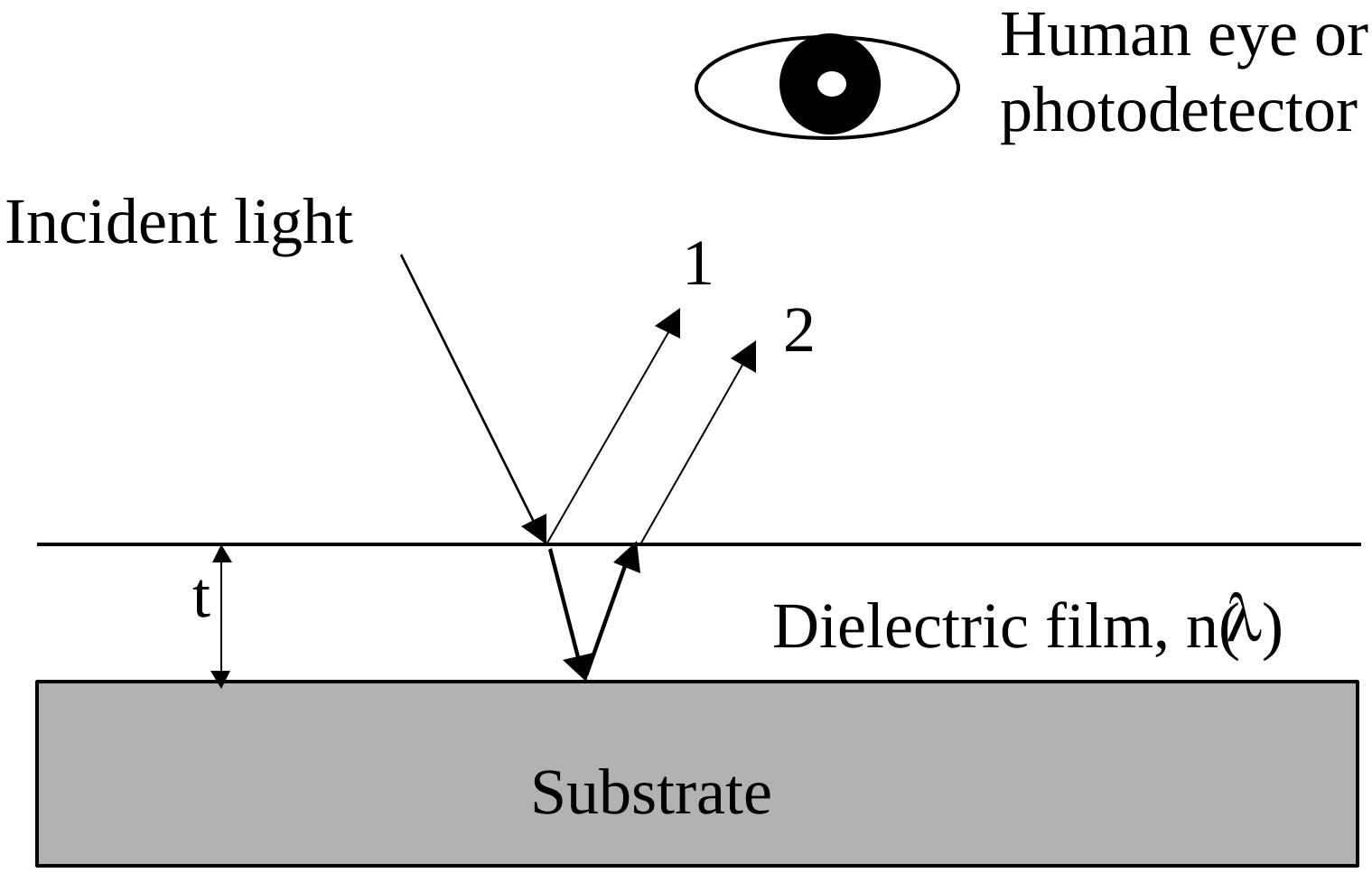
- Color chart
- Ellipsometry
- Reflectometry

- Gate oxide
- Break down voltage
- C-V characteristics

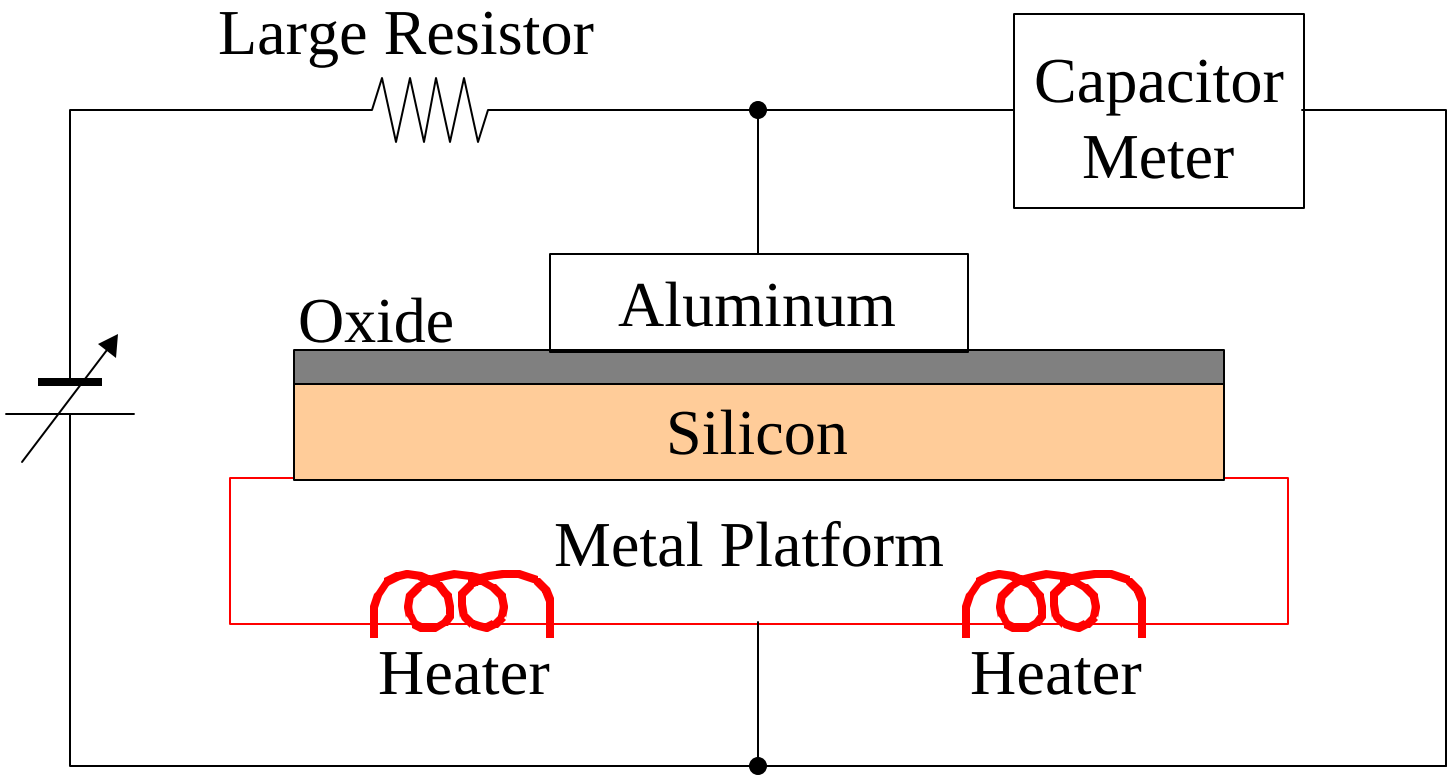
Ellipsometry



Reflectometry



C-V Test Configuration



Summary of Oxidation

- Oxidation of silicon
- High stability and relatively easy to get.
- Application
  - Isolation, masking, pad, barrier, gate, and etc.
- Wet and Dry
- More dry processes for advanced IC chips
- Rapid thermal oxidation and annealing for ultra-thin gate oxide

Diffusion

Diffusion

- Most common physics phenomena
- Materials disperse from higher concentration to lower concentration region
- Silicon dioxide as diffusion mask
- Was widely used for semiconductor doping
- “Diffusion Furnace” and “Diffusion Bay”

Illustration of Diffusion Doping

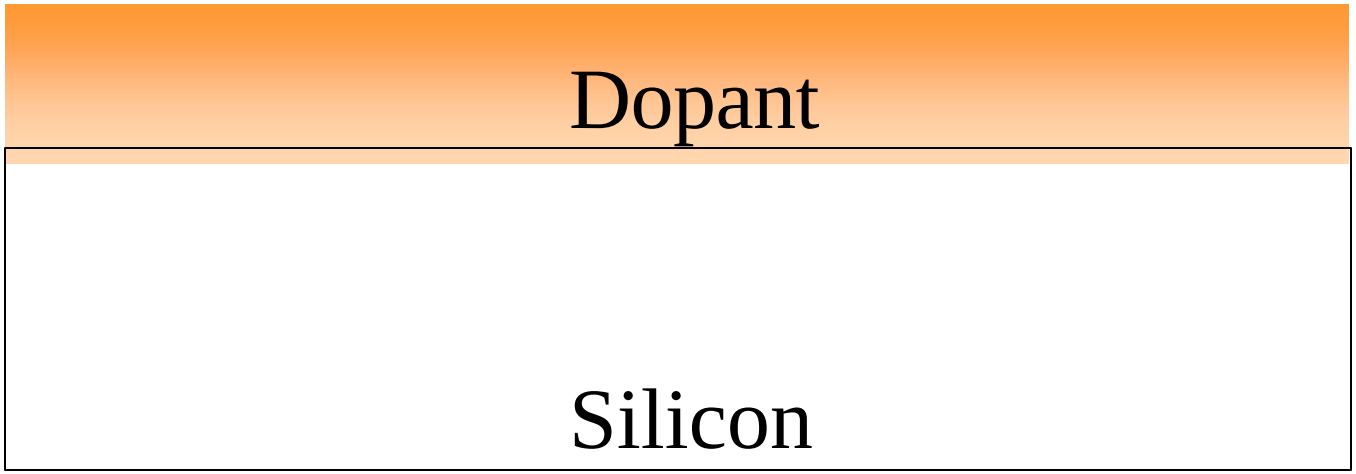
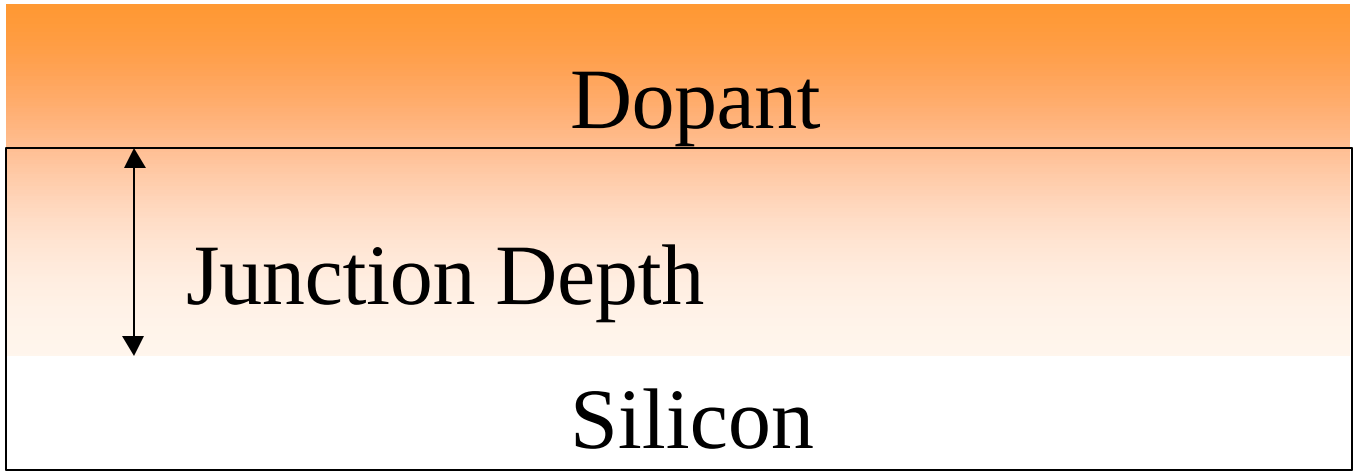
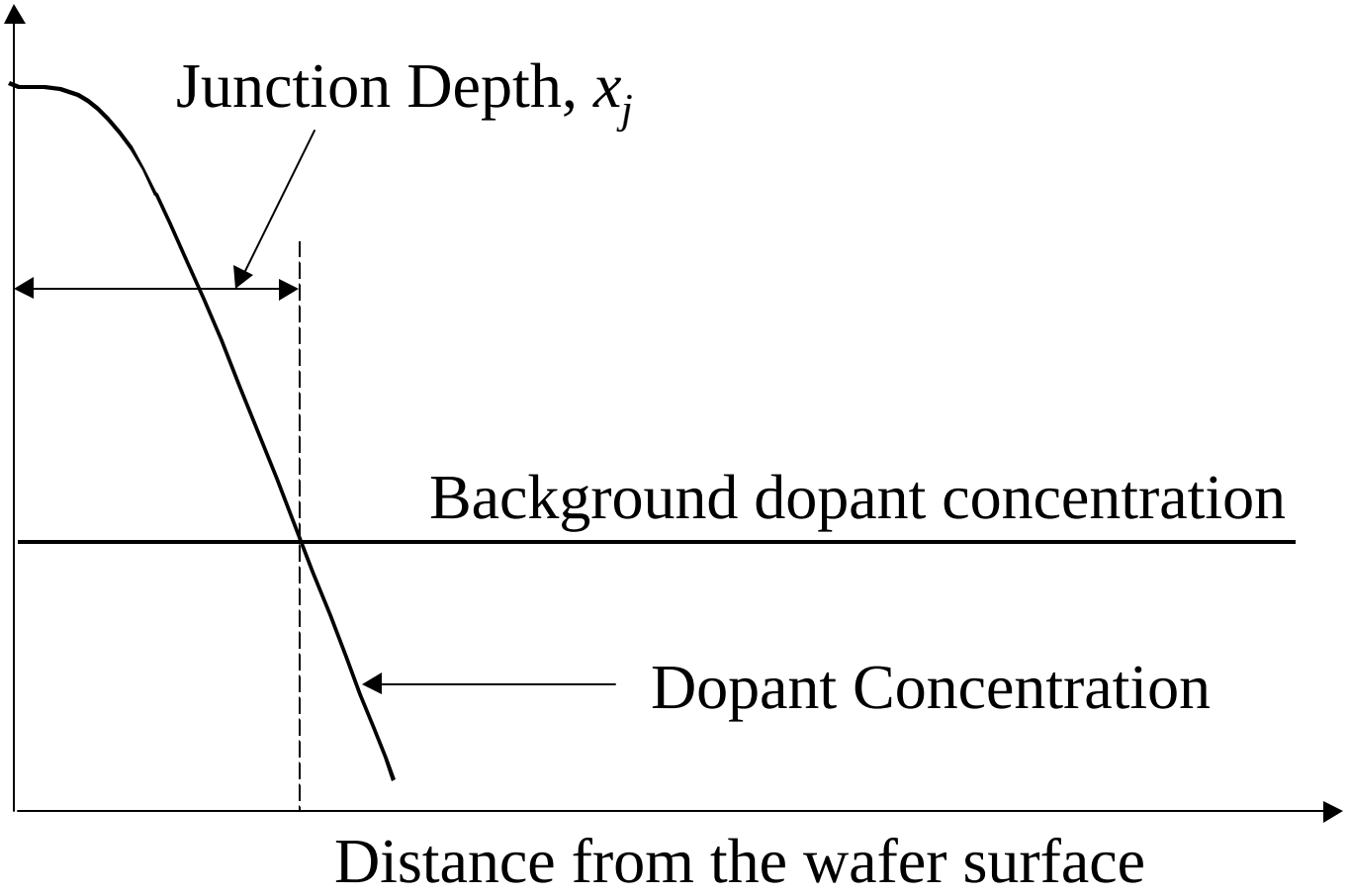


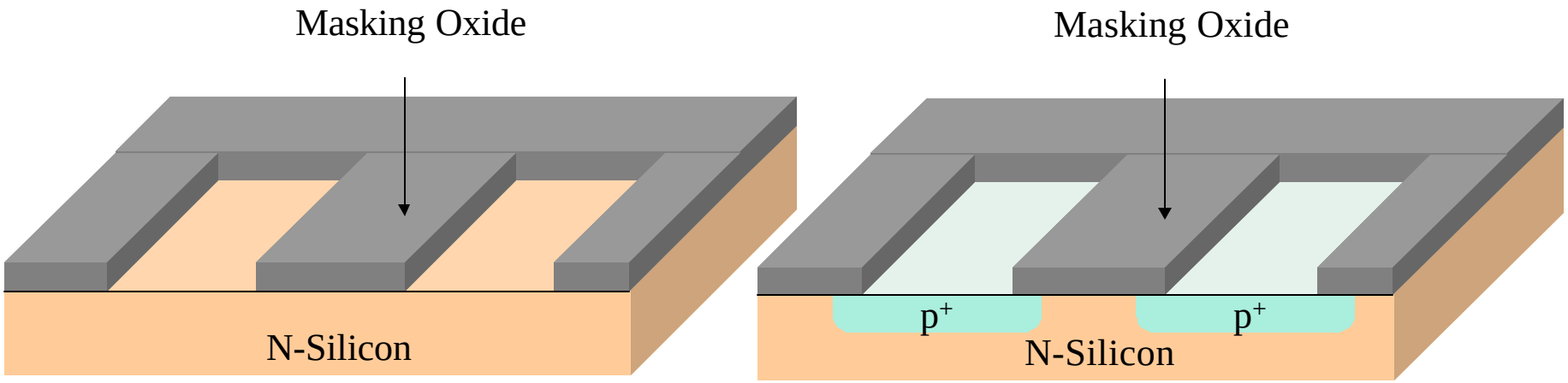
Illustration of Diffusion Doping



Definition of Junction depth



Diffusion



Diffusion

- Replaced by ion implantation due to the less process control
- Still being used in drive-in for well formation

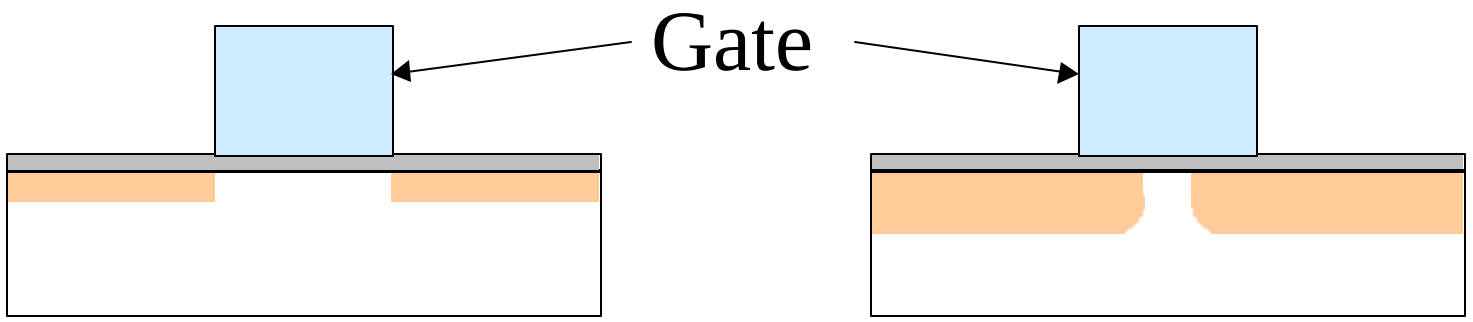
Thermal Budget

- Dopant atoms diffuse fast at high temperature

$$D = D_0 \exp\left(-E_A/kT\right)$$

- Smaller device geometry, less room for dopant thermal diffusion, less thermal budget
- Thermal budget determines the time and temperature of the post-implantation thermal processes

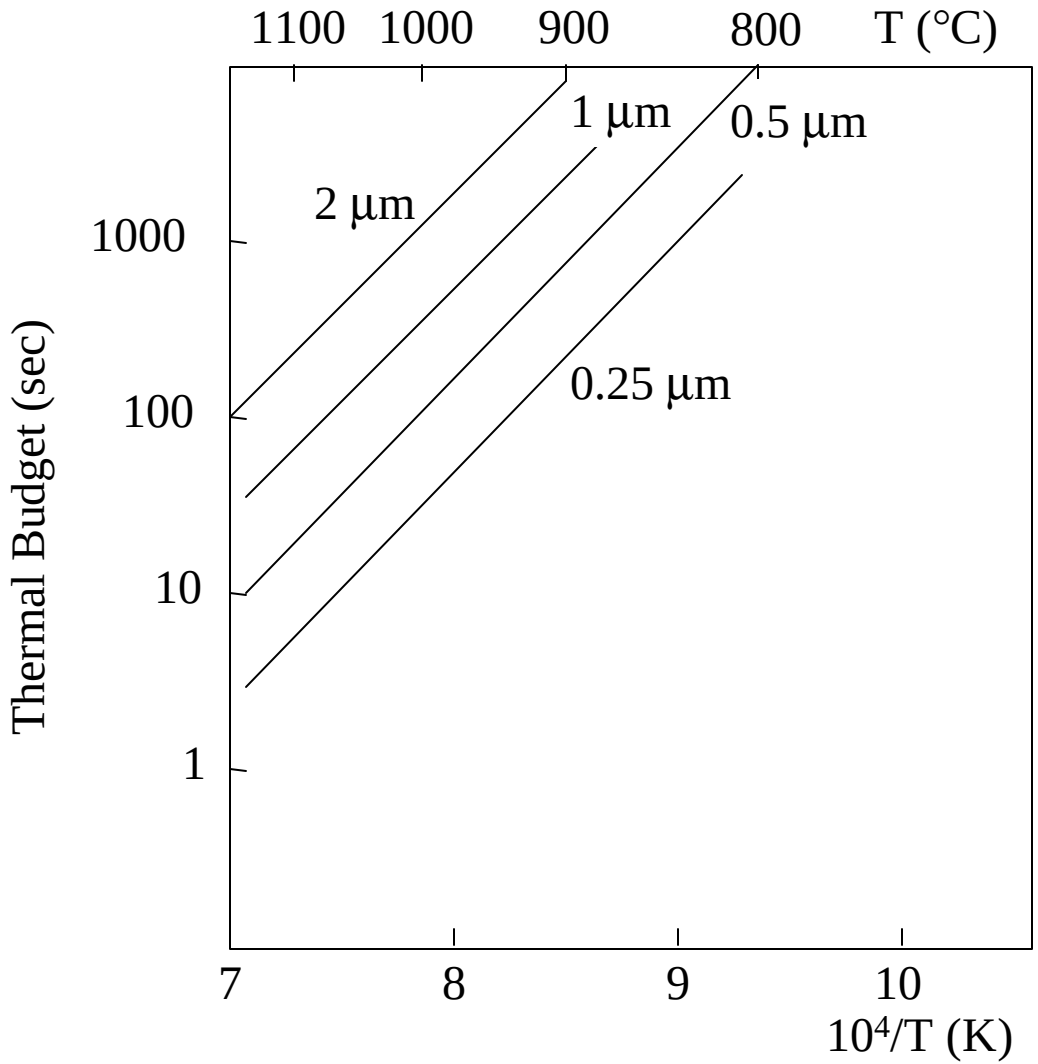
Illustration of Thermal Budget



As S/D Implantation

Over Thermal Budget

Thermal Budget



Source: Chang and Sze, *ULSI Technology*

Diffusion Doping Process

- Both dopant concentration and junction depth are related to temperature.
- No way to independently to control both factor
- Isotropic dopant profile
- Replaced by ion implantation after the mid-1970s.

Diffusion Doping Process

- Silicon dioxide as hard mask
- Deposit dopant oxide
- Cap oxidation
  - prevent dopant diffusion into gas phase
- Drive-in

Diffusion Doping Process

- Oxidation, photolithography and oxide etch
- Pre-deposition:

$$B_2H_6 + 2\ O_2 \rightarrow\ B_2O_3 + 3\ H_2O$$

- Cap oxidation:

$$2\ B_2O_3 + 3\ Si \rightarrow\ 3\ SiO_2 + 4\ B$$

$$2\ H_2O + Si \rightarrow\ SiO_2 + 2\ H_2$$

- Drive-in
  - Boron diffuses into silicon substrate

Diffusion Doping Process

- Oxidation, photolithography and oxide etch
- Deposit dopant oxide:

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 3Cl_2$$

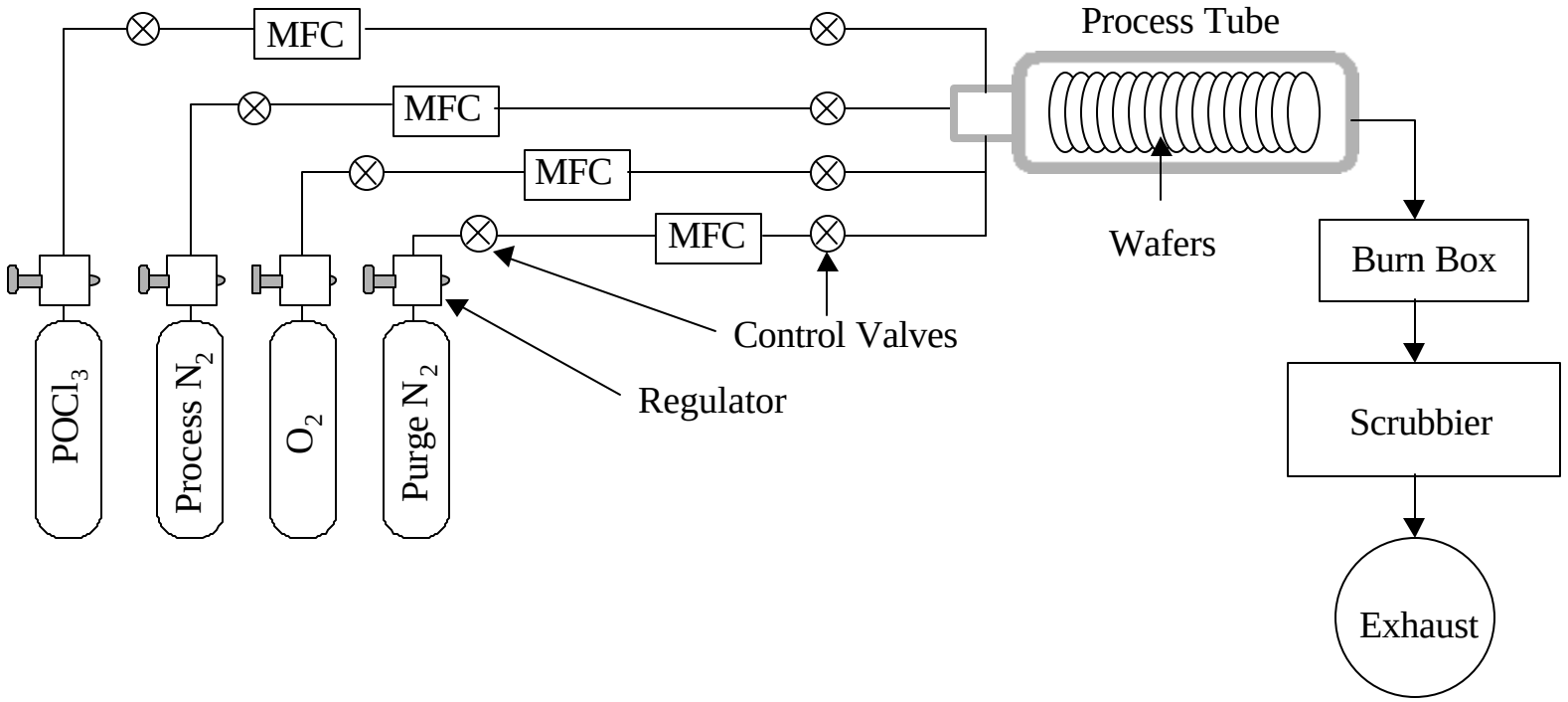
- Cap oxidation

$$2P_2O_5 + 5Si \rightarrow 5SiO_2 + 4P$$

  – Phosphorus concentrates on silicon surface

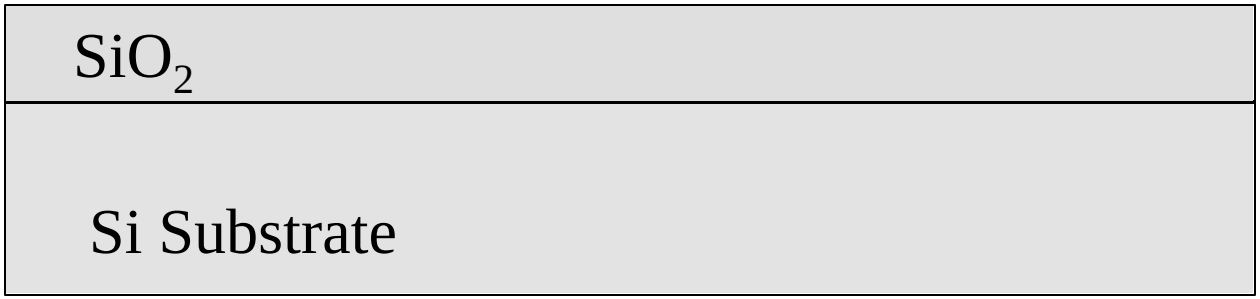
- Drive-in
  – Phosphorus diffuses into silicon substrate

Phosphorus Diffusion System

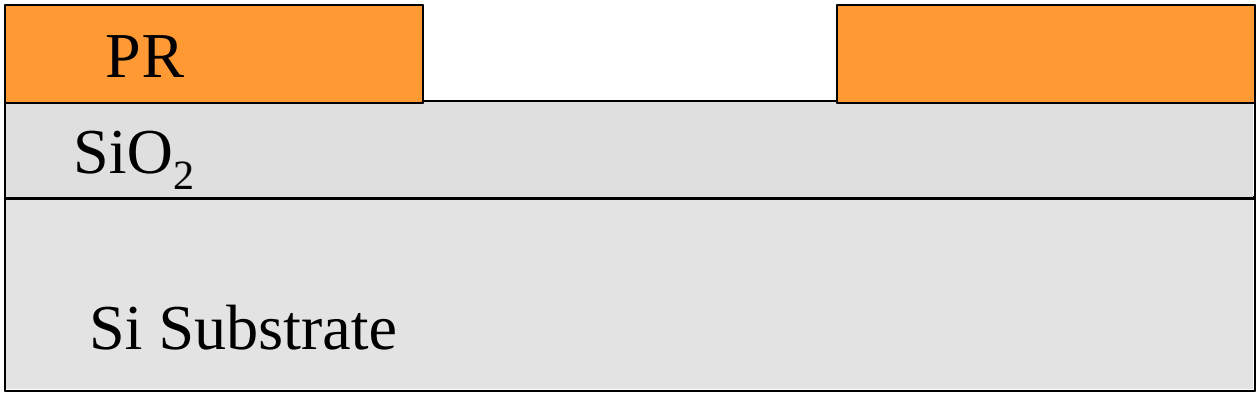


Wafer Clean

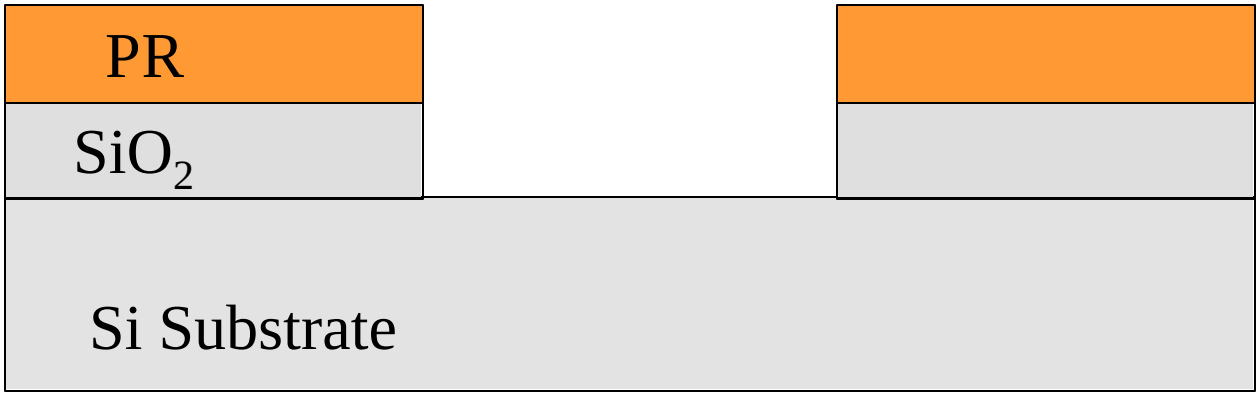
Oxidation



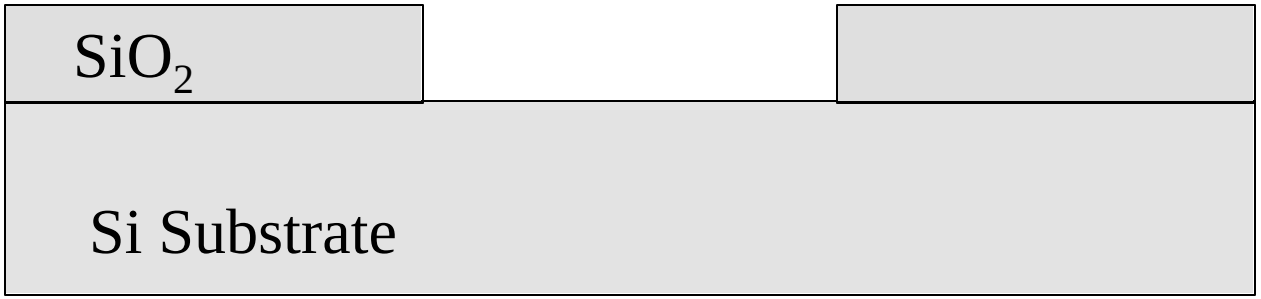
Doped Area Patterning



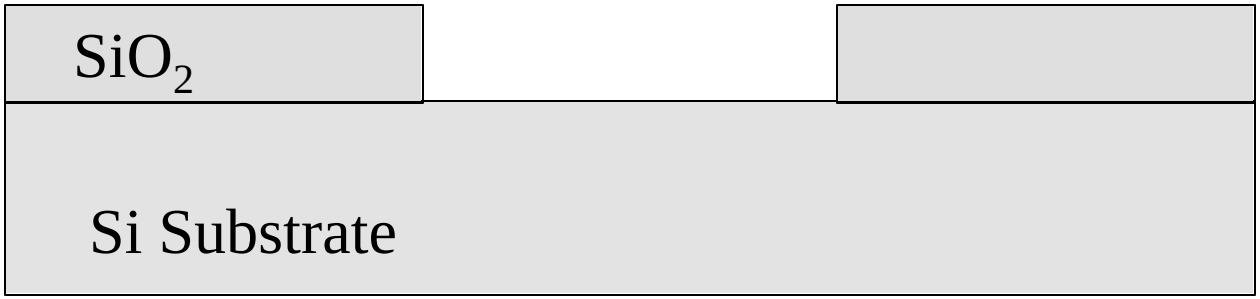
Etch Silicon Dioxide



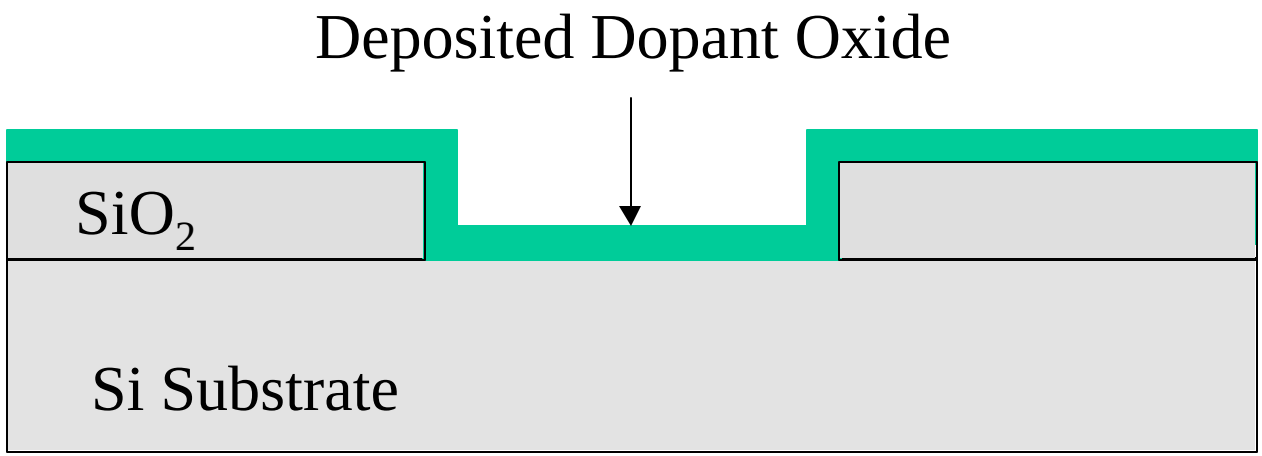
Strip Photoresist



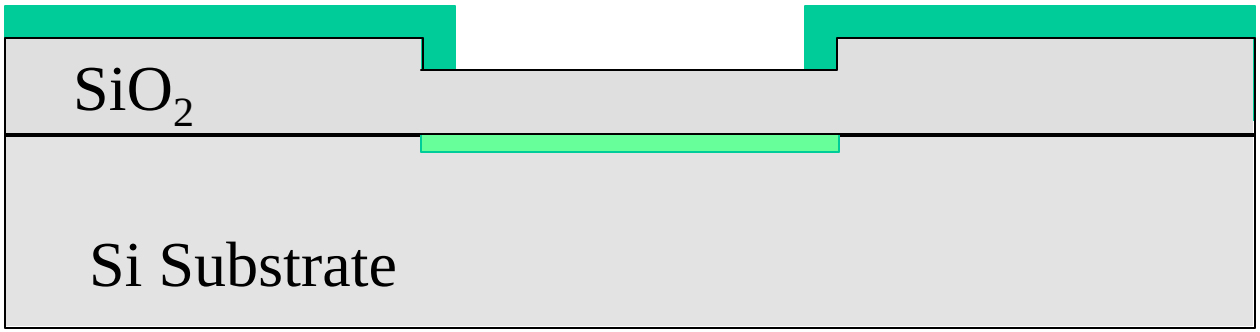
Wafer Clean



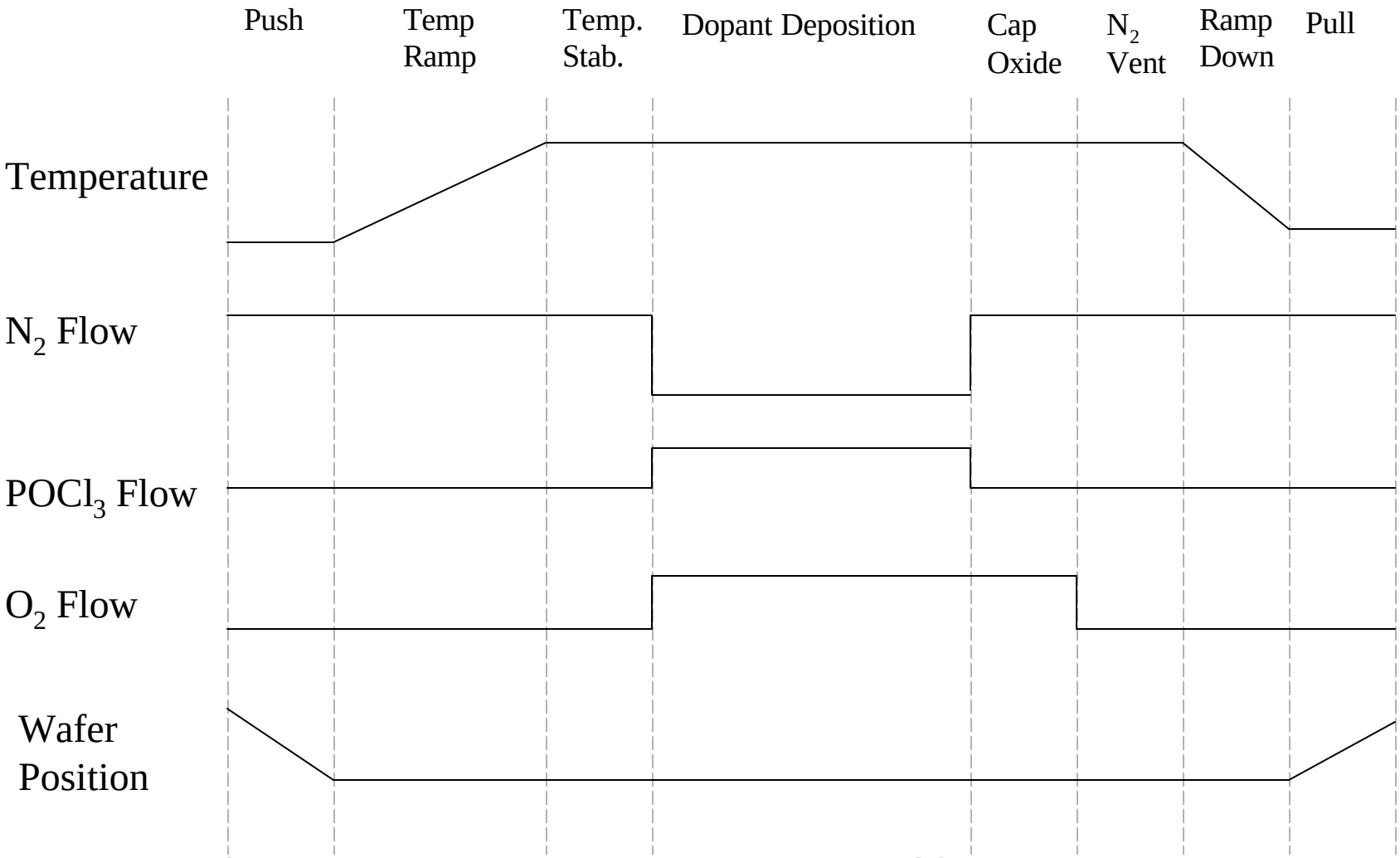
Dopant Oxide Deposition



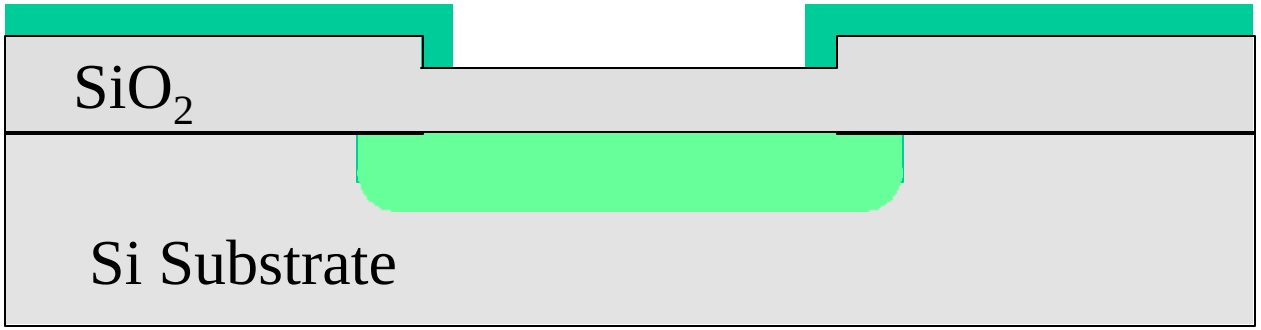
Cap Oxidation



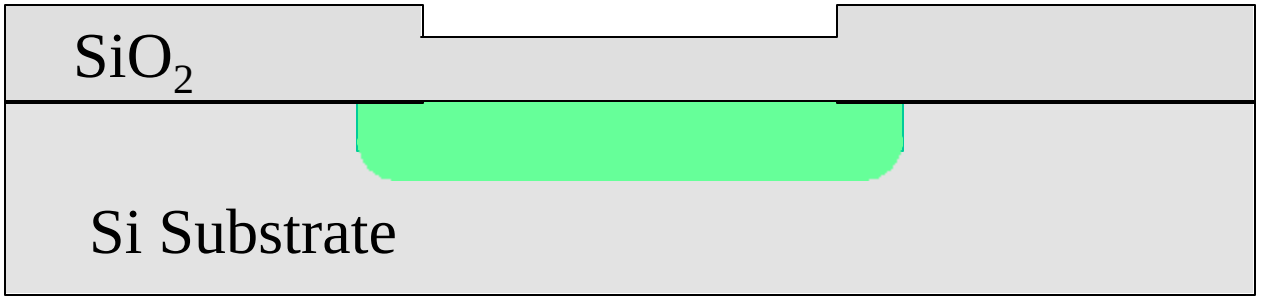
Phosphoric Oxide Deposition and Cap Oxidation



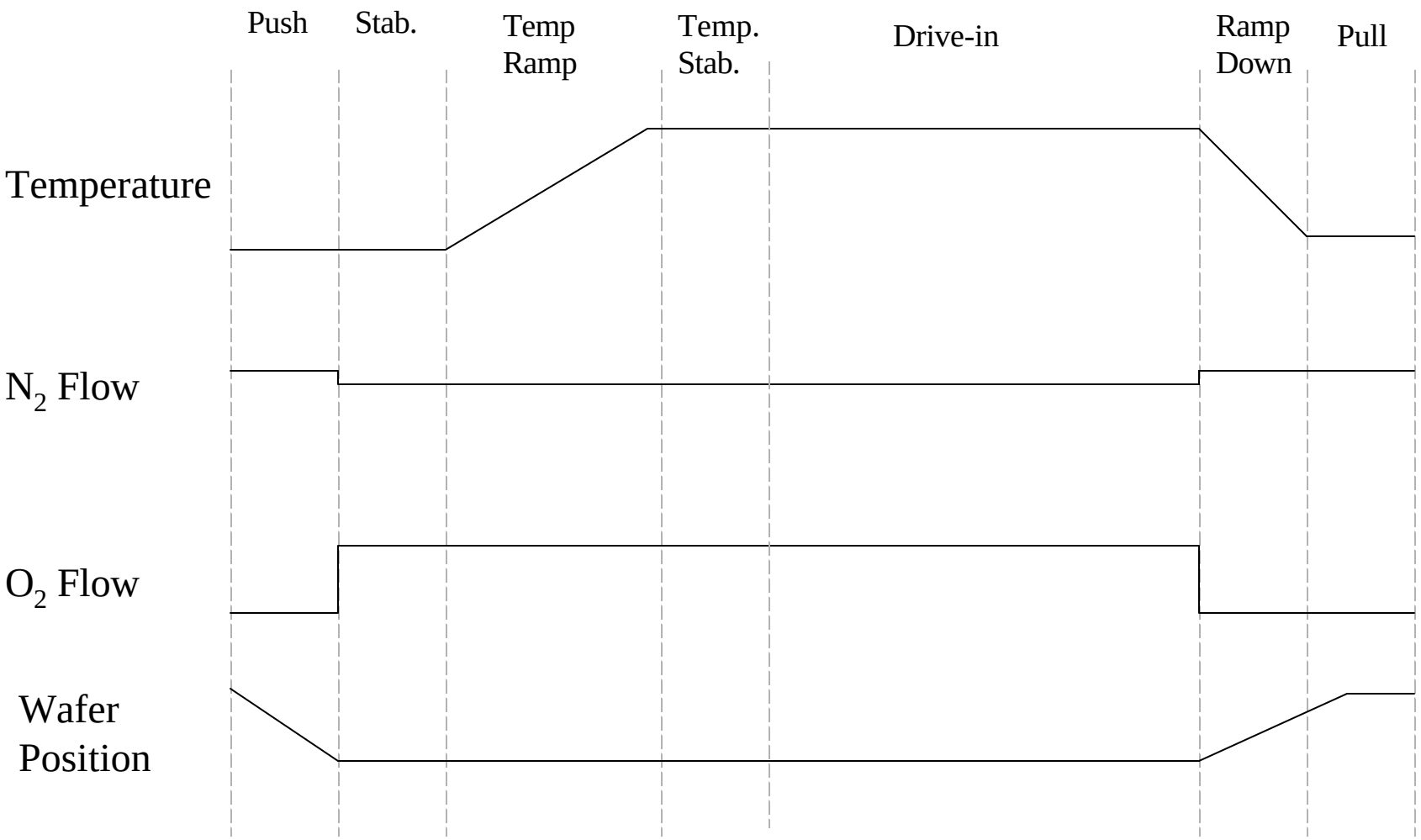
Drive-in



Strip Oxide, Ready for Next Step



Phosphorus Drive-in



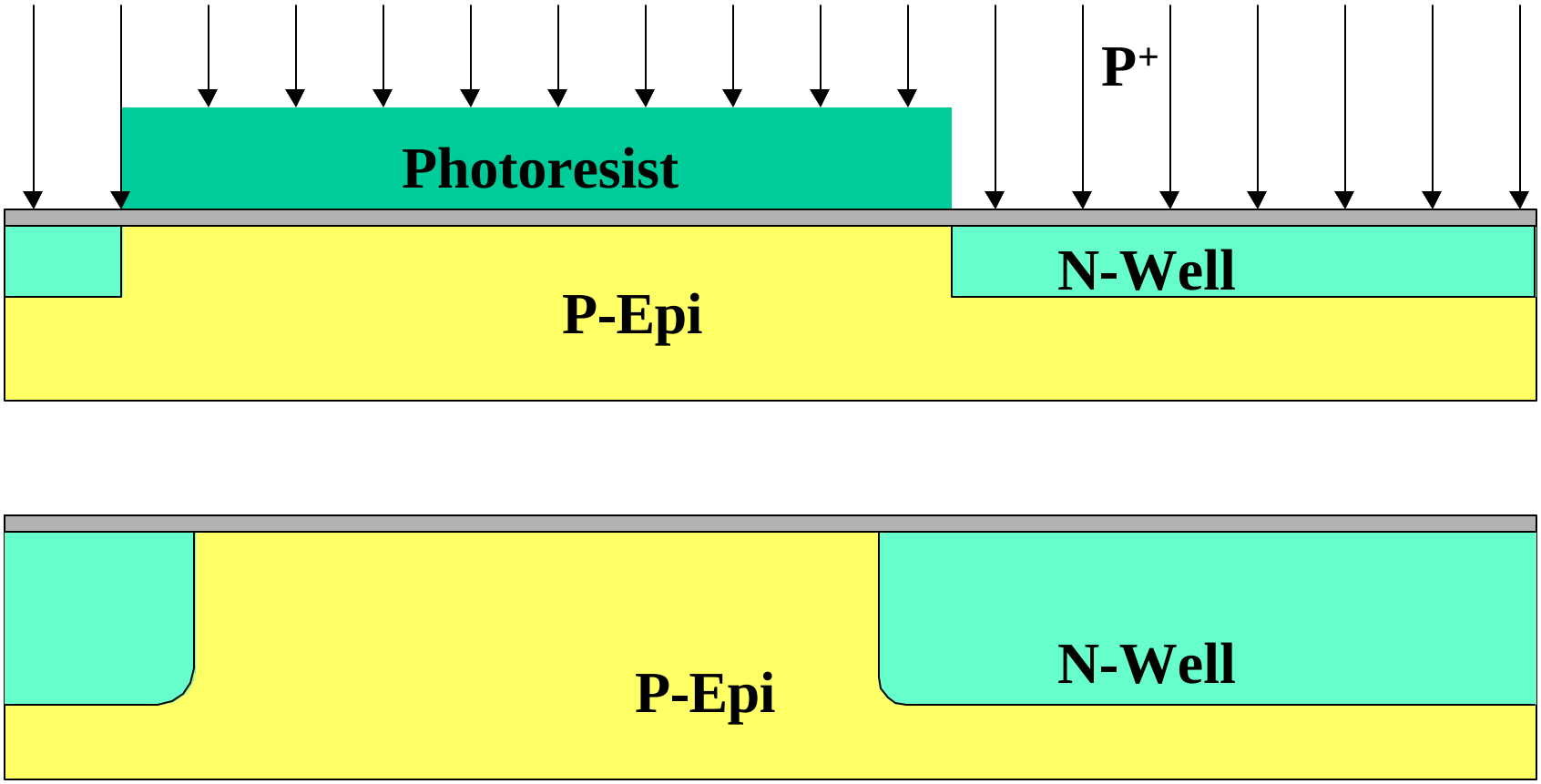
Limitations and Applications

- Diffusion is isotropic process and always dope underneath masking oxide
- Can’t independently control junction depth and dopant concentration
- Used for well implantation drive-in
- R&D for ultra shallow junction (USJ) formation

Application of Diffusion: Drive-in

- Wells have the deepest junction depth
- Need very high ion implantation energy
- Cost of MeV ion implanters is very high
- Diffusion can help to drive dopant to the desired junction depth while annealing

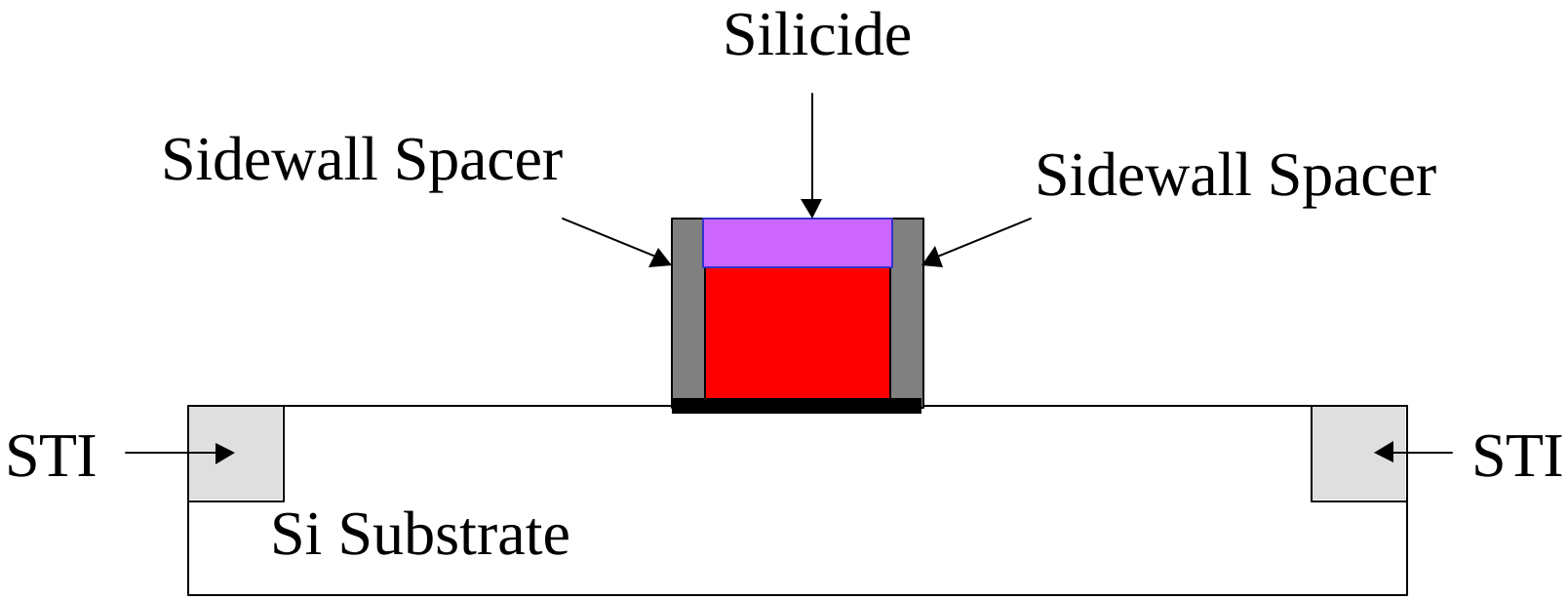
Well Implantation and Drive-in



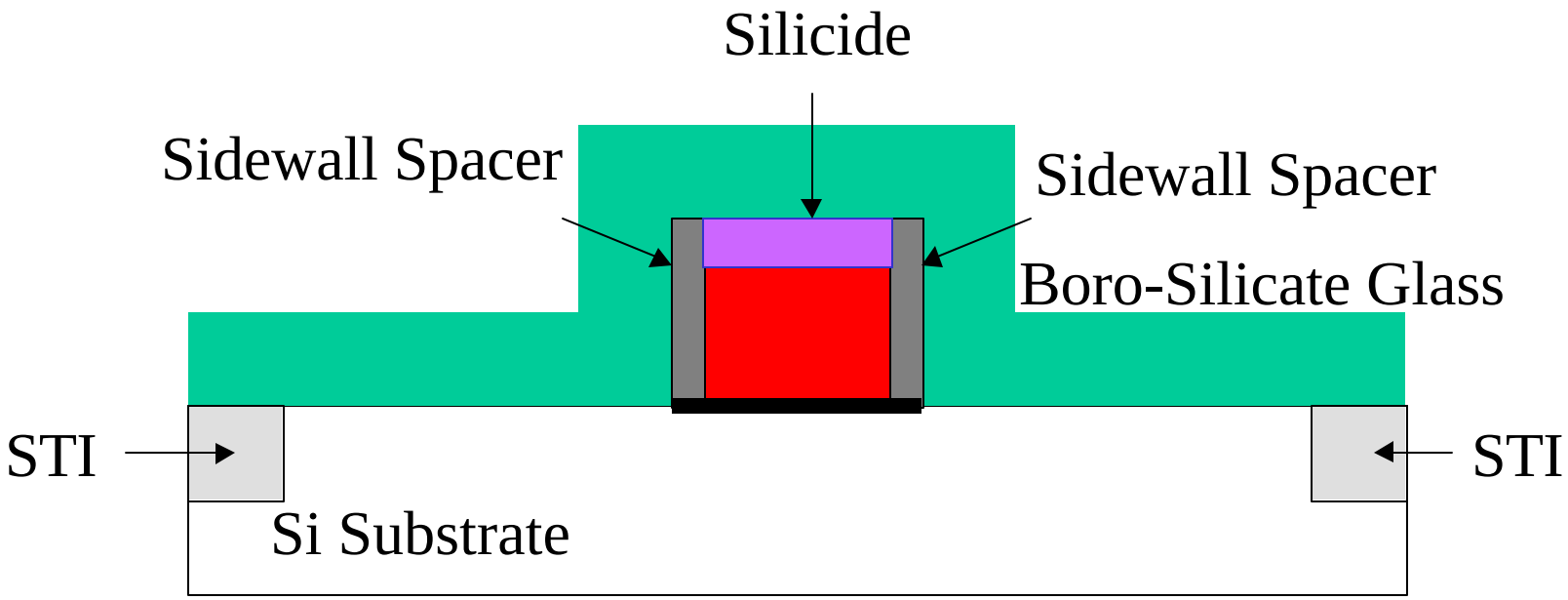
Diffusion for Boron USJ Formation

- Small devices needs ultra shallow junction
- Boron is small and light, implanter energy could be too high for it goes too deep
- Controlled thermal diffusion is used in R&D for shallow junction formation

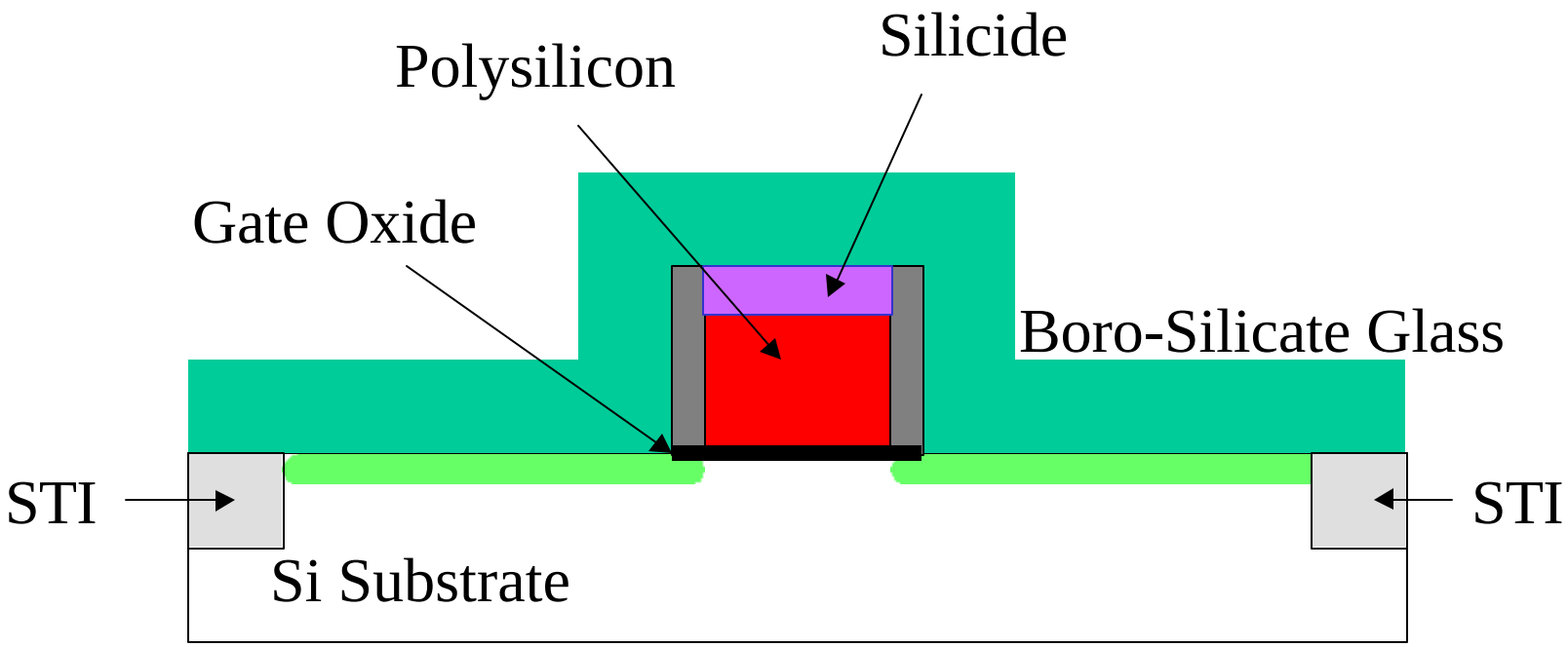
Surface Clean



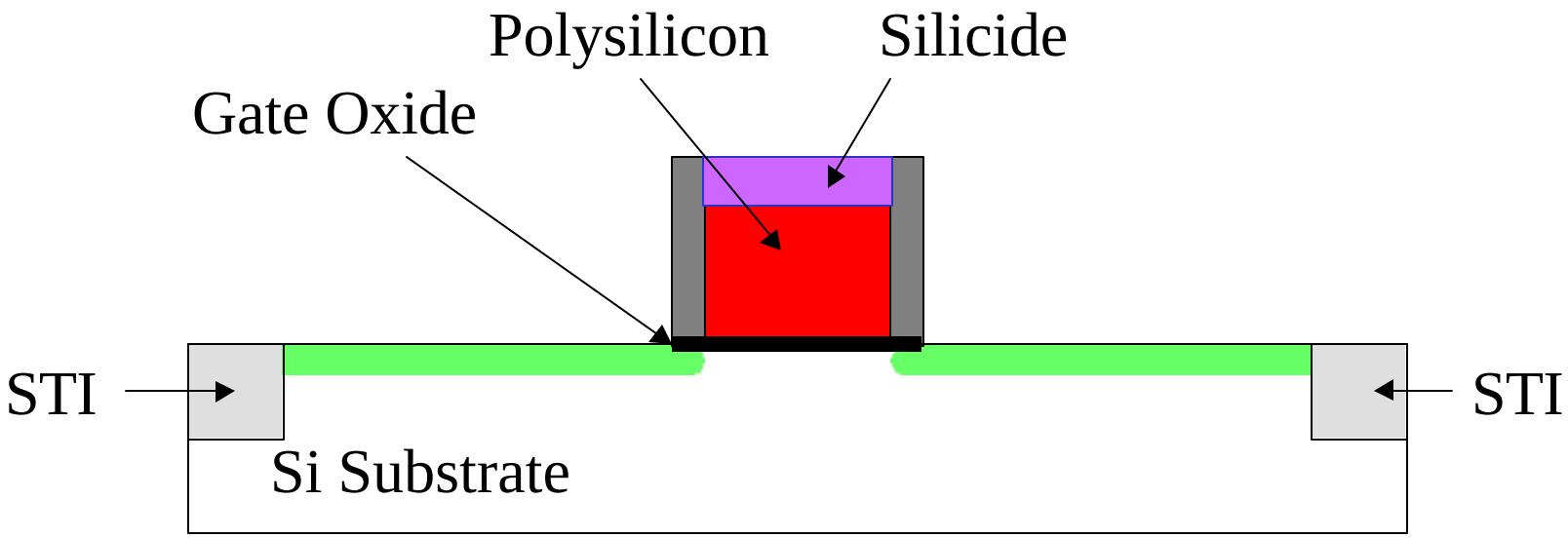
BSG CVD


Silicide
Sidewall Spacer
Sidewall Spacer
Boro-Silicate Glass
STI
STI
Si Substrate

RTP Dopant Drive-in



Strip BSG

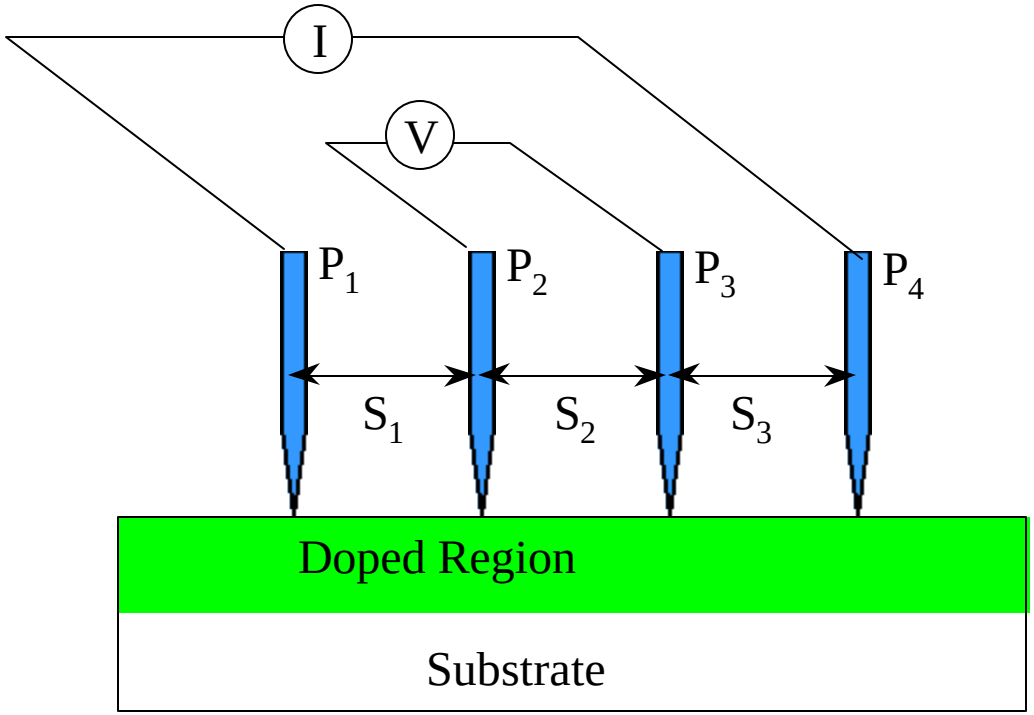


Doping Measurement

- Four-point probe

$$R_s = r/t$$

Four-Point Probe Measurement



Summary of Diffusion

- Physics of diffusion is well understood
- Diffusion was widely used in doping processes in early IC manufacturing
- Replaced by ion implantation since the mid-1970s

Annealing and RTP Processes

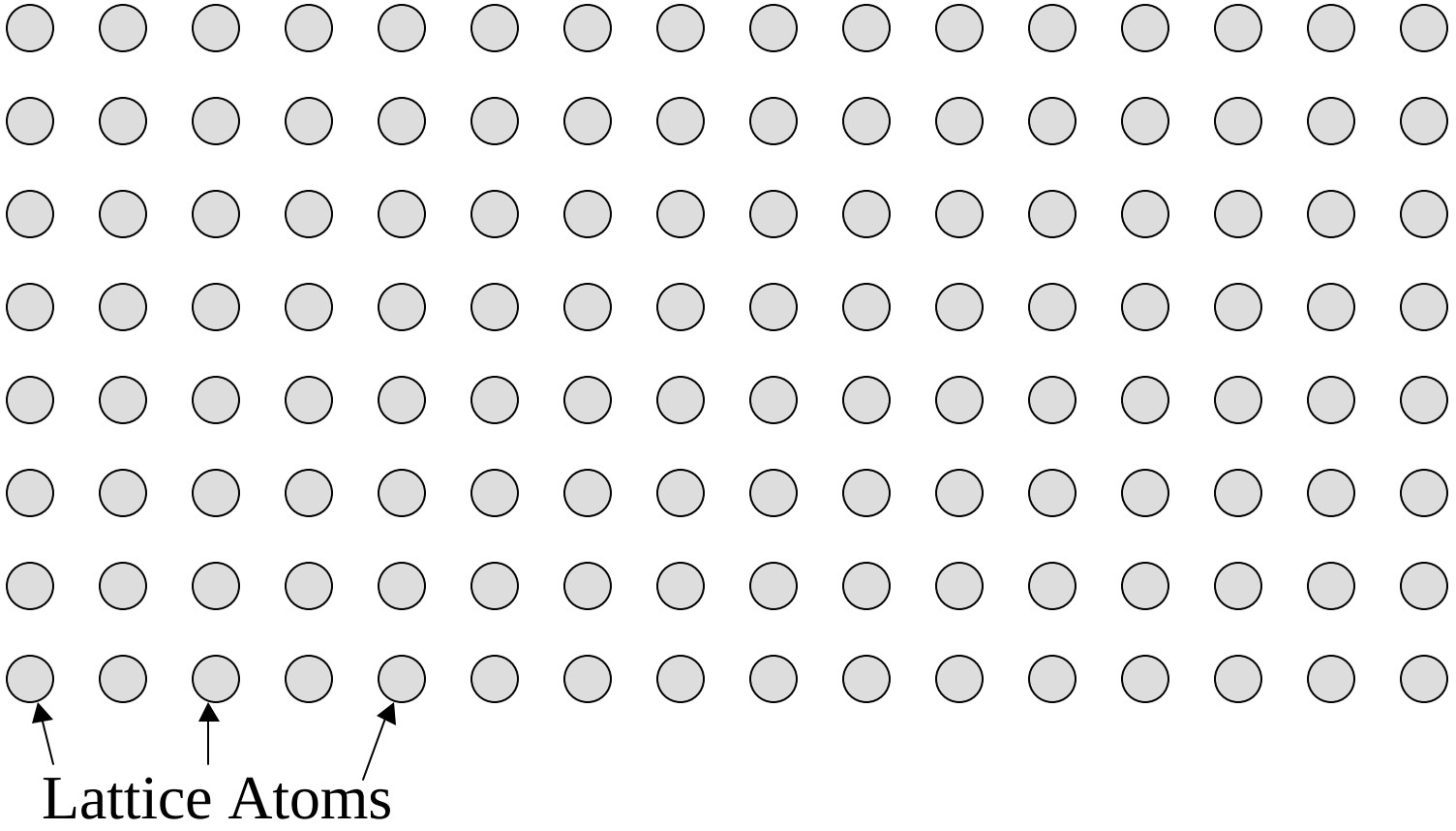
Post-implantation Annealing

- Energetic ions damage crystal structure
- Amorphous silicon has high resistivity
- Need external energy such as heat for atoms to recover single crystal structure
- Only in single crystal structure dopants can be activated

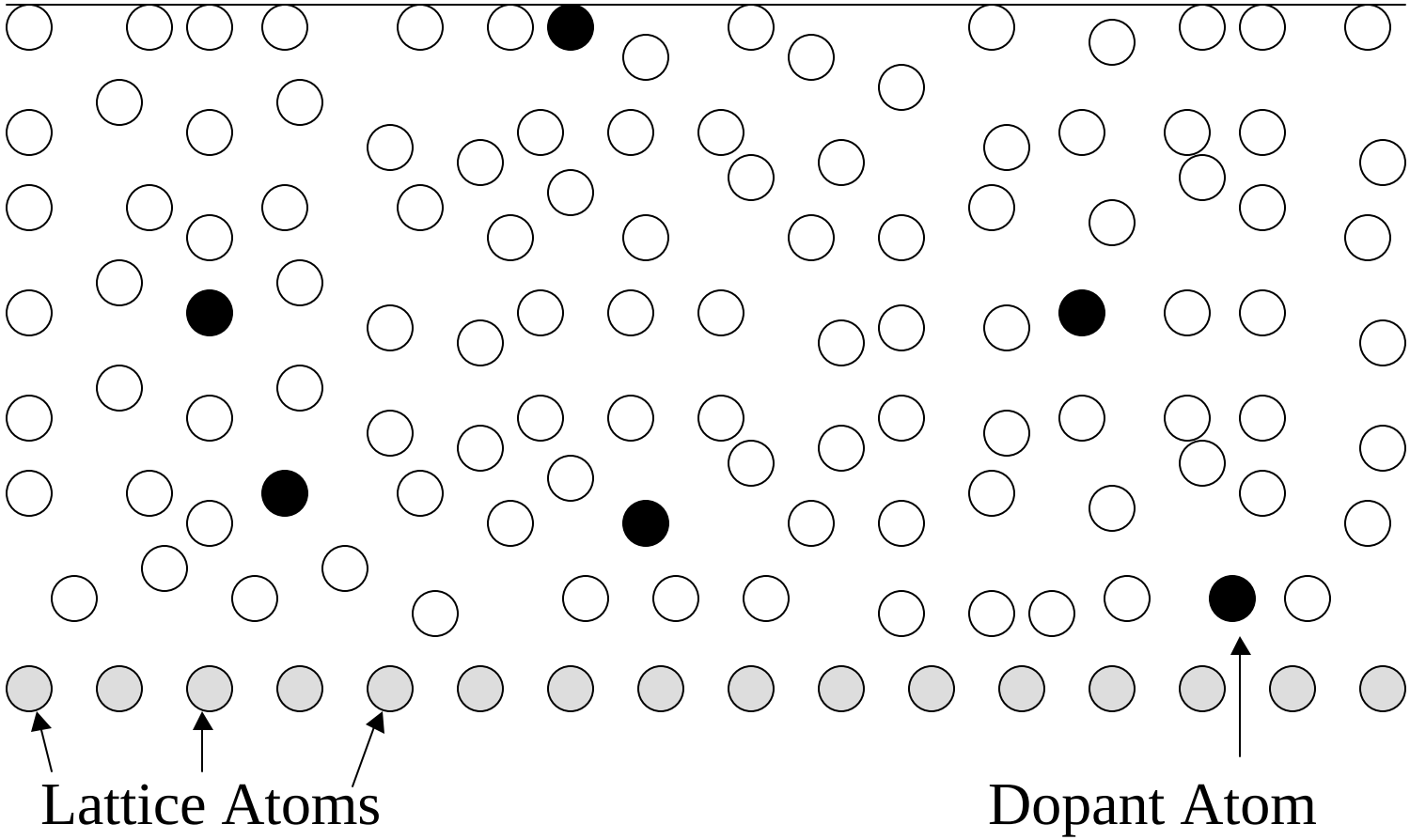
Post-implantation Annealing

- Single crystal structure has lowest potential energy
- Atoms tend to stop on lattice grid
- Heat can provide energy to atoms for fast thermal motion
- Atoms will find and settle at the lattice grid where has the lowest potential energy position
- Higher temperature, faster annealing

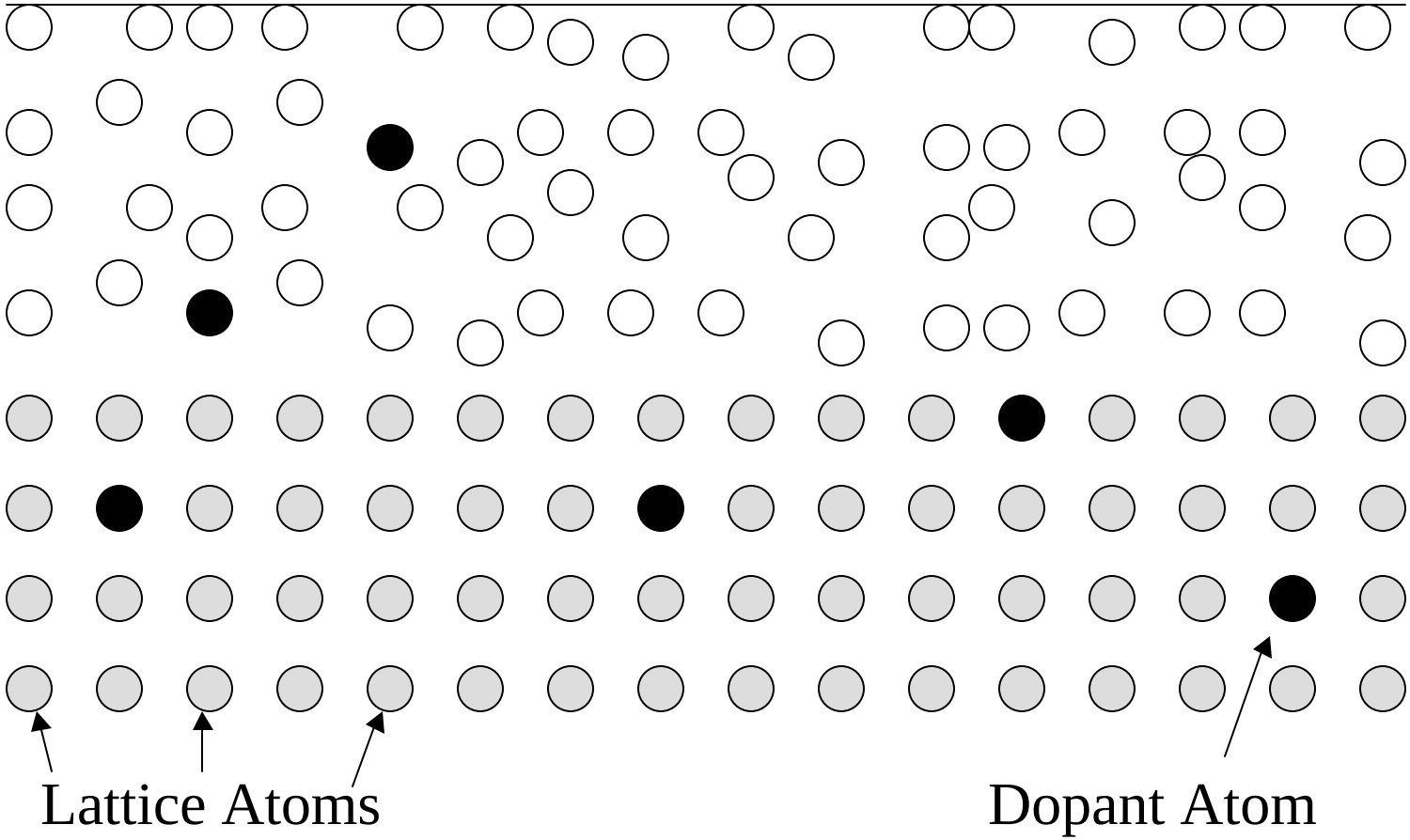
Before Ion Implantation



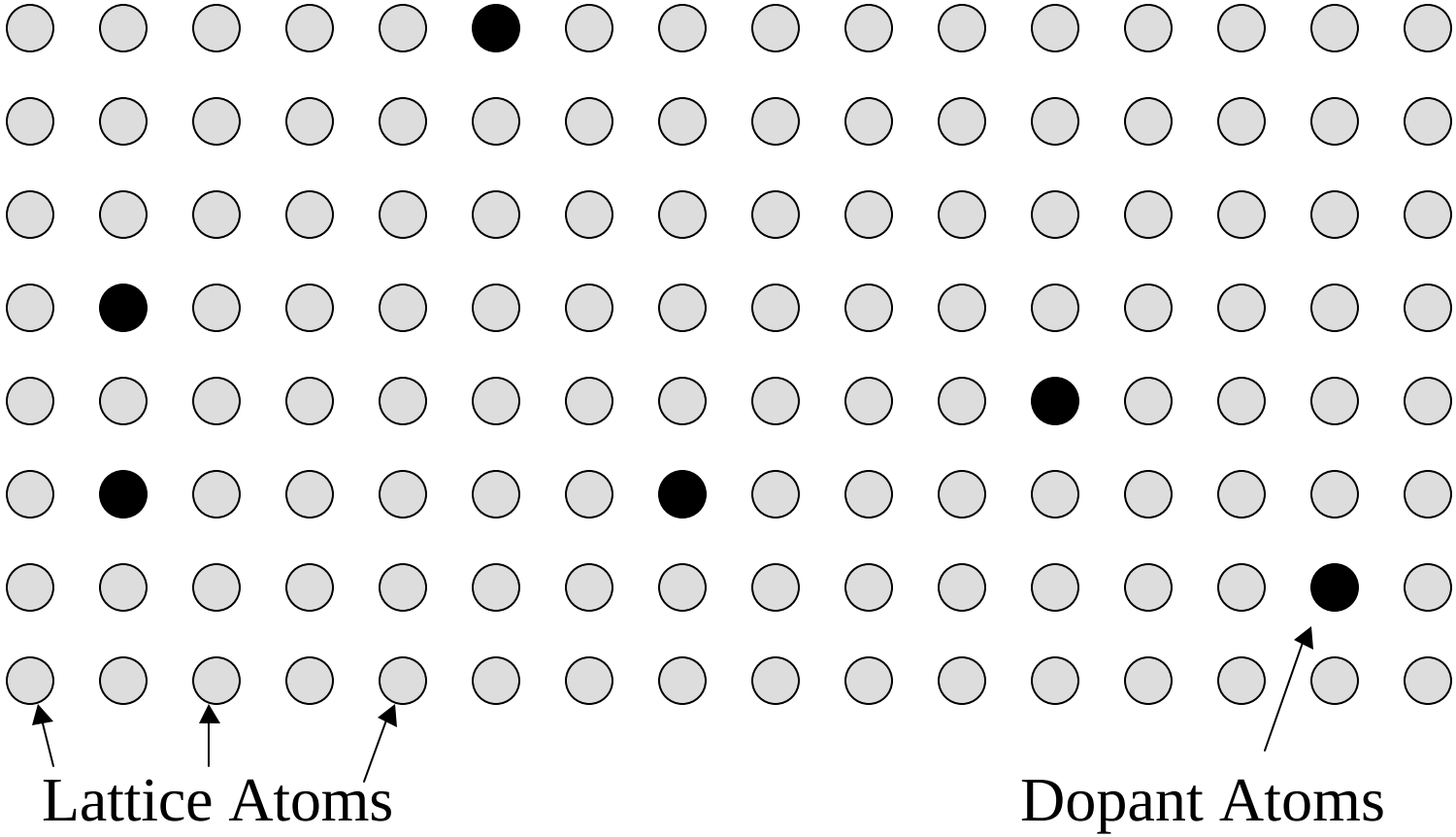
After Ion Implantation



Thermal Annealing



Thermal Annealing



Annoy Annealing

- A thermal process in which different atoms chemically bond with each other to form a metal alloy.
- Widely used in silicide formation
- Self aligned silicide (salicide)
  - Titanium silicide, $TiSi_2$
  - Cobalt silicide, $CoSi_2$
- Furnace and RTP

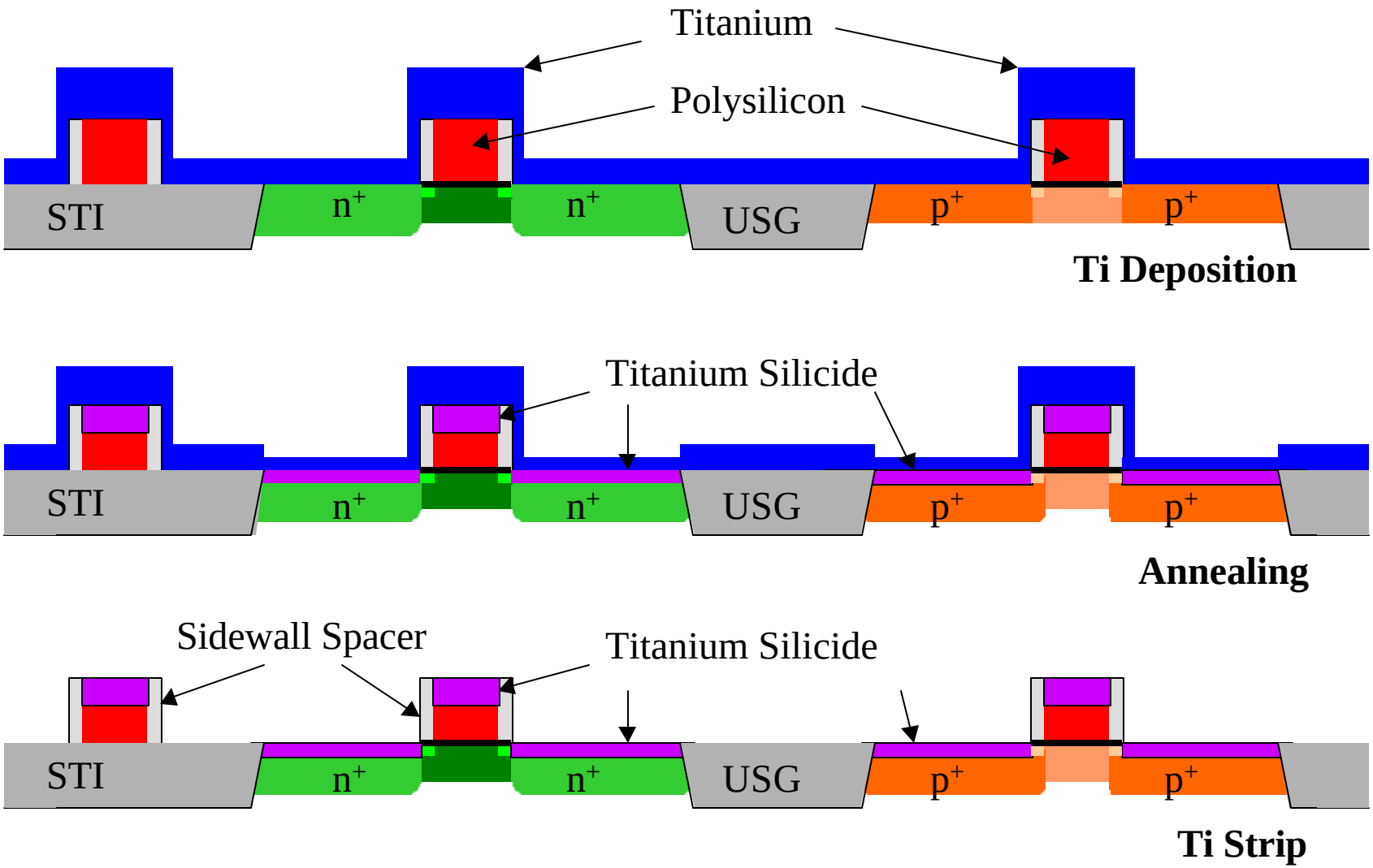
Silicide

- Much lower resistivity than polysilicon
- Used as gate and local interconnection
- Used as capacitor electrodes
- Improving device speed and reduce heat generation
- $TiSi_2$, WSi_2 are the most commonly used silicide
- $CoSi_2$, $MoSi_2$, and etc are also used

Titanium Silicide Process

- Argon sputtering clean
- Titanium PVD
- RTP Anneal, ~700 °C
- Strip titanium, H_2O_2:H_2SO_2

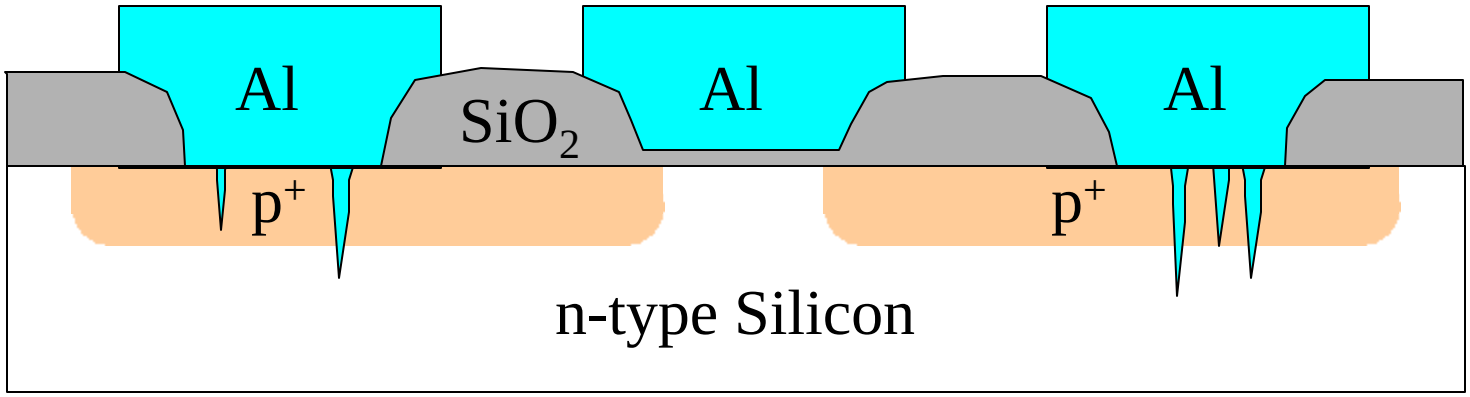
Titanium Silicide Process



Aluminum-silicon Alloy

- Form on silicon surface
- Prevent junction spiking due to silicon dissolving in aluminum

Junction Spike

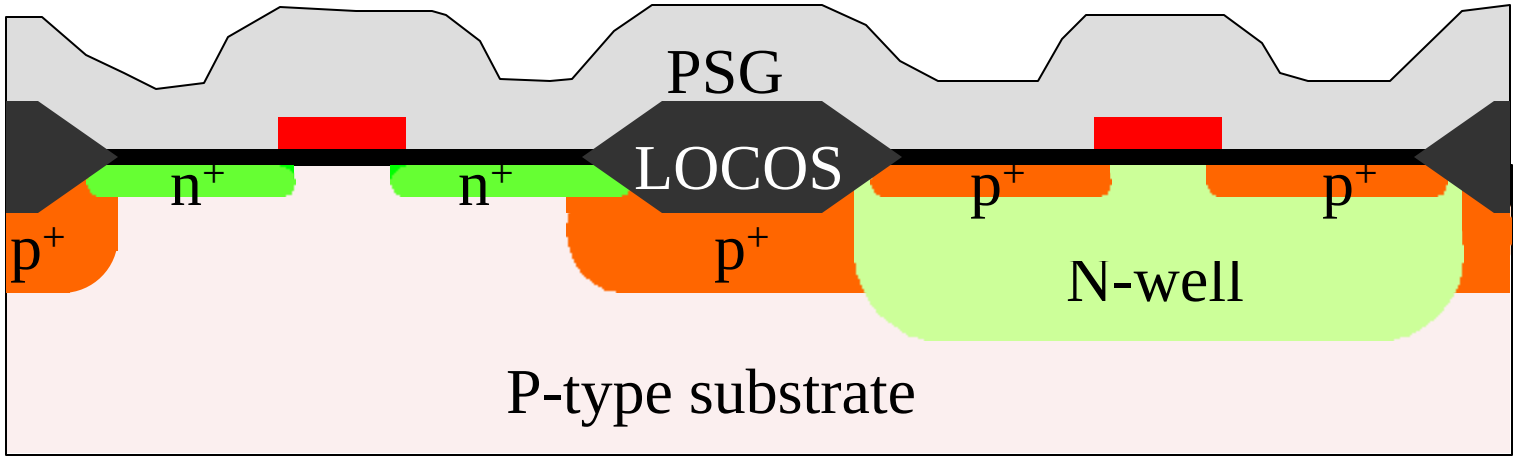


Reflow

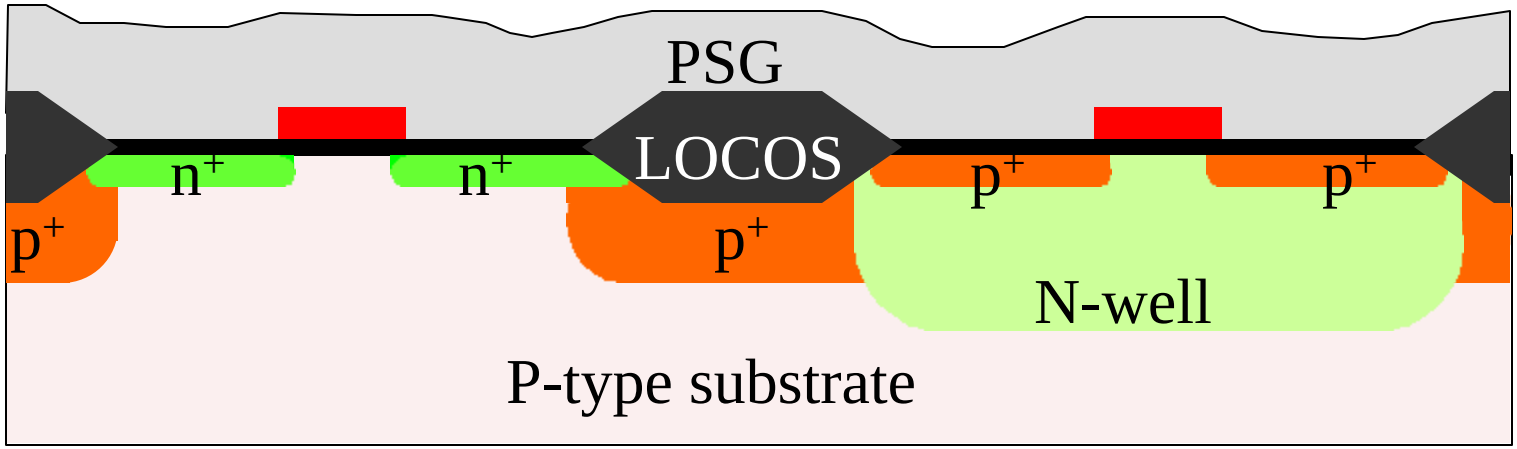
- Flowed surface is smoother and flatter
- Easier for photolithography and metallization
- Higher temperature, better flow result
- Reflow time and temperature are determined by the thermal budget
- Higher dopant concentration requires lower flow temperature

Illustration of BPSG Reflow

As Deposit



After Reflow



Reflow

- Undoped silicate glass (USG) becomes soften at very high temperature T > 1500 °C, will flow due to the surface tension
- PSG and BPSG become soften at significant lower temperature (< 1100 °C down to 850 °C)
- Phosphorus also can trap sodium
- PSG and BPSG is commonly used as pre-metal dielectric (PMD)

Reflow Process

- Wafer loading
- Temperature rump-up
- Temperature stabilization
- Reflow
- Temperature rump-down
- Wafer unloading

Reflow Process

- Reflow usually used N_2 ambient
- Sometimes H_2O vapor is also used
- H_2O helps to filly oxidize dopant atoms

Reflow Process

- Smaller device, less thermal budget
- No enough thermal budget for reflow for sub-0.25 μm devices
- PSG anneal (~750 °C) instead of reflow

Summary of Anneal

- The most commonly used anneal processes are post-implantation annealing, alloy annealing and reflow
- Thermal anneal is required after ion implantation for recover crystal structure and activation dopant atoms
- Thermal anneal helps metal to react with silicon to form silicides

Summary of Anneal

- Metal anneal helps to form larger grain size and reduces the resistivity
- PSG or BPSG reflow smoothens and flattens the dielectric surface and helps photolithography and metallization processes
- RTP becomes more commonly used in annealing processes

Summary of Anneal

- Advantages of RTP
  - Much faster ramp rate (75 to 150 °C/sec)
  - Higher temperature (up to 1200 °C)
  - Faster process
  - Minimize the dopant diffusion
  - Better control of thermal budget
  - Better wafer to wafer uniformity control

High Temperature Deposition Processes

What is CVD

Chemical Vapor Deposition

- Gas(es) or vapor(s) chemically react on substrate surface and form solid byproduct on the surface as deposited thin film.
- Other byproducts are gases and leave the surface.
- Widely used in IC processing for metal, dielectric and silicon thin film deposition.

High Temperature CVD

- Epitaxy
- Polysilicon
- Silicon Nitride

Epitaxy

- Monocrystralline layer
- Epitaxy silicon
- Epitaxy silicon-germanium
- Epitaxy GaAs

Epitaxy Silicon

- Provide high quality silicon substrate without trace amount of oxygen and carbon.
- Required for bipolar devices.
- Needed for high performance CMOS devices.

Epitaxy Silicon

- High temperature (~1000 °C) processes.
- Silane (SiH_4), DCS (SiH_2Cl_2) or TCS ($SiHCl_3$) as silicon source gases.
- Hydrogen as process gas and purge gas
- Arsine (AsH_3), Phosphine (PH_3), and Diborane (B_2H_6) are used as dopant gases.

Epitaxy Silicon Deposition

- Silane process

$$SiH_4 \xrightarrow{\text{Heat (1000 °C)}} Si + H_2$$

Silane — Epi-Si — Hydrogen

- DCS process

$$SiH_2Cl_2 \xrightarrow{\text{Heat (1150 °C)}} Si + 2HCl$$

Silane — Epi-Si — Hydrochloride

Epitaxy Silicon Doping

- N-type Dopant

Heat (1000 °C)

$$AsH_3 \rightarrow As + 3/2\ H_2$$

Arsine — As — Hydrogen

Heat (1000 °C)

$$PH_3 \rightarrow P + 3/2\ H_2$$

Arsine — Phosphorus — Hydrogen

Epitaxy Silicon Doping

- P-type Dopant

$$B_2H_6 \xrightarrow{\text{Heat (1000 °C)}} 2\,B + 3\,H_2$$

Diborane — Boron — Hydrogen

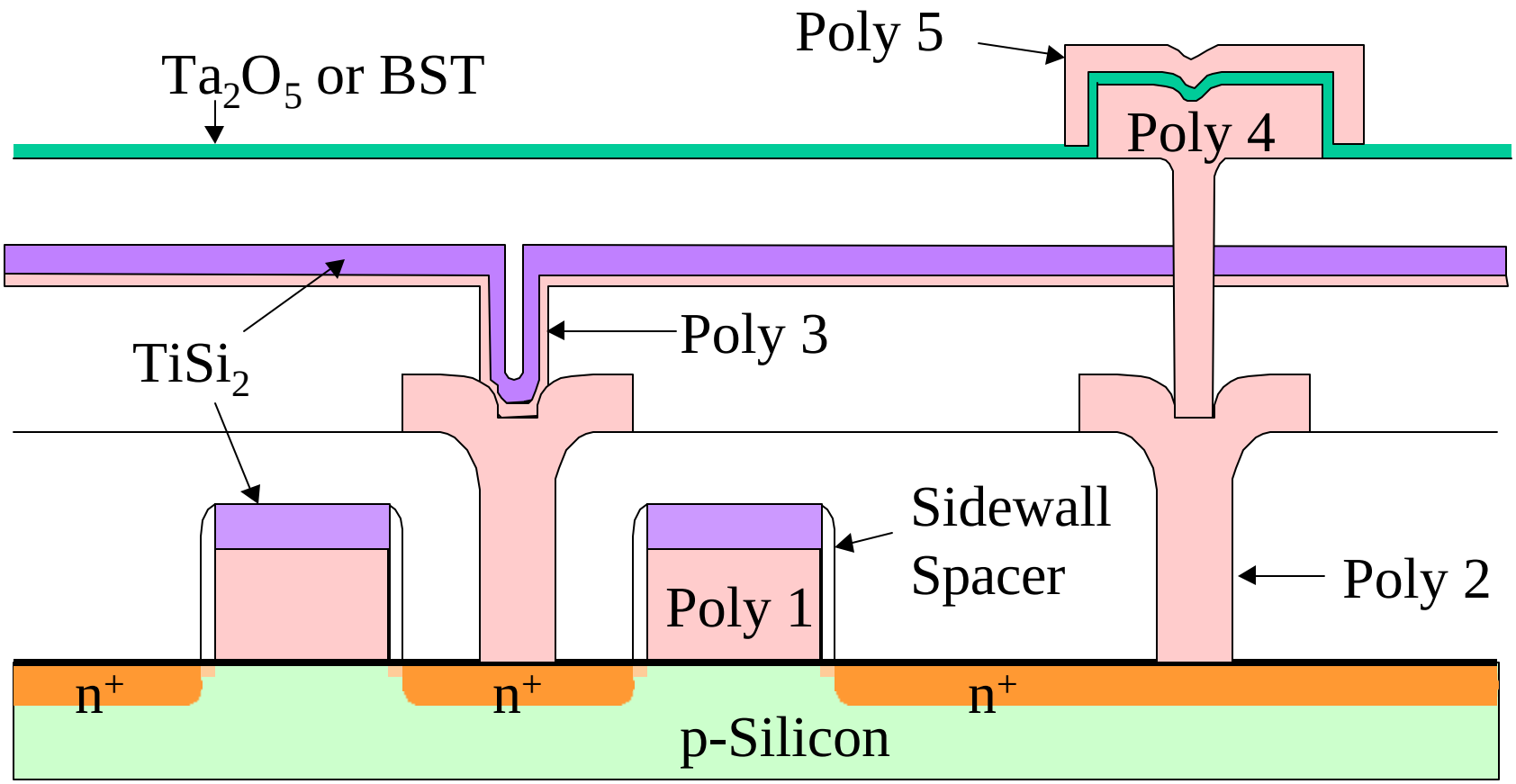
Epitaxy Silicon

- Usually deposited (“grown”) by wafer manufacturer instead by IC fab.
- In fab epi process: special needs such as usually dopant concentration and epi thickness.
- Selective epi for raised source/drain.
- Single wafer epitaxy process.

Polysilicon

- High temperature stability.
- Reasonable good conductivity.
- Widely used for the gate and local interconnection in MOS devices.
- Also widely used as the capacitor electrodes in memory devices, especially DRAM.

Polysilicon Applications in DRAM



Polysilicon

- High temperature (~700 °C) furnace LPCVD processes.
- Silane (SiH_4) or DCS (SiH_2Cl_2) as silicon source gases.
- Nitrogen as purge gas
- Arsine (AsH_3), Phosphine (PH_3), and Diborane (B_2H_6) are used as dopant gases.

Polysilicon Deposition

- Silane process

$$SiH_4 \xrightarrow{\text{Heat (750 °C)}} Si + H_2$$

Silane — Poly-Si — Hydrogen

- DCS process

$$SiH_2Cl_2 \xrightarrow{\text{Heat (750 °C)}} Si + 2HCl$$

Silane — Poly-Si — Hydrochlride

Polysilicon Doping

- N-type Dopant

$$AsH_3 \xrightarrow{\text{Heat (750 °C)}} As + \frac{3}{2} H_2$$

Arsine — As — Hydrogen

$$PH_3 \xrightarrow{\text{Heat (750 °C)}} P + \frac{3}{2} H_2$$

Phosphine — Phosphorus — Hydrogen

Polysilicon Doping

- P-type Dopant

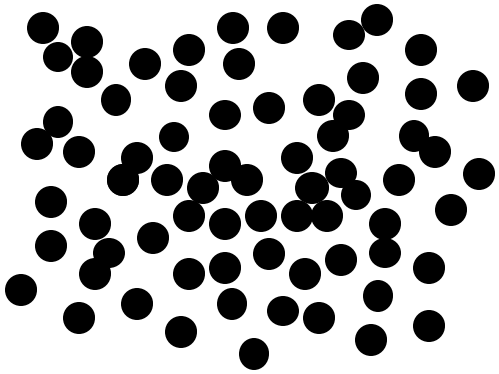
$$B_2H_6 \xrightarrow{\text{Heat (750 °C)}} 2\,B + 3\,H_2$$

Diborane — Boron — Hydrogen

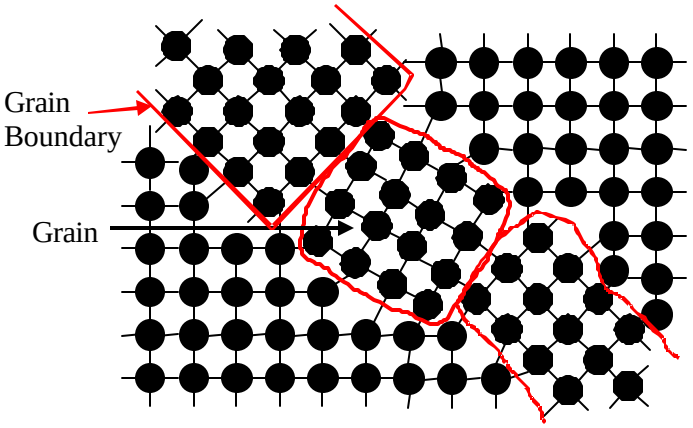
Temperature Relationship of Silane Process

- On single crystal silicon substrate
- Silane as source gases
- T > 900 °C deposit *single crystal silicon*
- 900 °C > T > 550 °C deposit *polysilicon*
- T < 550 °C deposit *amorphous silicon*

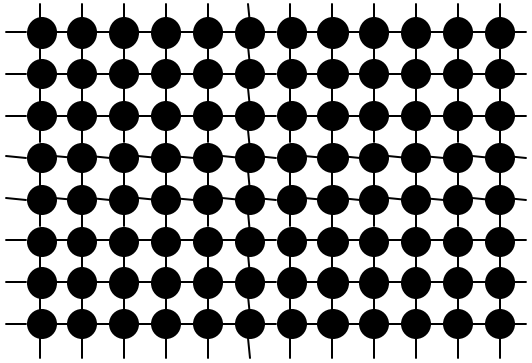
Temperature and Crystal Structure for Silane Processes



T<550 °C
Amorphous Si

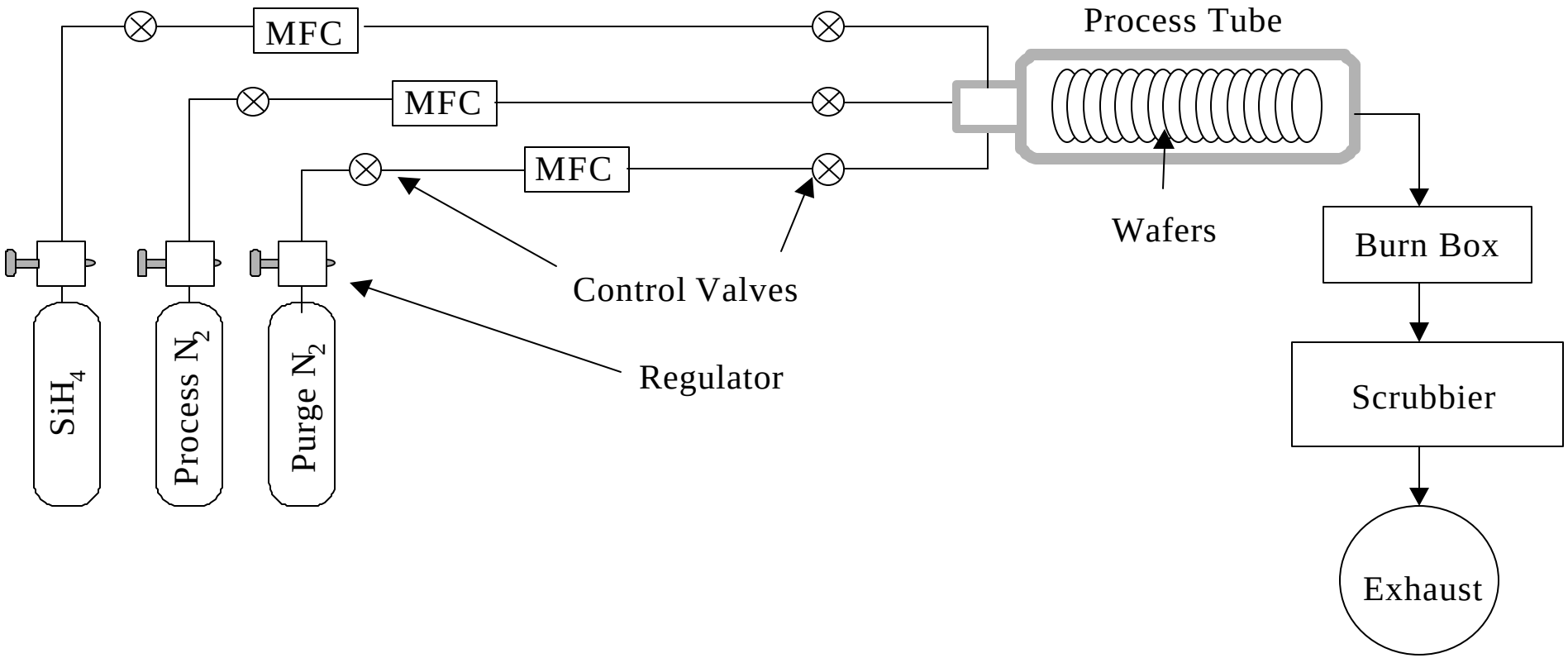


550 °C <T< 900 °C
Polysilicon



T > 900 °C
Single Crystal Si

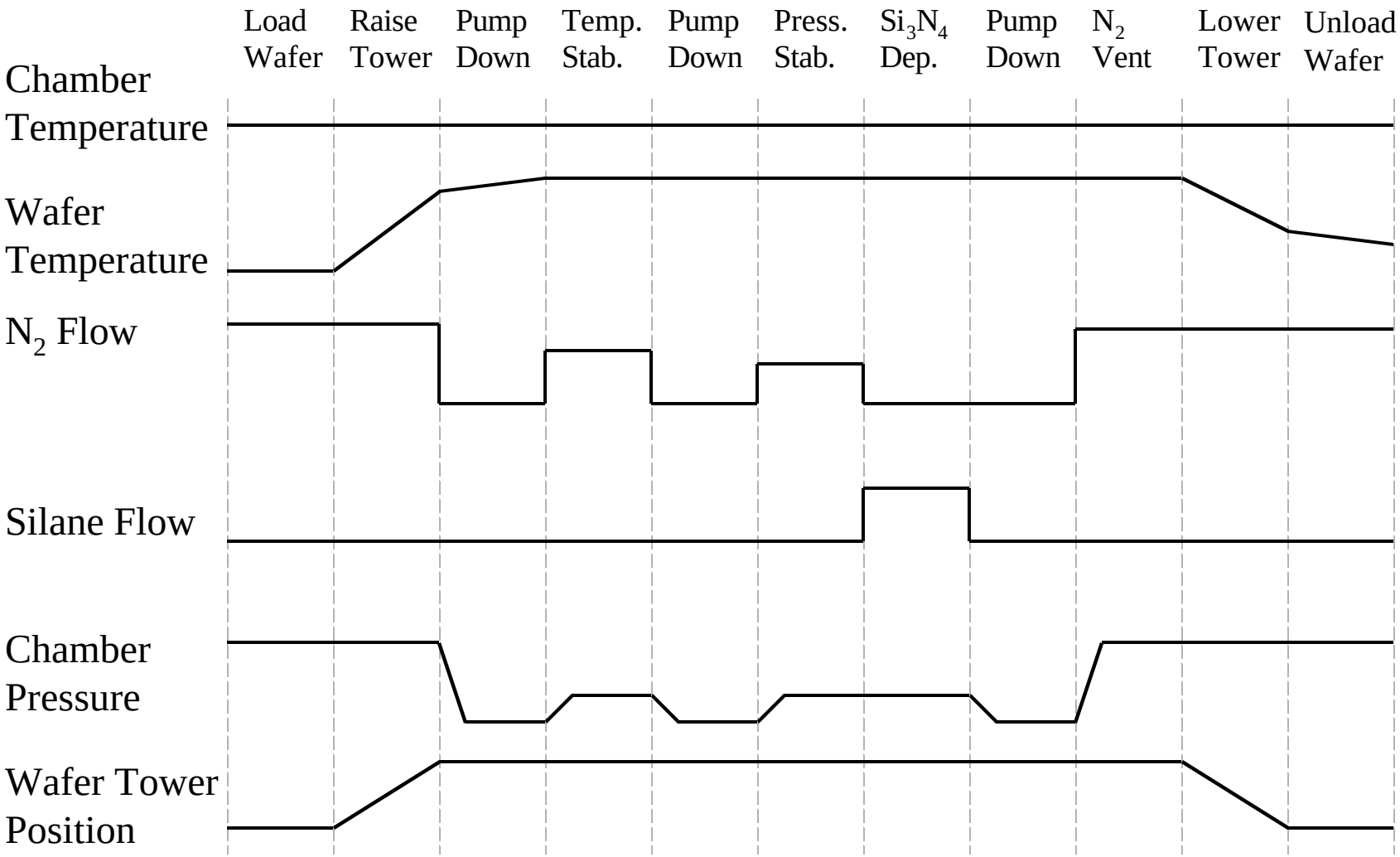
Polysilicon LPCVD System



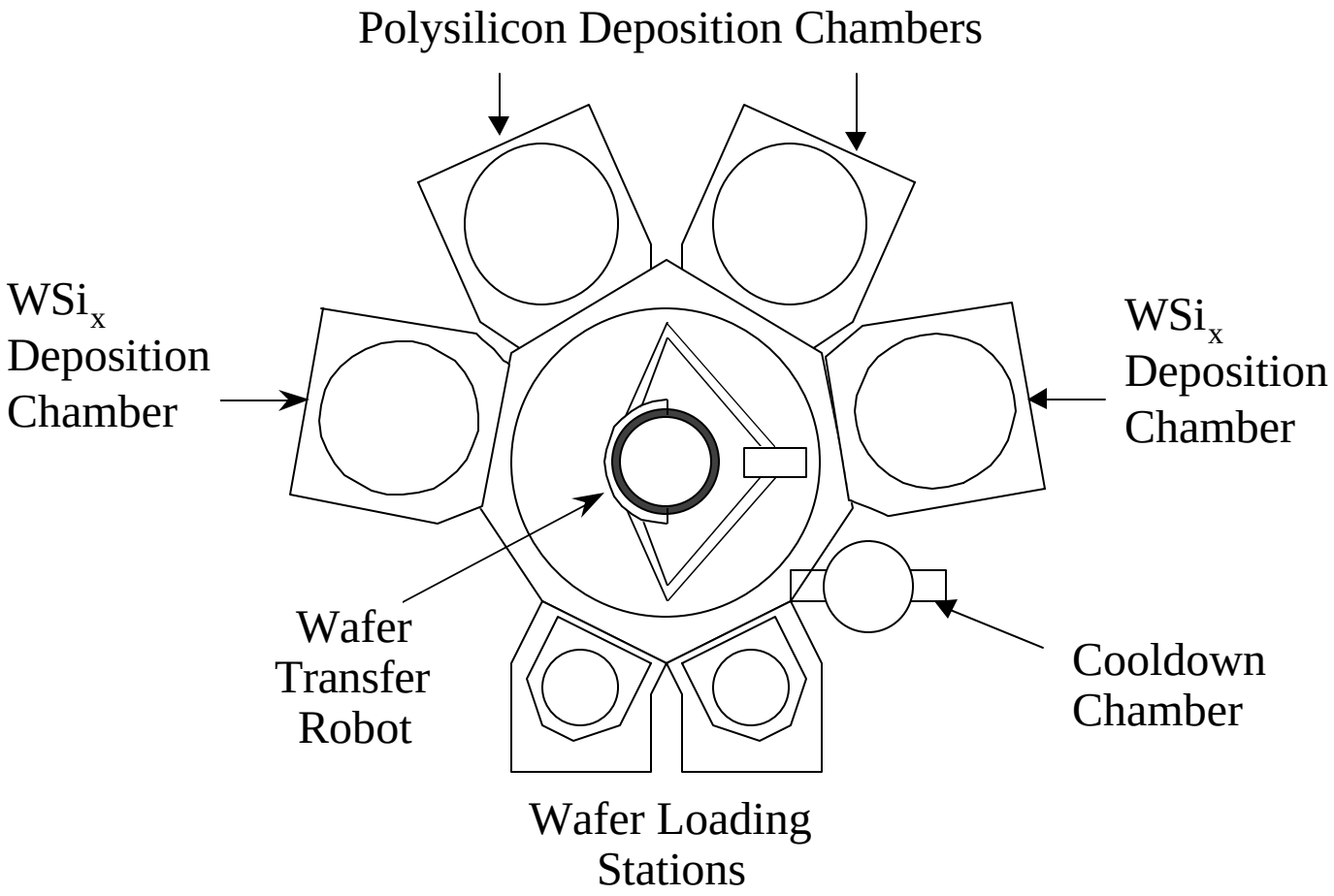
Polysilicon Deposition Process

- Idle with purge N_2 flow
- Idle with process N_2 flow
- Wafer load into tower with process N_2 flow
- Tower raises into process chamber (bell jar) with process N_2 flow
- Pump down chamber to base pressure (< 2 mTorr) by turning-off N_2 flow
- Stabilize wafer temperature with N_2 flow and leak check
- Set up process pressure (~250 mTorr) and with N_2 flow
- Turn-on SiH_4 flow and turn-off N_2, start deposition
- Close gate valve, fill N_2 and ramp-up pressure to atmospheric pressure
- Tower lowed and wafer temperature cooled down, with process N_2 flow
- Unload wafer with process N_2 flow
- Idle with purge N_2 flow

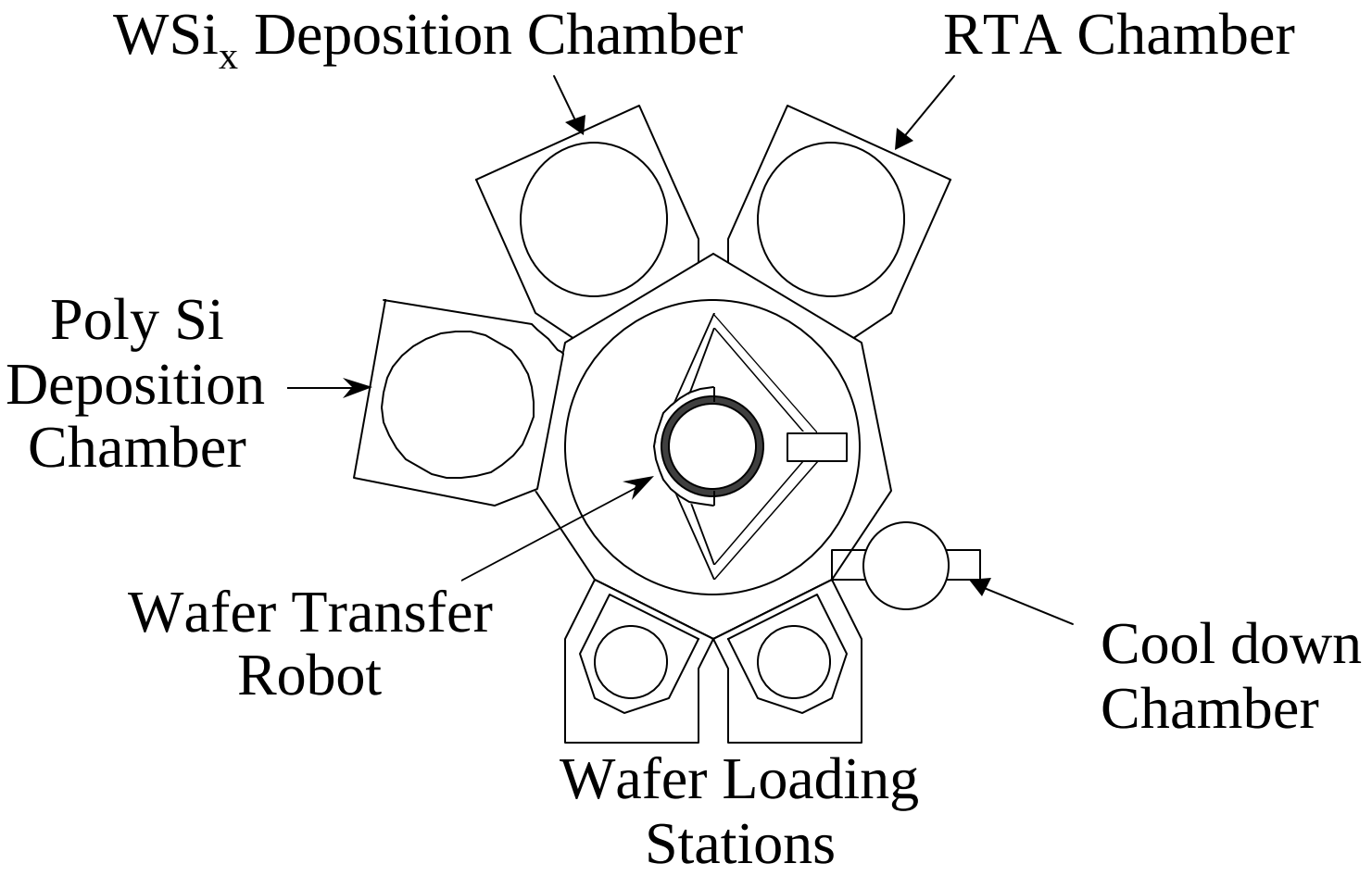
Polysilicon Deposition Process



Polycide Deposition System



Polycide Deposition System



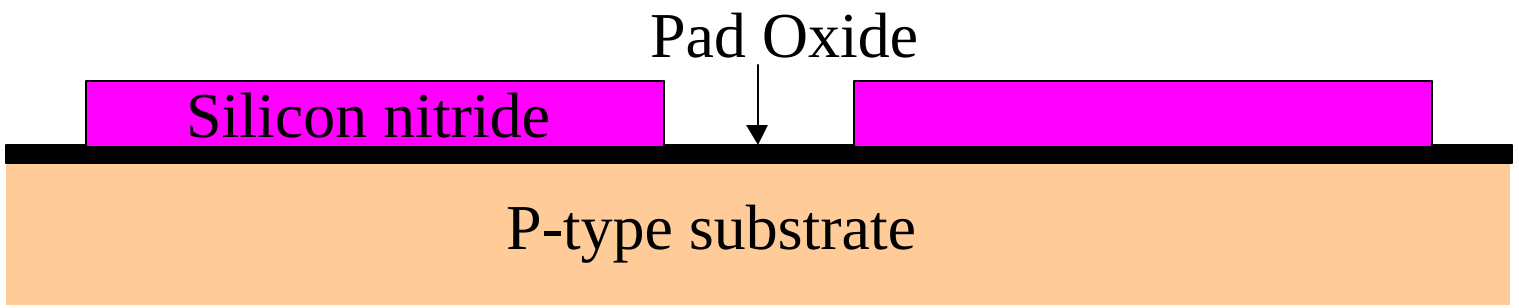
Silicon Nitride

- Dense material
- Widely used as diffusion barrier layer and passivation layer
- LPCVD (front-end) and PECVD (back-end)
- LPCVD nitride usually is deposited in a furnace

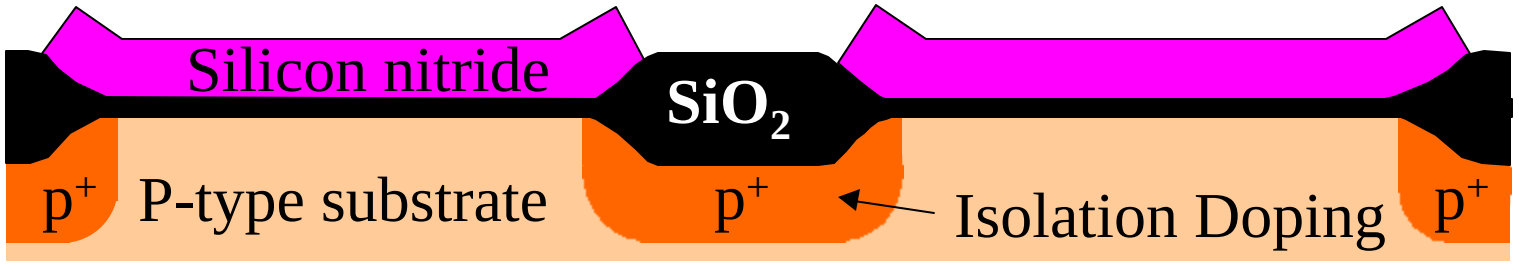
Application of Silicon Nitride

- LOCOS formation as oxygen diffusion barrier
- STI formation as oxide CMP stop
- PMD barrier layer
- Etch stop layer

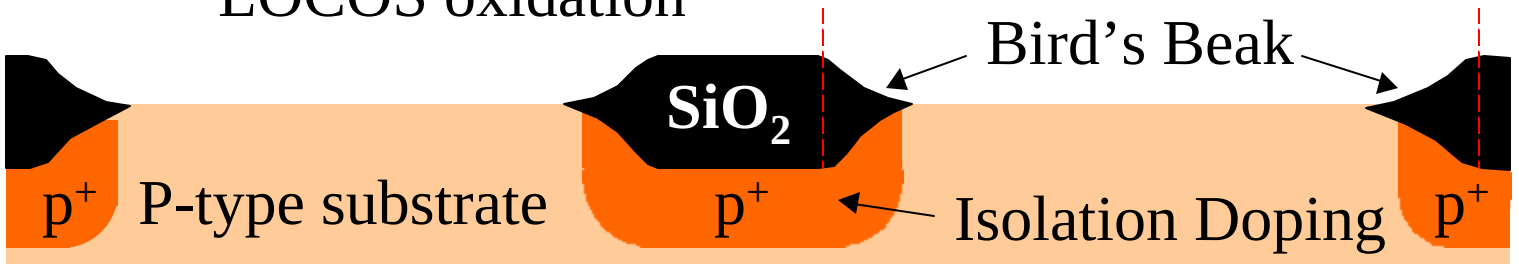
LOCOS Process



Pad oxidation, nitride deposition and patterning

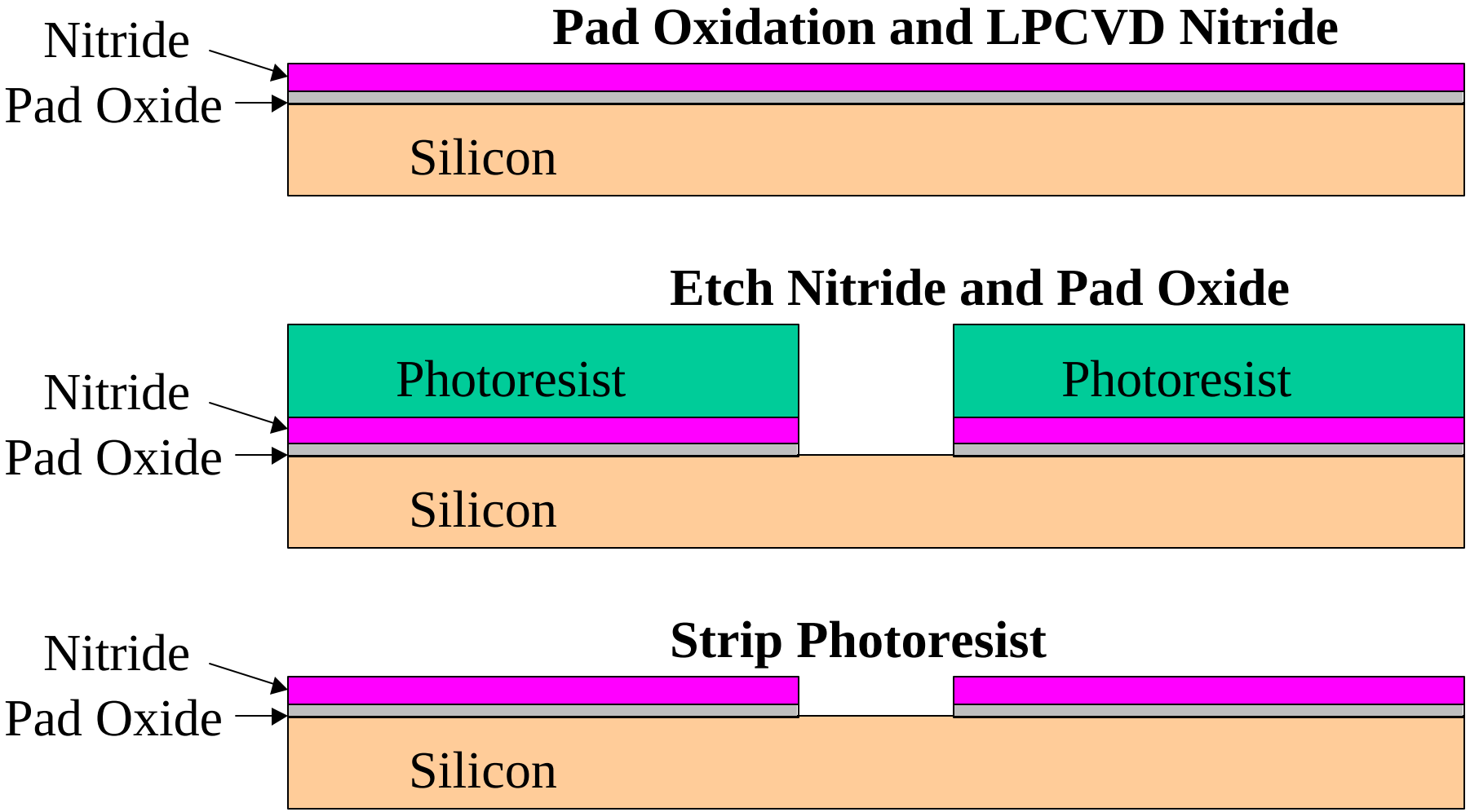


LOCOS oxidation

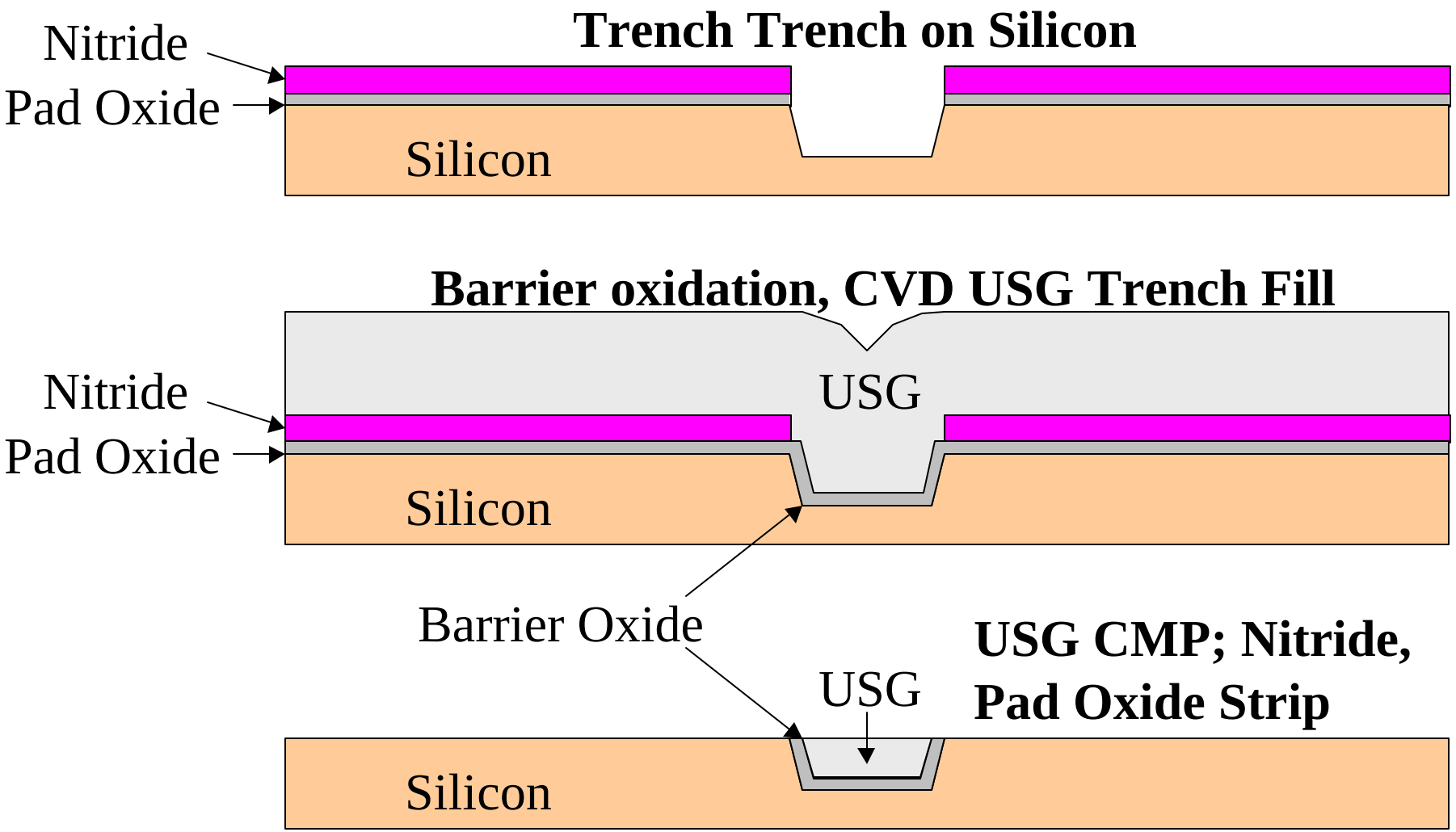


Nitride and pad oxide strip

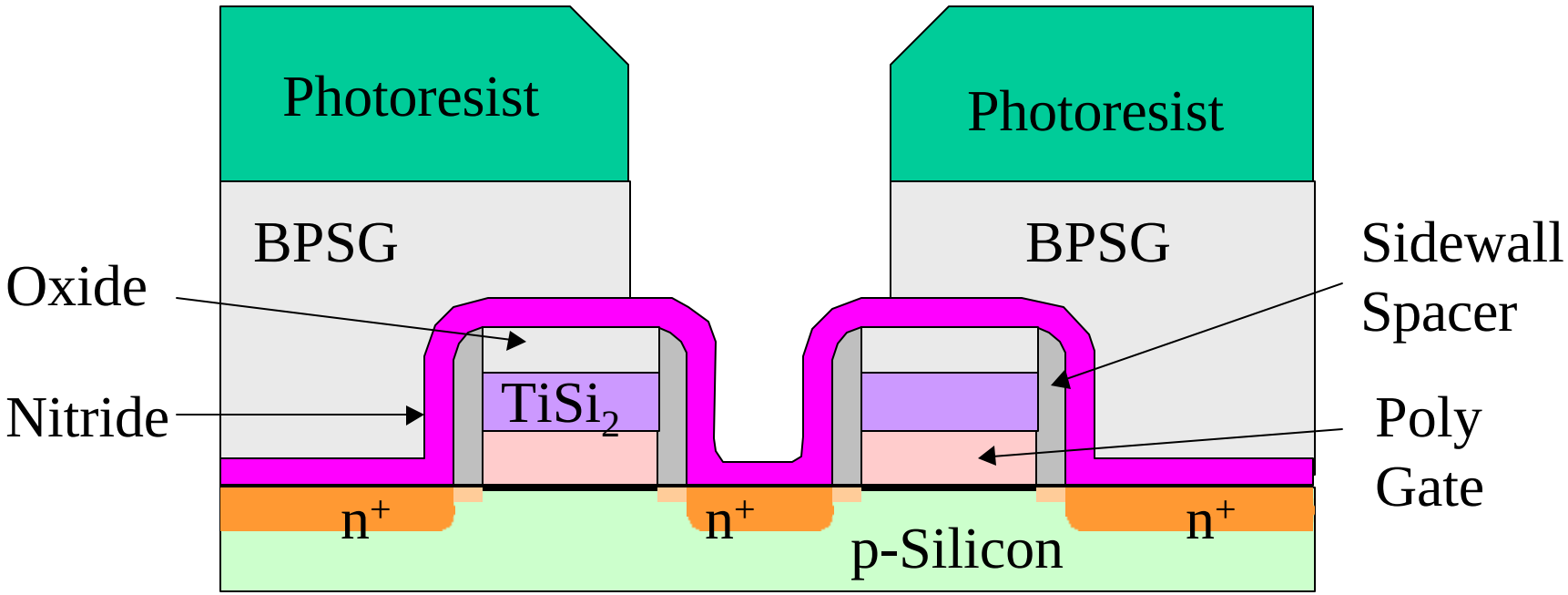
STI Process


Pad Oxidation and LPCVD Nitride
Nitride
Pad Oxide
Silicon
Etch Nitride and Pad Oxide
Photoresist
Photoresist
Nitride
Pad Oxide
Silicon
Strip Photoresist
Nitride
Pad Oxide
Silicon

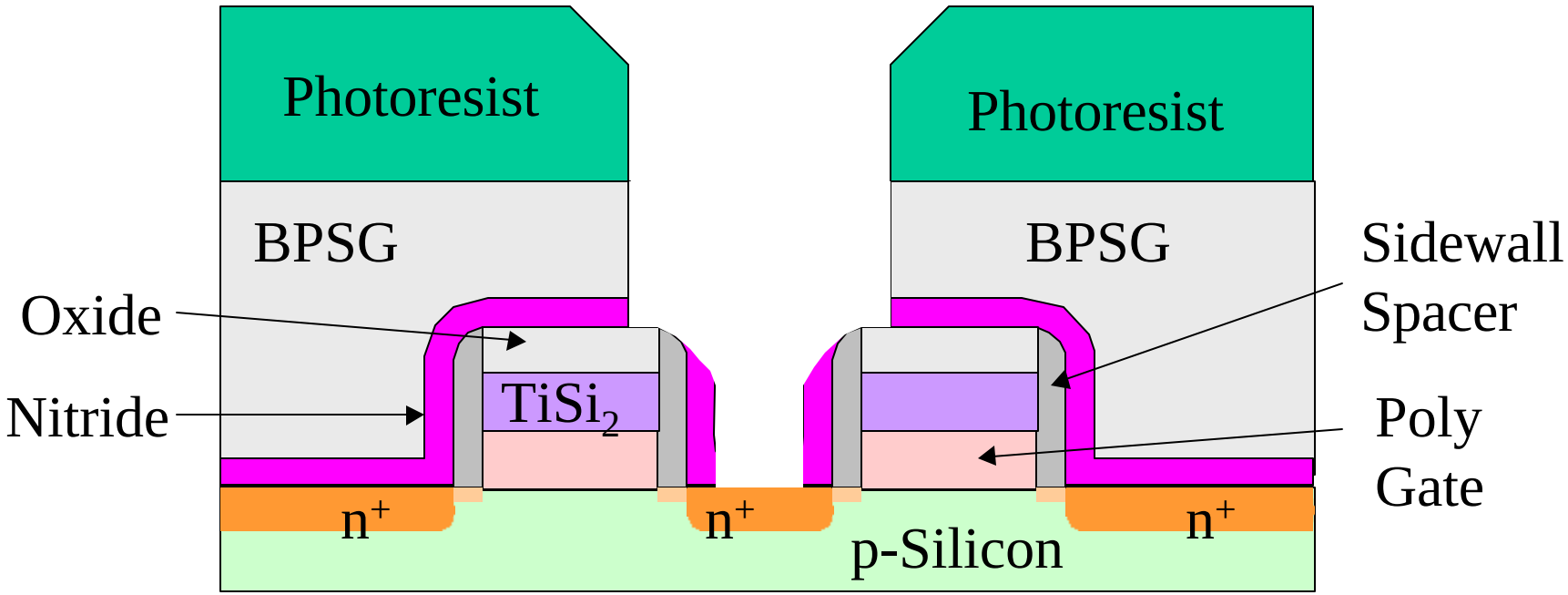
STI Process


Trench Trench on Silicon
Nitride
Pad Oxide
Silicon
Barrier oxidation, CVD USG Trench Fill
Nitride
Pad Oxide
USG
Silicon
Barrier Oxide
USG CMP; Nitride,
Pad Oxide Strip
USG
Silicon

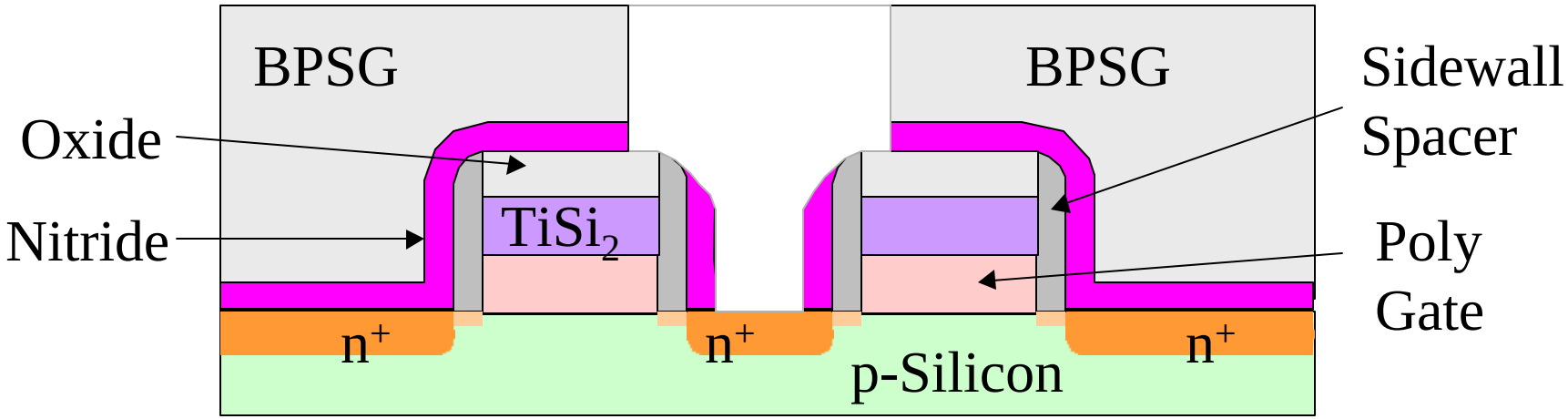
Self-aligned Contact Etch Stop



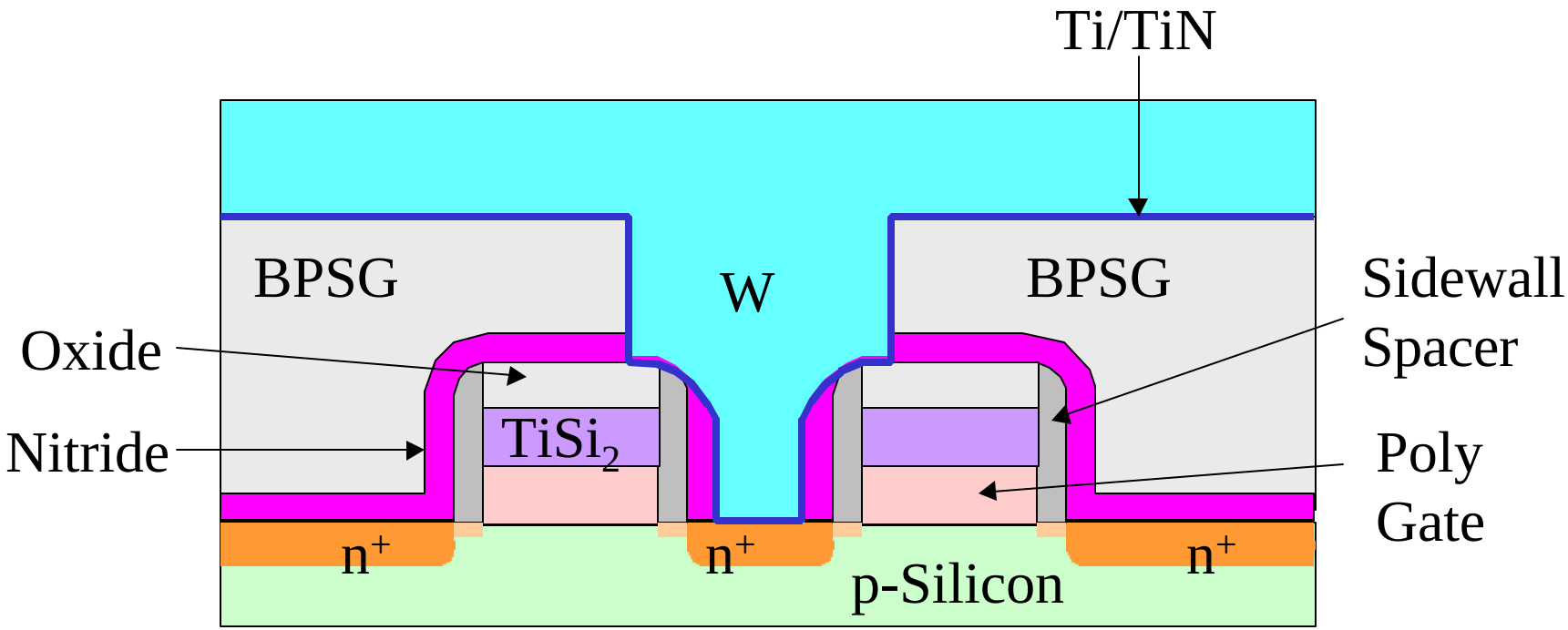
Nitride Breakthrough



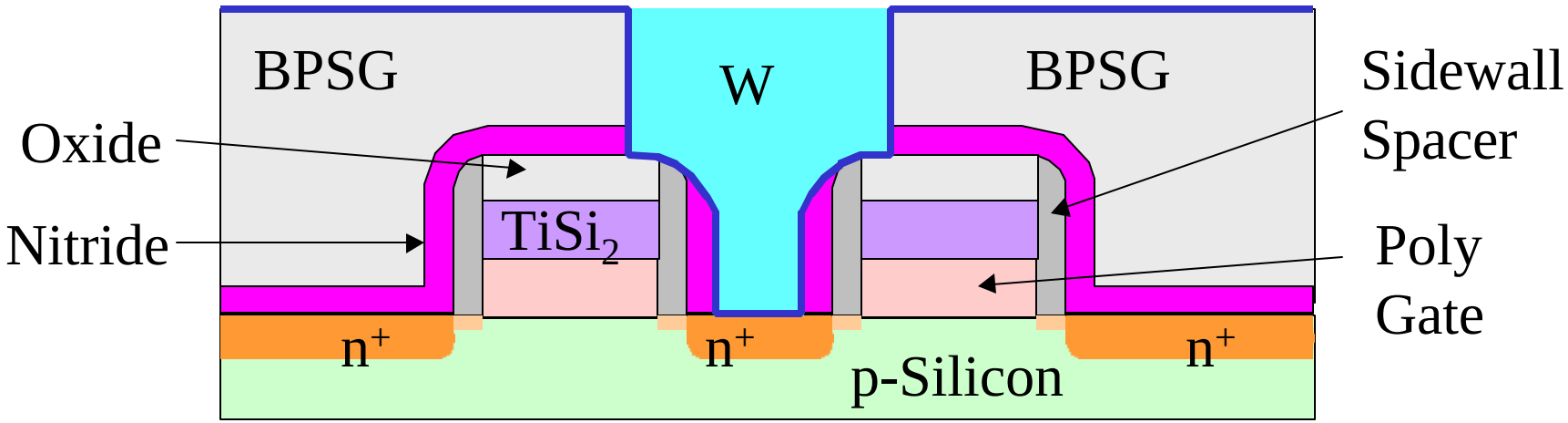
Strip Photoresist



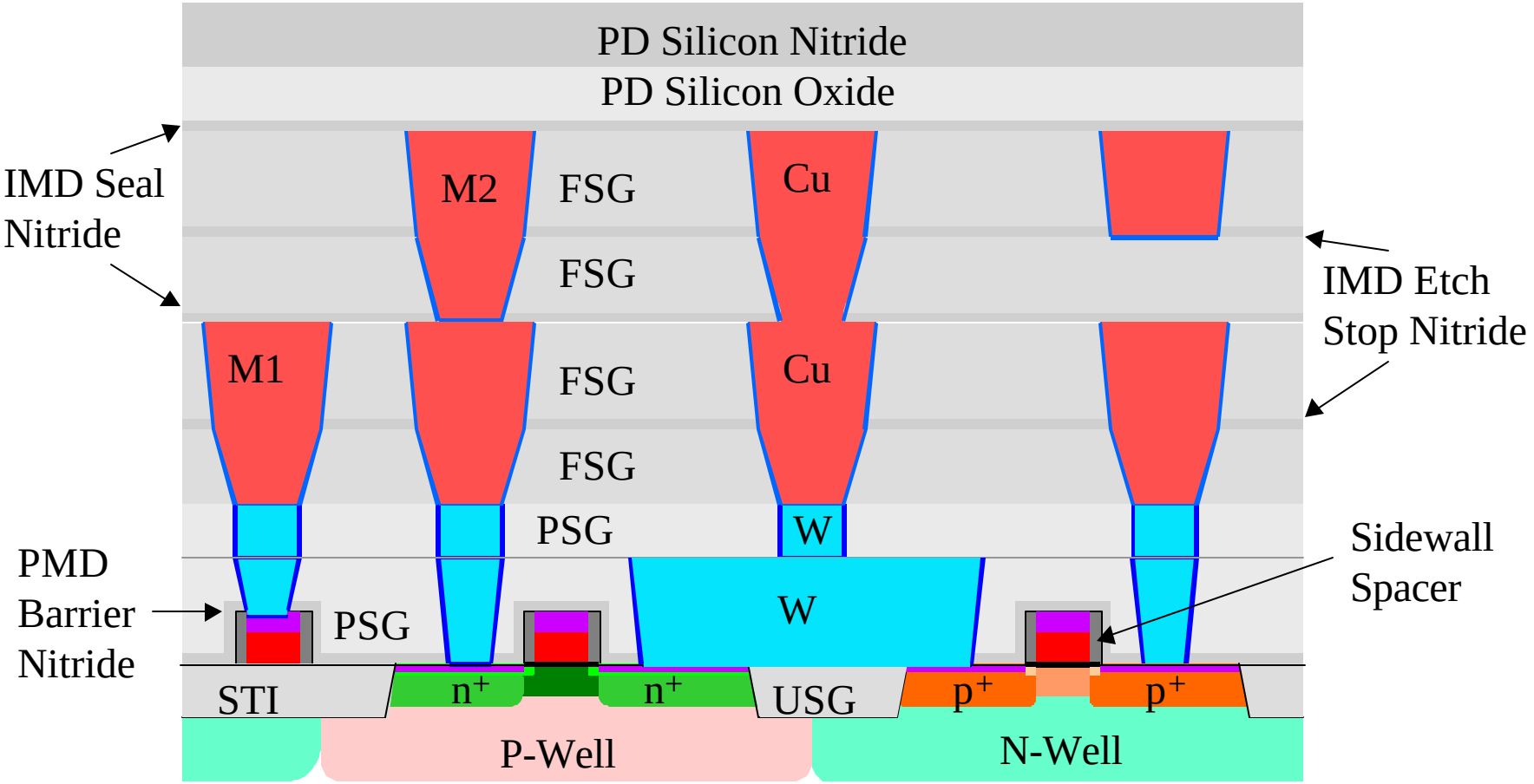
Deposit Ti/TiN and Tungsten



CMP Tungsten and TiN/Ti



Silicon Nitride Applications



Silicon Nitride Deposition

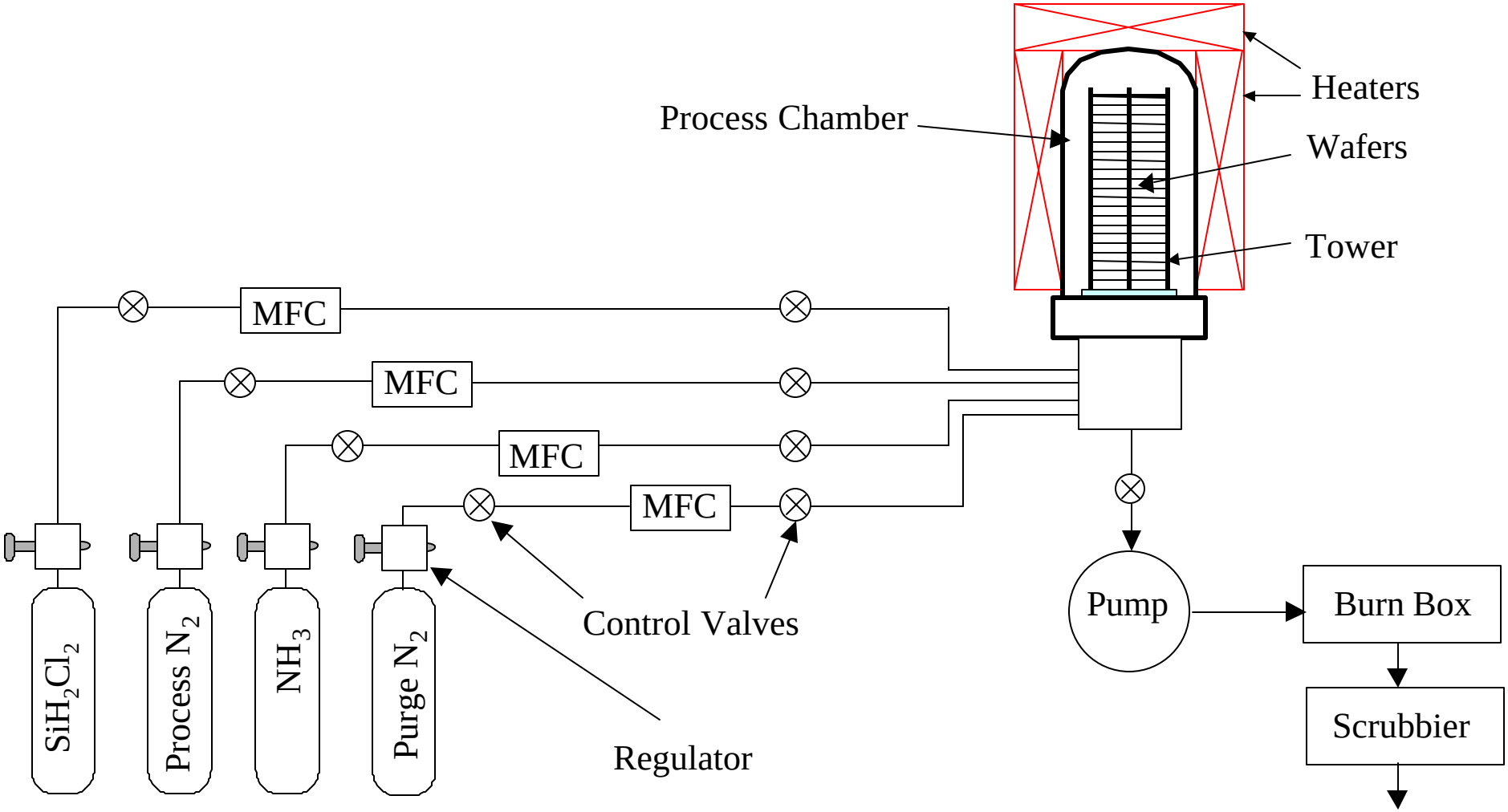
- Silane or DCS as silicon source
- NH_3 as nitrogen source
- N_2 as purge gas

$$3\ SiH_2Cl_2 + 4\ NH_3 \rightarrow Si_3N_4 + 6\ HCl + 6\ H_2$$

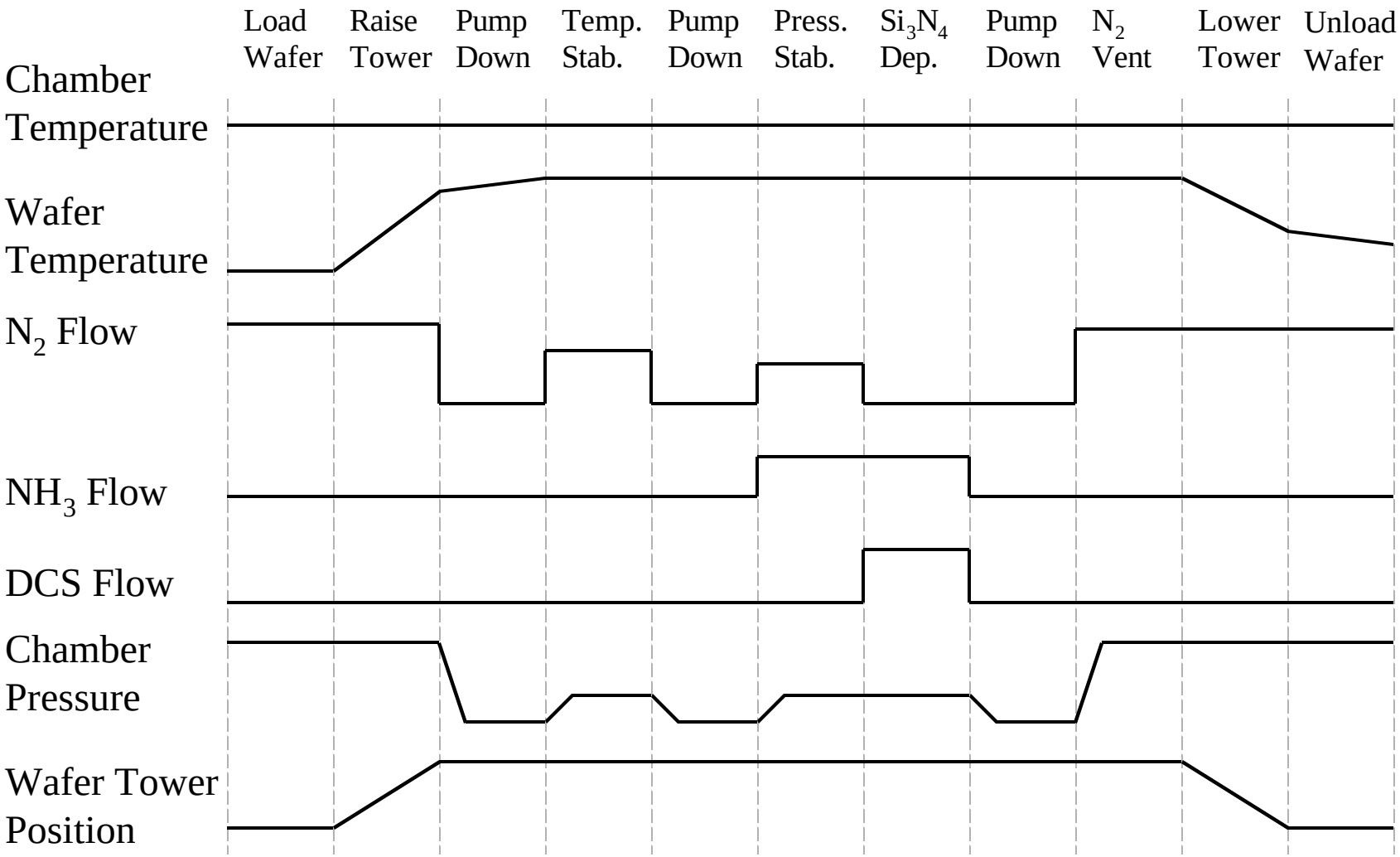
or

$$3\ SiH_4 + 4\ NH_3 \rightarrow Si_3N_4 + 12\ H_2$$

Silicon Nitride LPCVD System



Nitride Deposition Process Sequence



Future Trends of HT-CVD

- More single wafer rapid thermal CVD
- Integrated processes in cluster tools

Summary of Furnace Deposition

- Polysilicon and silicon nitride are the two most commonly film deposited in high temperature furnace
- Silane and DCS are the two most commonly used silicon sources.
- Polysilicon can be doped while deposition by flowing phosphine, arsine or diborane

Rapid Thermal Process

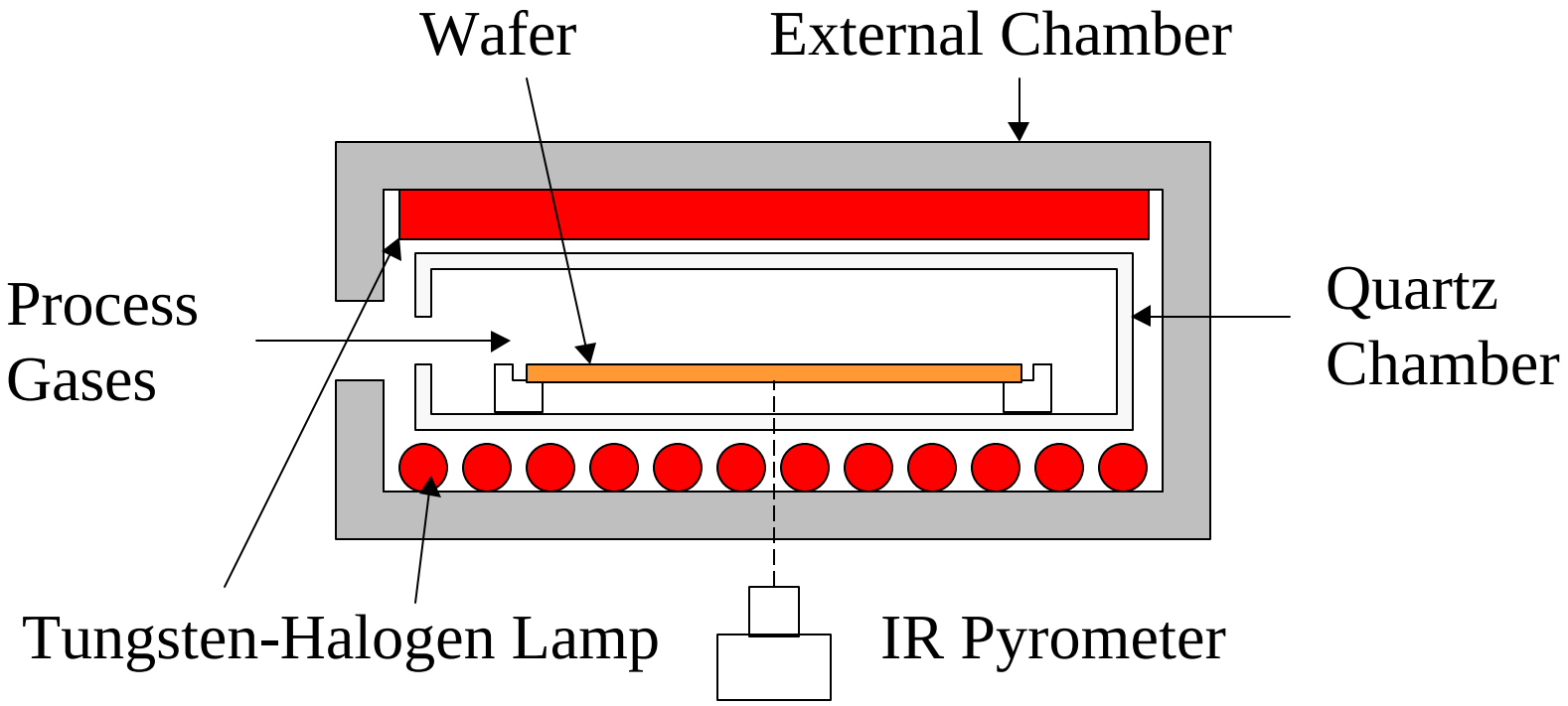
Rapid Thermal Processing (RTP)

- Mainly used for post-implantation rapid thermal anneal (RTA) process.
- Fast temperature ramp-up, 100 to 150 °C/sec compare with 15 °C/min in horizontal furnace.
- Reduce thermal budge and easier process control.

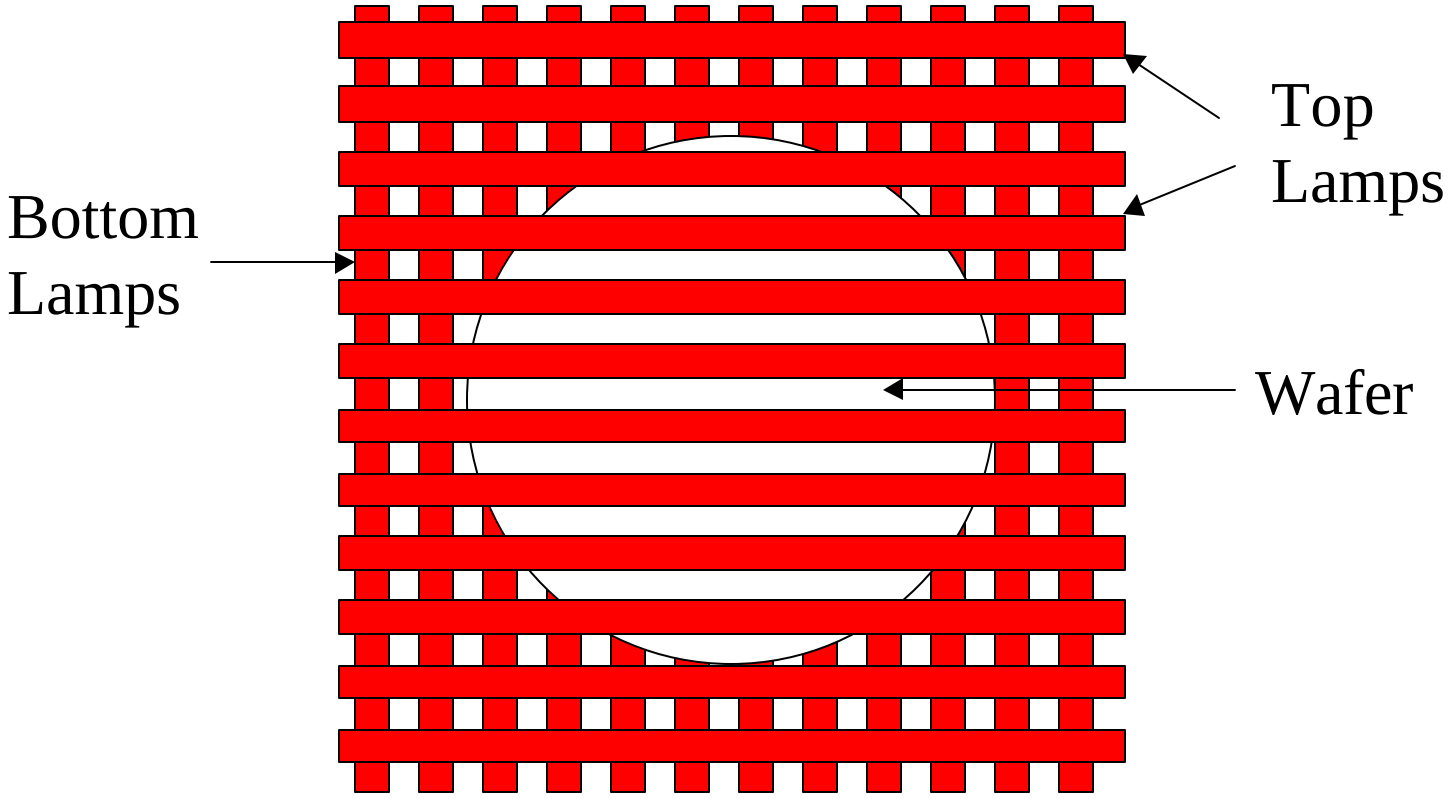
Rapid Thermal Processing (RTP)

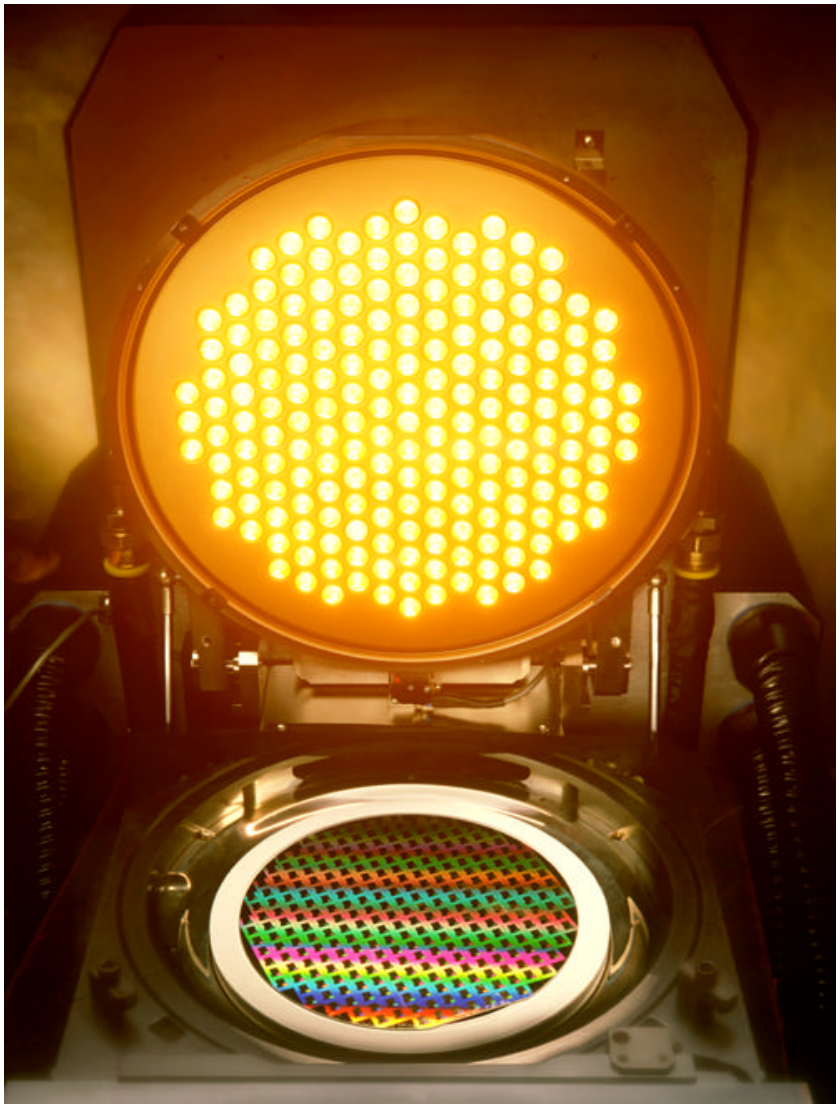
- Single wafer rapid thermal CVD (RTCVD) chamber can be used to deposit polysilicon and silicon nitride.
- RTCVD chamber can be integrated with other process chamber in a cluster tool for in-line process.
- Thin oxide layer (< 40 Å) is likely to be grown with RTO for WTW uniformity control.

Schematic of RTP Chamber



Lamp Array





RTP Chamber

Photo courtesy of
Applied Materials, Inc

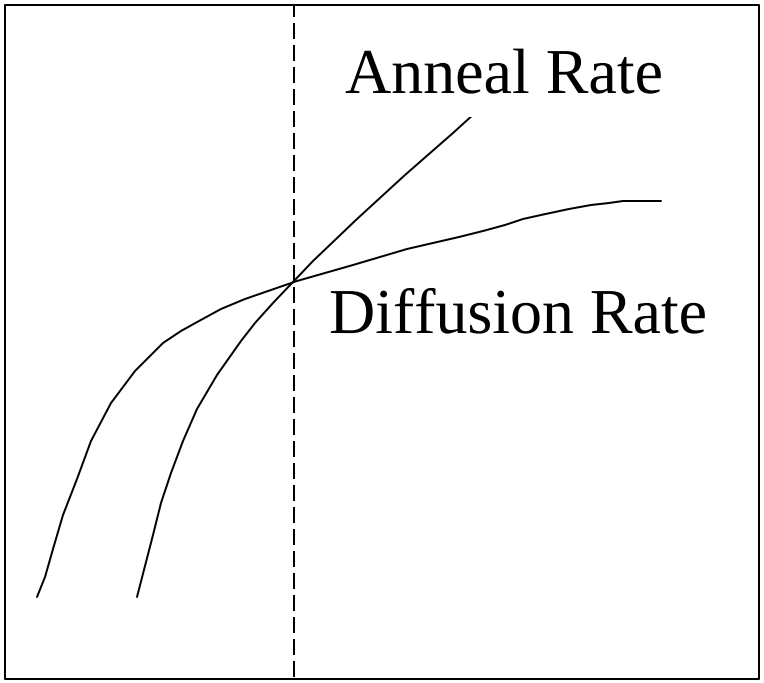
Annealing and Dopant Diffusion

- At higher temperature >1100 °C anneal is faster than diffusion
- Post implantation prefer high temperature and high temperature ramp rate.
- Single wafer rapid thermal process tool has been developed initially for this application

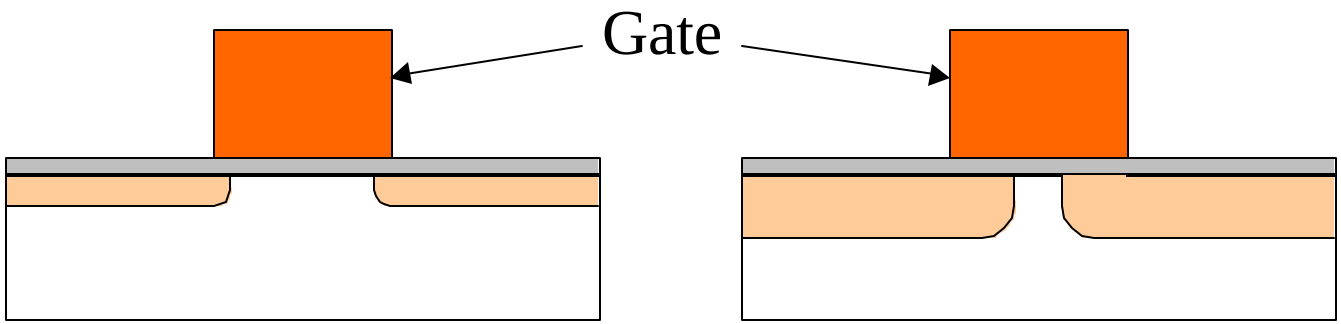
Annealing and Dopant Diffusion

- Dopant atoms diffuse at high temperature
- Furnace has low temperature ramp rate (~10 °C/min) due to large thermal capacity
- Furnace annealing is a long process which causes more dopant diffusion
- Wafer at one end gets more anneal than wafer at another end

Anneal Rate and Diffusion Rate



Dopant Diffusion After Anneal

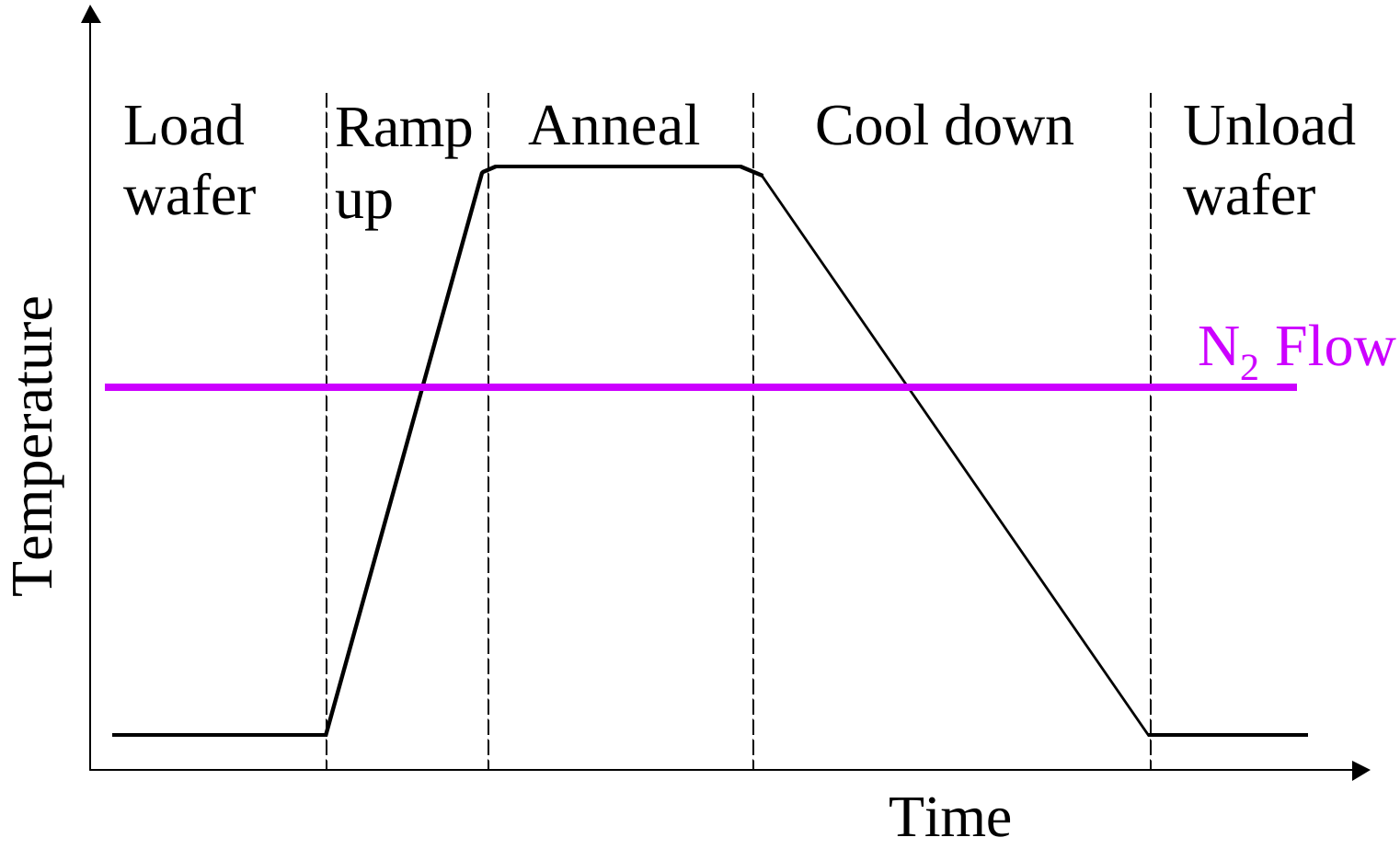


RTA Furnace anneal

Advantage of RTP over Furnace

- Much faster ramp rate (75 to 150 °C/sec)
- Higher temperature (up to 1200 °C)
- Faster process
- Minimize the dopant diffusion
- Better control of thermal budget
- Better wafer to wafer uniformity control

RTP Temperature Change

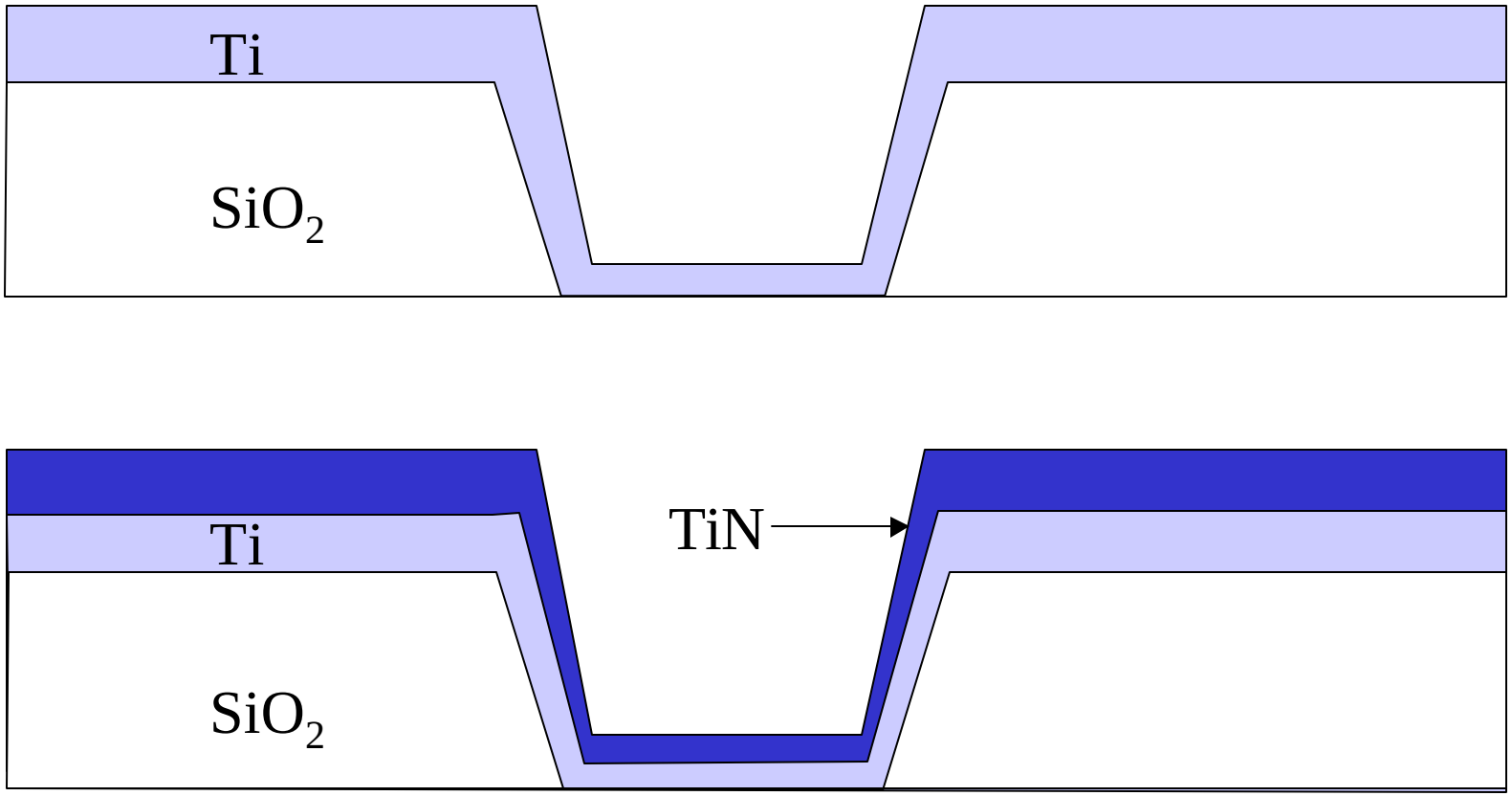


Thermal Nitridization

- Titanium PVD
- Thermal nitridization with NH_3

$$NH_3 + Ti \rightarrow TiN + 3/2\ H_2$$

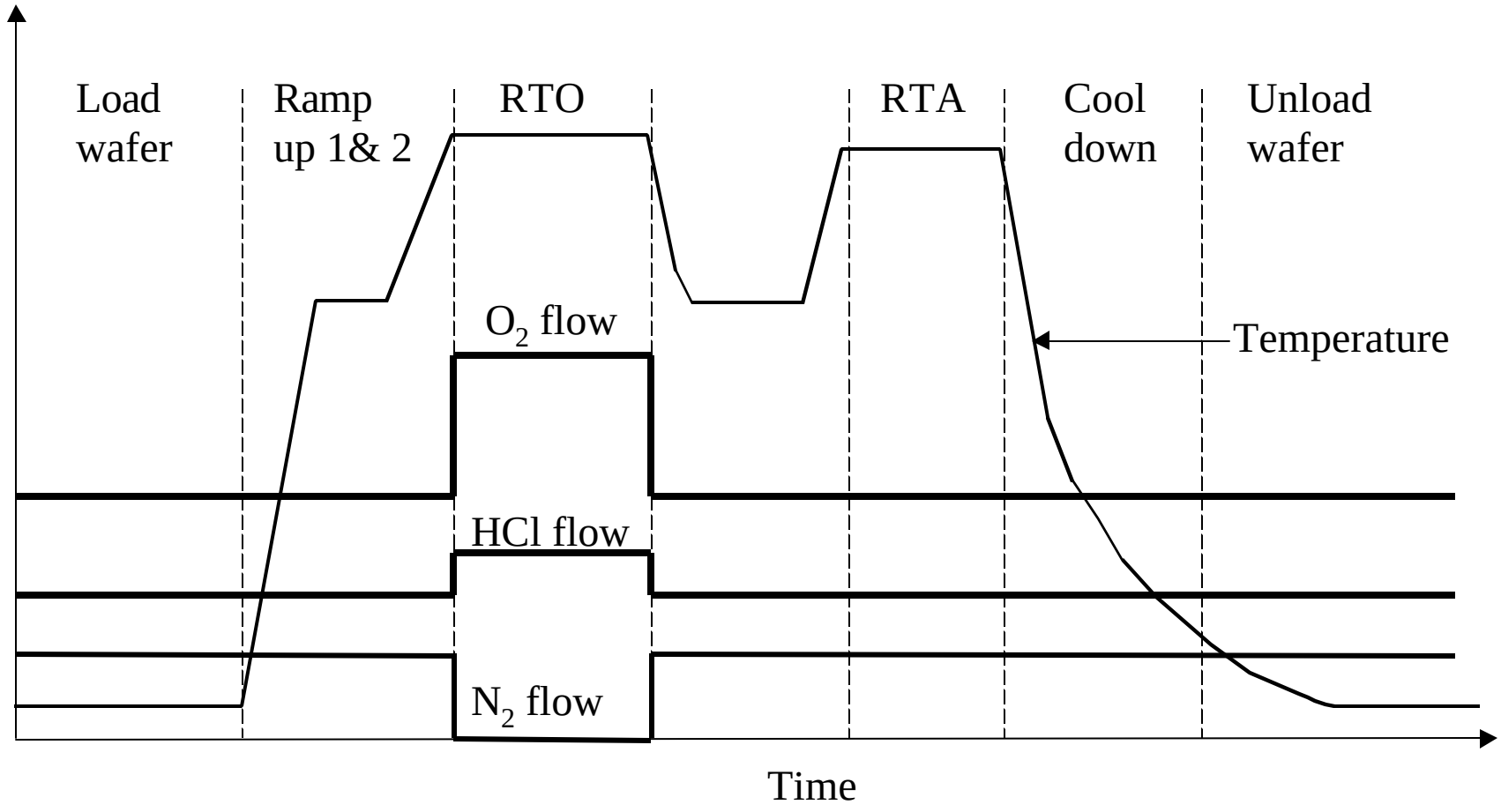
Titanium Nitridization



RTO Process

- Ultra thin silicon dioxide layer < 30Å
- Better WTW uniformity
- Better thermal budget control

RTP Process Diagram

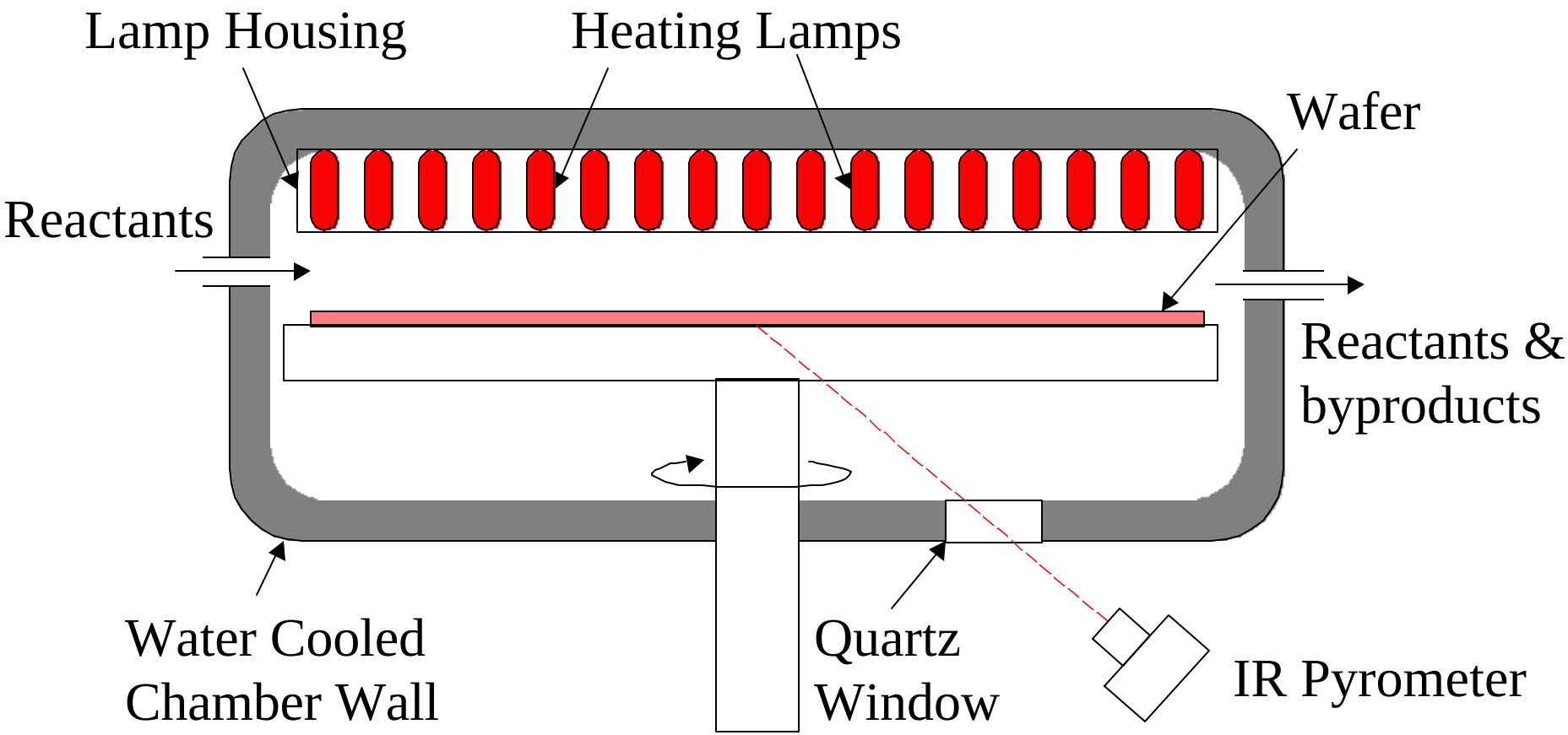


Future Tends

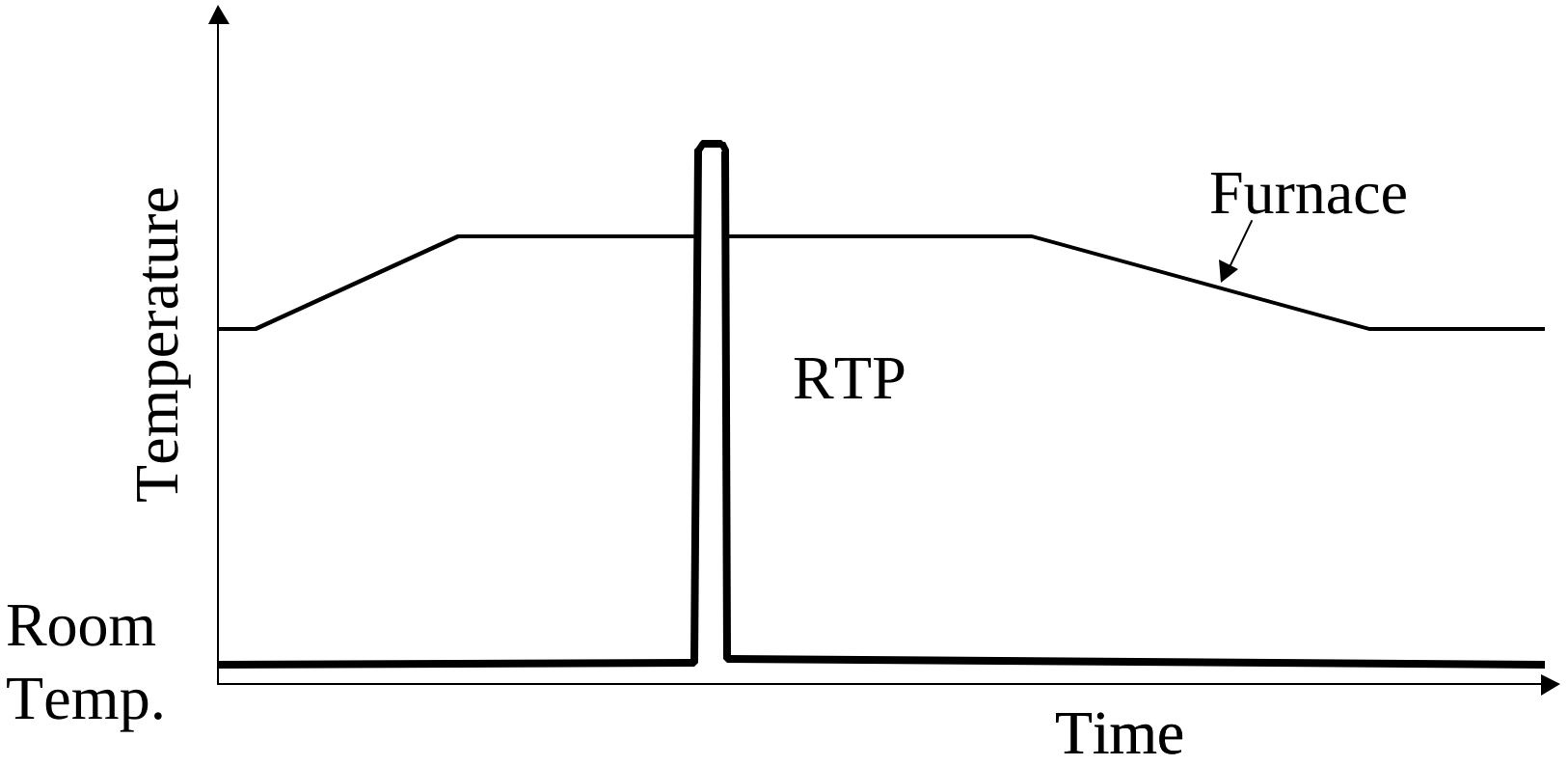
- Rapid thermal process (RTP)
- In-situ process monitoring
- Cluster tools

- Furnace will still be used

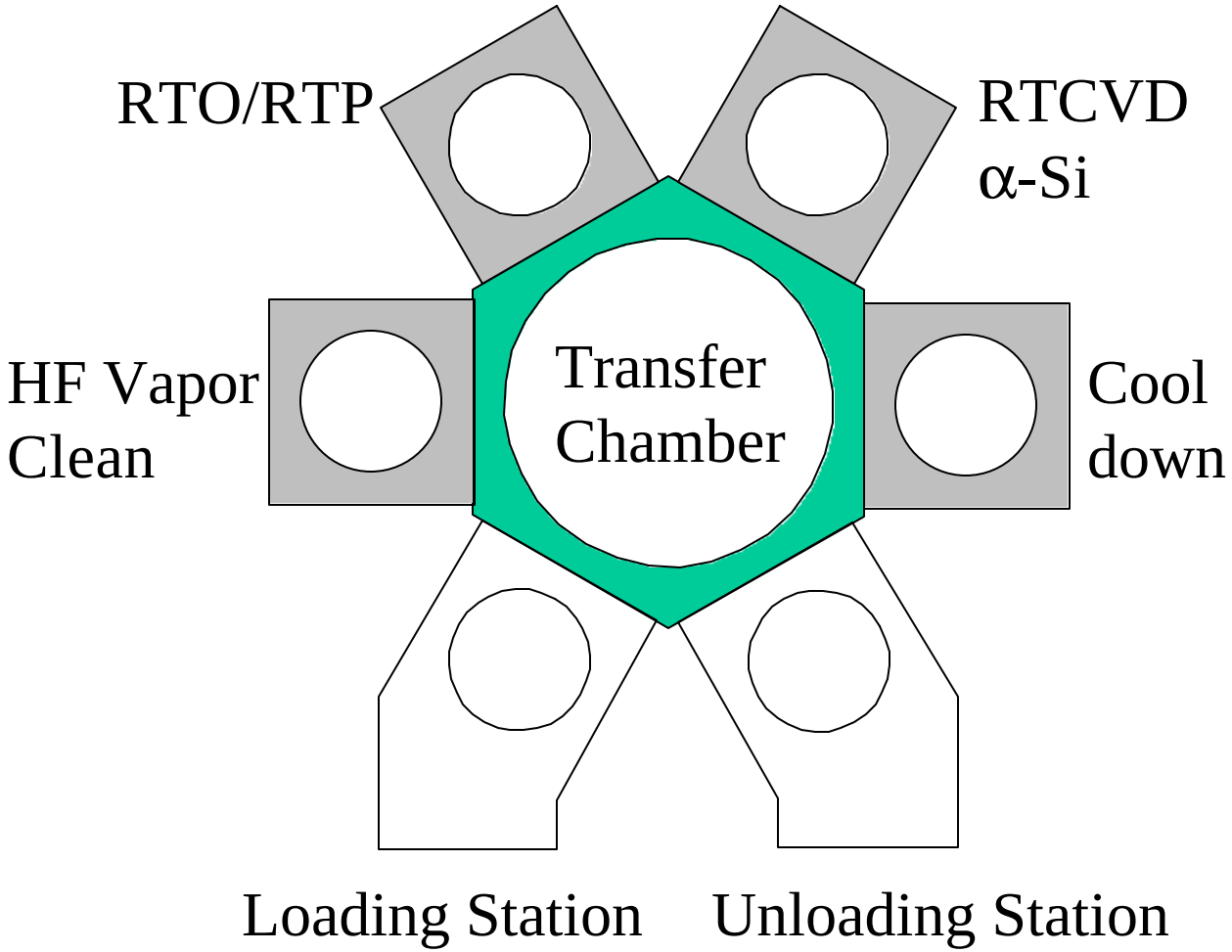
RTCVD Chamber



Temperature of RTP & Furnace



Cluster Tool



Summary of RTP

- Fast
- Better process control
  - Thermal budget
  - Wafer to wafer uniformity
- Minimized dopant diffusion
- Cluster tool, easy process integration

Summary of Thermal Process

- Oxidation, diffusion, annealing, and deposition
- Wet oxidation is faster, dry oxidation has better film quality. Advanced fab: mainly dry oxidation.
- Diffusion doping with oxide mask, used in lab
- LPCVD polysilicon and front-end silicon nitride
- Annealing recovers crystal and activates dopants
- RTP: better control, faster and less diffusion
- Furnaces: high throughput and low cost, will continue to be used in the future fabs