Chapter 5
Thermal Processes

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Objective

- List four thermal processes
- Describe thermal process in IC fabrication
- Describe thermal oxidation process
- Explain the advantage of RTP over furnace
- Relate your job or products to the processes
Topics

• Introduction
• Hardware
• Oxidation
• Diffusion
• Annealing
  – Post-Implantation
  – Alloying
  – Reflow
• High Temp CVD
  – Epi
  – Poly
  – Silicon Nitride
• RTP
  – RTA
  – RTP
• Future Trends
Definition

• Thermal processes are the processes operate at high temperature, which is usually higher than melting point of aluminum.

• They are performed in the front-end of the semiconductor process, usually in high temperature furnace commonly called diffusion furnace.
Introduction

• Advantages of Silicon
  – Abundant, cheap
  – Stable and useful oxide

• Oxidation and Diffusion are the backbone processes in early IC fabrications
Thermal Processes in IC Fabrication
Hardware Overview
Horizontal Furnace

- Commonly used tool for thermal processes
- Often be called as *diffusion furnace*
- Quartz tube inside a ceramic liner called muffle
- Multi-tube system
Layout of a Horizontal Furnace
Control System
Gas Deliver System

Gas cylinders

Control Valve

Regulator

To Process Tube

MFC

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Source Cabinet

- Source Gases
  - Oxygen
  - Water Vapor
  - Nitrogen
  - Hydrogen
- Gas control panel
- Gas flow controller
- Gas flow meter
Oxidation Sources

- Dry Oxygen
- Water vapor sources
  - Bubblers
  - Flash systems
- Hydrogen and oxygen, $\text{H}_2 + \text{O}_2 \rightarrow \text{H}_2\text{O}$
- Chlorine sources, for minimized mobile ions in gate oxidation
  - Anhydrous hydrogen chloride HCl
  - Trichloroethylene (TCE), Trichloroethane (TCA)
Diffusion Sources

• P-type dopant
  – B$_2$H$_6$, burnt chocolate, sickly sweet odor
  – Poisonous, flammable, and explosive

• N-type dopants
  – PH$_3$, rotten fish smell
  – AsH$_3$, garlic smell
  – Poisonous, flammable, and explosive

• Purge gas
  – N$_2$
Deposition Sources

- Silicon source for poly and nitride deposition:
  - Silane, $\text{SiH}_4$, pyrophoric, toxic and explosive
  - DCS, $\text{SiH}_2\text{Cl}_2$, extremely flammable

- Nitrogen source for nitride deposition:
  - $\text{NH}_3$, pungent, irritating odor, corrosive

- Dopants for polysilicon deposition
  - $\text{B}_2\text{H}_6$, $\text{PH}_3$ and $\text{AsH}_3$

- Purge gas
  - $\text{N}_2$
Anneal Sources

- High purity N$_2$, is used for most anneal processes.
- H$_2$O sometimes used as ambient for PSG or BPSG reflow.
- O$_2$ is used for USG anneal after USG CMP in STI formation process.
- Lower grade N$_2$ is used for idle purge.
Exhaust System

• Removal of hazardous gases before release
• Poisonous, flammable, explosive and corrosive gases.
• Burn box removes most poisonous, flammable and explosive gases
• Scrubber removes burned oxide and corrosive gases with water.
• Treated gases exhaust to the atmosphere.
Wafer Loading, Horizontal System

Process gases → Wafers in Process Tube → Wafer Boat → Paddle → To Exhaust
Wafer Loading, Vertical System

Wafers

Susceptor

Tower
Temperature Control

- Thermal processes are very sensitive to the temperature
- Precisely temperature control is vital
- $\pm 0.5 \, ^\circ C$ at central zone
- $\pm 0.05\%$ at 1000 $^\circ C$!
Temperature Control System

- Thermocouples touching the reaction tube
- Proportional band controllers feed the power to the heating coils
- The heating power is proportional to difference between setting point and measured value
Reaction Chamber

• High-purity Quartz
  – Stability at high temperature
  – Basic Cleanliness

• Drawback
  – Fragility
  – Some metallic ions
  – Not a sodium barrier
  – Small flakes at > 1200 °C, devitrification
Horizontal Furnace

- **Quartz Tube**
- **Heating Coils**
- **Wafers**
- **Gas flow**

Temperature:
- **Center Zone**
- **Flat Zone**

Distance
Vertical Furnace, Process Position

Process Chamber

Wafers

Susceptor

Heaters

Tower
Quartz Tube

- Electric Fused
- Flame Fused
- Both of them as trace amount of metals
- Flame-fused tubes produced devices have better characteristics.
Quartz Tube Clean

- Very important especially for deposition furnace to prevent particle contamination

- Outside fab, ex-situ
  - Hydrofluoric acid (HF) tank
  - Remove a thin layer of quartz every time
  - Limited tube lifetime

- In-situ clean
  - Plasma generator inside tube
  - Free fluorine from NF₃ etch away contaminant
Silicon Carbide Tube

• Pro
  – Higher thermal stability
  – Better metallic ion barrier

• Con
  – Heavier
  – More expensive
Temperature Control
Anti-Warp Methods

• Ramping
  – Load wafer slowly at a lower temperature (idle temperature, ~ 800 °C)
  – Ramp temperature to process point after a short stabilization period

• Slow loading
  – 1 inch/min
  – thermal capacity of 200 six-inch wafers can drop temperature as much as 50 °C
Horizontal Furnace

• Contain 3 or 4 tubes (reaction chambers)
• Separate temperature control system for each tube
Horizontal Furnace

- Heating Coils
- Quartz Tube
- Wafers
- Gas flow
- Temperature
- Center Zone
- Flat Zone
- Distance
Furnace

- Wafer Clean Station
- Wafer Loading Station
  - Manual wafer loading
  - Automatic wafer loading
- Oxidation Process Automation
Vertical Furnaces

• Place the process tube in vertical direction
• Smaller footprint
• Better contamination control
• Better wafer handling
• Lower maintenance cost and higher uptime
Vertical Furnace, Loading and Unloading Position
Smaller Footprint

- Clean room footage becomes very expensive
- Small footprint reduces cost of ownership (COO)
Better Contamination Control

- Gas flow from top to bottom
- Better uniformity for Laminar gas flow control
- Particles has less chance to fall at the center of the wafers
Better Wafer Handling

• High torque on paddle of horizontal when it handle large amount of large diameter wafers

• Zero torque for wafer tower in vertical system
Summery of Hardware

• Furnaces are commonly used in thermal processes.
• Furnaces usually consist of a control system, gas delivery system, process tube or chamber, wafer loading system, and exhaust system.
• Vertical furnace is more widely used due to its smaller footprint, better contamination control, and lower maintenance.
• Precise temperature and its uniformity are vital for the success of the thermal processes.
Oxidation
Oxidation

- Introduction
- Applications
- Mechanism
- Process
- System
- RTO
Introduction

- Silicon reacts with oxygen
- Stable oxide compound
- Widely used in IC manufacturing

\[ \text{Si} + \text{O}_2 \rightarrow \text{SiO}_2 \]
Oxidation
# Some Facts About Silicon

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Silicon</td>
</tr>
<tr>
<td>Symbol</td>
<td>Si</td>
</tr>
<tr>
<td>Atomic number</td>
<td>14</td>
</tr>
<tr>
<td>Atomic weight</td>
<td>28.0855</td>
</tr>
<tr>
<td>Discoverer</td>
<td>Jöns Jacob Berzelius</td>
</tr>
<tr>
<td>Discovered at</td>
<td>Sweden</td>
</tr>
<tr>
<td>Discovery date</td>
<td>1824</td>
</tr>
<tr>
<td>Origin of name</td>
<td>From the Latin word &quot;silicis&quot; meaning &quot;flint&quot;</td>
</tr>
<tr>
<td>Bond length in single crystal Si</td>
<td>2.352 Å</td>
</tr>
<tr>
<td>Density of solid</td>
<td>2.33 g/cm³</td>
</tr>
<tr>
<td>Molar volume</td>
<td>12.06 cm³</td>
</tr>
<tr>
<td>Velocity of sound</td>
<td>2200 m/sec</td>
</tr>
<tr>
<td>Hardness</td>
<td>6.5</td>
</tr>
<tr>
<td>Electrical resistivity</td>
<td>100,000 µΩ ⋅ cm</td>
</tr>
<tr>
<td>Reflectivity</td>
<td>28%</td>
</tr>
<tr>
<td>Melting point</td>
<td>1414 °C</td>
</tr>
<tr>
<td>Boiling point</td>
<td>2900 °C</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>150 W m⁻¹ K⁻¹</td>
</tr>
<tr>
<td>Coefficient of linear thermal expansion</td>
<td>2.6×10⁻⁶ K⁻¹</td>
</tr>
<tr>
<td>Etchants (wet)</td>
<td>HNO₄ and HF, KOH, etc.</td>
</tr>
<tr>
<td>Etchants (dry)</td>
<td>HBr, Cl₂, NF₃, etc.</td>
</tr>
<tr>
<td>CVD Precursor</td>
<td>SiH₄, SiH₂Cl₂, SiHCl₃, and SiCl₄</td>
</tr>
</tbody>
</table>
## Fact About Oxygen

<table>
<thead>
<tr>
<th>Name</th>
<th>Oxygen</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
<td>O</td>
</tr>
<tr>
<td>Atomic number</td>
<td>8</td>
</tr>
<tr>
<td>Atomic weight</td>
<td>15.9994</td>
</tr>
<tr>
<td>Discoverer</td>
<td>Joseph Priestley, Carl Scheele</td>
</tr>
<tr>
<td>Discovered at</td>
<td>England, Sweden</td>
</tr>
<tr>
<td>Discovery date</td>
<td>1774</td>
</tr>
<tr>
<td>Origin of name</td>
<td>From the Greek words &quot;oxy genes&quot; meaning &quot;acid&quot; (sharp) and &quot;forming&quot; (acid former)</td>
</tr>
<tr>
<td>Molar volume</td>
<td>17.36 cm$^3$</td>
</tr>
<tr>
<td>Velocity of sound</td>
<td>317.5 m/sec</td>
</tr>
<tr>
<td>Refractivity</td>
<td>1.000271</td>
</tr>
<tr>
<td>Melting point</td>
<td>54.8 K = -218.35 °C</td>
</tr>
<tr>
<td>Boiling point</td>
<td>90.2 K = -182.95 °C</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>0.02658 W m$^{-1}$ K$^{-1}$</td>
</tr>
<tr>
<td>Applications</td>
<td>Thermal oxidation, oxide CVD, reactive sputtering and photoresist stripping</td>
</tr>
<tr>
<td>Main sources</td>
<td>O$_2$, H$_2$O, N$_2$O, O$_3$</td>
</tr>
</tbody>
</table>
Application of Oxidation

• Diffusion Masking Layer

• Surface Passivation
  – Screen oxide, pad oxide, barrier oxide

• Isolation
  – Field oxide and LOCOS

• Gate oxide
Diffusion Barrier

- Much lower B and P diffusion rates in SiO$_2$ than that in Si
- SiO$_2$ can be used as diffusion mask
Application, Surface Passivation

Pad Oxide
Sacrificial Oxide
Screen Oxide
Barrier Oxide

Normally thin oxide layer (~150Å) to protect silicon defects from contamination and over-stress.
Screen Oxide

![Diagram showing Screen Oxide, Photoresist, Dopant Ions, and Si Substrate]
Pad and Barrier Oxides in STI Process

- Nitride
- Pad Oxide
- Silicon
- Trench Etch
- USG
- Barrier Oxide
- USG
- Trench Fill
- USG CMP; USG Anneal; Nitride and Pad Oxide Strip
Application, Pad Oxide

- Relieve strong tensile stress of the nitride
- Prevent stress induced silicon defects

Silicon nitride

Silicon Substrate
Application, Device Isolation

• Electronic isolation of neighboring devices
• Blanket field oxide
• Local oxidation of silicon (LOCOS)
• Thick oxide, usually 3,000 to 10,000 Å
Blanket Field Oxide Isolation

- Silicon
- Wafer Clean
- Silicon Dioxide
- Activation Area
- Field Oxidation
- Field Oxide
- Oxide Etch
- Silicon
LOCOS Process

Pad Oxide

Silicon nitride

P-type substrate

Pad oxidation, nitride deposition and patterning

Silicon nitride

SiO$_2$

P-type substrate

p$^+$

Isolation Doping

LOCOS oxidation

SiO$_2$

Bird’s Beak

Nitride and pad oxide strip

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LOCOS

• Compare with blanket field oxide
  – Better isolation
  – Lower step height
  – Less steep sidewall
• Disadvantage
  – rough surface topography
  – Bird’s beak
• Replacing by shallow trench isolation (STI)
Application, Sacrificial Oxide

- Defects removal from silicon surface
Application, Device Dielectric

- Gate oxide: thinnest and most critical layer
- Capacitor dielectric
# Oxide and Applications

<table>
<thead>
<tr>
<th>Name of the Oxide</th>
<th>Thickness</th>
<th>Application</th>
<th>Time in application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Native</td>
<td>15 - 20 Å</td>
<td>undesirable</td>
<td>-</td>
</tr>
<tr>
<td>Screen</td>
<td>~ 200 Å</td>
<td>Implantation</td>
<td>Mid-70s to present</td>
</tr>
<tr>
<td>Masking</td>
<td>~ 5000 Å</td>
<td>Diffusion</td>
<td>1960s to mid-1970s</td>
</tr>
<tr>
<td>Field and LOCOS</td>
<td>3000 - 5000 Å</td>
<td>Isolation</td>
<td>1960s to 1990s</td>
</tr>
<tr>
<td>Pad</td>
<td>100 - 200 Å</td>
<td>Nitride stress buffer</td>
<td>1960s to present</td>
</tr>
<tr>
<td>Sacrificial</td>
<td>&lt;1000 Å</td>
<td>Defect removal</td>
<td>1970s to present</td>
</tr>
<tr>
<td>Gate</td>
<td>30 - 120 Å</td>
<td>Gate dielectric</td>
<td>1960s to present</td>
</tr>
<tr>
<td>Barrier</td>
<td>100 - 200 Å</td>
<td>STI</td>
<td>1980s to present</td>
</tr>
</tbody>
</table>

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Silicon Dioxide Grown on Improperly Cleaned Silicon Surface
Pre-oxidation Wafer Clean

• Particulates
• Organic residues
• Inorganic residues
• Native oxide layers
RCA Clean

- Developed by Kern and Puotinen in 1960 at RCA
- Most commonly used clean processes in IC fabs
- SC-1-- $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ with 1:1:5 to 1:2:7 ratio at 70 to 80 °C to remove organic contaminants.
- SC-2-- $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ with 1:1:6 to 1:2:8 ratio at 70 to 80 °C to remove inorganic contaminants.
- DI water rinse
- HF dip or HF vapor etch to remove native oxide.
Pre-oxidation Wafer Clean
Particulate Removal

• High purity deionized (DI) water or $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ followed by DI $\text{H}_2\text{O}$ rinse.
• High pressure scrub or immersion in heated dunk tank followed by rinse, spin dry and/or dry bake (100 to 125 °C).
Pre-oxidation Wafer Clean
Organic Removal

• Strong oxidants remove organic residues.
• $\text{H}_2\text{SO}_4$:$\text{H}_2\text{O}_2$ or $\text{NH}_3\text{OH}$:$\text{H}_2\text{O}_2$ followed by DI $\text{H}_2\text{O}$ rinse.
• High pressure scrub or immersion in heated dunk tank followed by rinse, spin dry and/or dry bake (100 to 125 °C).
Pre-oxidation Wafer Clean
Inorganic Removal

• HCl:H$_2$O.
• Immersion in dunk tank followed by rinse, spin dry and/or dry bake (100 to 125 °C).
Pre-oxidation Wafer Clean
Native Oxide Removal

- HF:H$_2$O.
- Immersion in dunk tank or single wafer vapor etcher followed by rinse, spin dry and/or dry bake (100 to 125 °C).
Oxidation Mechanism

• $\text{Si} + \text{O}_2 \rightarrow \text{SiO}_2$
• Oxygen comes from gas
• Silicon comes from substrate
• Oxygen diffuse cross existing silicon dioxide layer and react with silicon
• The thicker of the film, the lower of the growth rate
Oxide Growth Rate Regime

Linear Growth Regime

\[ X = \frac{B}{A} t \]

Diffusion-limited Regime

\[ X = \sqrt{B t} \]
<100> Silicon Dry Oxidation

Oxide Thickness (micron)

Oxidation Time (hours)

1200 °C
1150 °C
1100 °C
1050 °C
1000 °C
950 °C
900 °C
Wet (Steam) Oxidation

- **Si + 2H₂O → SiO₂ + 2H₂**
- At high temperature H₂O is dissociated to H and H-O
- H-O diffuses faster in SiO₂ than O₂
- Wet oxidation has higher growth rate than dry oxidation.
Silicon Wet Oxidation Rate

Oxide Thickness (micron) vs. Oxidation Time (hours)

<100> Silicon Wet Oxidation

Temperature:
- 1150 °C
- 1100 °C
- 1050 °C
- 1000 °C
- 950 °C
- 900 °C
Oxidation Rate

- Temperature
- Chemistry, wet or dry oxidation
- Thickness
- Pressure
- Wafer orientation (<100> vs. <111>)
- Silicon dopant
Oxidation Rate Temperature

- Oxidation rate is very sensitive (exponentially related) to temperature.
- Higher temperature will have much higher oxidation rate.
- The higher of temperature is, the higher of the chemical reaction rate between oxygen and silicon is and the higher diffusion rate of oxygen in silicon dioxide is.
Oxidation Rate
Wafer Orientation

• $<111>$ surface has higher oxidation rate than $<100>$ surface.
• More silicon atoms on the surface.
Wet Oxidation Rate

- **<111> Orientation**
  - 1200 °C
  - 1100 °C
  - 1000 °C
  - 920 °C

- 95 °C Water

![Graph showing wet oxidation rate with oxide thickness on the y-axis and oxidation time on the x-axis.](image)
Oxidation Rate
Dopant Concentration

• Dopant elements and concentration
• Highly phosphorus doped silicon has higher growth rate, less dense film and etch faster.
• Generally highly doped region has higher grow rate than lightly doped region.
• More pronounced in the linear stage (thin oxides) of oxidation.
Oxidation: Dopants
Pile-up and Depletion Effects

• N-type dopants (P, As, Sb) have higher solubility in Si than in SiO$_2$, when SiO$_2$ grow they move into silicon, it is called pile-up or snowplow effect.

• Boron tends to go to SiO$_2$, it is called depletion effect.
Depletion and Pile-up Effects

Si-SiO$_2$ interface

Original Si Surface

Original Distribution

Original Si Surface

Si-SiO$_2$ interface

P-type Dopant Depletion

N-type dopant Pile-up

Dopant Concentration

SiO$_2$ Si
Oxidation Rate
Doped oxidation (HCl)

- HCl is used to reduce mobile ion contamination.
- Widely used for gate oxidation process.
- Growth rate can increase from 1 to 5 percent.
Oxidation Rate
Differential Oxidation

• The thicker of the oxide film is, the slower of the oxidation rate is.

• Oxygen need more time to diffuse cross the existing oxide layer to react with substrate silicon.
Pre-oxidation Clean

- Thermally grown SiO$_2$ is amorphous.
- Tends to cross-link to form a crystal
- In nature, SiO$_2$ exists as quartz and sand
- Defects and particles can be the nucleation sites
- Crystallized SiO$_2$ with poor barrier capability.

- Need clean silicon surface before oxidation.
Oxidation Process

• Dry Oxidation, thin oxide
  – Gate oxide
  – Pad oxide, screen oxide, sacrificial oxide, etc.

• Wet Oxidation, thick oxide
  – Field oxide
  – Diffusion masking oxide
Dry Oxidation System

To Process Tube

Control Valves

Regulator

MFC

HCl
Process N₂
O₂
Purge N₂
Dry Oxidation

- Dry $O_2$ as the main process gas
- HCl is used to remove mobile ions for gate oxidation
- High purity $N_2$ as process purge gas
- Lower grade $N_2$ as idle purge gas
Gate Oxidation Steps

• Idle with purge $N_2$ flow
• Idle with process $N_2$ flow
• Wafer boats push-in with process $N_2$ flow
• Temperature ramp-up with process $N_2$ flow
• Temperature stabilization with process $N_2$ flow
• Oxidation with $O_2$, HCl, stop $N_2$ flow
Dangling Bonds and Interface Charge

Interface State Charge (Positive)

Dangling Bond

Si-SiO₂ Interface

SiO₂

Si
Gate Oxidation Steps, Continue

• Oxide annealing, stop O₂, start process flow N₂
• Temperature cool-down with process N₂ flow
• Wafer boats pull-out with process N₂ flow
• Idle with process N₂ flow
• Next boats and repeat process
• Idle with purge N₂ flow
Wet Oxidation Process

- Faster, higher throughput
- Thick oxide, such as LOCOS
- Dry oxide has better quality

<table>
<thead>
<tr>
<th>Process</th>
<th>Temperature</th>
<th>Film Thickness</th>
<th>Oxidation Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dry oxidation</td>
<td>1000 °C</td>
<td>1000 Å</td>
<td>~ 2 hours</td>
</tr>
<tr>
<td>Wet oxidation</td>
<td>1000 °C</td>
<td>1000 Å</td>
<td>~ 12 minutes</td>
</tr>
</tbody>
</table>
Water Vapor Sources

- Boiler
- Bubbler
- Flush
- Pyrogenic
Boiler System

Heated Gas line  Heated Fore line

MFC  Process Tube  Exhaust

Vapor Bubbles

Water

Heater
Bubbler System

\[ N_2 \rightarrow \text{MFC} \]

Heated Gas Line

\[ N_2 + H_2O \rightarrow \text{Process Tube} \]

Water

N\(_2\) Bubbles

Heater

Exhaust
Flush System

Water

Hot Plate

Heater

N₂ → MFC → Process Tube
Pyrogenic Steam System

Hydrogen Flame, \( 2 \text{H}_2 + \text{O}_2 \rightarrow 2 \text{H}_2\text{O} \)
Pyrogenic System

• Advantage
  – All gas system
  – Precisely control of flow rate

• Disadvantage
  – Introducing of flammable, explosive hydrogen

• Typical $\text{H}_2: \text{O}_2$ ratio is between 1.8:1 to 1.9:1.
Pyrogenic Wet Oxidation System
Wet Oxidation Process Steps

- Idle with purge N\textsubscript{2} flow
- Idle with process N\textsubscript{2} flow
- Ramp O\textsubscript{2} with process N\textsubscript{2} flow
- Wafer boat push-in with process N\textsubscript{2} and O\textsubscript{2} flows
- Temperature ramp-up with process N\textsubscript{2} and O\textsubscript{2} flows
- Temperature stabilization with process N\textsubscript{2} and O\textsubscript{2} flows
- Ramp O\textsubscript{2}, turn-off N\textsubscript{2} flow
- Stabilize the O\textsubscript{2} flow
Wet Oxidation Process Steps

- Turn-on H₂ flow, ignition and H₂ flow stabilization
- Steam oxidation with O₂ and H₂ flow
- Hydrogen termination, turn-off H₂ while keeping O₂ flow
- Oxygen termination, turn-off O₂ start process N₂ flow
- Temperature ramp-down with process N₂ flow
- Wafer boat pull-out with process N₂ flow
- Idle with process N₂ flow
- Next boats and repeat process
- Idle with purge N₂ flow
Rapid Thermal Oxidation

• For gate oxidation of deep sub-micron device
• Very thin oxide film, < 30 Å
• Need very good control of temperature uniformity, WIW and WTW.
• RTO will be used to achieve the device requirement.
RTP Process Diagram

Load wafer

Ramp up 1& 2

RTO

O$_2$ flow

HCl flow

N$_2$ flow

RTA

Cool down

Unload wafer

Time

Temperature
High Pressure Oxidation

• Faster growth rate
• Reducing oxidation temperature:
  – 1 amt. = –30 °C
• Higher dielectric strength
High Pressure Oxidation

Stainless Steel Jacket

- High Pressure Inert Gas
- High Pressure Oxidant Gas

Quartz Process Chamber
High Pressure Oxidation

Oxidation time to grow 10,000 Å wet oxide

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Pressure</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>1 atmosphere</td>
<td>5 hours</td>
</tr>
<tr>
<td></td>
<td>5 atmosphere</td>
<td>1 hour</td>
</tr>
<tr>
<td></td>
<td>25 atmosphere</td>
<td>12 minutes</td>
</tr>
</tbody>
</table>
High Pressure Oxidation

Oxidation temperature to grow 10,000 Å wet oxide in 5 hours

<table>
<thead>
<tr>
<th>Time</th>
<th>Pressure</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 hours</td>
<td>1 atmosphere</td>
<td>1000 °C</td>
</tr>
<tr>
<td></td>
<td>10 atmosphere</td>
<td>700 °C</td>
</tr>
</tbody>
</table>
High Pressure Oxidation

• Complex system
• Safety issues

• Not widely used in IC production
Oxide Measurement

- Thickness
- Uniformity
- Color chart
- Ellipsometry
- Reflectometry

- Gate oxide
- Break down voltage
- C-V characteristics
Ellipsometry

Linearly Polarized Incident Light

Elliptically Polarized Reflected Light

$n_1, k_1, t_1$

$n_2, k_2$
Reflectometry

Incident light

Dielectric film, $n(\lambda)$

Substrate

Human eye or photodetector
C-V Test Configuration

![Diagram of C-V Test Configuration]

- Large Resistor
- Capacitor
- Meter
- Oxide
- Aluminum
- Silicon
- Metal Platform
- Heater
Summary of Oxidation

• Oxidation of silicon
• High stability and relatively easy to get.
• Application
  – Isolation, masking, pad, barrier, gate, and etc.
• Wet and Dry
• More dry processes for advanced IC chips
• Rapid thermal oxidation and annealing for ultra-thin gate oxide
Diffusion
Diffusion

- Most common physics phenomena
- Materials disperse from higher concentration to lower concentration region
- Silicon dioxide as diffusion mask
- Was widely used for semiconductor doping
- “Diffusion Furnace” and “Diffusion Bay”
Illustration of Diffusion Doping

Dopant

Silicon
Illustration of Diffusion Doping
Definition of Junction depth

Junction Depth, $x_j$

Distance from the wafer surface

Background dopant concentration

Dopant Concentration
Diffusion

Masking Oxide

N-Silicon

Masking Oxide

p⁺

N-Silicon

p⁺
Diffusion

• Replaced by ion implantation due to the less process control
• Still being used in drive-in for well formation
Thermal Budget

- Dopant atoms diffuse fast at high temperature
  \[ D = D_0 \exp \left( -\frac{E_A}{kT} \right) \]
- Smaller device geometry, less room for dopant thermal diffusion, less thermal budget
- Thermal budget determines the time and temperature of the post-implantation thermal processes
Illustration of Thermal Budget

As S/D Implantation

Over Thermal Budget
Thermal Budget

Source: Chang and Sze, *ULSI Technology*
Diffusion Doping Process

- Both dopant concentration and junction depth are related to temperature.
- No way to independently to control both factor
- Isotropic dopant profile
- Replaced by ion implantation after the mid-1970s.
Diffusion Doping Process

• Silicon dioxide as hard mask
• Deposit dopant oxide
• Cap oxidation
  – prevent dopant diffusion into gas phase
• Drive-in
Diffusion Doping Process

• Oxidation, photolithography and oxide etch

• Pre-deposition:

$$\text{B}_2\text{H}_6 + 2 \text{O}_2 \rightarrow \text{B}_2\text{O}_3 + 3 \text{H}_2\text{O}$$

• Cap oxidation:

$$2 \text{B}_2\text{O}_3 + 3 \text{Si} \rightarrow 3 \text{SiO}_2 + 4\text{B}$$

$$2 \text{H}_2\text{O} + \text{Si} \rightarrow \text{SiO}_2 + 2 \text{H}_2$$

• Drive-in

  – Boron diffuses into silicon substrate
Diffusion Doping Process

• Oxidation, photolithography and oxide etch
• Deposit dopant oxide:
  \[ 4\text{POCl}_3 + 3\text{O}_2 \rightarrow 2\text{P}_2\text{O}_5 + 3\text{Cl}_2 \]
• Cap oxidation
  \[ 2\text{P}_2\text{O}_5 + 5\text{Si} \rightarrow 5\text{SiO}_2 + 4\text{P} \]
  – Phosphorus concentrates on silicon surface
• Drive-in
  – Phosphorus diffuses into silicon substrate
Phosphorus Diffusion System

[Diagram of the Phosphorus Diffusion System]

- POCl₃
- Process N₂
- O₂
- Purge N₂
- MFC
- Control Valves
- Regulator
- Process Tube
- Wafers
- Burn Box
- Scrubbier
- Exhaust
Wafer Clean

Si Substrate
Oxidation

\[
\begin{array}{|c|}
\hline
\text{SiO}_2 \\
\hline
\text{Si Substrate} \\
\hline
\end{array}
\]
Doped Area Patterning

PR

SiO$_2$

Si Substrate
Etch Silicon Dioxide

- PR
- SiO$_2$
- Si Substrate
Strip Photoresist

SiO$_2$

Si Substrate
Wafer Clean

SiO$_2$  
Si Substrate
Dopant Oxide Deposition

Deposited Dopant Oxide

\[ \text{SiO}_2 \]

Si Substrate
Cap Oxidation
Phosphoric Oxide Deposition and Cap Oxidation

Temperature

$N_2$ Flow

$POCl_3$ Flow

$O_2$ Flow

Wafer Position

Push Temp Ramp Temp. Stab. Dopant Deposition Cap Oxide $N_2$ Vent Ramp Down Pull
Drive-in

SiO$_2$

Si Substrate
Strip Oxide, Ready for Next Step
Phosphorus Drive-in

Temperature

N₂ Flow

O₂ Flow

Wafer Position

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Limitations and Applications

- Diffusion is isotropic process and always dope underneath masking oxide
- Can’t independently control junction depth and dopant concentration
- Used for well implantation drive-in
- R&D for ultra shallow junction (USJ) formation
Application of Diffusion: Drive-in

- Wells have the deepest junction depth
- Need very high ion implantation energy
- Cost of MeV ion implanters is very high
- Diffusion can help to drive dopant to the desired junction depth while annealing
Well Implantation and Drive-in

- Photoresist
- P-Epi
- N-Well
- P+
Diffusion for Boron USJ Formation

- Small devices need ultra shallow junction
- Boron is small and light, implanter energy could be too high for it goes too deep
- Controlled thermal diffusion is used in R&D for shallow junction formation
Surface Clean

- Silicide
- Sidewall Spacer
- STI
- Si Substrate
BSG CVD

Silicide

Sidewall Spacer

Boro-Silicate Glass

Si Substrate

STI
RTP Dopant Drive-in

Polysilicon

Silicide

Gate Oxide

Boro-Silicate Glass

Si Substrate

STI

STI
Strip BSG

Si Substrate

Gate Oxide

Polysilicon

Silicide
Doping Measurement

• Four-point probe

\[ R_s = \rho/t \]
Four-Point Probe Measurement

\[ V \]
\[ I \]

\[ P_1 \quad P_2 \quad P_3 \quad P_4 \]

\[ S_1 \quad S_2 \quad S_3 \]

Doped Region

Substrate
Summary of Diffusion

• Physics of diffusion is well understood
• Diffusion was widely used in doping processes in early IC manufacturing
• Replaced by ion implantation since the mid-1970s
Annealing and RTP Processes
Post-implantation Annealing

- Energetic ions damage crystal structure
- Amorphous silicon has high resistivity
- Need external energy such as heat for atoms to recover single crystal structure
- Only in single crystal structure dopants can be activated
Post-implantation Annealing

- Single crystal structure has lowest potential energy
- Atoms tend to stop on lattice grid
- Heat can provide energy to atoms for fast thermal motion
- Atoms will find and settle at the lattice grid where has the lowest potential energy position
- Higher temperature, faster annealing
Before Ion Implantation

Lattice Atoms
After Ion Implantation

Lattice Atoms

Dopant Atom
Thermal Annealing
Thermal Annealing

Lattice Atoms

Dopant Atoms
Annoy Annealing

• A thermal process in which different atoms chemically bond with each other to form a metal alloy.
• Widely used in silicide formation
• Self aligned silicide (salicide)
  – Titanium silicide, TiSi$_2$
  – Cobalt silicide, CoSi$_2$
• Furnace and RTP
Silicide

- Much lower resistivity than polysilicon
- Used as gate and local interconnection
- Used as capacitor electrodes
- Improving device speed and reduce heat generation
- TiSi$_2$, WSi$_2$ are the most commonly used silicide
- CoSi$_2$, MoSi$_2$, and etc are also used
Titanium Silicide Process

- Argon sputtering clean
- Titanium PVD
- RTP Anneal, ~700 °C
- Strip titanium, $\text{H}_2\text{O}_2$:H$\text{H}_2\text{SO}_4$
Titanium Silicide Process

Ti Deposition

Annealing

Ti Strip

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Aluminum-silicon Alloy

• Form on silicon surface
• Prevent junction spiking due to silicon dissolving in aluminum
Junction Spike
Reflow

• Flowed surface is smoother and flatter
• Easier for photolithography and metallization
• Higher temperature, better flow result
• Reflow time and temperature are determined by the thermal budget
• Higher dopant concentration requires lower flow temperature
Illustration of BPSG Reflow

As Deposit

After Reflow

P-type substrate

LOCOS

PSG

N-well

p⁺
n⁺

p⁺
n⁺

p⁺
n⁺

p⁺
n⁺

p⁺
n⁺
Reflow

- Undoped silicate glass (USG) becomes soften at very high temperature $T > 1500 \, ^\circ C$, will flow due to the surface tension
- PSG and BPSG become soften at significant lower temperature ($< 1100 \, ^\circ C$ down to $850 \, ^\circ C$)
- Phosphorus also can trap sodium
- PSG and BPSG is commonly used as pre-metal dielectric (PMD)
Reflow Process

- Wafer loading
- Temperature ramp-up
- Temperature stabilization
- Reflow
- Temperature ramp-down
- Wafer unloading
Reflow Process

- Reflow usually used $N_2$ ambient
- Sometimes $H_2O$ vapor is also used
- $H_2O$ helps to fully oxidize dopant atoms
Reflow Process

• Smaller device, less thermal budget
• No enough thermal budget for reflow for sub-0.25 µm devices
• PSG anneal (~750 °C) instead of reflow
Summary of Anneal

• The most commonly used anneal processes are post-implantation annealing, alloy annealing and reflow

• Thermal anneal is required after ion implantation for recover crystal structure and activation dopant atoms

• Thermal anneal helps metal to react with silicon to form silicides
Summary of Anneal

• Metal anneal helps to form larger grain size and reduces the resistivity
• PSG or BPSG reflow smoothens and flattens the dielectric surface and helps photolithography and metallization processes
• RTP becomes more commonly used in annealing processes
Summary of Anneal

• Advantages of RTP
  – Much faster ramp rate (75 to 150 °C/sec)
  – Higher temperature (up to 1200 °C)
  – Faster process
  – Minimize the dopant diffusion
  – Better control of thermal budget
  – Better wafer to wafer uniformity control
High Temperature Deposition Processes
What is CVD

Chemical Vapor Deposition

- Gas(es) or vapor(s) chemically react on substrate surface and form solid byproduct on the surface as deposited thin film.
- Other byproducts are gases and leave the surface.
- Widely used in IC processing for metal, dielectric and silicon thin film deposition.
High Temperature CVD

• Epitaxy
• Polysilicon
• Silicon Nitride
Epitaxy

- Monocrystralline layer
- Epitaxy silicon
- Epitaxy silicon-germanium
- Epitaxy GaAs
Epitaxy Silicon

• Provide high quality silicon substrate without trace amount of oxygen and carbon.
• Required for bipolar devices.
• Needed for high performance CMOS devices.
Epitaxy Silicon

- High temperature (~1000 °C) processes.
- Silane (SiH$_4$), DCS (SiH$_2$Cl$_2$) or TCS (SiHCl$_3$) as silicon source gases.
- Hydrogen as process gas and purge gas
- Arsine (AsH$_3$), Phosphine (PH$_3$), and Diborane (B$_2$H$_6$) are used as dopant gases.
Epitaxy Silicon Deposition

• Silane process

\[ \text{SiH}_4 \rightarrow \text{Si} + \text{H}_2 \]

Silane Epi-Si Hydrogen

Heat (1000 °C)

• DCS process

\[ \text{SiH}_2\text{Cl}_2 \rightarrow \text{Si} + 2\text{HCl} \]

Silane Epi-Si Hydrochloride

Heat (1150 °C)
Epitaxy Silicon Doping

• N-type Dopant

\[
\text{Heat (1000 °C)} \\
\text{AsH}_3 \rightarrow \text{As} + \frac{3}{2} \text{H}_2 \\
\text{Arsine} \quad \text{As} \quad \text{Hydrogen}
\]

\[
\text{Heat (1000 °C)} \\
\text{PH}_3 \rightarrow \text{P} + \frac{3}{2} \text{H}_2 \\
\text{Arsine} \quad \text{Phosphorus} \quad \text{Hydrogen}
\]
Epitaxy Silicon Doping

• P-type Dopant

Heat (1000 °C)

\[ \text{B}_2\text{H}_6 \rightarrow 2 \text{B} + 3 \text{H}_2 \]

Diborane  Boron         Hydrogen
Epitaxy Silicon

• Usually deposited ("grown") by wafer manufacturer instead by IC fab.
• In fab epi process: special needs such as usually dopant concentration and epi thickness.
• Selective epi for raised source/drain.
• Single wafer epitaxy process.
Polysilicon

• High temperature stability.
• Reasonable good conductivity.
• Widely used for the gate and local interconnection in MOS devices.
• Also widely used as the capacitor electrodes in memory devices, especially DRAM.
Polysilicon Applications in DRAM

- Ta$_2$O$_5$ or BST
- TiSi$_2$
- Poly 5
- Poly 4
- Poly 3
- Poly 2
- Sidewall Spacer
- Poly 1
- n$^+$
- n$^+$
- n$^+$
- p-Silicon

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Polysilicon

- High temperature (~700 °C) furnace LPCVD processes.
- Silane (SiH$_4$) or DCS (SiH$_2$Cl$_2$) as silicon source gases.
- Nitrogen as purge gas
- Arsine (AsH$_3$), Phosphine (PH$_3$), and Diborane (B$_2$H$_6$) are used as dopant gases.
Polysilicon Deposition

• **Silane process**

  Heat (750 °C)

  $$\text{SiH}_4 \rightarrow \text{Si} + \text{H}_2$$

  **Silane**

  **Poly-Si**

  **Hydrogen**

• **DCS process**

  Heat (750 °C)

  $$\text{SiH}_2\text{Cl}_2 \rightarrow \text{Si} + 2\text{HCl}$$

  **Silane**

  **Poly-Si**

  **Hydrochloride**
Polysilicon Doping

• N-type Dopant

\[
\begin{align*}
\text{Heat (750 °C)} & \\
\text{AsH}_3 & \rightarrow \text{As} + \frac{3}{2}\text{H}_2 \\
\text{Arsine} & \quad \text{As} \quad \text{Hydrogen} \\
\text{Heat (750 °C)} & \\
\text{PH}_3 & \rightarrow \text{P} + \frac{3}{2}\text{H}_2 \\
\text{Phosphine} & \quad \text{Phosphorus} \quad \text{Hydrogen}
\end{align*}
\]
Polysilicon Doping

- P-type Dopant

Heat (750 °C)

\[ \text{B}_2\text{H}_6 \rightarrow 2 \text{B} + 3 \text{H}_2 \]

Diborane \quad \rightarrow \quad \text{Boron} \quad + \quad \text{Hydrogen}
Temperature Relationship of Silane Process

• On single crystal silicon substrate
• Silane as source gases
• $T > 900 \, ^\circ\text{C}$ deposit *single crystal silicon*
• $900 \, ^\circ\text{C} > T > 550 \, ^\circ\text{C}$ deposit *polysilicon*
• $T < 550 \, ^\circ\text{C}$ deposit *amorphous silicon*
Temperature and Crystal Structure for Silane Processes

- $T < 550 \, ^\circ C$
  - Amorphous Si

- $550 \, ^\circ C < T < 900 \, ^\circ C$
  - Polysilicon

- $T > 900 \, ^\circ C$
  - Single Crystal Si
Polysilicon LPCVD System

SiH₄  Process N₂  Purge N₂

MFC  MFC  MFC

Control Valves

Regulator

Process Tube

Wafers

Burn Box

Scrubbier

Exhaust
Polysilicon Deposition Process

- Idle with purge $N_2$ flow
- Idle with process $N_2$ flow
- Wafer load into tower with process $N_2$ flow
- Tower raises into process chamber (bell jar) with process $N_2$ flow
- Pump down chamber to base pressure (< 2 mTorr) by turning-off $N_2$ flow
- Stabilize wafer temperature with $N_2$ flow and leak check
- Set up process pressure (~250 mTorr) and with $N_2$ flow
- Turn-on SiH$_4$ flow and turn-off $N_2$, start deposition
- Close gate valve, fill $N_2$ and ramp-up pressure to atmospheric pressure
- Tower lowed and wafer temperature cooled down, with process $N_2$ flow
- Unload wafer with process $N_2$ flow
- Idle with purge $N_2$ flow
Polysilicon Deposition Process

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Polycide Deposition System
Polycide Deposition System

WSi$_x$ Deposition Chamber

RTA Chamber

Poly Si Deposition Chamber

Wafer Transfer Robot

Cool down Chamber

Wafer Loading Stations
Silicon Nitride

- Dense material
- Widely used as diffusion barrier layer and passivation layer
- LPCVD (front-end) and PECVD (back-end)
- LPCVD nitride usually is deposited in a furnace
Application of Silicon Nitride

- LOCOS formation as oxygen diffusion barrier
- STI formation as oxide CMP stop
- PMD barrier layer
- Etch stop layer
LOCOS Process

Pad Oxide

Silicon nitride

P-type substrate

Pad oxidation, nitride deposition and patterning

Silicon nitride

SiO$_2$

P-type substrate

p$^+$

Isolation Doping

p$^+$

LOCOS oxidation

Bird’s Beak

SiO$_2$

P-type substrate

p$^+$

Isolation Doping

p$^+$

Nitride and pad oxide strip

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STI Process

1. **Pad Oxidation and LPCVD Nitride**
   - Nitride
   - Pad Oxide
   - Silicon

2. **Etch Nitride and Pad Oxide**
   - Nitride
   - Pad Oxide
   - Photoresist
   - Photoresist
   - Silicon

3. **Strip Photoresist**
   - Nitride
   - Pad Oxide
   - Silicon
STI Process

- Nitride
- Pad Oxide
- Trench on Silicon
- Silicon
- USG
- Barrier Oxide
- USG CMP; Nitride, Pad Oxide Strip
Self-aligned Contact Etch Stop

- Photoresist
- BPSG
- TiSi₂
- Oxide
- Nitride
- Sidewall Spacer
- Poly Gate
- p-Silicon
- n⁺

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Nitride Breakthrough

Nitride Breakthrough
Strip Photoresist

BPSG

Oxide

Nitride

TiSi₂

n⁺

p-Silicon

n⁺

n⁺

Sidewall Spacer

Poly Gate

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Deposit Ti/TiN and Tungsten
CMP Tungsten and TiN/Ti
Silicon Nitride Applications

- IMD Seal Nitride
- IMD Etch Stop Nitride
- Sidewall Spacer
- PMD Barrier Nitride
- PD Silicon Nitride
- PD Silicon Oxide
- M2
- FSG
- Cu
- M1
- FSG
- W
- PSG
- PSG
- W
- STI
- n+ USG
- p+
- P-Well
- N-Well
- n+
Silicon Nitride Deposition

- Silane or DCS as silicon source
- NH₃ as nitrogen source
- N₂ as purge gas

\[
3 \text{SiH}_2\text{Cl}_2 + 4 \text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 6 \text{HCl} + 6 \text{H}_2
\]

or

\[
3 \text{SiH}_4 + 4 \text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 12 \text{H}_2
\]
Silicon Nitride LPCVD System

Heaters

Tower

MFC

Wafers

Process Chamber

Control Valves

Regulator

Pump

Burn Box

Scrubber

Exhaust

SiH₂Cl₂, Process N₂, NH₃, Purge N₂, MFC, Scrubbier, Exhaust

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Nitride Deposition Process Sequence

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Future Trends of HT-CVD

- More single wafer rapid thermal CVD
- Integrated processes in cluster tools
Summary of Furnace Deposition

• Polysilicon and silicon nitride are the two most commonly film deposited in high temperature furnace
• Silane and DCS are the two most commonly used silicon sources.
• Polysilicon can be doped while deposition by flowing phosphine, arsine or diborane
Rapid Thermal Process
Rapid Thermal Processing (RTP)

- Mainly used for post-implantation rapid thermal anneal (RTA) process.
- Fast temperature ramp-up, 100 to 150 °C/sec compare with 15 °C/min in horizontal furnace.
- Reduce thermal budge and easier process control.
Rapid Thermal Processing (RTP)

- Single wafer rapid thermal CVD (RTCVD) chamber can be used to deposit polysilicon and silicon nitride.
- RTCVD chamber can be integrated with other process chamber in a cluster tool for in-line process.
- Thin oxide layer (< 40 Å) is likely to be grown with RTO for WTW uniformity control.
Schematic of RTP Chamber

- Wafer
- External Chamber
- Process Gases
- Quartz Chamber
- Tungsten-Halogen Lamp
- IR Pyrometer
Lamp Array

Bottom Lamps

Top Lamps

Wafer
RTP Chamber

Photo courtesy of Applied Materials, Inc
Annealing and Dopant Diffusion

• At higher temperature >1100 °C anneal is faster than diffusion
• Post implantation prefer high temperature and high temperature ramp rate.
• Single wafer rapid thermal process tool has been developed initially for this application
Annealing and Dopant Diffusion

- Dopant atoms diffuse at high temperature
- Furnace has low temperature ramp rate (~10 °C/min) due to large thermal capacity
- Furnace annealing is a long process which causes more dopant diffusion
- Wafer at one end gets more anneal than wafer at another end
Anneal Rate and Diffusion Rate

Anneal Rate

Diffusion Rate

Temperature
Dopant Diffusion After Anneal

RTA

Furnace anneal
Advantage of RTP over Furnace

- Much faster ramp rate (75 to 150 °C/sec)
- Higher temperature (up to 1200 °C)
- Faster process
- Minimize the dopant diffusion
- Better control of thermal budget
- Better wafer to wafer uniformity control
RTP Temperature Change

![Diagram of RTP Temperature Change](image)

- **Load wafer**
- **Ramp up**
- **Anneal**
- **Cool down**
- **Unload wafer**

- **N₂ Flow**
Thermal Nitridization

- Titanium PVD
- Thermal nitridization with NH$_3$

\[ \text{NH}_3 + \text{Ti} \rightarrow \text{TiN} + 3/2 \text{H}_2 \]
Titanium Nitridization
RTO Process

- Ultra thin silicon dioxide layer < 30Å
- Better WTW uniformity
- Better thermal budget control
RTP Process Diagram

- Load wafer
- Ramp up 1 & 2
- RTO
  - O₂ flow
- HCl flow
- N₂ flow
- RTA
- Cool down
- Unload wafer

- Temperature

Time
Future Tends

• Rapid thermal process (RTP)
• In-situ process monitoring
• Cluster tools

• Furnace will still be used
Temperature of RTP & Furnace

![Graph showing temperature changes over time for RTP and Furnace]
Cluster Tool

- RTO/RTP
- RTCVD $\alpha$-Si
- HF Vapor
- Clean
- Cool down
- Transfer Chamber
- Loading Station
- Unloading Station
Summary of RTP

• Fast
• Better process control
  – Thermal budget
  – Wafer to wafer uniformity
• Minimized dopant diffusion
• Cluster tool, easy process integration
Summary of Thermal Process

- Oxidation, diffusion, annealing, and deposition
- Wet oxidation is faster, dry oxidation has better film quality. Advanced fab: mainly dry oxidation.
- Diffusion doping with oxide mask, used in lab
- LPCVD polysilicon and front-end silicon nitride
- Annealing recovers crystal and activates dopants
- RTP: better control, faster and less diffusion
- Furnaces: high throughput and low cost, will continue to be used in the future fabs