Chapter 10
CVD and Dielectric Thin Film

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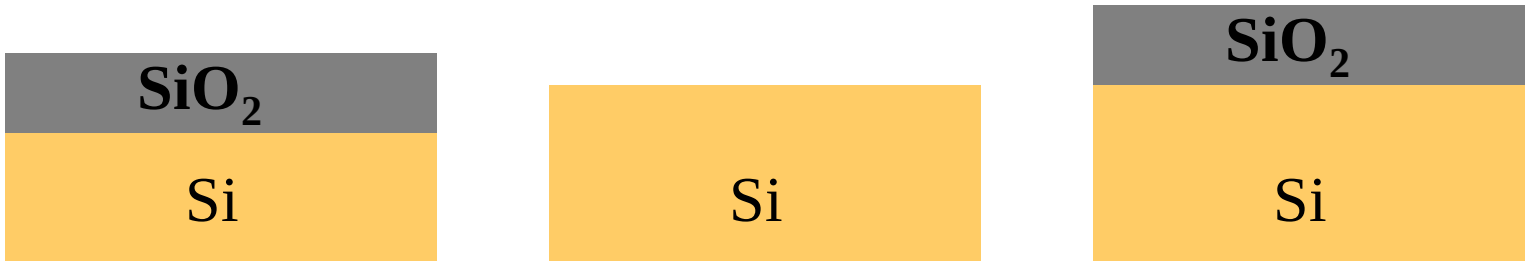
Objectives

- Identify at least four CVD applications
- Describe CVD process sequence
- List the two deposition regimes and describe their relation to temperature
- List two dielectric thin films
- Name the two most commonly used silicon precursors for dielectric CVD

CVD Oxide vs. Grown Oxide



Grown film Bare silicon Deposited film

CVD Oxide vs. Grown Oxide

Grow

- Oxygen is from gas phase
- Silicon from substrate
- Oxide grow into silicon
- Higher quality

CVD

- Both oxygen and silicon are from gas phase
- Deposit on substrate surface
- Lower temperature
- Higher growth rate

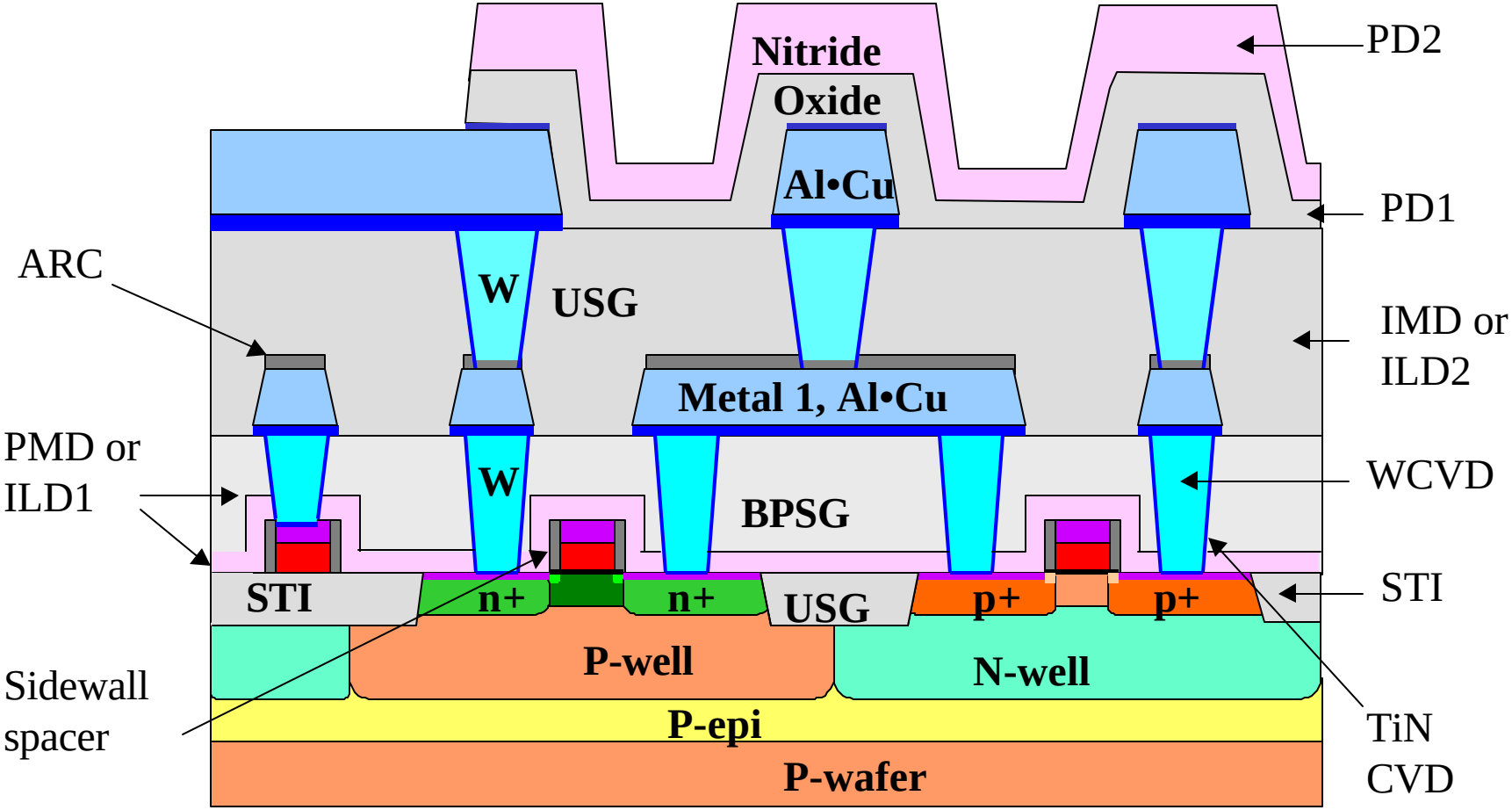
Dielectric Thin Film Applications

- Multi-level metal interconnection
- CVD and SOG plus CVD dielectrics
- Shallow trench isolation (STI)
- Sidewall spacer for salicide, LDD, and the source/drain diffusion buffer
- The passivation dielectric (PD)
- Dielectric ARC for feature size < 0.25 μm

Dielectric Thin Film Applications

- Inter layer dielectric, or ILD, include PMD and IMD
- Pre-metal dielectric: PMD
  - normally PSG or BPSG
  - Temperature limited by thermal budget
- Inter-metal dielectric: IMD
  - USG or FSG
  - Normally deposited around 400 °C

Figure 10.2


Nitride
Oxide
Al•Cu
PD2
PD1
ARC
W
USG
IMD or
ILD2
Metal 1, Al•Cu
PMD or
ILD1
W
BPSG
WCVD
STI
n+
n+
USG
p+
p+
STI
P-well
N-well
Sidewall
spacer
P-epi
TiN
CVD
P-wafer

Dielectric Processes

An N-layer metal interconnection IC chip with STI, the minimum number of dielectric process is:

$$\text{Dielectric layer} = \underbrace{1}_{\text{STI}} + \underbrace{1}_{\text{spacer}} + \underbrace{1}_{\text{PMD}} + \underbrace{(N-1)}_{\text{IMD}} + \underbrace{1}_{\text{PD}} = N + 3$$

CVD

- Chemical Vapor Deposition

- Chemical gases or vapors react on the surface of solid, produce solid byproduct on the surface in the form of thin film. Other byproducts are volatile and leave the surface.

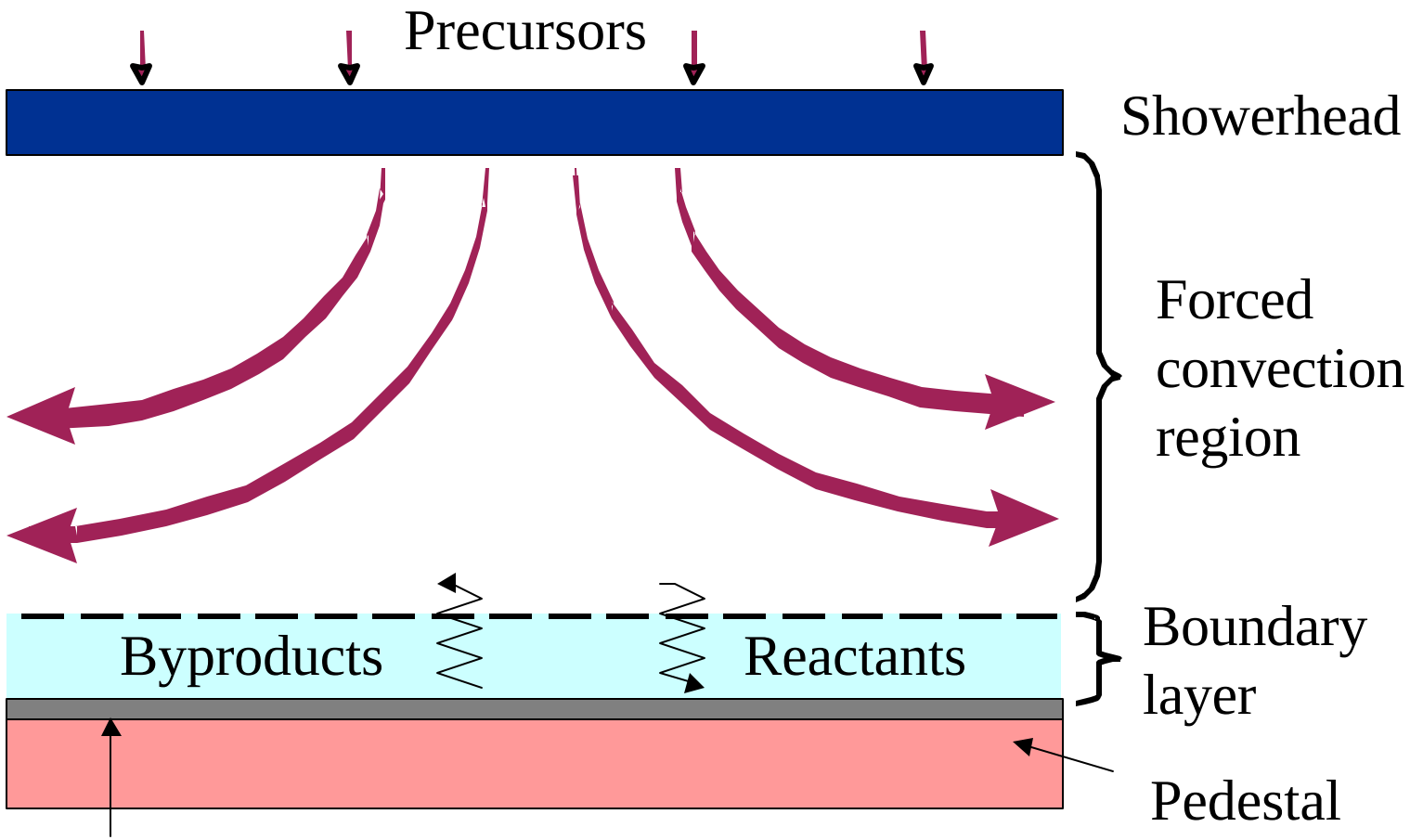
CVD Applications

	FILMS	***PRECURSORS***
Semiconductor	Si (poly) Si (epi)	SiH_4 (silane) $SiCl_2H_2$ (DCS) $SiCl_3H$ (TCS) $SiCl_4$ (Siltet)
Dielectrics	SiO_2 (glass)	LPCVD SiH_4, O_2 PECVD SiH_4, N_2O PECVD $Si(OC_2H_5)_4$ (TEOS), O_2
		LPCVD TEOS APCVD&SACVD™ TEOS, O_3 (ozone)
	Oxynitride	SiH_4, N_2O, N_2, NH_3
	Si_3N_4	PECVD SiH_4, N_2, NH_3 LPCVD SiH_4, N_2, NH_3 LPCVD $C_8H_{22}N_2Si$ (BTBAS)
Conductors	W (Tungsten) WSi_2 TiN Ti Cu	WF_6 (Tungsten hexafluoride), SiH_4, H_2 WF_6 (Tungsten hexafluoride), SiH_4, H_2 $Ti[N(CH_3)_2]_4$ (TDMAT) $TiCl_4$

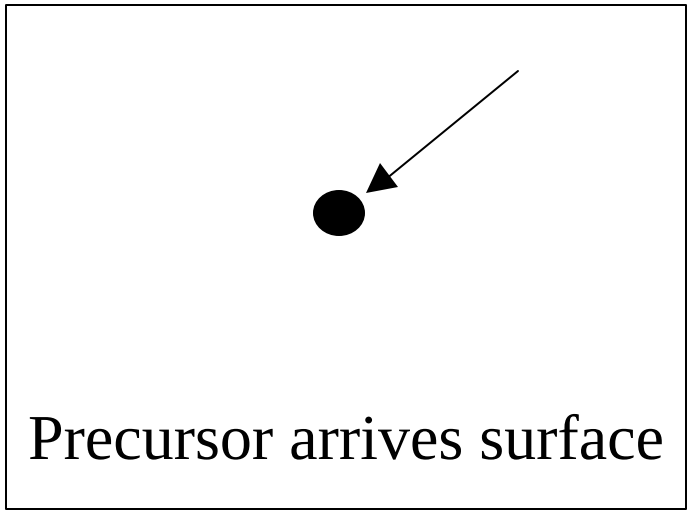
CVD

- Gas or vapor phase precursors are introduced into the reactor
- Precursors across the boundary layer and reach the surface
- Precursors adsorb on the substrate surface
- Adsorbed precursors migrate on the substrate surface
- Chemical reaction on the substrate surface
- Solid byproducts form nuclei on the substrate surface
- Nuclei grow into islands
- Islands merge into the continuous thin film
- Other gaseous byproducts desorb from the substrate surface
- Gaseous byproducts diffuse across the boundary layer
- Gaseous byproducts flow out of the reactor.

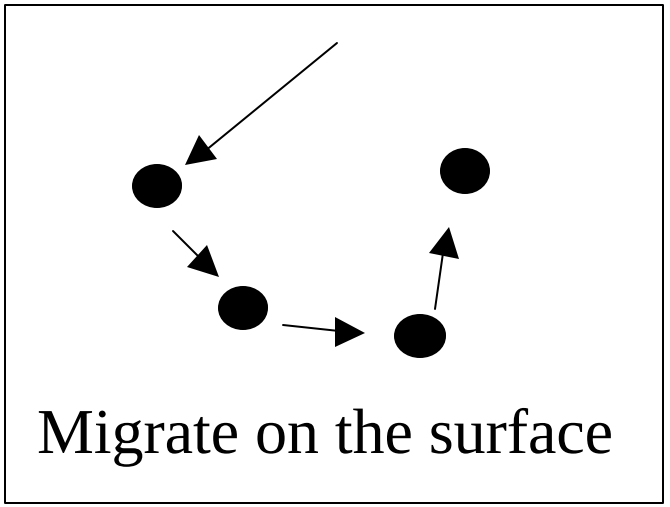
Figure 10.3


Precursors
Showerhead
Forced convection region
Byproducts
Reactants
Boundary layer
Pedestal
Wafer

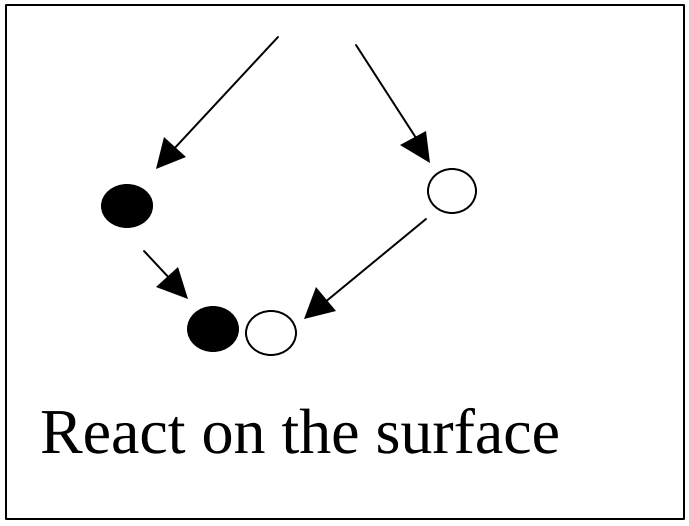
Deposition Process



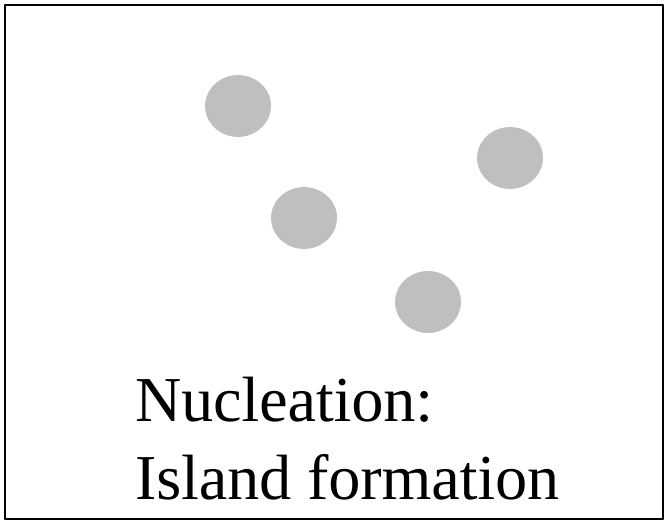
Precursor arrives surface



Migrate on the surface

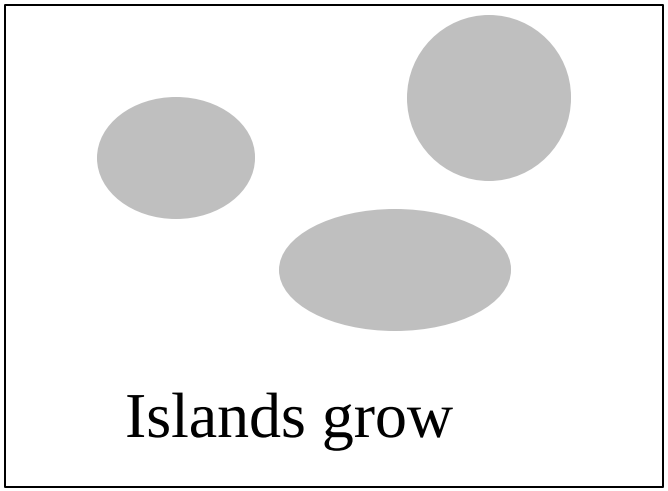


React on the surface

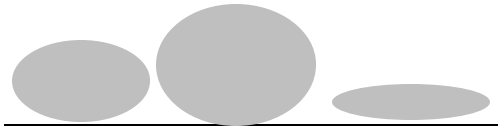


Nucleation:
Island formation

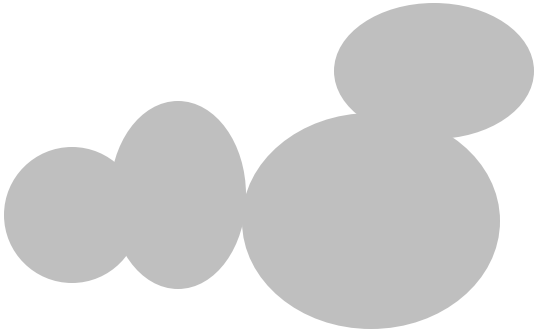
Deposition Process



Islands grow



Islands grow, cross-section



Islands merge

Continuous thin film

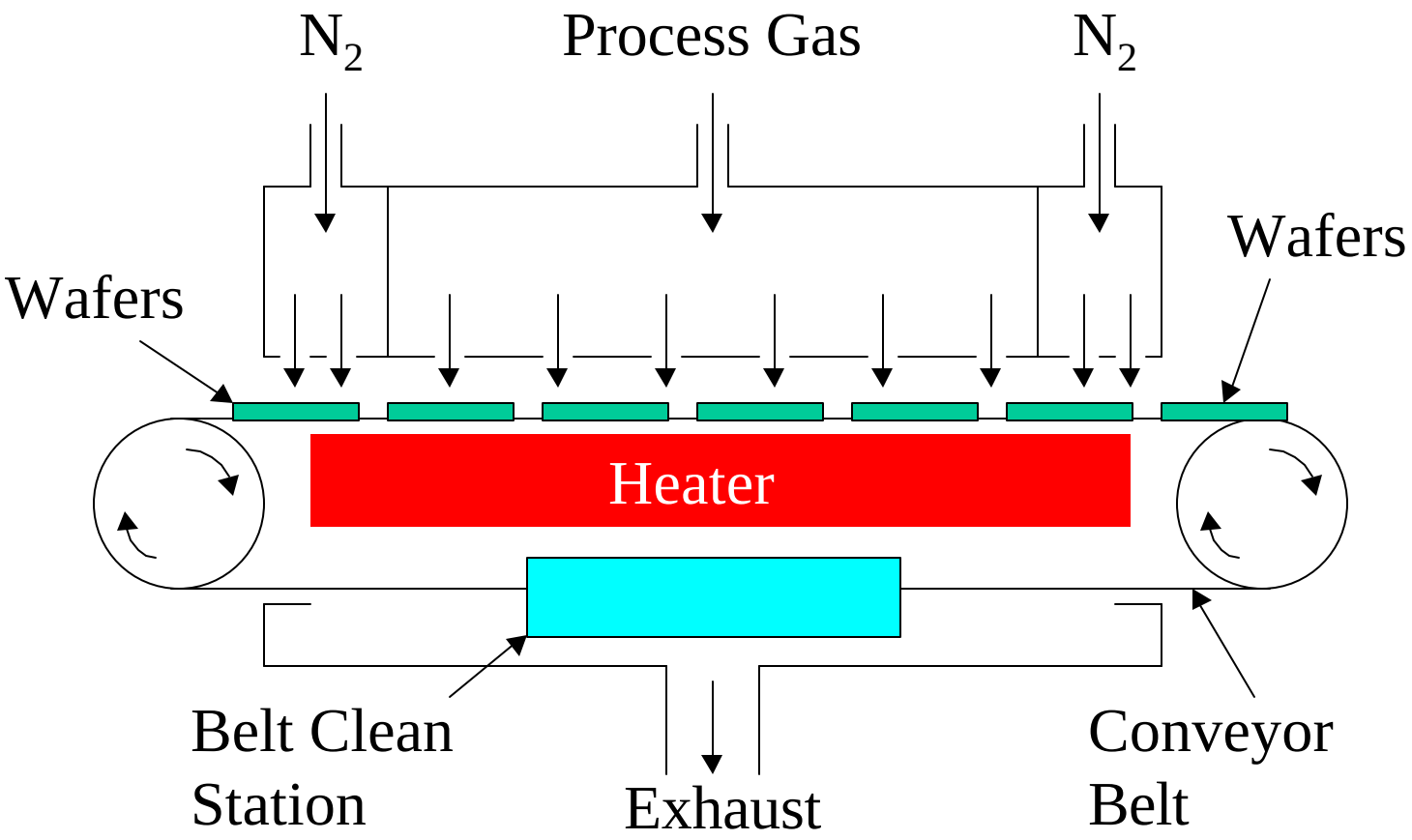
CVD Processes

- APCVD
- LPCVD
- PECVD

Atmospheric Pressure CVD

- CVD process taking place at atmospheric pressure
- APCVD process has been used to deposit silicon oxide and silicon nitride
- APCVD O_3-TEOS oxide process is widely used in the semiconductor industry, especially in STI and PMD applications
- Conveyor belt system with in-situ belt clean

APCVD Reactor



Question

- A semiconductor manufacturer has its R&D lab on the coast near sea level and one of its manufacturing fabs on a high altitude plateau. It was found that the APCVD processes developed in the R&D lab couldn’t directly apply in that particular fab. Why?

Answer

- On a high-altitude plateau, the atmospheric pressure is significantly lower than at sea level. Because earlier APCVD reactor didn’t have a pressure-control system, a process that worked fine in the R&D lab at sea level might not work well in the high altitude fab because of pressure difference

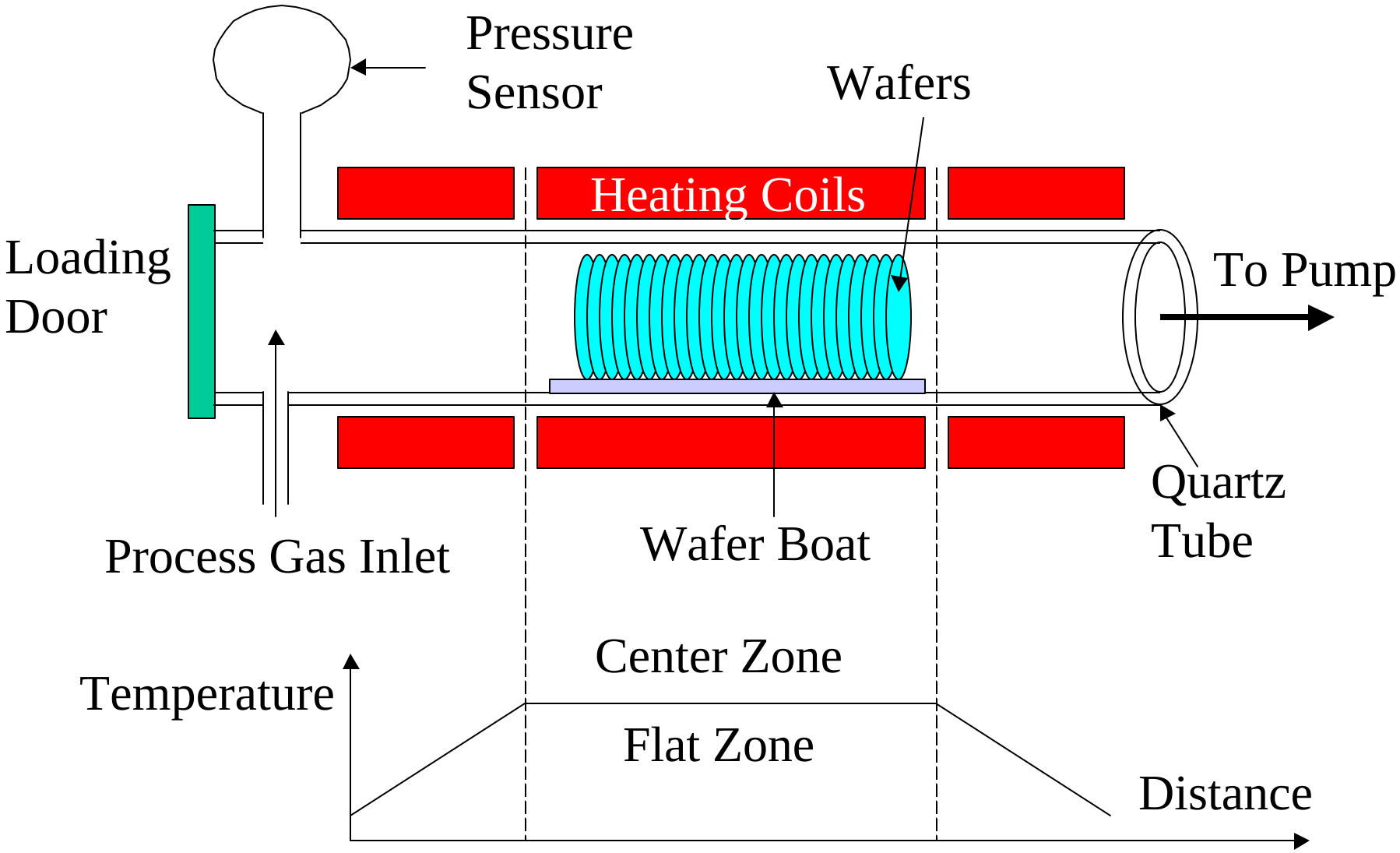
LPCVD

- Longer MFP
- Good step coverage & uniformity
- Vertical loading of wafer
- Fewer particles and increased productivity
- Less dependence on gas flow
- Vertical and horizontal furnace

Horizontal Conduction-Convection-heated LPCVD

- Adaptation of horizontal tube furnace
  - Low pressure: from 0.25 to 2 Torr
  - Used mainly for polysilicon, silicon dioxide and silicon nitride films
  - Can process 200 wafers per batch

LPCVD System

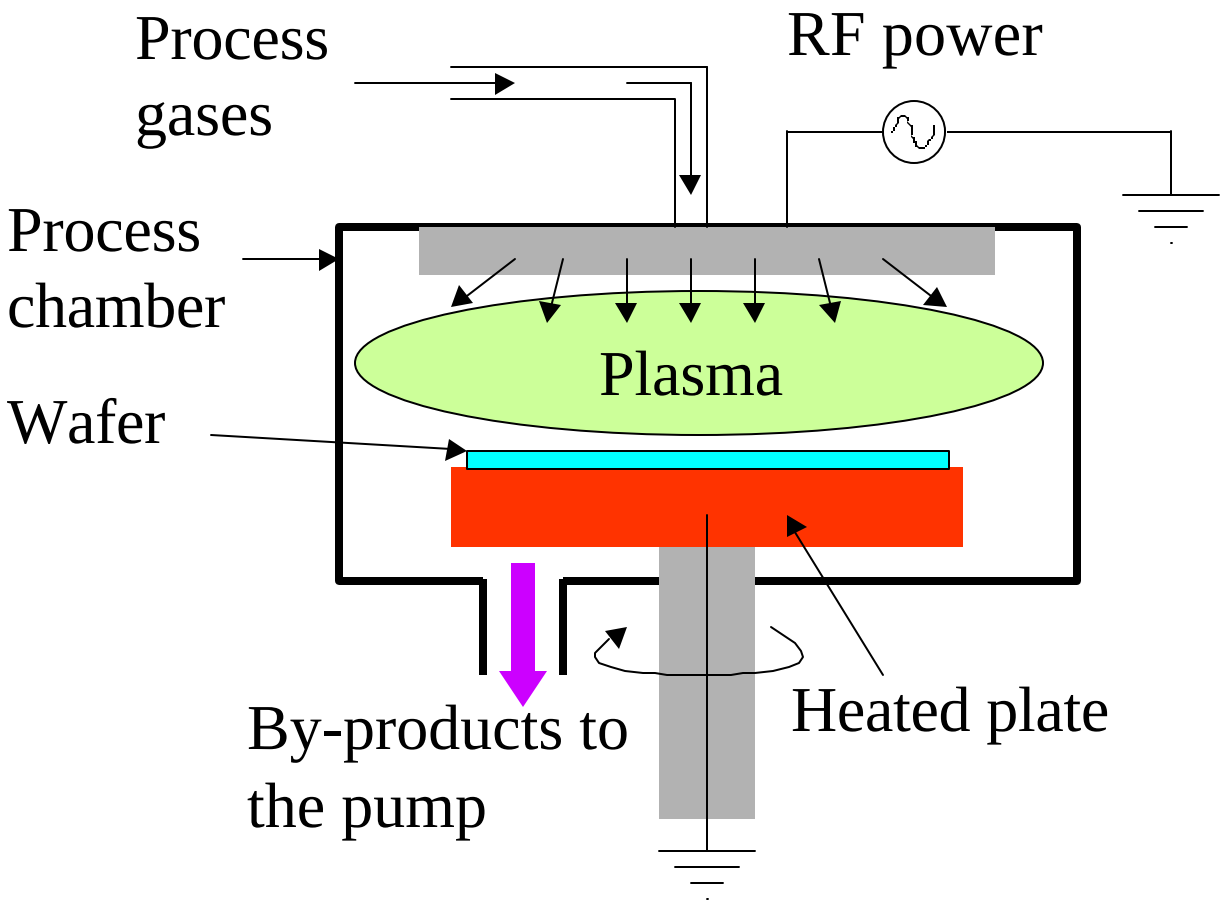


PECVD

- Developed when silicon nitride replaced silicon dioxide for passivation layer.

- High deposition rate at relatively low temp.
- RF induces plasma field in deposition gas
- Stress control by RF
- Chamber plasma clean.

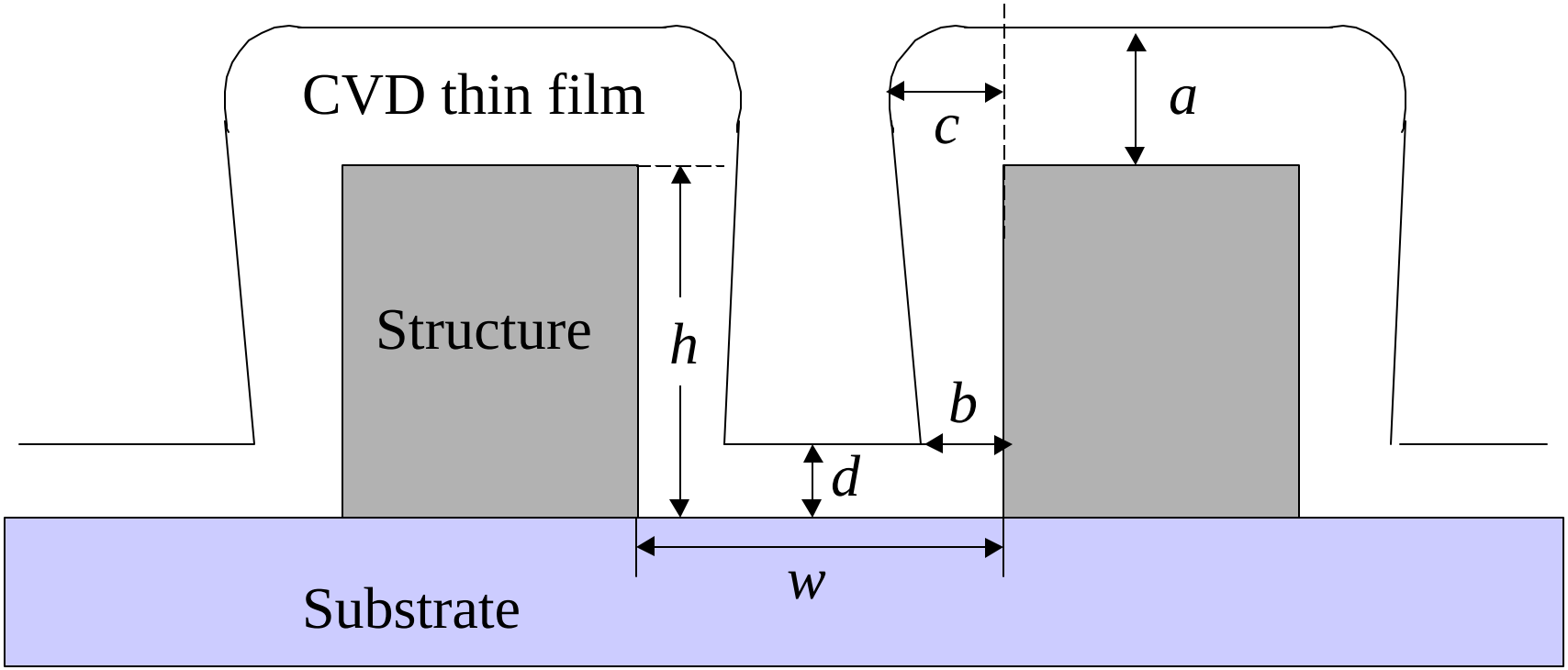
Plasma Enhanced CVD System



Step Coverage

- A measurement of the deposited film reproducing the slope of a step on the substrate surface
- One of the most important specifications
  - Sidewall step coverage
  - Bottom step coverage
  - Conformality
  - Overhang

Step Coverage and Conformity



Sidewall step coverage = b/a

Bottom step coverage = d/a

Conformity = b/c

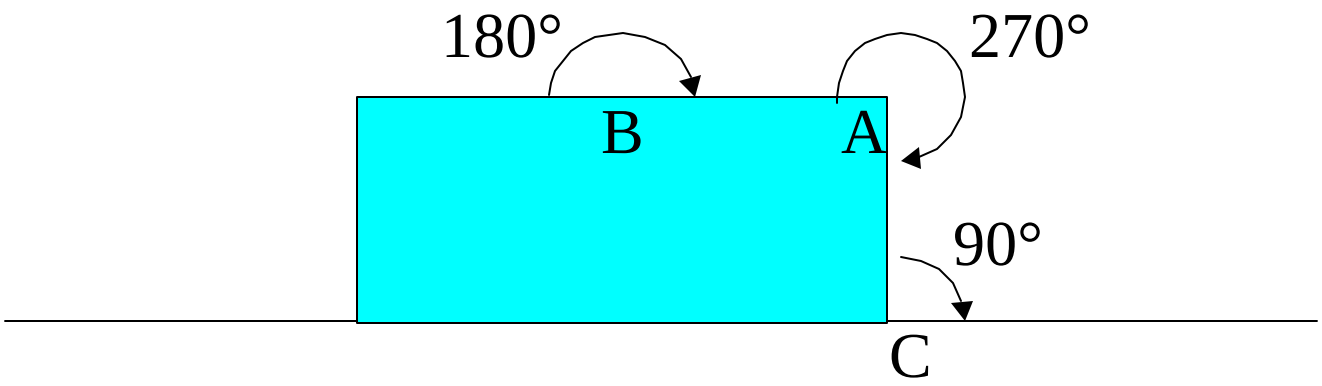
Overhang = $(c - b)/b$

Aspect ratio = h/w

Factors Affect Step Coverage

- Arriving angle of precursor
- Surface mobility of adsorbed precursor

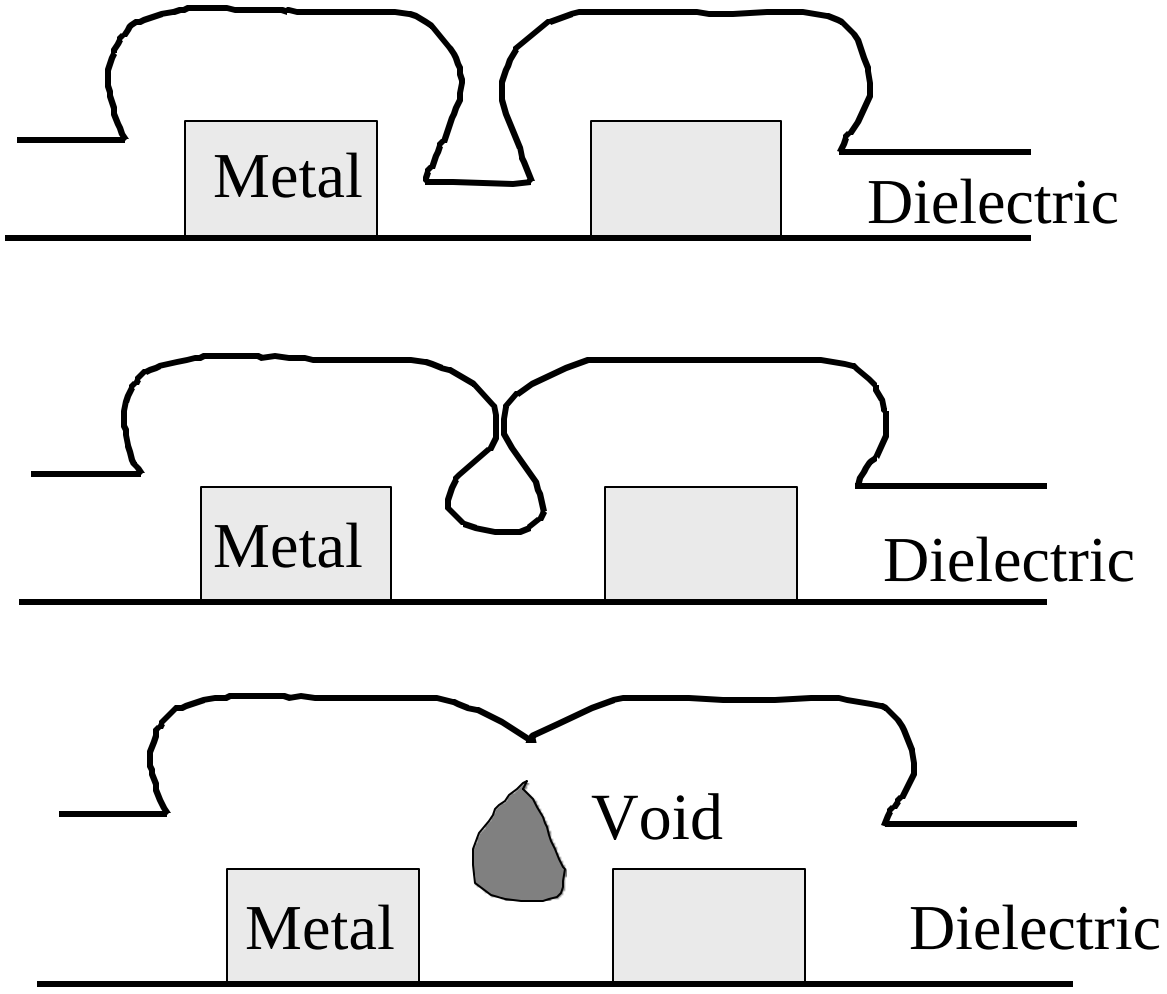
Arriving Angles



Arriving Angle

- Corner A: 270°, corner C: 90°
- More precursors at corner A
- More deposition
- Form the overhang
- Overhang can cause voids or keyholes

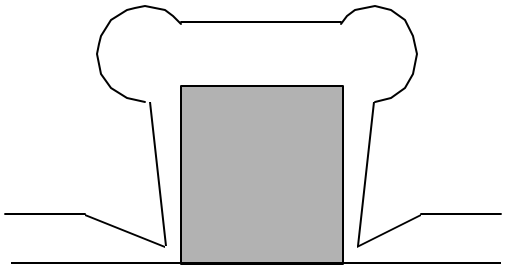
Void Formation Process



Control of Arriving Angle

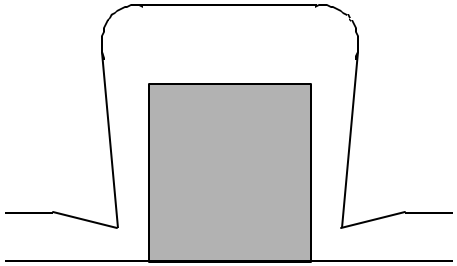
- |Changing pressure
- Tapering opening

Step Coverage, Pressure and Surface Mobility



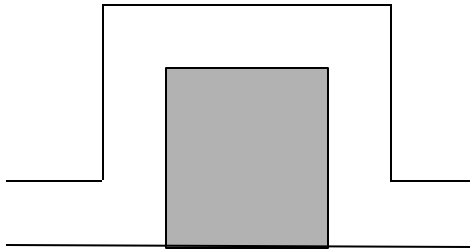
APCVD

No mobility



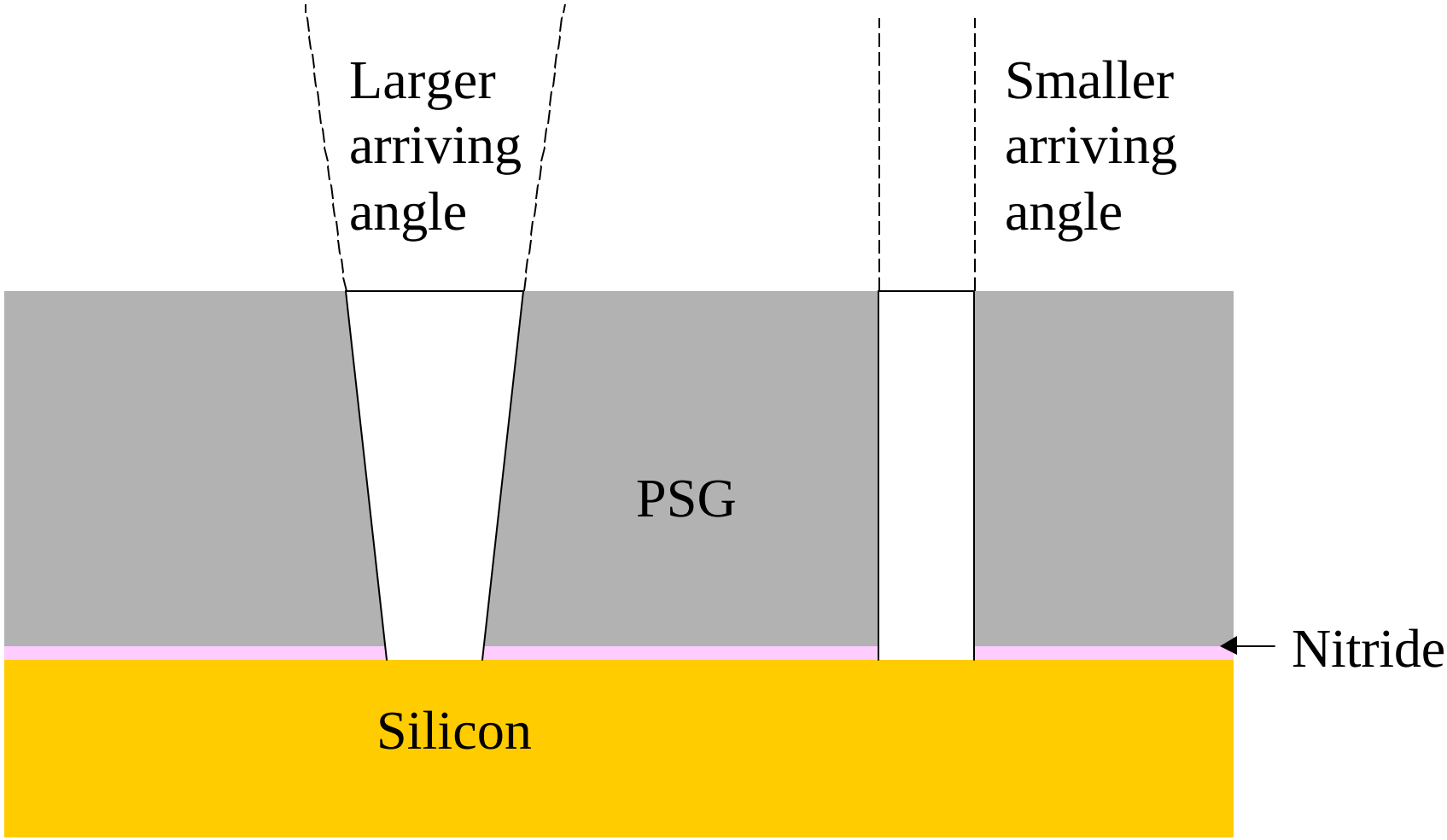
LPCVD

No mobility



High mobility

Arriving Angles, Contact Holes



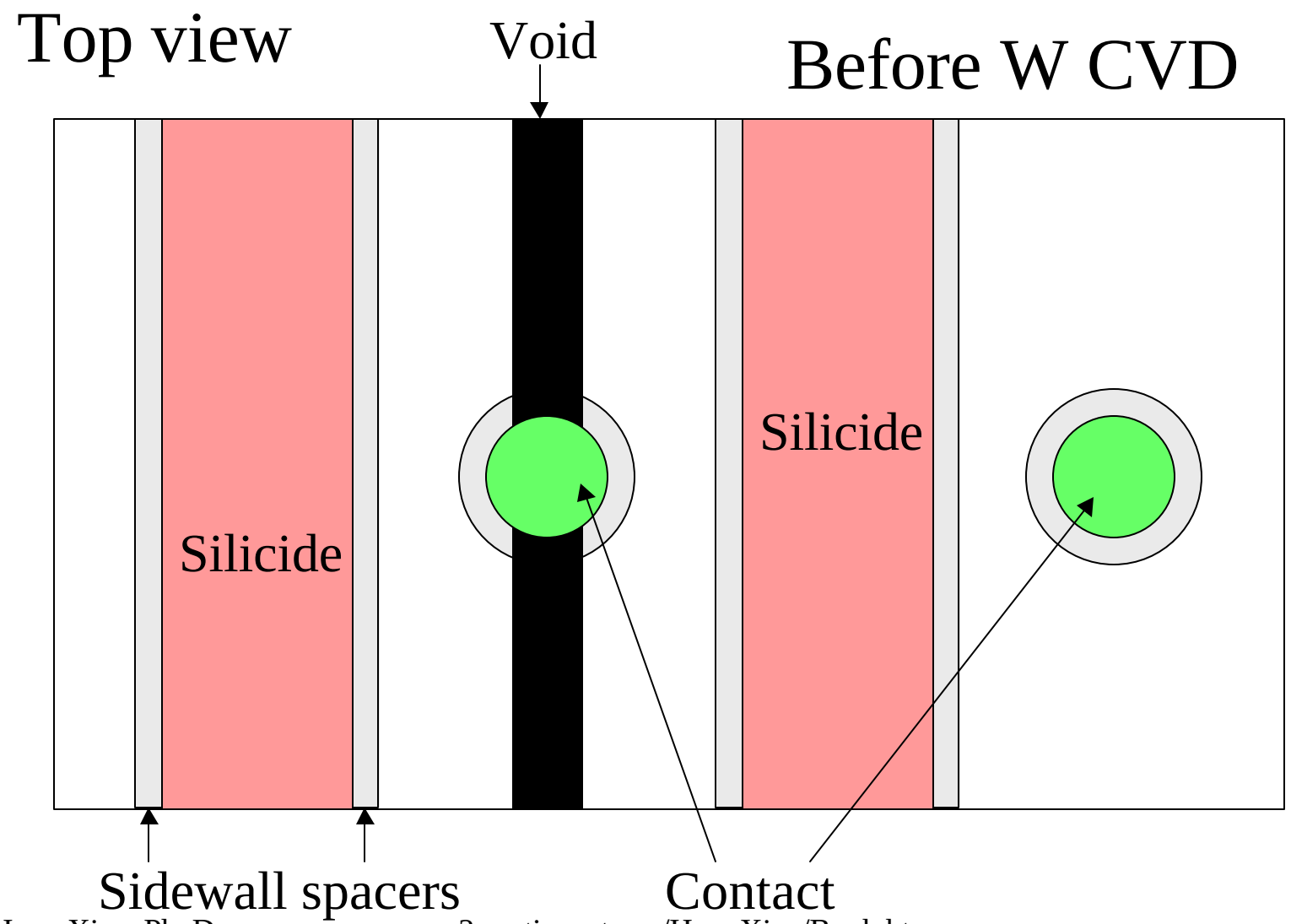
Gap Fill

- Fill a gap without voids
- Voids: cause defect and reliability problems
- Deposition/Etchback/Deposition
  - Silane and PE-TEOS film
- Conformal deposition
  - O_3-TEOS and tungsten CVD
- High density plasma CVD

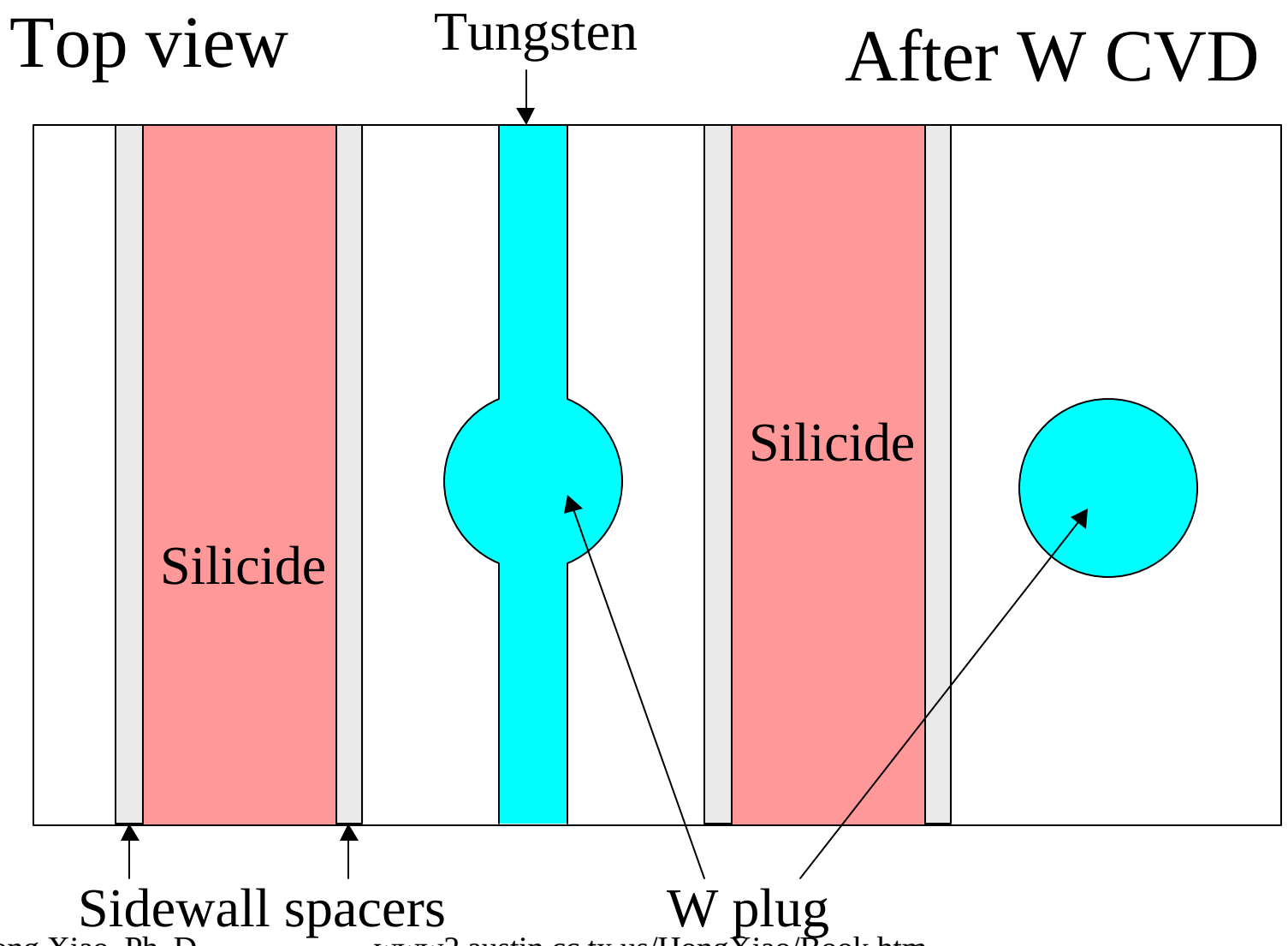
Gap Fill

- PMD: zero tolerance voids
  - Tungsten can be deposited into these voids
  - Causing shorts
- IMD: voids below metal may tolerable
  - reducing κ
  - process gas could come out later and cause reliability problem

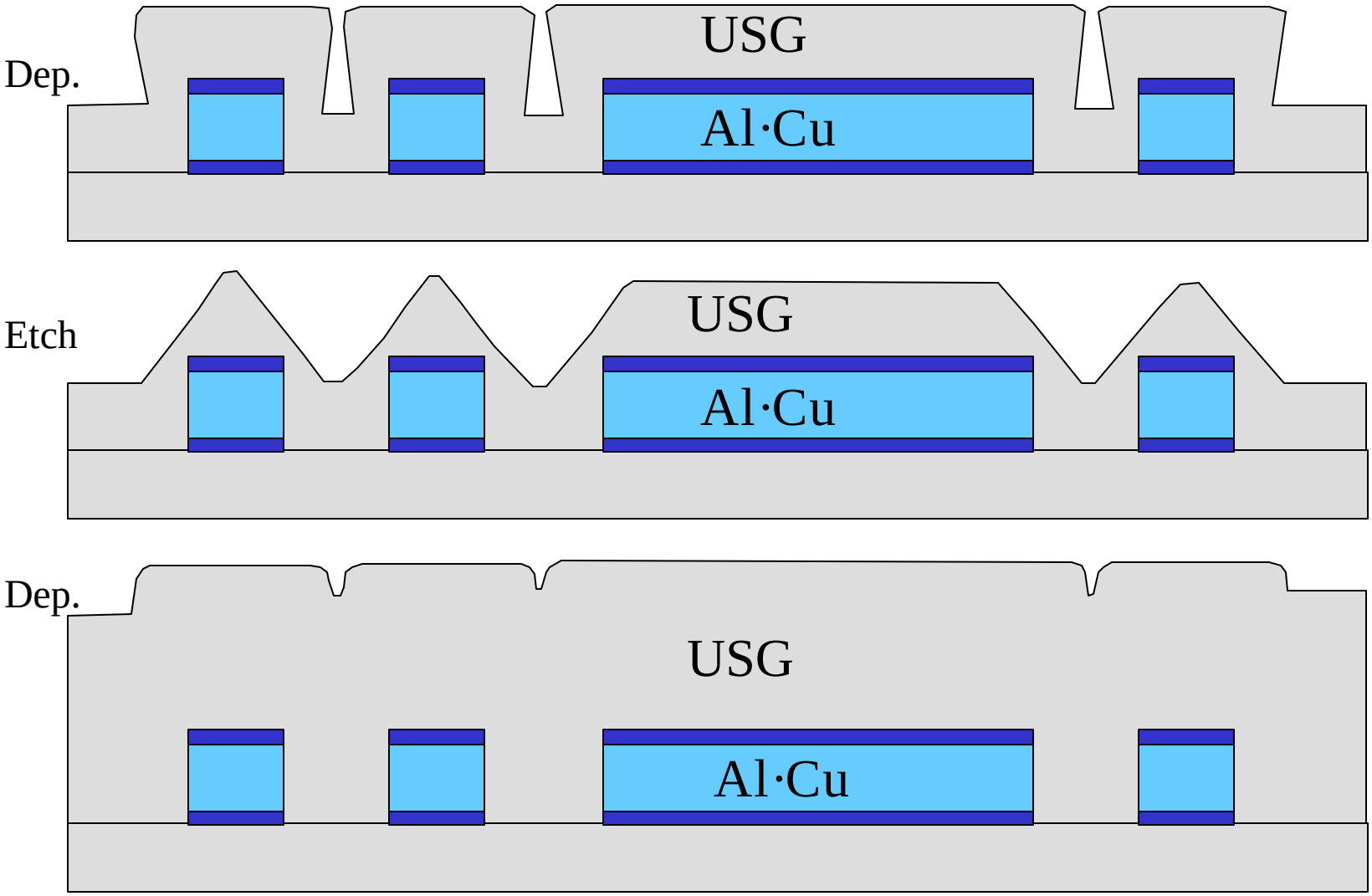
Void in PMD


Top view
Void
Before W CVD
Silicide
Silicide
Sidewall spacers
Contact

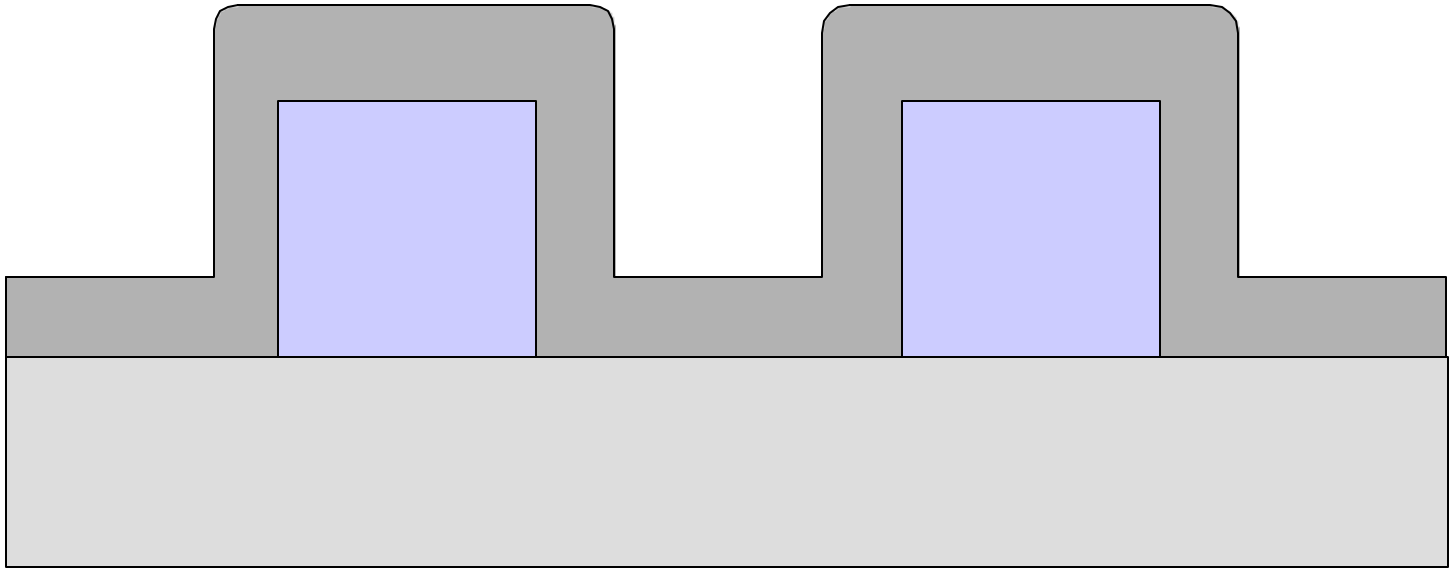
Unwanted W Line Between Gates



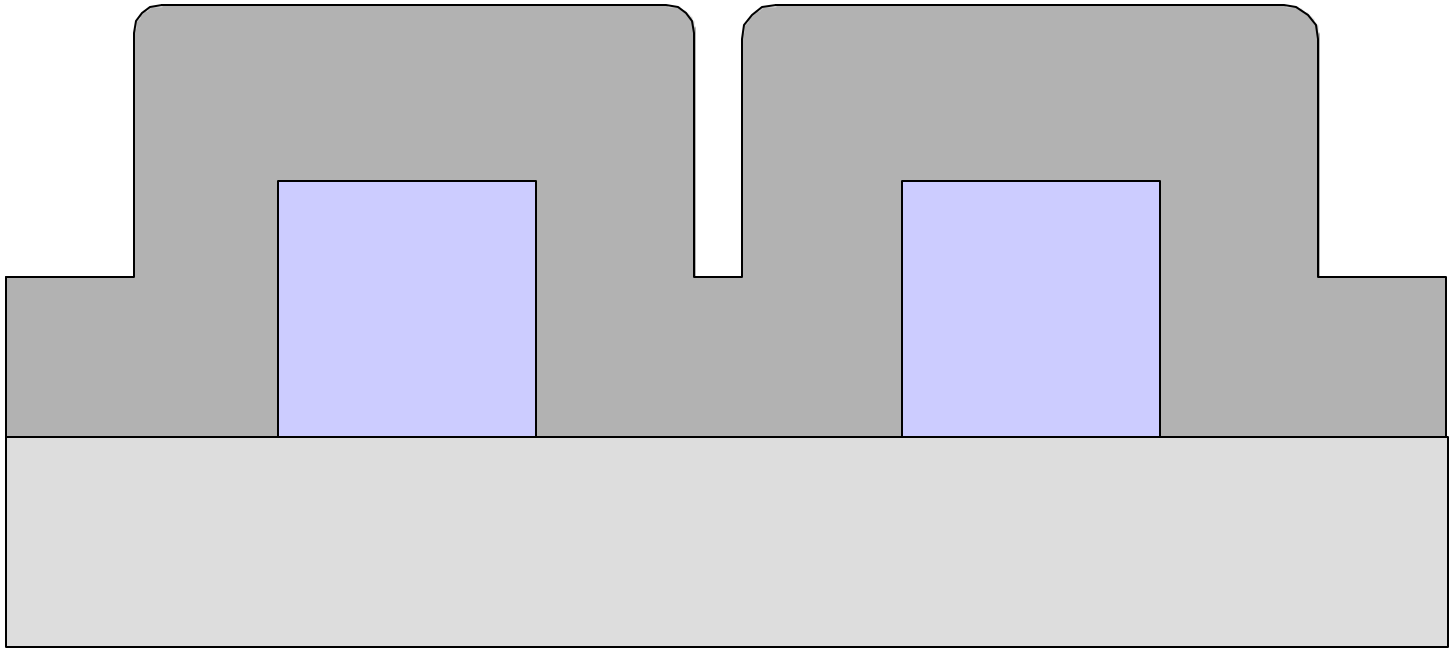
Deposition/Etchback/Deposition



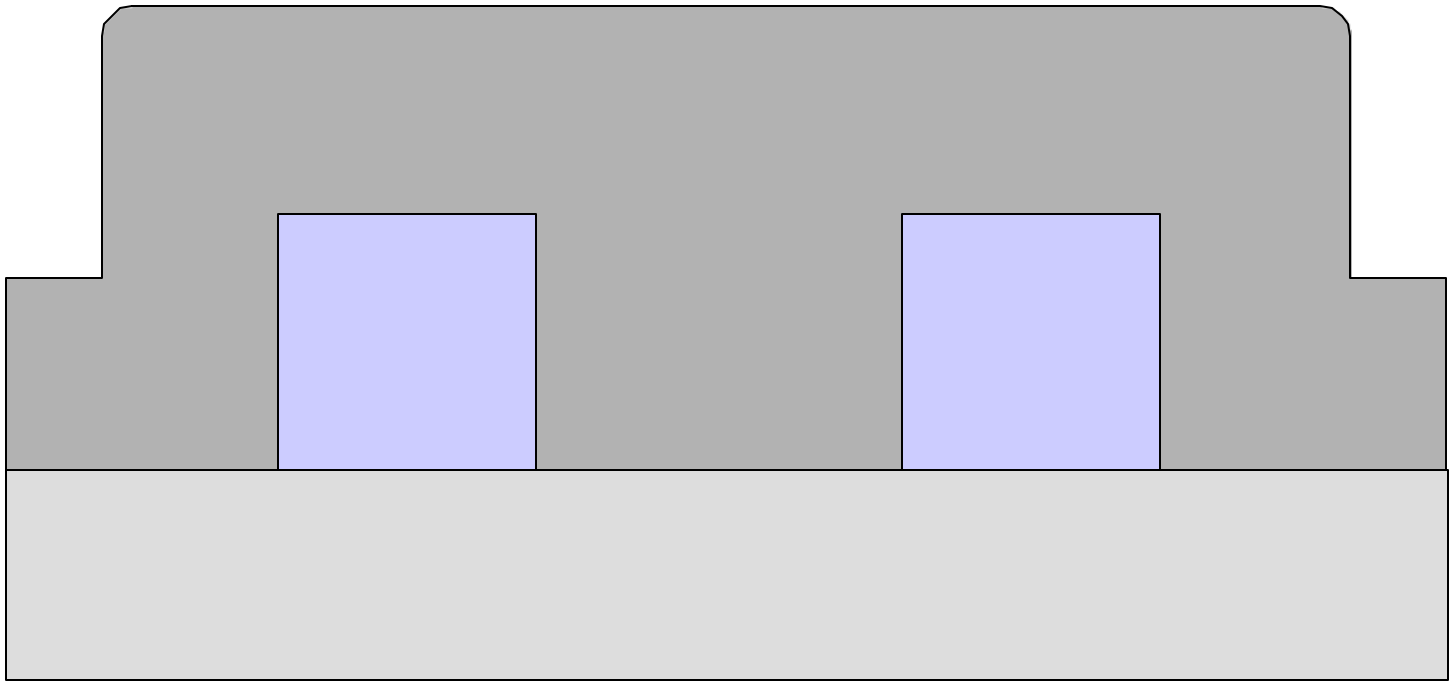
Conformal Deposition Gap Fill



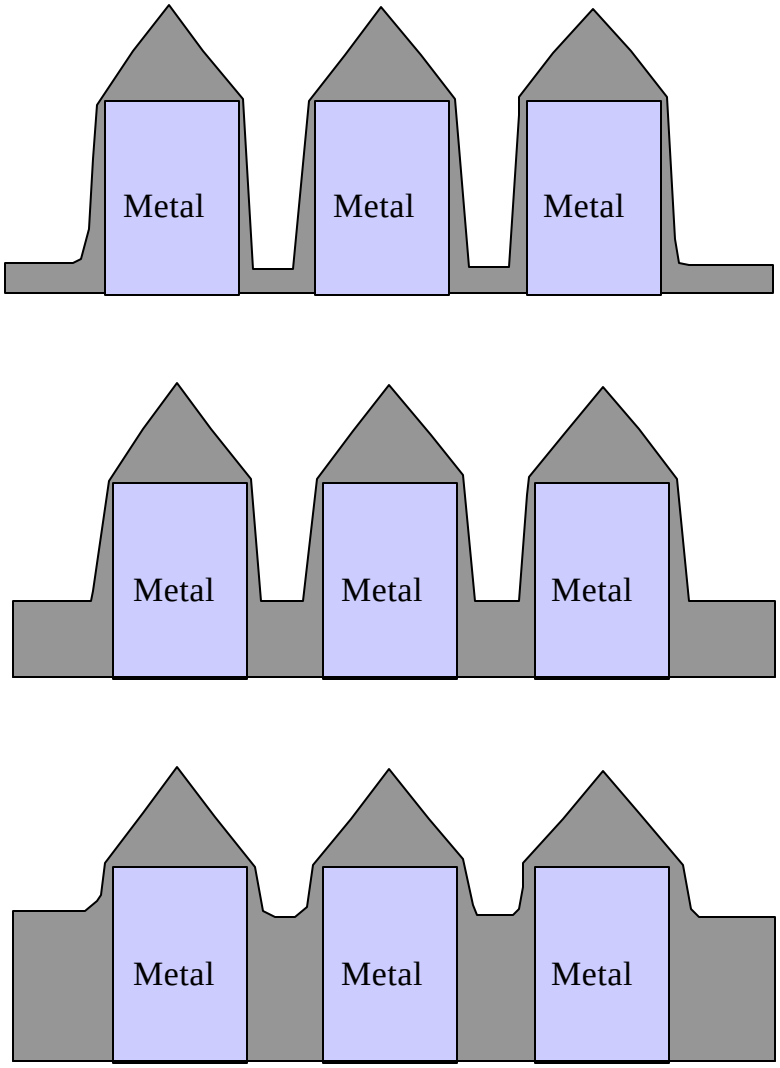
Conformal Deposition Gap Fill



Conformal Deposition Gap Fill



HDP CVD Gap Fill



Surface Adsorption

- Determine precursors surface mobility
- Affect step coverage and gap fill

- Physical adsorption (physisorption)
- Chemical adsorption (chemisorption)

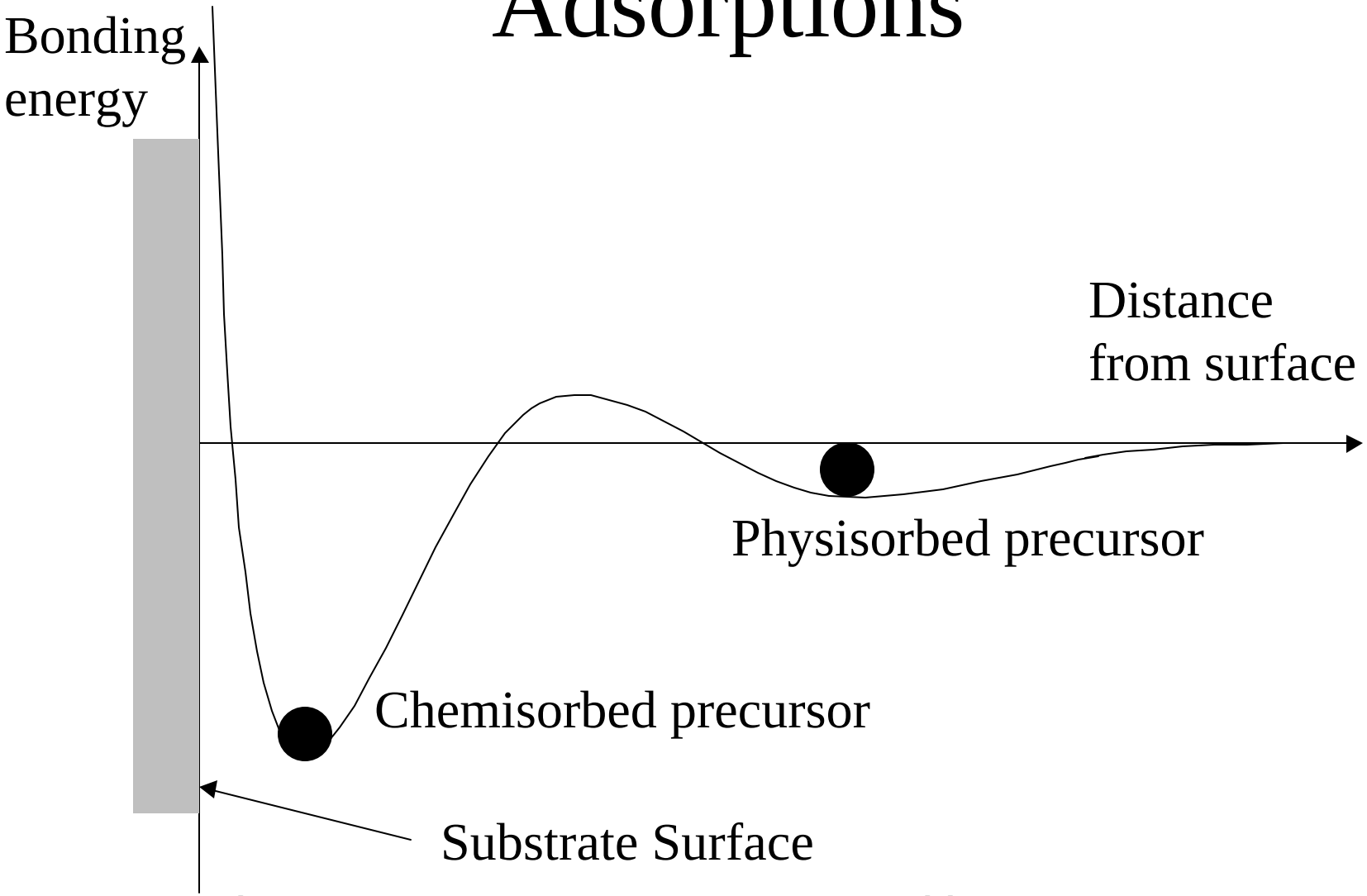
Chemisorption

- Actual chemical bonds between surface atom and the adsorbed precursor molecule
- Bonding energy usually exceeding 2 eV
- Low surface mobility
- Ion bombardment with10 to 20 eV energy in PECVD processes can cause some surface migration of chemisorbed precursors

Physisorption

- Weak bond between surface and precursor
- Bonding energy usually less than 0.5 eV
  - Hydrogen bonding
  - Van der Waals forces
- Ion bombardment and thermal energy at 400 °C can cause migration of physisorbed precursors
- High surface mobility

Adsorptions



Dielectric CVD Precursors

- Silane (SiH_4)
- TEOS (tetra-ethyl-oxy-silane, $Si(OC_2H_5)_4$)

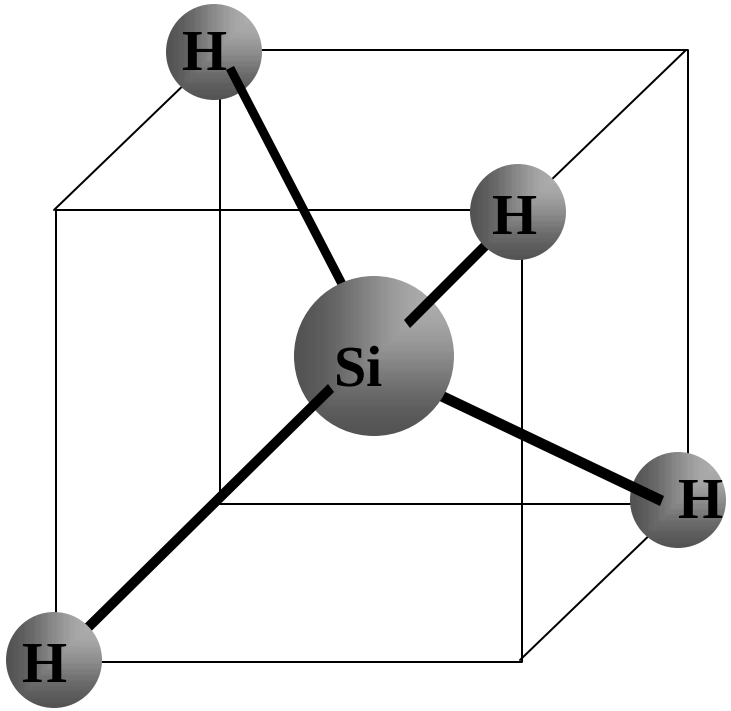
CVD Precursor: Silane

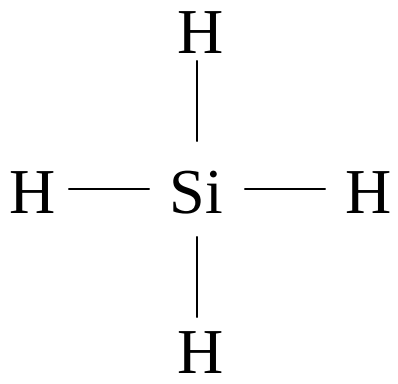
- Dielectric CVD
  - PECVD passivation dielectric depositions
  - PMD barrier nitride layer
  - Dielectric anti reflective coating (DARC)
  - High density plasma CVD oxide processes
- LPCVD poly-Si and silicon nitride
- Metal CVD
  - W CVD process for nucleation step
  - Silicon source for WSi_x deposition

Dielectric CVD Precursor: Silane

- Pyrophoric (ignite itself), explosive, and toxic
- Open silane line without thoroughly purging can cause fire or minor explosion and dust line

Structure of Silane Molecule





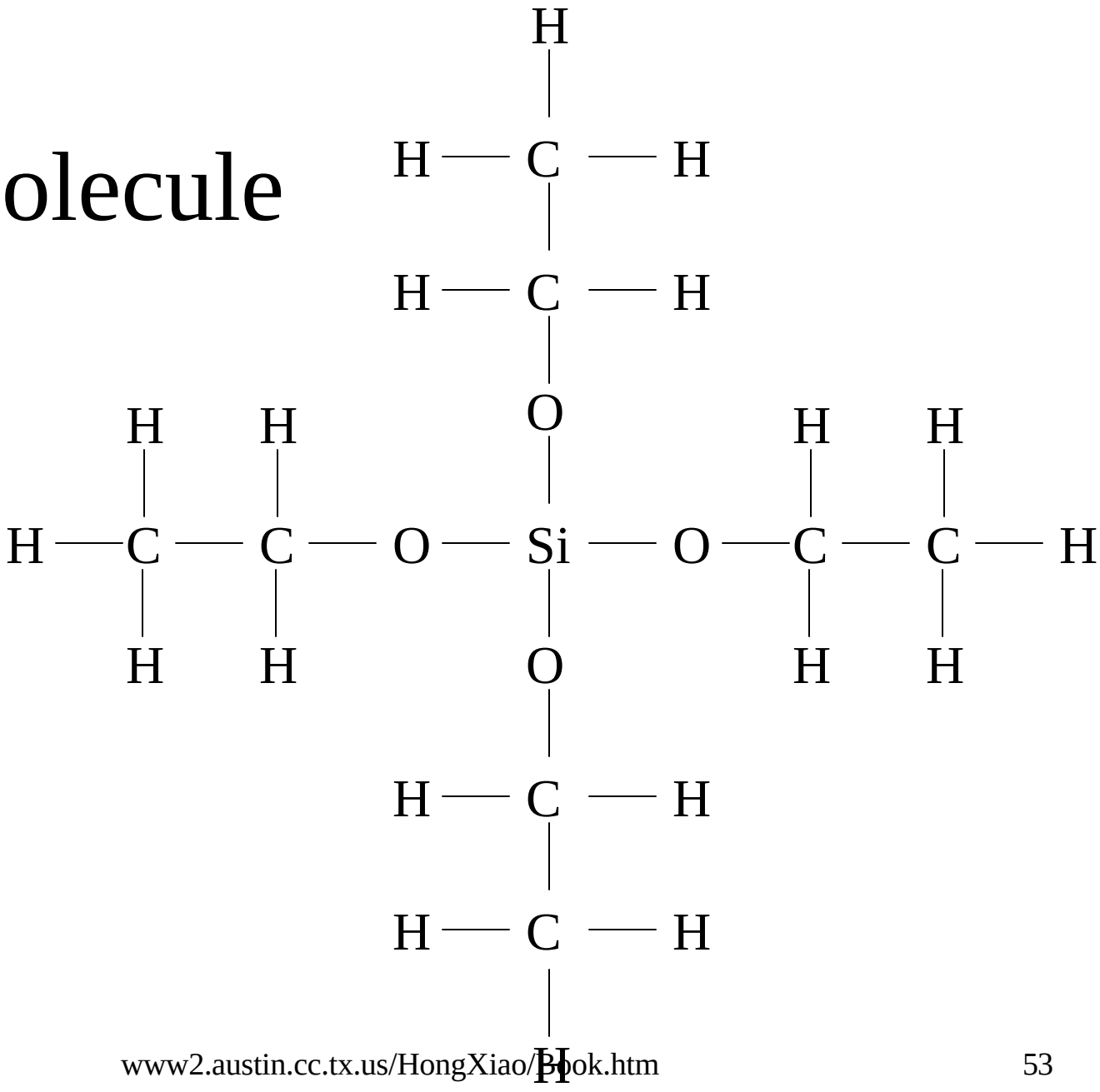
CVD Precursor Adsorption: Silane

- Silane molecule is perfectly symmetrical
- Neither chemisorb nor physisorb
- Fragments of silane, SiH_3, SiH_2, or SiH, can easily form chemical bonds with surface
- Low surface mobility, overhangs and poor step coverage

CVD Precursor Adsorption: TEOS

- TEOS (tetra-ethyl-oxy-silane, $Si(OC_2H_5)_4$)
- Big organic molecule
- TEOS molecule is not perfectly symmetric
- Can form hydrogen bond and physisorb
- High surface mobility
- Good step coverage, conformality, and gap fill
- Widely used for oxide deposition

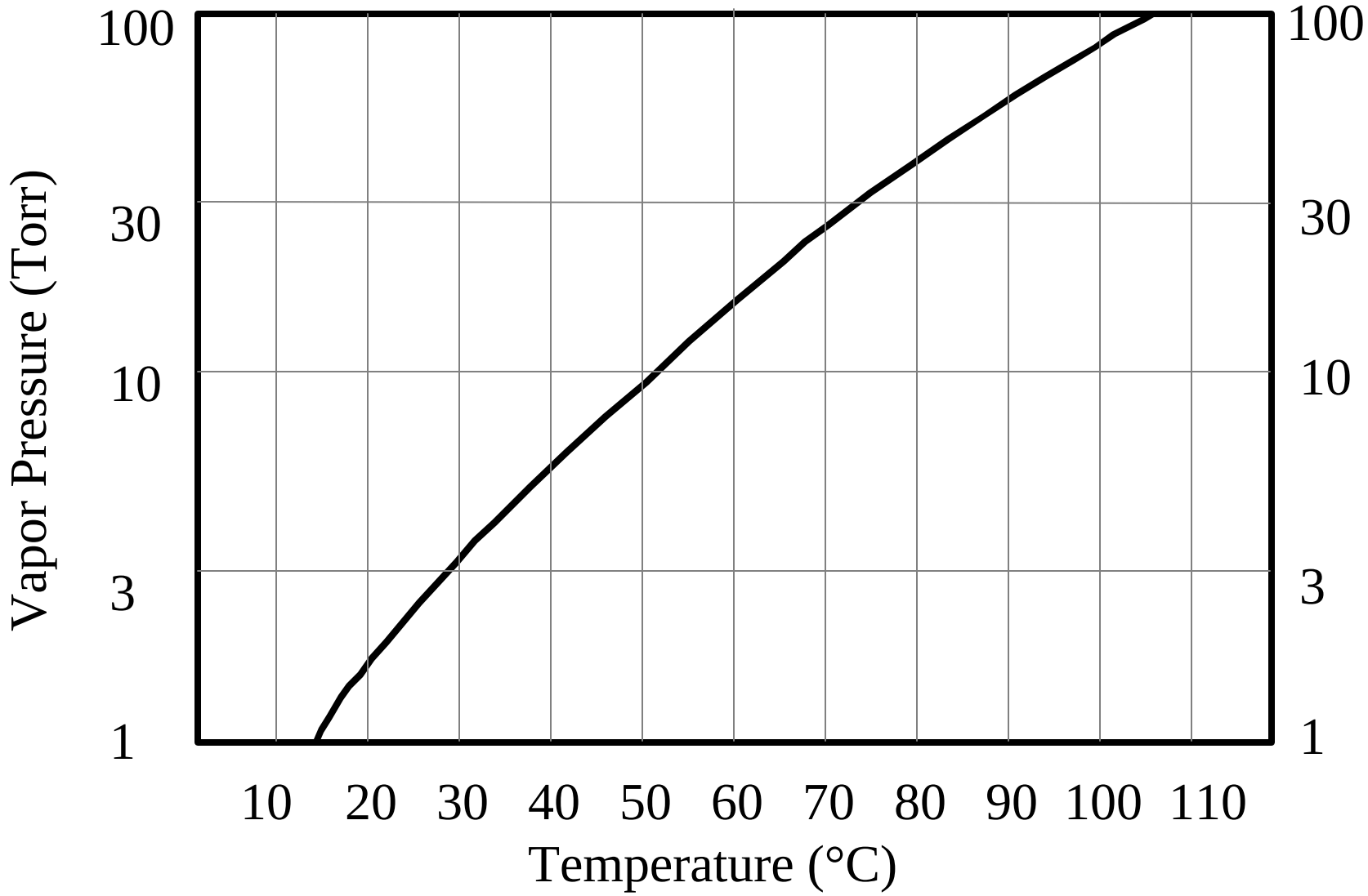
TEOS Molecule



TEOS Applications

- STI, sidewall spacer, PMD, and IMD
- Most dielectric CVD processes are TEOS based oxide processes

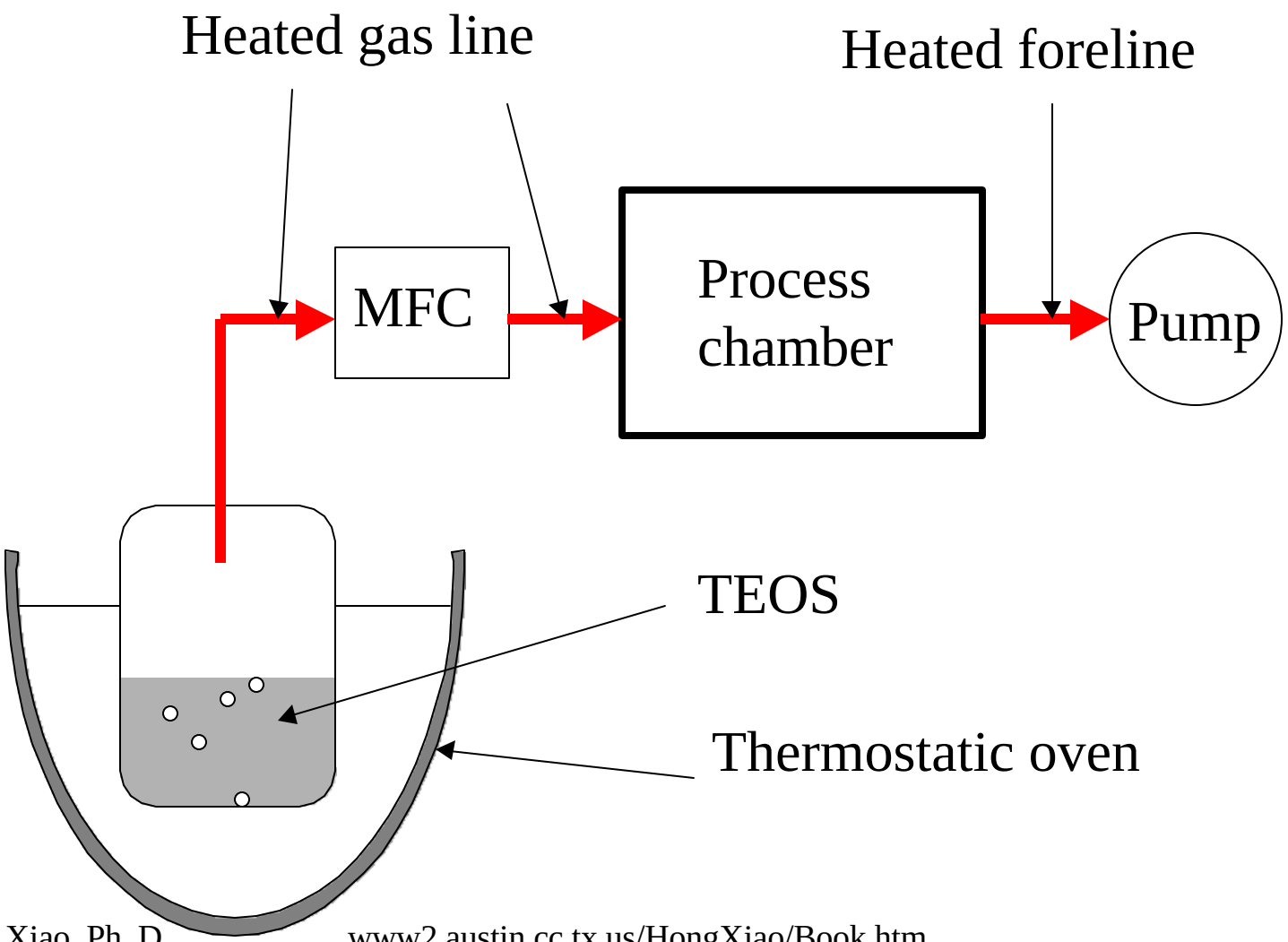
TEOS Vapor Pressure



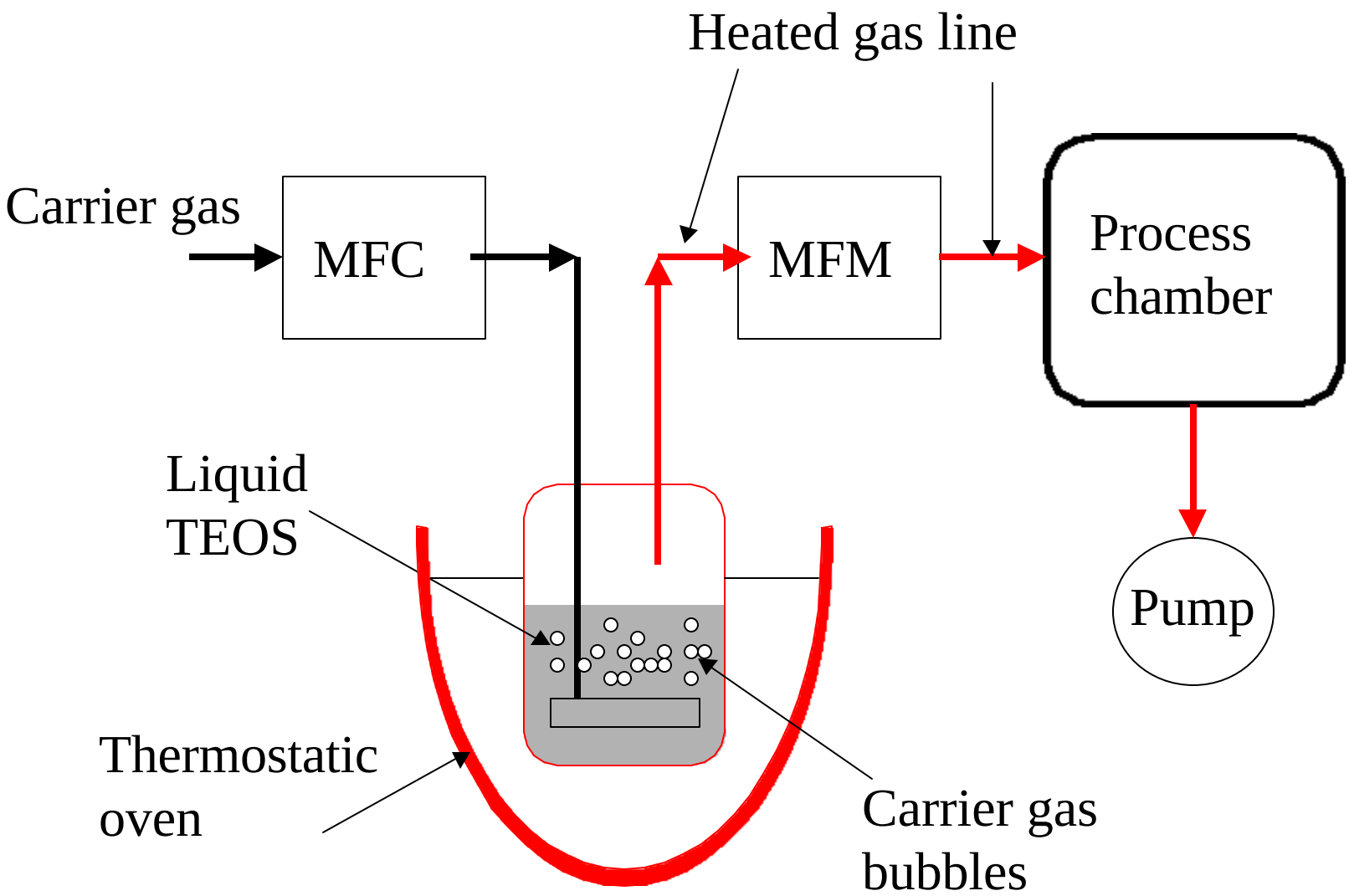
TEOS Delivery

- A liquid at room temperature with boiling point at the sea level is 168 °C
  - As a reference, boiling point of water (H_2O) at sea level is 100 °C
- Need delivery system to send its vapor to process chamber
- Boiler, bubbler, and injection systems

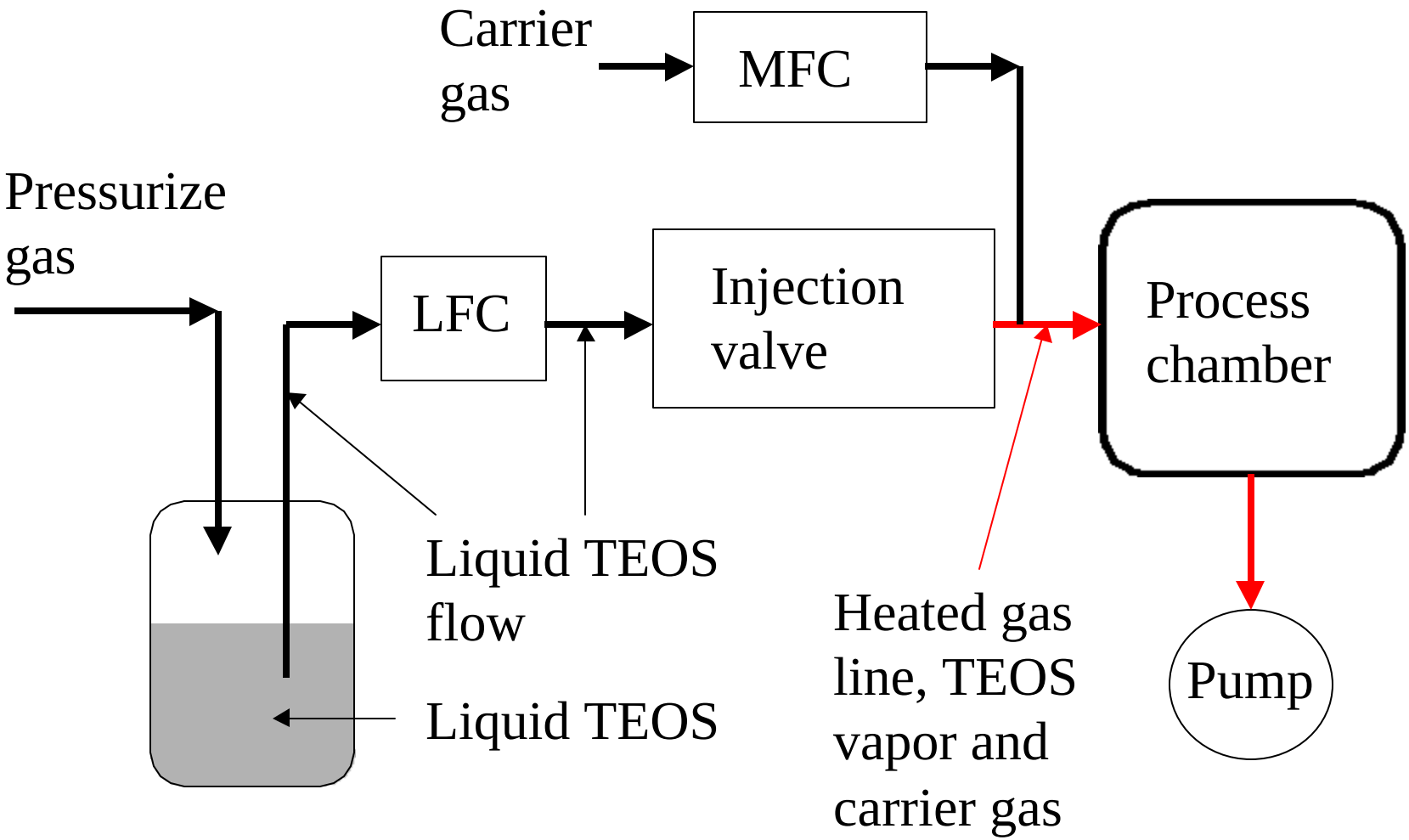
Boiler System



Bubbler System



Injection System



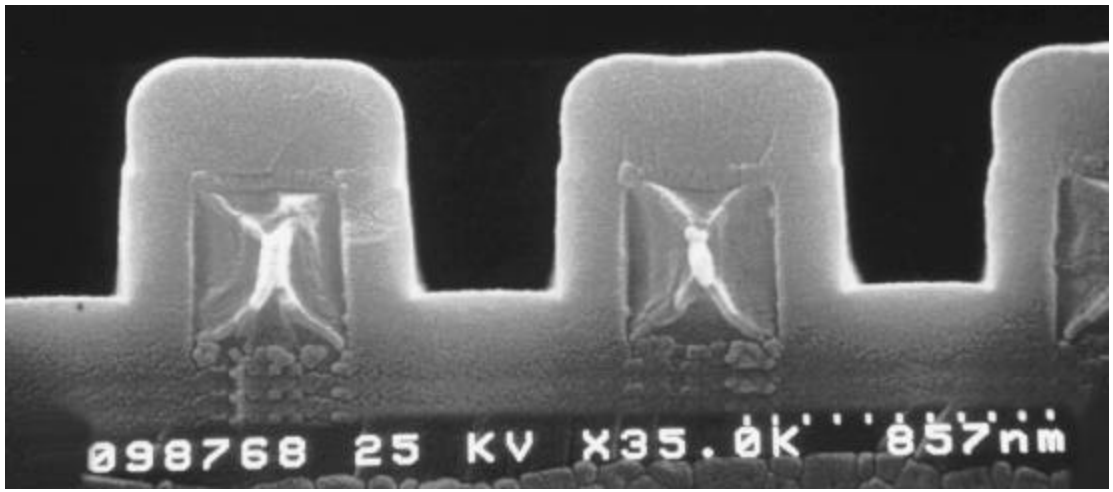
Sticking Coefficient

- The probability that precursor atom forms chemical bond with surface atom in one collision
- Can be calculated by comparing the calculated deposition rate with 100% sticking coefficient and the measured actual deposition rate

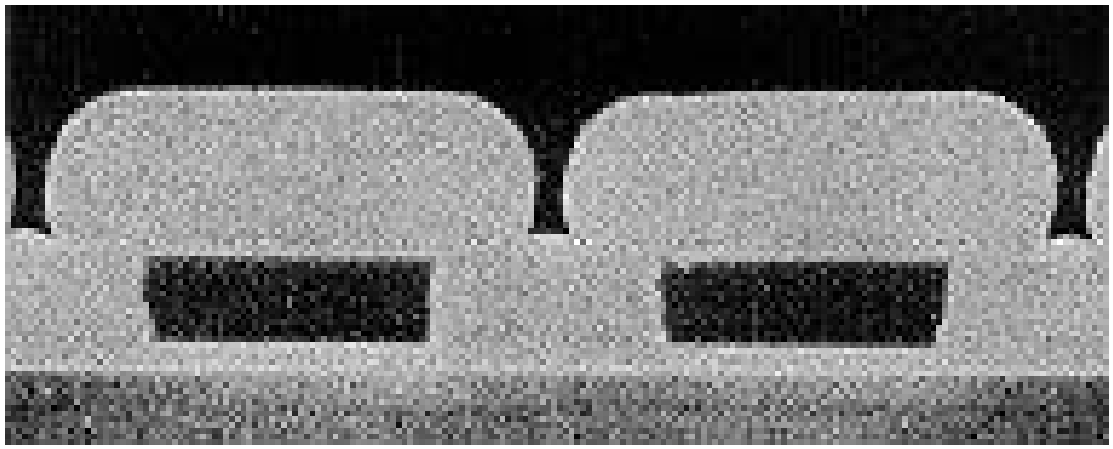
Sticking Coefficient

Precursors	Sticking Coefficient
SiH_4	3×10^{-4} to 3×10^{-5}
SiH_3	0.04 to 0.08
SiH_2	0.15
SiH	0.94
TEOS	10^{-3}
WF_6	10^{-4}

Step Coverage of TEOS and Silane Oxide



TEOS



Silane

Question

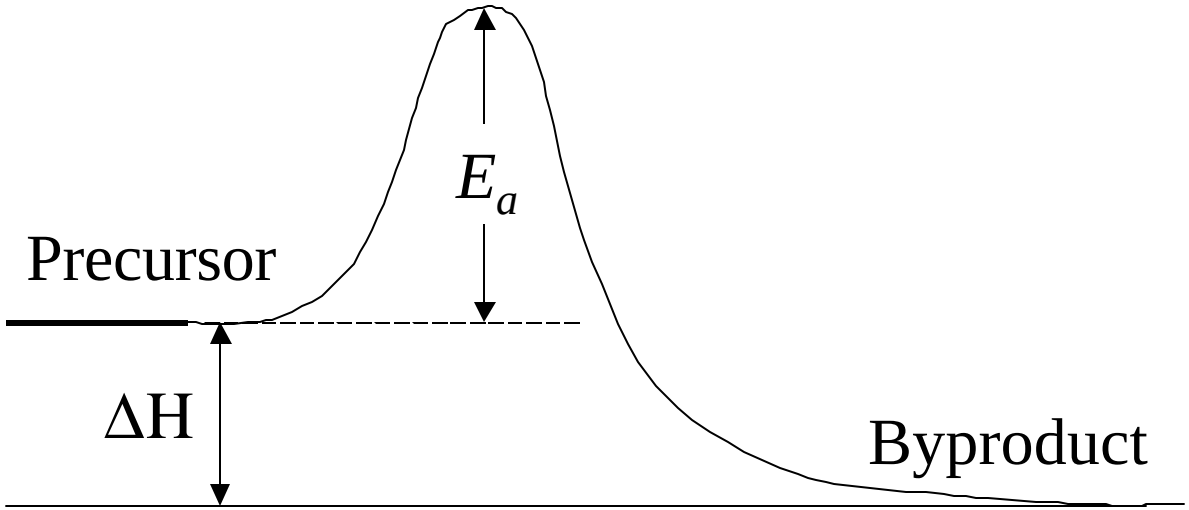
- Why don’t people apply TEOS as the silicon source gas for the silicon nitride deposition to get better step coverage for the nitride film

Answer

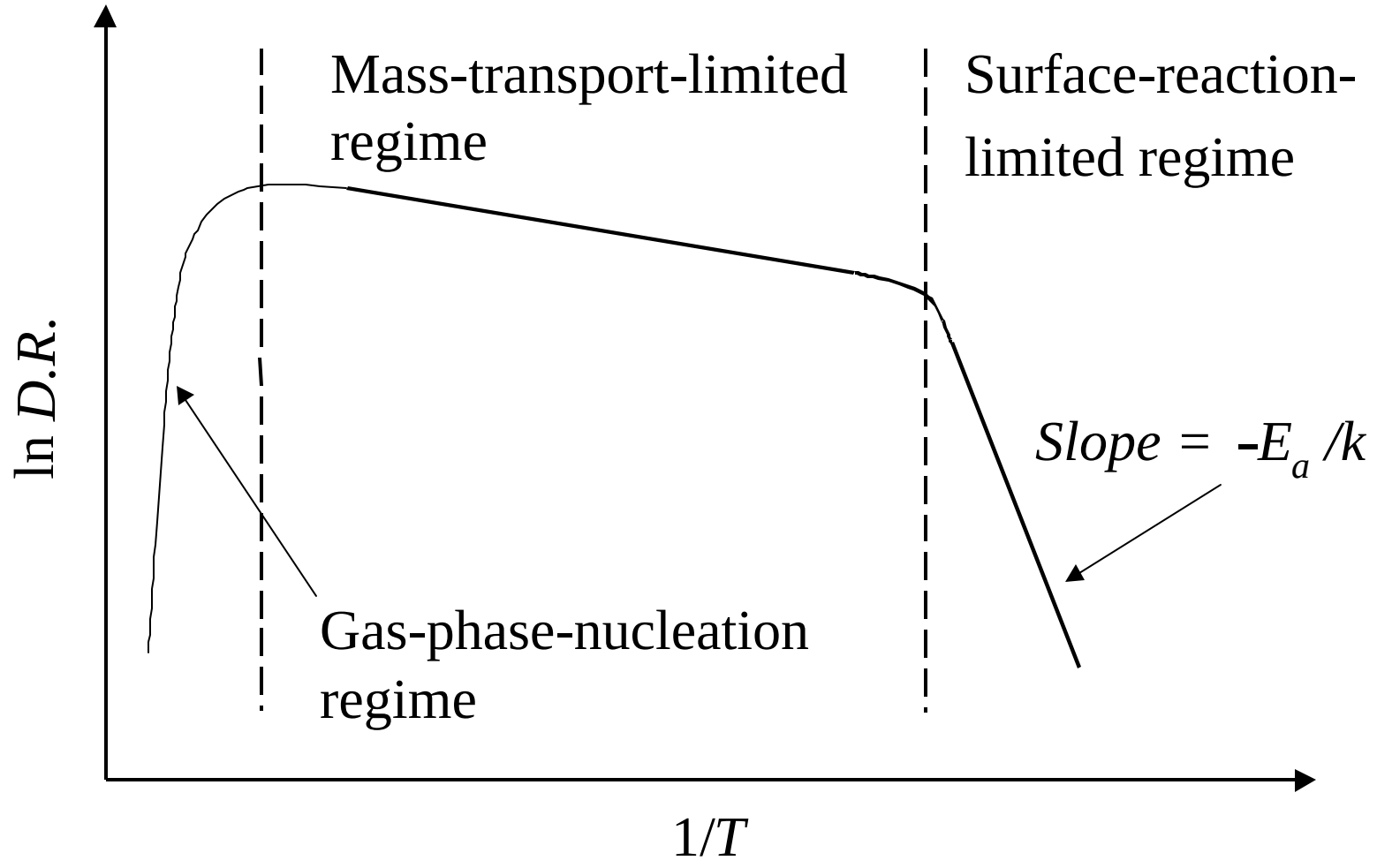
- In the TEOS molecule, the silicon atom is bonded with four oxygen atoms. It is almost impossible to strip all oxygen atoms and have silicon bonded only with nitrogen. Therefore, TEOS is mainly used for the oxide deposition and the nitride deposition normally uses silane as the silicon source gas

Chemical Reaction Rate

$$C.R. = A \exp(-E_a/kT)$$



Deposition Regimes



Surface-Reaction-Limited Regime

- Chemical reaction rate can't match precursor diffusion and adsorption rates; precursors pile up on the substrate surface and wait their turn to react.

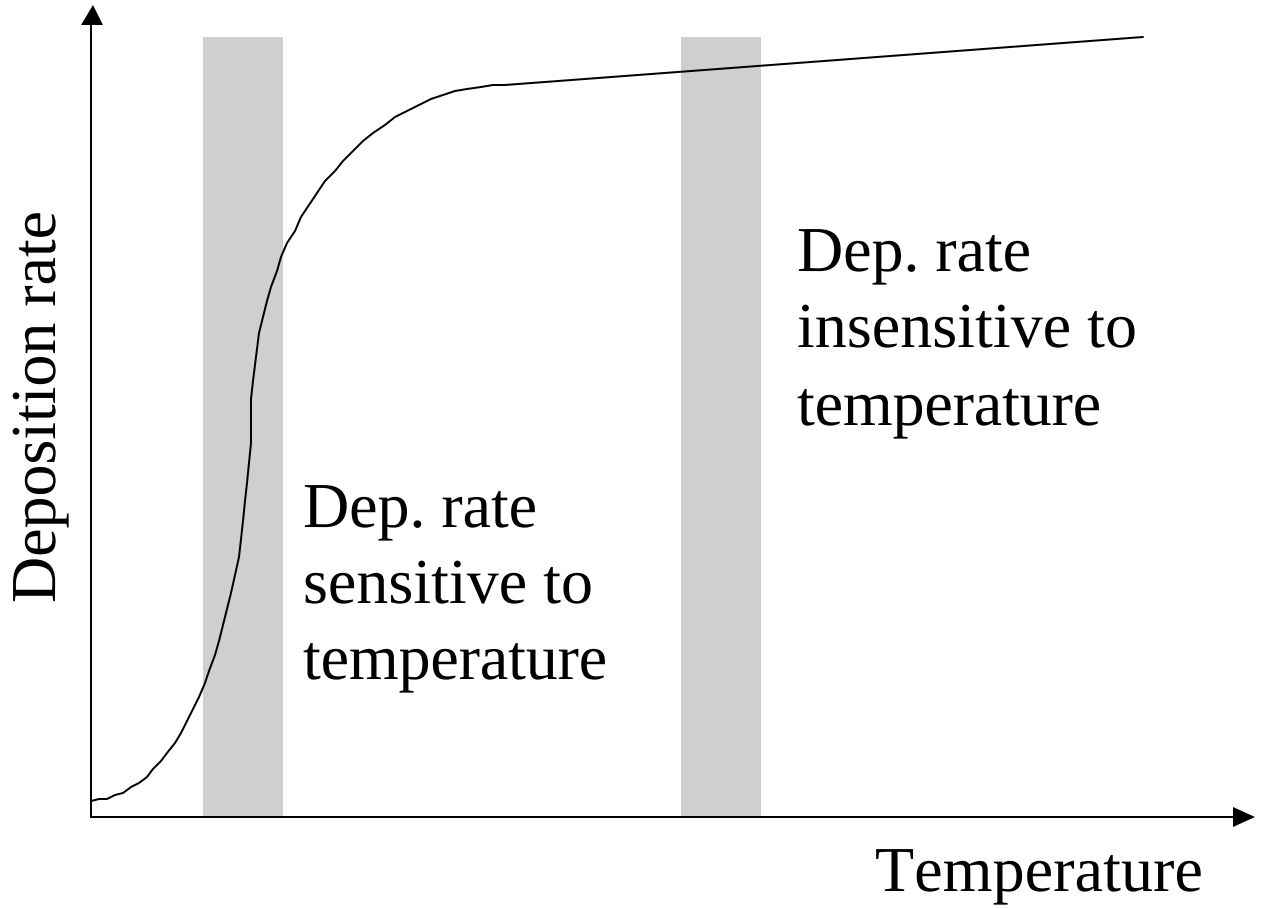
$$D.R. = C.R.\,[B]\,[C]\,[]\ldots$$

- Deposition rate is very sensitive to temperature

Mass-Transport-Limited Regime

- When the surface chemical reaction rate is high enough, the chemical precursors react immediately when they adsorb on the substrate surface.
- *Deposition rate = D dn/dx [B] [C] []…*
- Deposition rate is insensitive to temperature
- Mainly controlled by gas flow rates

Deposition Rage Regimes



CVD Reactor Deposition Regime

- Most single wafer process reactors are designed in mass-transport-limited regime
- It is easier to control the gas flow rate
- Plasma or unstable chemicals such as ozone are used to achieve mass-transport-limited-regime at relatively low temperature

Applications of Dielectric Thin film

- Shallow trench isolation (STI, USG)
- Sidewall Spacer (USG)
- Pre-metal dielectric (PMD, PSG or BPSG)
- Inter-metal dielectric (IMD, USG or FSG)
- Anti-reflection coating (ARC, SiON)
- Passivation dielectric (PD, Oxide/Nitride)

Dielectric CVD, Oxide and Nitride

Oxide (SiO_2)	**Nitride (Si_3N_4)**
Similar dielectric strength, > 1×10^7 V/cm	Similar dielectric strength, > 1×10^7 V/cm
Lower dielectric constant, $\kappa = 3.9$	Higher dielectric constant, $\kappa = 7.0$
Not a good barrier for moisture and mobile ion (Na^+)	Good barrier for moisture and mobile ion (Na^+)
Transparent to UV	Conventional nitride opaque to UV
Can be doped with P and B	

Shallow Trench Isolation (STI)

Grow pad oxide
Deposition nitride

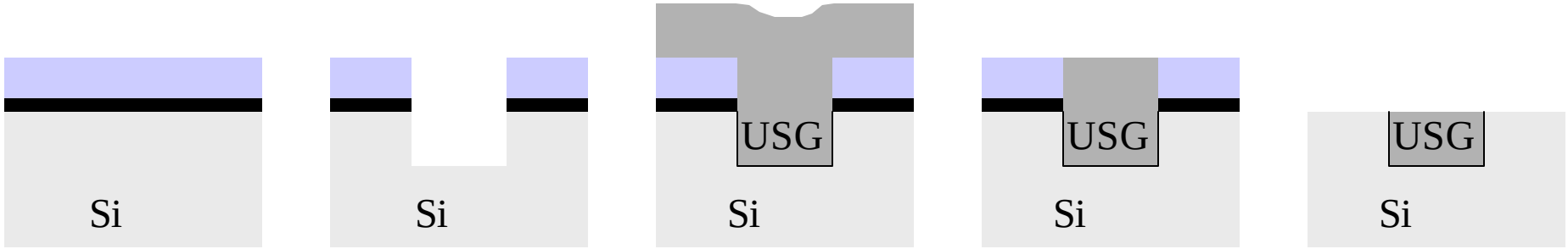
Etch nitride, oxide and silicon

Grow barrier oxide

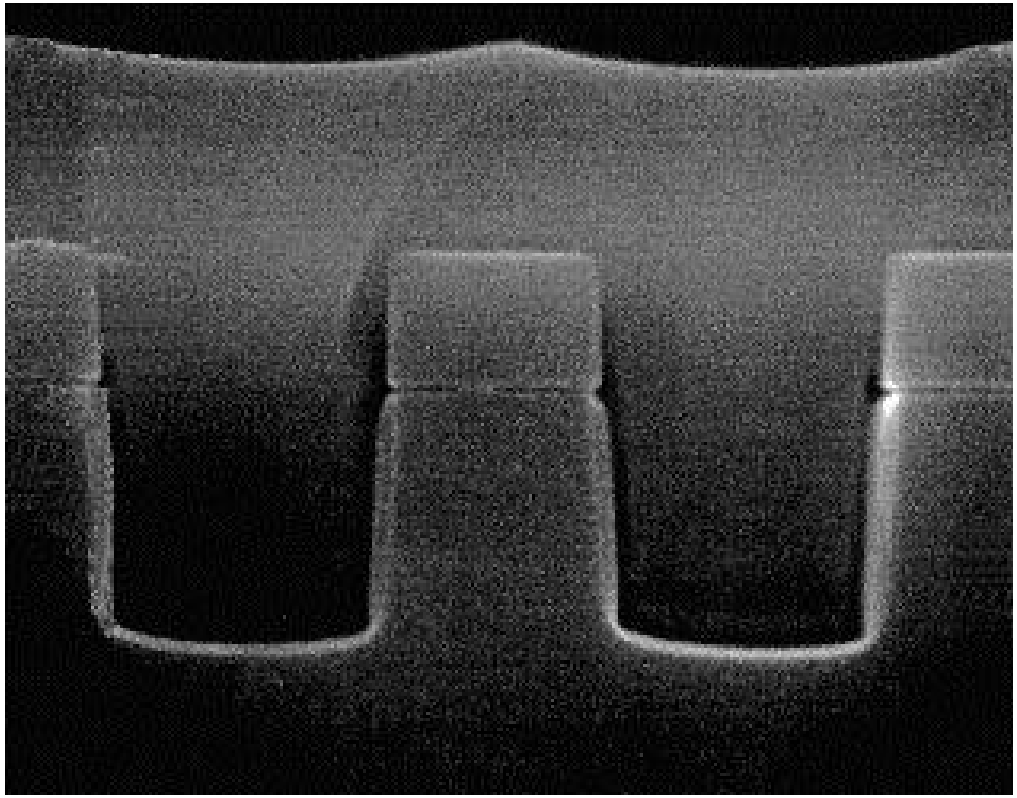
CVD USG trench fill

CMP USG
Anneal USG

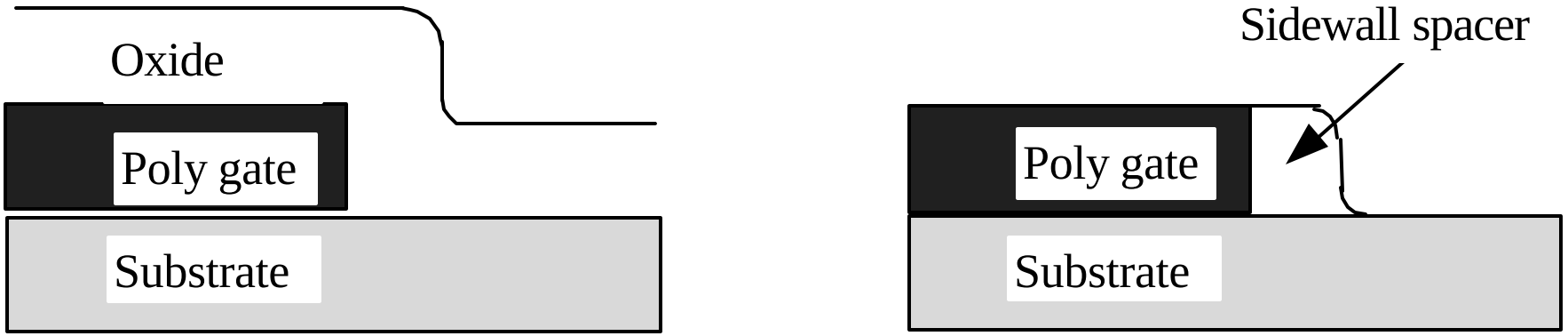
Strip nitride and oxide



Shallow Trench Isolation (STI)



Sidewall Spacer Formation

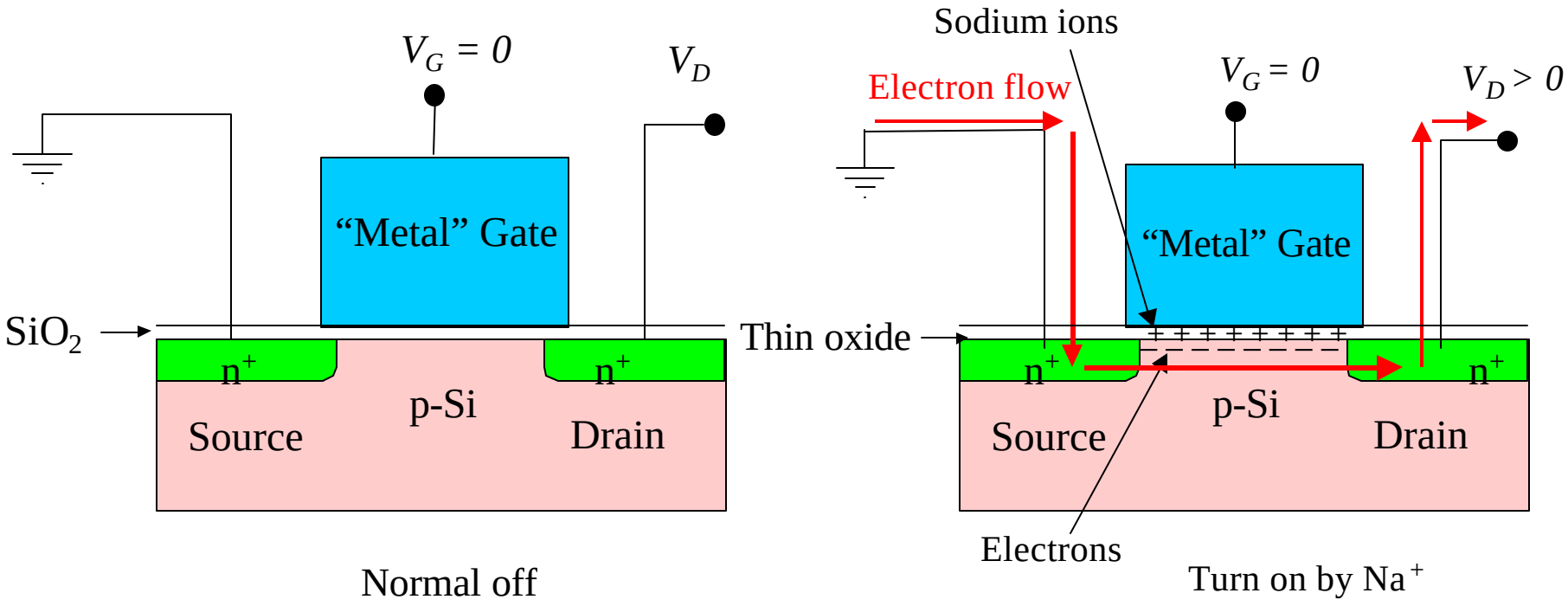


- Lightly doped drain (LDD)
- Self aligned silicide (Salicide)

PMD

- Doped oxide
- PSG or BPSG
- Phosphorus: gettering sodium and reduce flow temperature.
- Boron: further reduces flow temperature without excessive phosphorus

Sodium Ion Turn-on the MOSFET



PMD

- More phosphorus, lower reflow temperature
- >7wt% phosphorus, hygroscope

$$P_2O_5 + 3H_2O \rightarrow 2H_3PO_4$$

- H_3PO_4 etches aluminum causes metal corrosion
- Too much boron will cause crystallization of boric acid. H_3BO_3.
- Limit, P% + B% < 10%

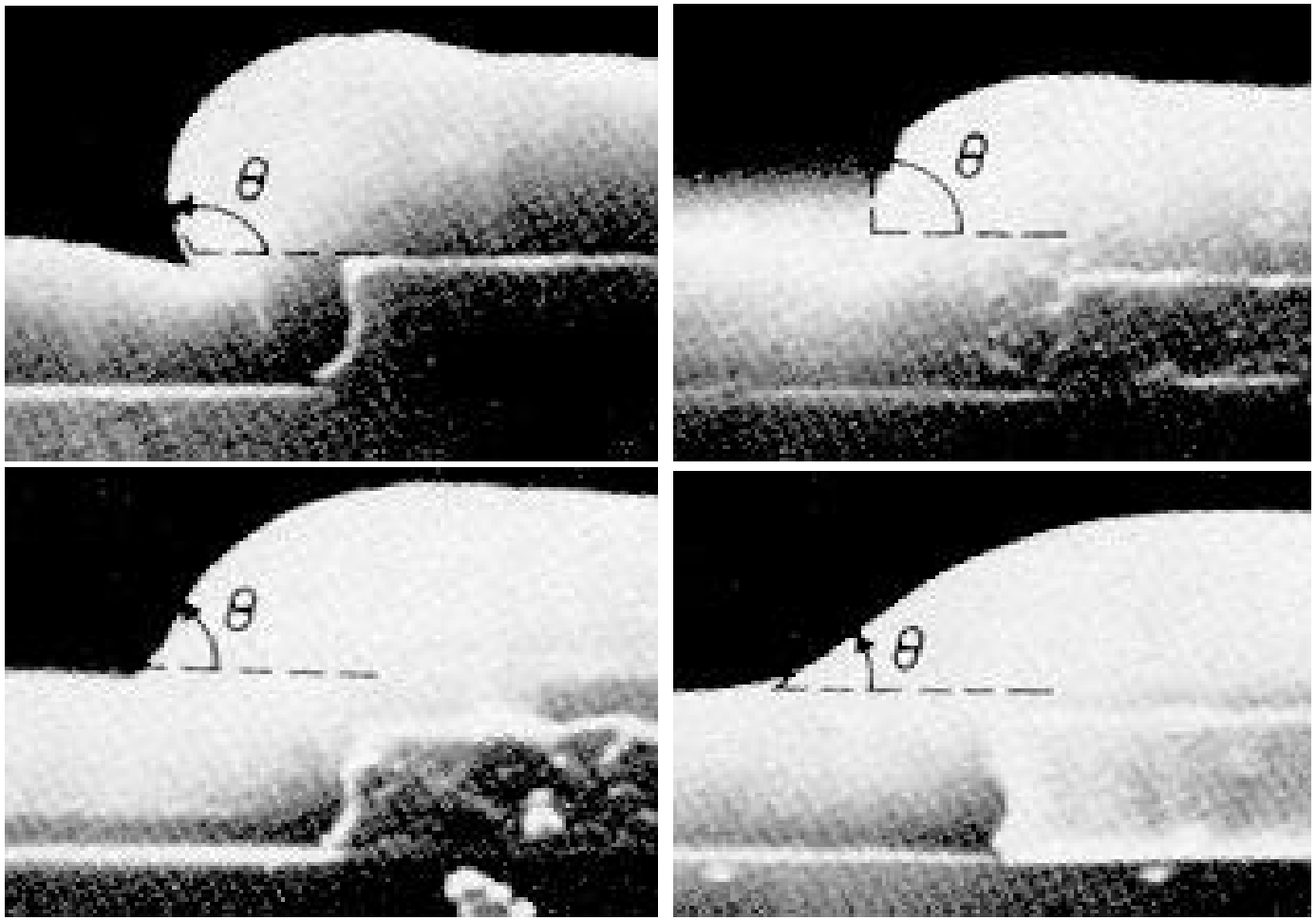
Question

- Silicon nitride is a better sodium barrier layer than silicon oxide. Why don’t people just use nitride for PMD layer?

Answer

- Silicon nitride has higher dielectric constant
- Using nitride can cause longer *RC* time delay and reduce circuit speed
- A thin layer of nitride (~ 200 Å) is commonly used as a diffusion barrier layer in the PMD application
- Prevent diffusion of phosphorus and boron from BPSG diffusing into source/drain

PSG Reflow at 1100 °C, N_2, 20 min.

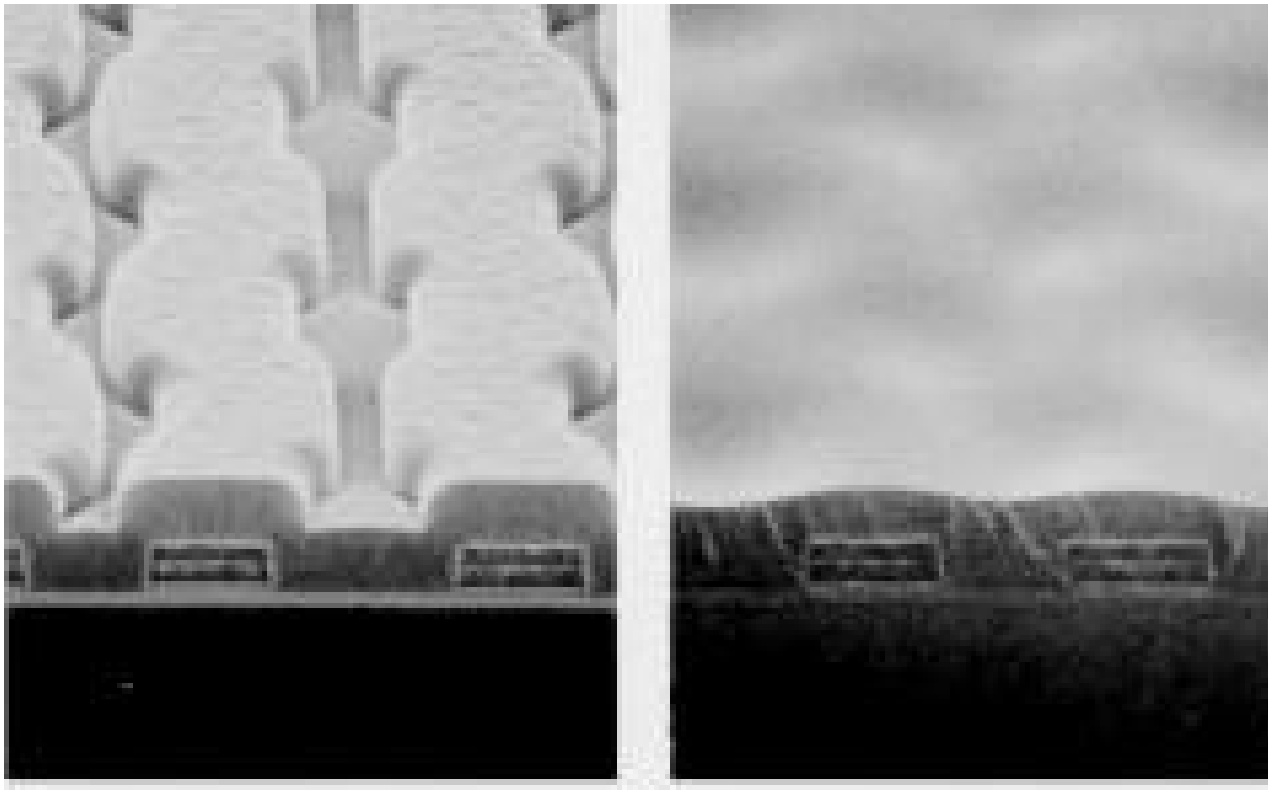


Source: *VLSI Technology*, by S.M. Sze

Some Facts about Sodium

Name	Sodium
Symbol	Na
Atomic number	11
Atomic weight	22.989770
Discoverer	Sir Humphrey Davy
Discovered at	England
Discovery date	1807
Origin of name	From the English word "soda" (the origin of the symbol Na comes from the Latin word "natrium")
Density of solid	0.968 g/cm^3
Molar volume	23.78 cm^3
Velocity of sound	3200 m/sec
Electrical resistivity	4.7 $\mu\Omega \cdot cm$
Reflectivity	No data
Melting point	97.72 °C
Boiling point	882.85 °C
Thermal conductivity	140 $W\ m^{-1}\ K^{-1}$
Coefficient of linear thermal expansion	$71 \times 10^{-6}\ K^{-1}$
Applications	Major contaminant, needs to be strictly controlled
Main removal agent	HCl
Barrier materials used	Silicon nitride and PSG

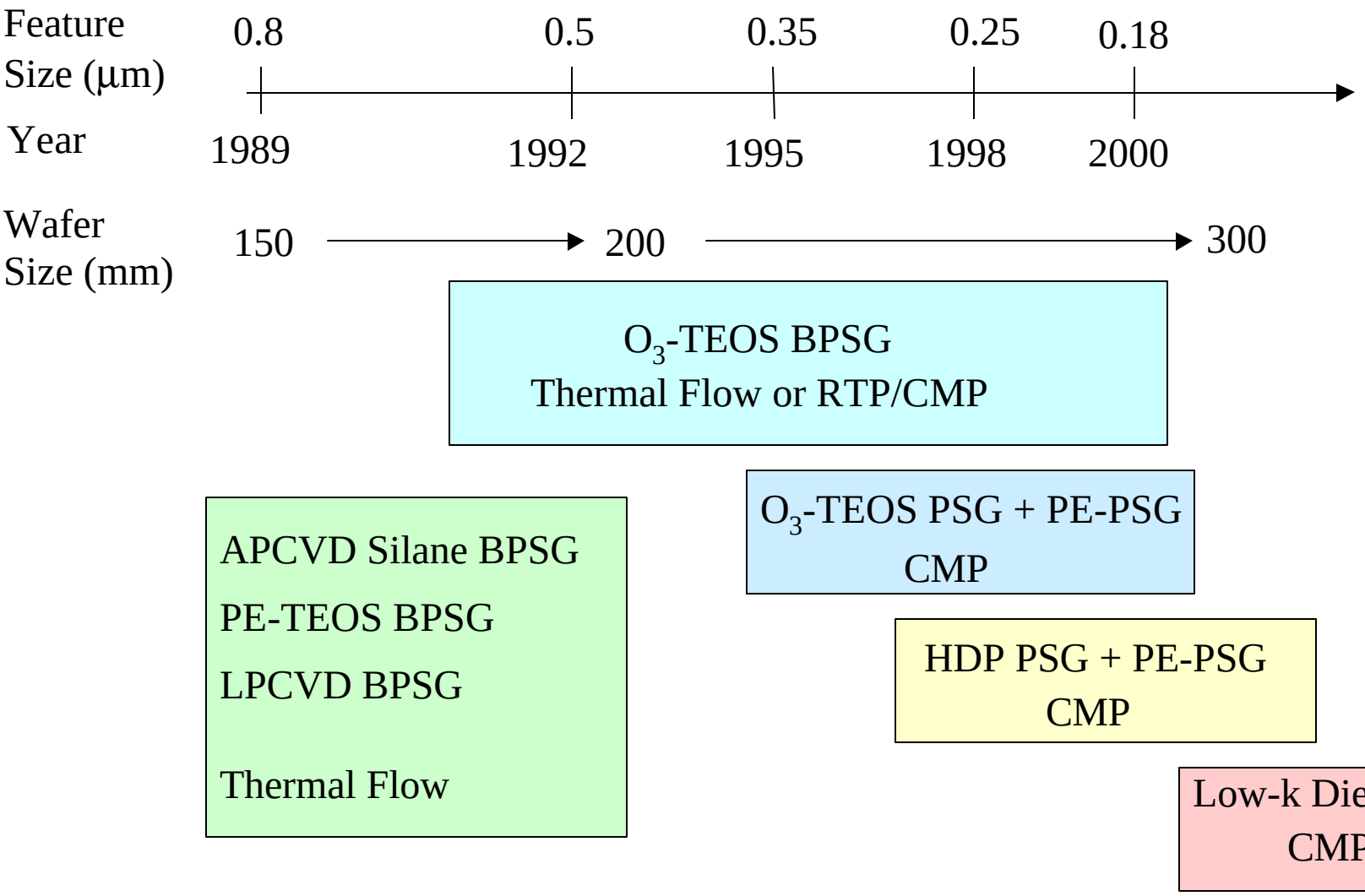
4×4 BPSG Reflow at 850 °C, 30 Minutes in N_2 Ambient



Development of PMD Processes

Dimension	PMD	Planarization	Reflow temperature
> 2 μm	PSG	Reflow	1100°C
2 - 0.35 μm	BPSG	Reflow	850 - 900°C
0.25 μm	BPSG	Reflow + CMP	750°C
0.18 μm	PSG	CMP	-

PMD Applications Roadmap

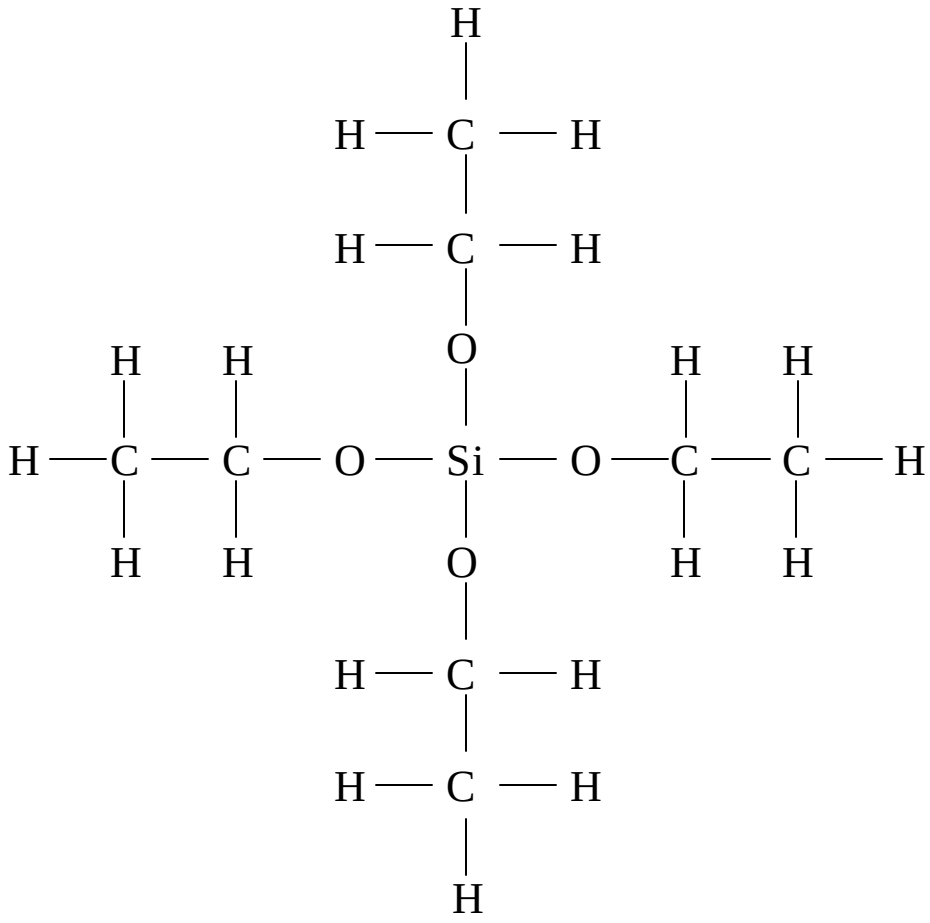


IMD

- Inter-metal dielectric
- Undoped silicate glass (USG) or FSG
- SOG
- Gap fill and planarization
- Temperature limited by metal melting
  - Normally 400 °C
- PE-TEOS, O_3-TEOS, and HDP

TEOS

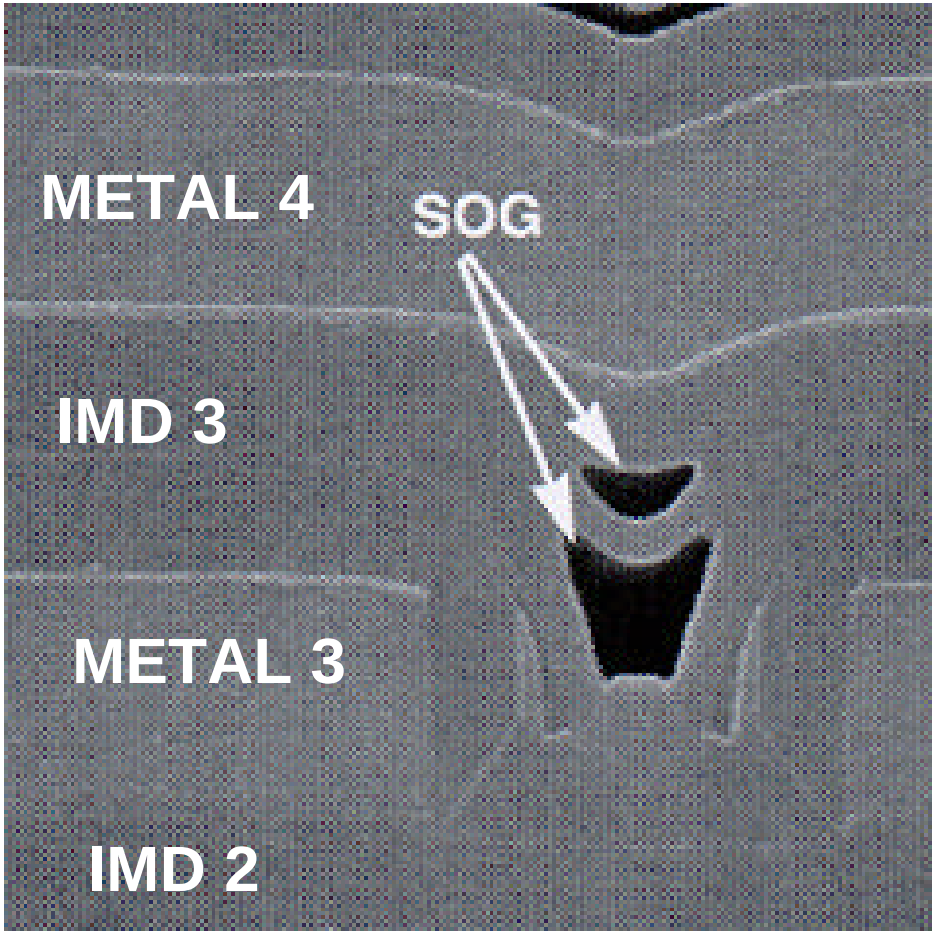
- Tetraethyloxysilane, $Si(OC_2H_5)_4$
- Liquid silicon source
- Commonly used for SiO_2 deposition
- Good step coverage and gap fill



PE-TEOS

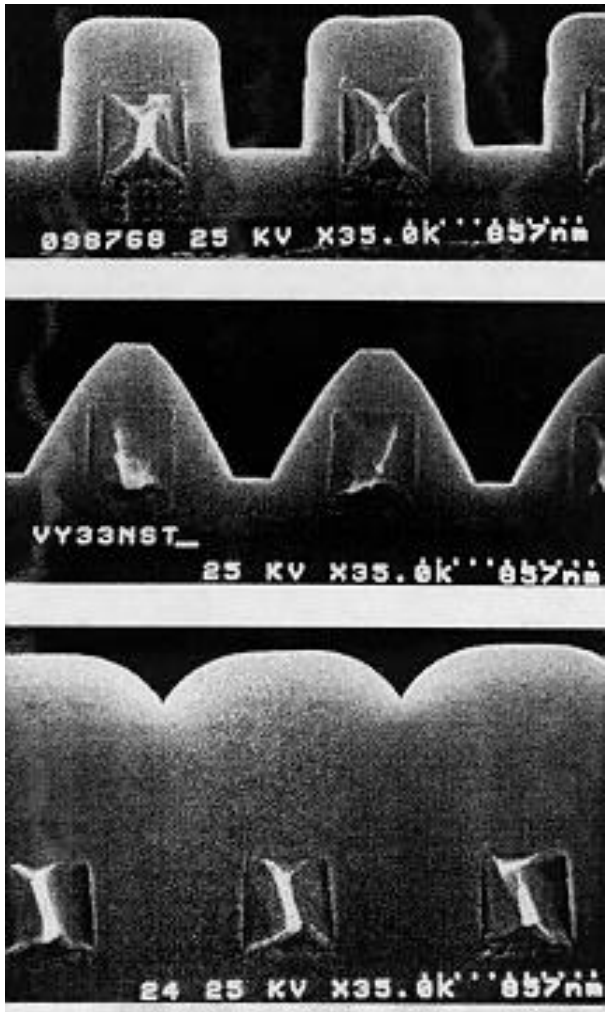
- Plasma-enhanced TEOS CVD processes
- TEOS and O_2
- Most commonly used dielectric CVD process
- Deposit USG at ~400 °C
- Mainly for IMD

Spin-on Glass (SOG) Processes



PE-TEOS

Photo courtesy:
Applied Materials



- PE-TEOS
- Sputtering etchback
- PE-TEOS

O_3-TEOS

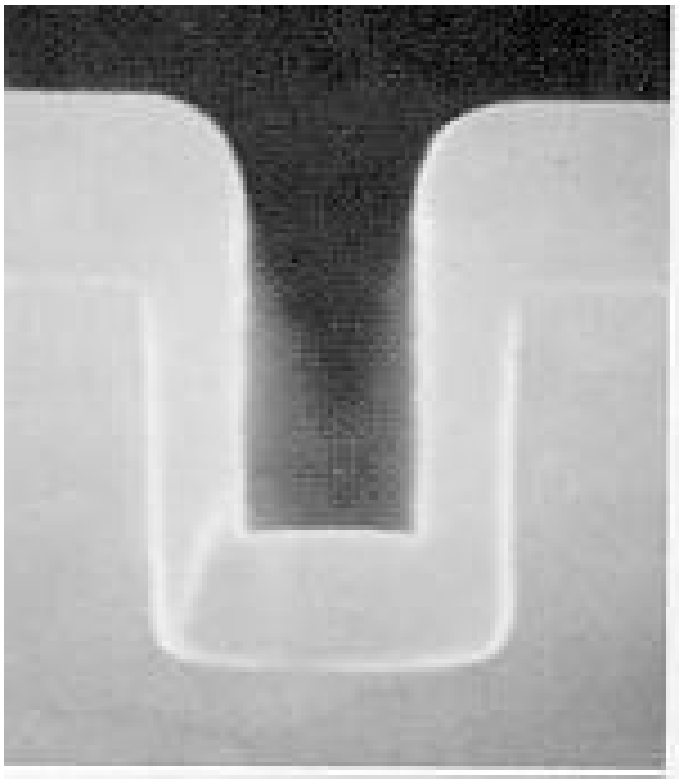
- TEOS and Ozone

- $O_3 \rightarrow O_2 + O$ (half-life time: 86 hours at 22 °C, < 1ms at 400 °C)
- $O + TEOS \rightarrow USG$ + other volatile byproducts

- Excellent step coverage and gap fill.
- Applied for IMD and PMD

O_3-TEOS vs PE-TEOS

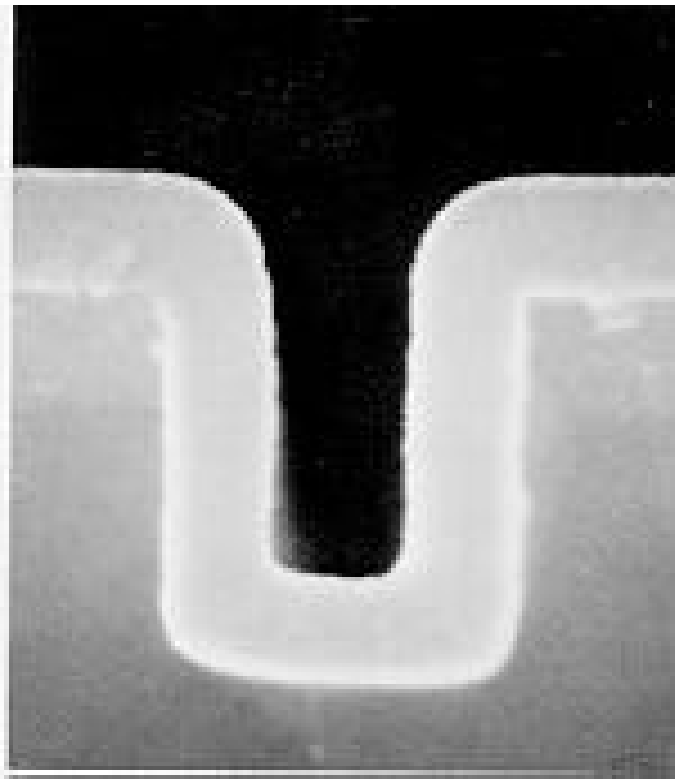
PE-TEOS



Step coverage: 50%

Conformality: 87.5%

Ozone-TEOS



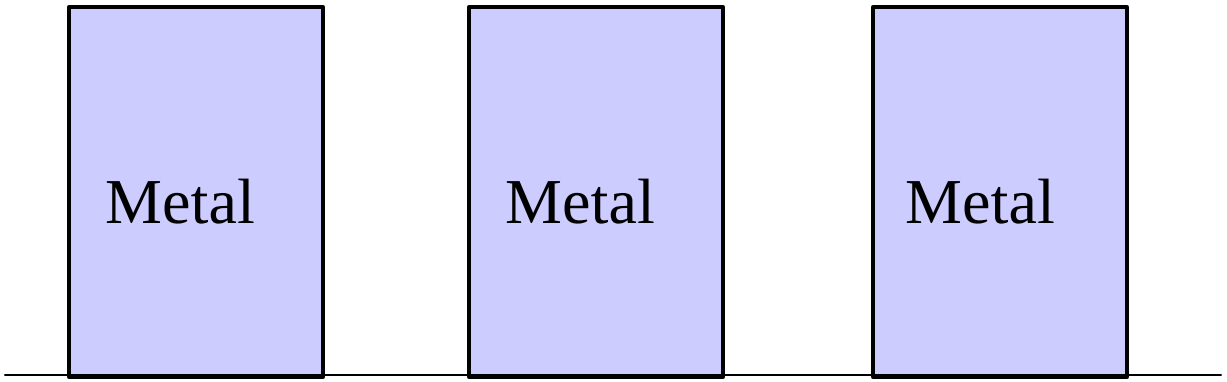
Step coverage: 90%

Conformality: 100%

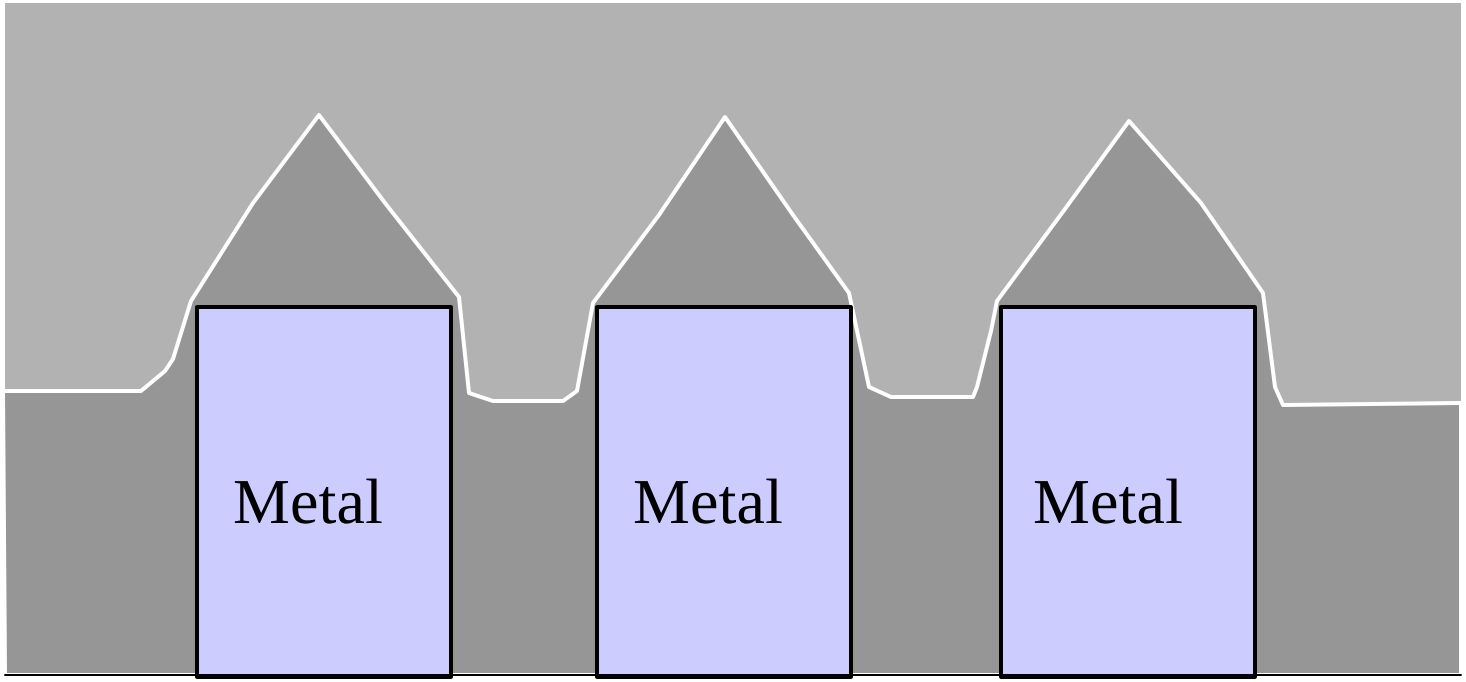
High Density Plasma CVD

- HDP-CVD: deposition and sputtering etch at the same time.
- USG for STI application
- USG and FSG for IMD applications
- PMD for PMD application

HDP-CVD, IMD Application



Oxide CMP



Passivation

- Nitride and oxide
- Nitride is very good barrier layer, oxide help nitride stick with metal
- Silane process
- NH_3, N_2 and nitrogen precursors, N_2O as oxygen precursor
- In-situ CVD process

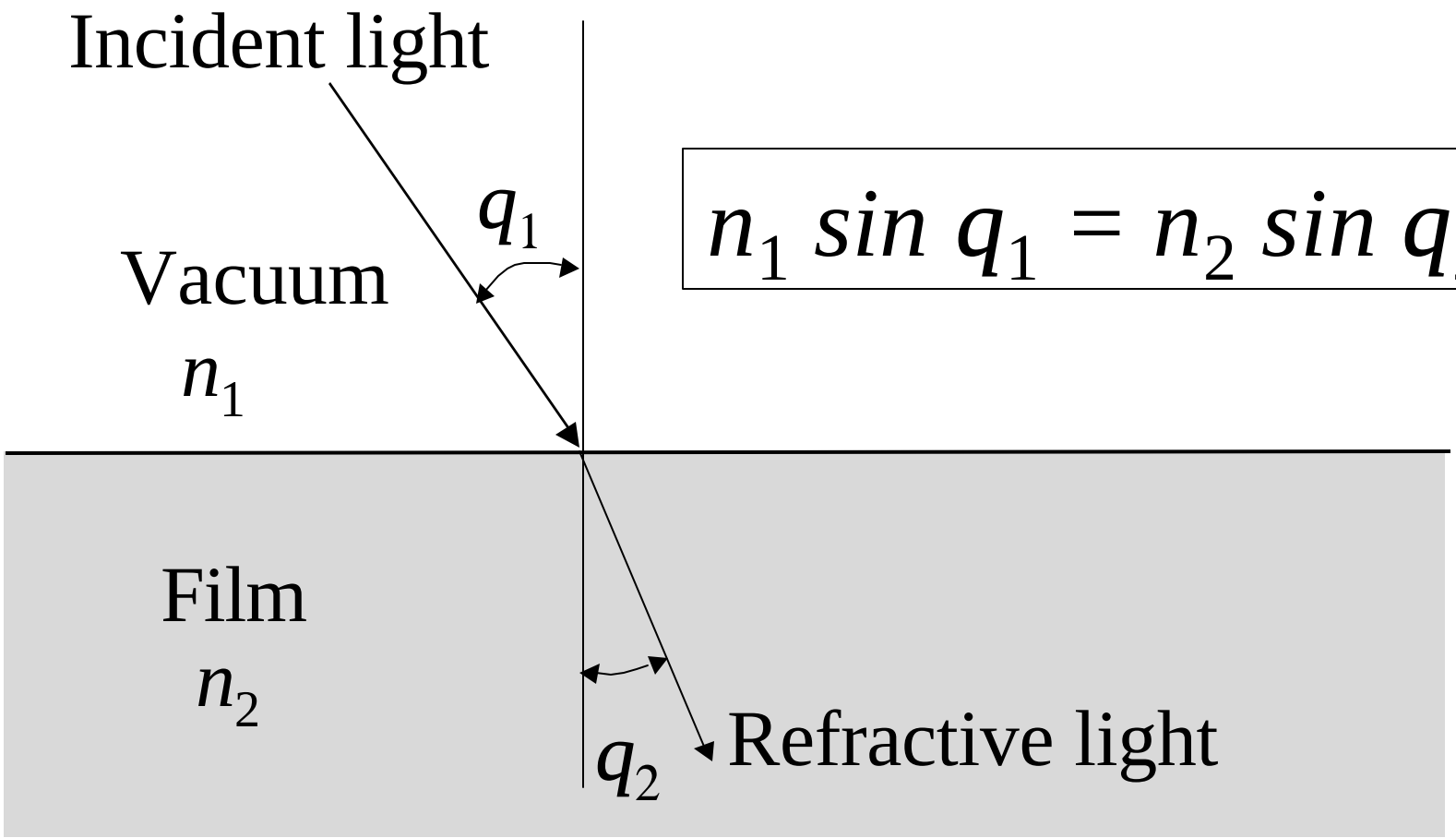
Dielectric Thin Film Characteristics

- Refractive index
- Thickness
- Uniformity
- Stress
- Particles

Refractive Index

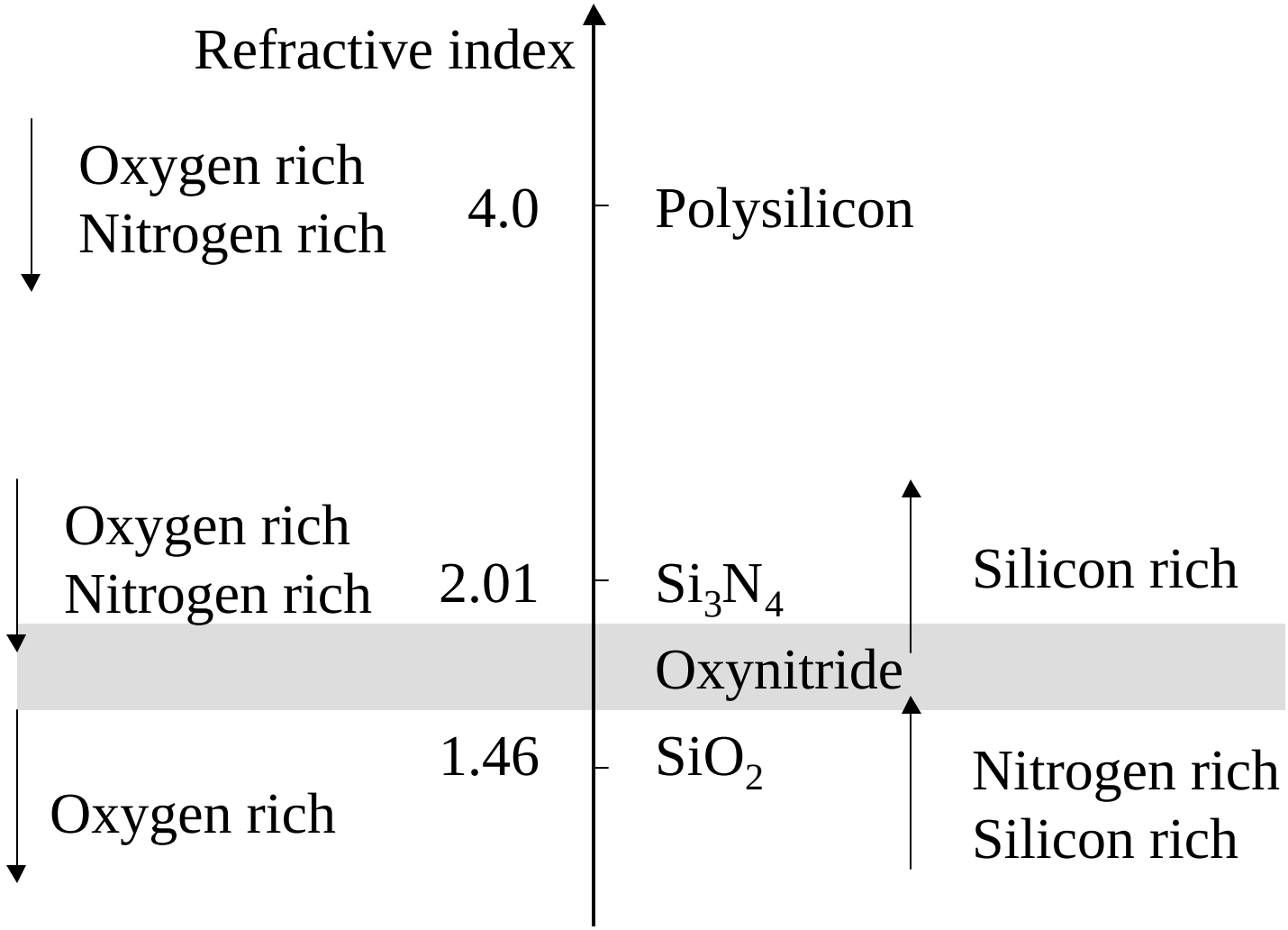
$$\text{Refractive index, } n = \frac{\text{Speed of light in vacuum}}{\text{Speed of light in the film}}$$

Refractive Index



$$n_1 \sin q_1 = n_2 \sin q_2$$

Film Information from R.I.



Ellipsometry R.I. Measurement

Elliptically Polarized
Reflected Light

Linearly Polarized Incident Light

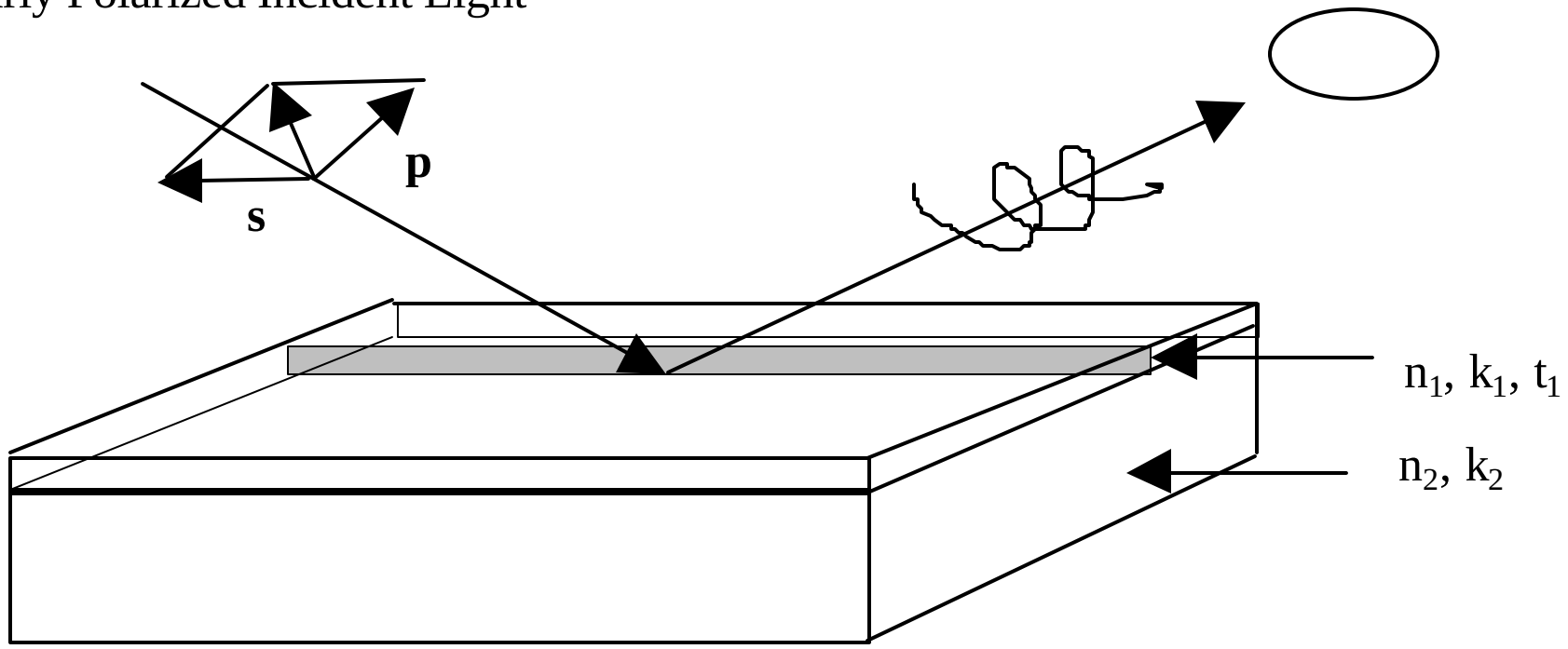
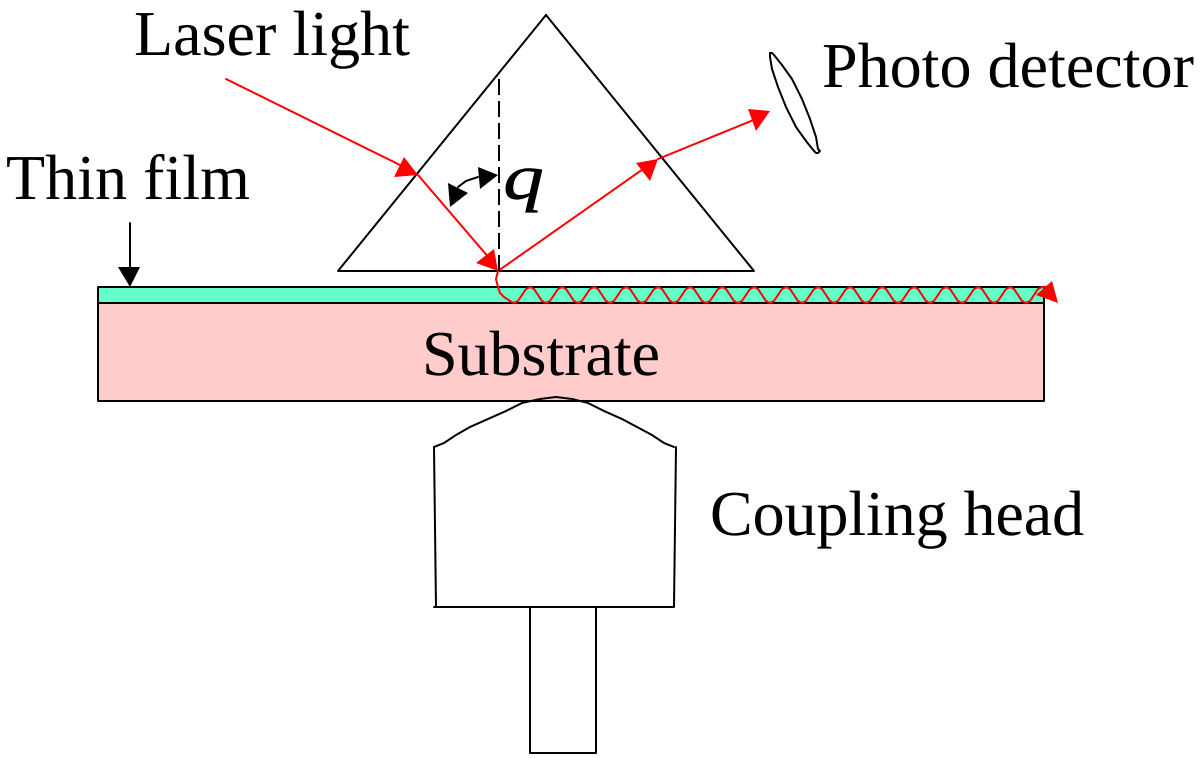
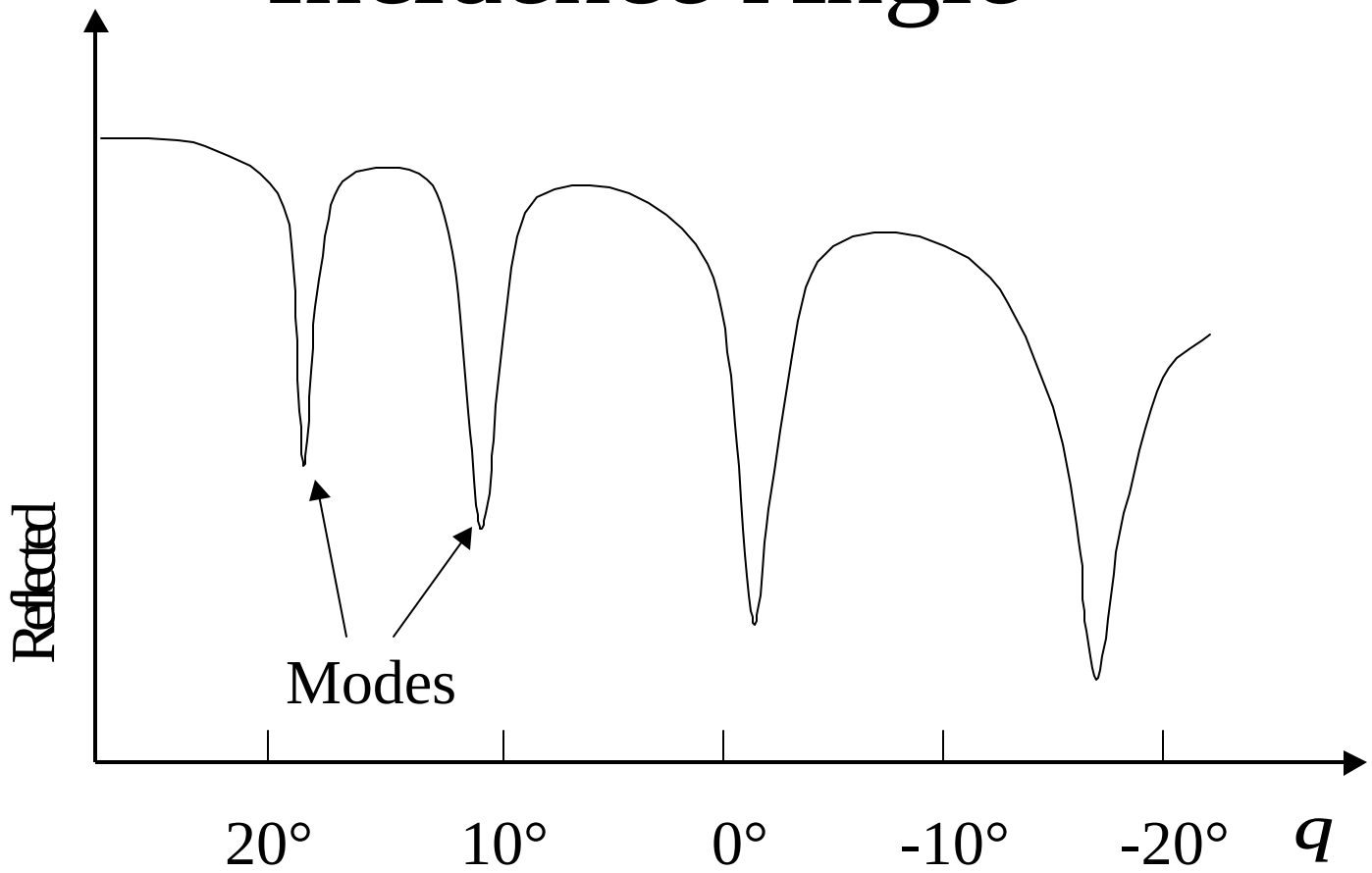


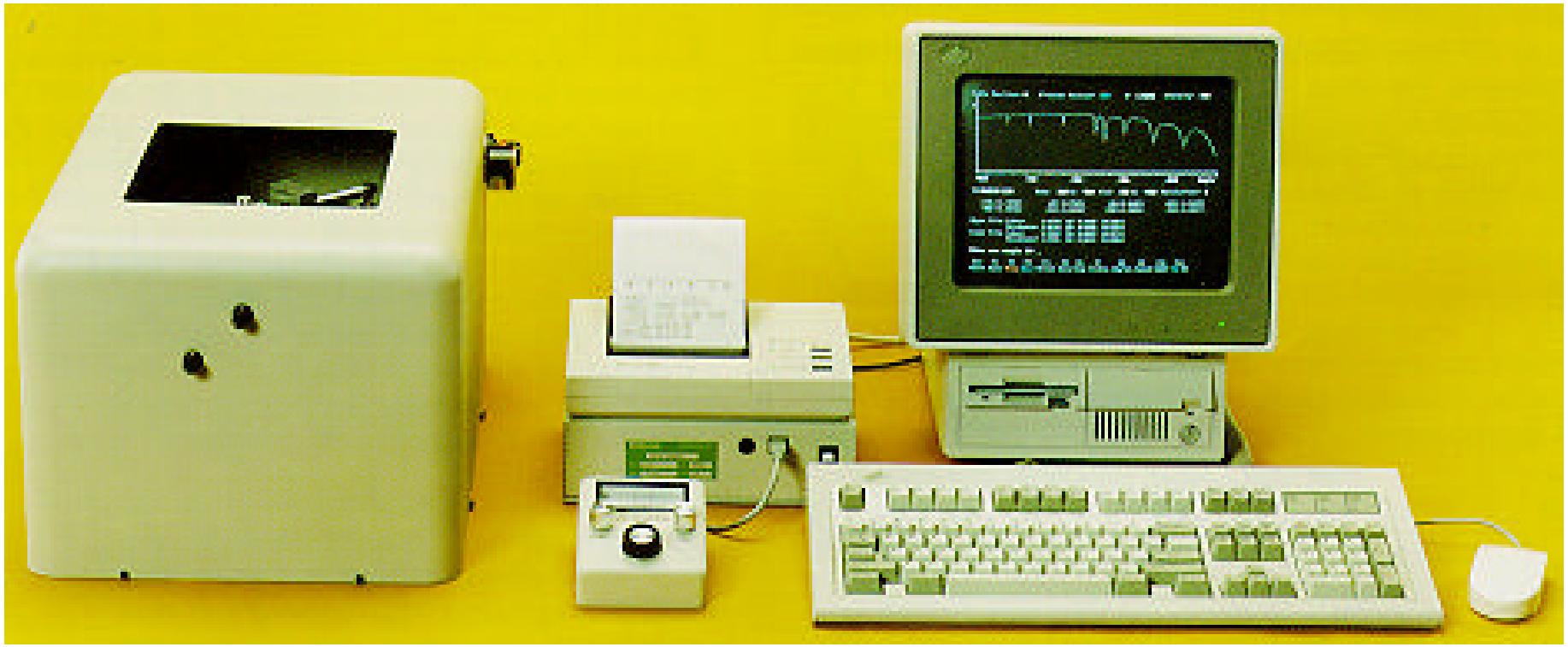
Illustration of Prism Coupler



Reflected Light Intensity vs. Incidence Angle



Metricon Model 2010 Prism Coupler



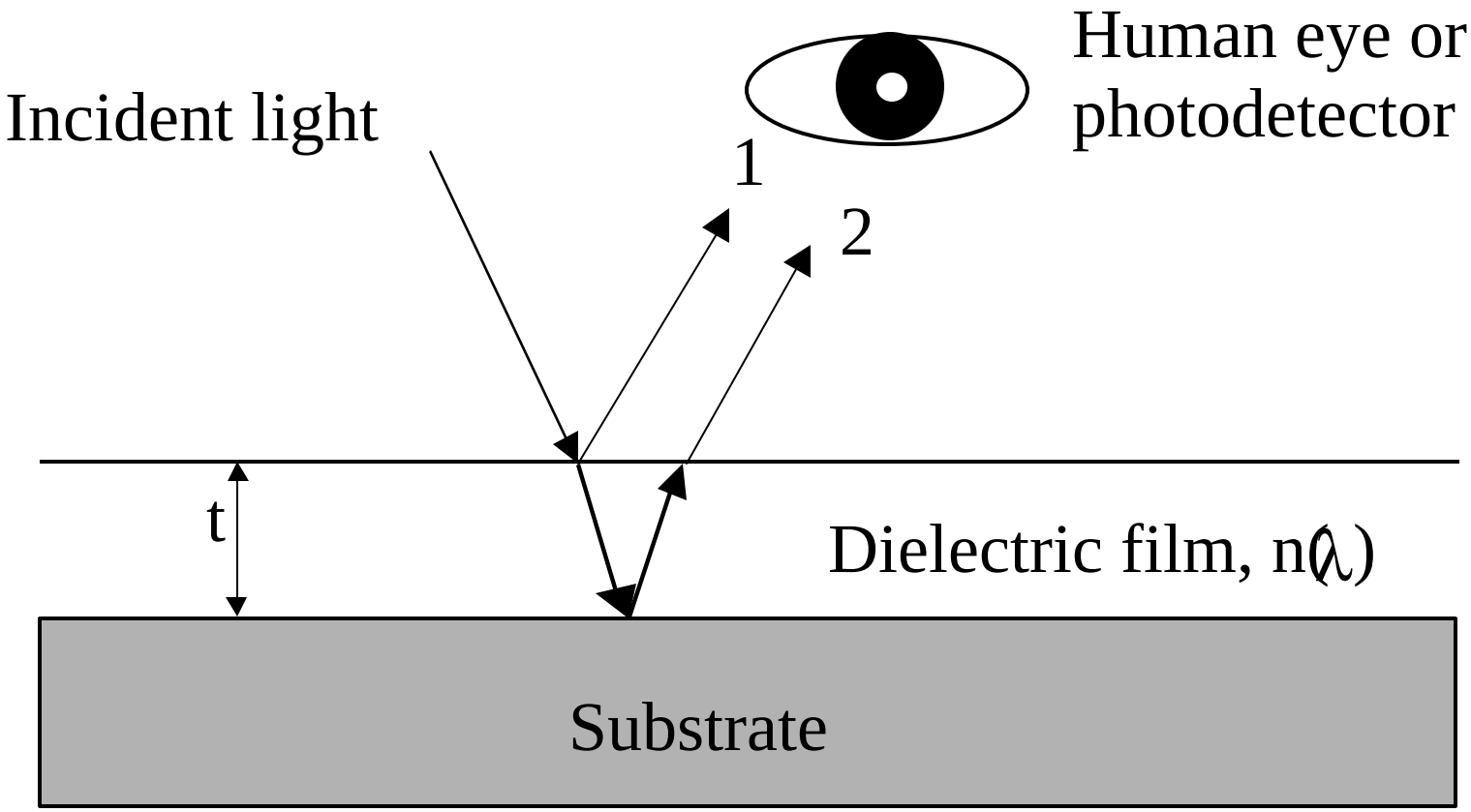
Comparison of the Two Methods

Ellipsometry	Prism coupler
• Need know rough film thickness before hand • Can measure thickness if R.I. is know	• Need certain thickness of the film, > 3000 Å • Can measure thickness if film thick enough to support enough modes

Thickness Measurement

- One of the most important measurements for dielectric thin film processes.
- Determines
  - Film deposition rate
  - Wet etch rate
  - Shrinkage

Dielectric Thin Film Thickness Measurement



Dielectric Thin Film Thickness Measurement

- Different thickness has different color
- Tilting wafer also changes the color

Question

- If you see some beautiful color rings on a wafer with a CVD dielectric layer, what is your conclusion?

Answer

- Color change indicates the dielectric thin film thickness change, thus we know the film with the color rings must have problem with thickness uniformity, which is most likely caused by a non-uniform thin film deposition process.

Question

- Why does the thin film color change when one look at the wafer from different angle?

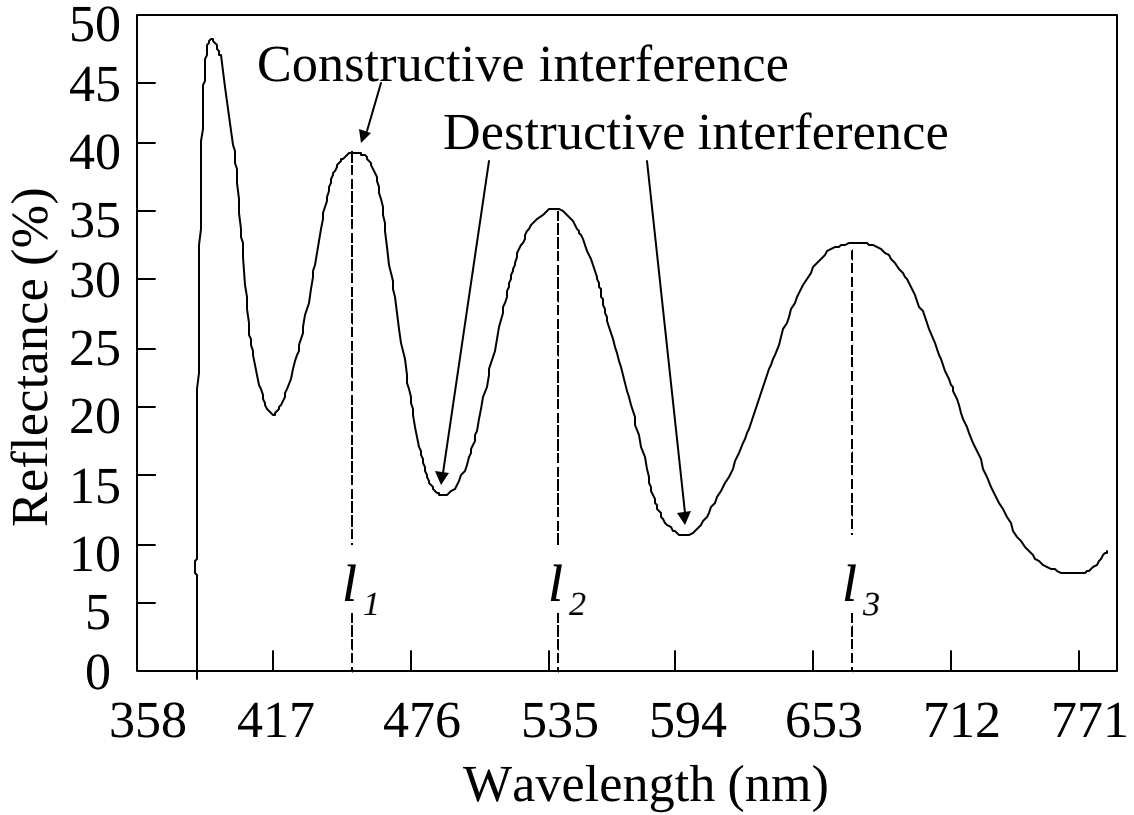
Answer

- When one looking at wafer from a different angle, phase shift will change, thus wavelength for constructive interference will change, which causes color change
- It is important to hold the wafer straight when using the color chart to measure film thickness
- Tilt wafer makes the film thickness thicker than it actually is

Spectroreflectometry

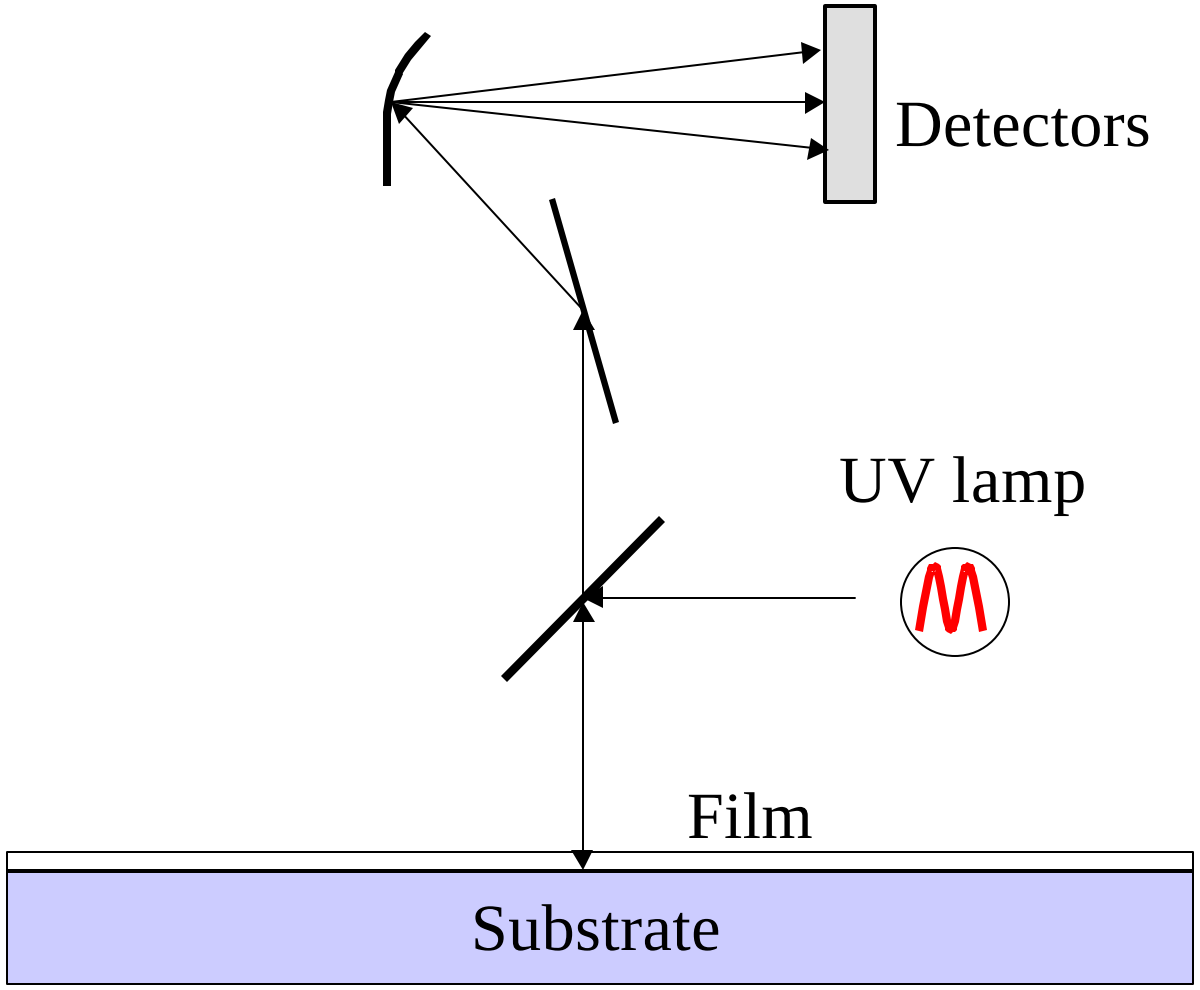
- Measure the reflected light intensity at different wavelengths
- Calculate thin film thickness from the relationship between reflected light intensity and wavelength.
- Photodetector is more sensitive than human eyes
- Spectroreflectometry can obtain much higher resolution and accuracy for the film thickness

Relation of Reflectance and Wavelength



$$\frac{1}{l_m} - \frac{1}{l_{m+1}} = \frac{1}{2nt}$$

Spectroreflectometry System



Question

- Many advance thin film thickness measurement tools allows user to choose the refractive index of the film. If someone mistakenly chooses the PE-TEOS USG film refractive index to measure O_3-TEOS USG films thickness, what will be the effect on the measurement result?

Answer

- Since the *nt* always coupled together
- A wrong *n* will cause wrong *t* measurement
- O_3-TEOS USG is a porous film and has a R.I., about 1.44
- Slightly lower than 1.46 of PE-TEOS USG
- Measured O_3-TEOS film thickness will be slightly thinner than its actual value

Deposition Rate

$$\text{Deposition Rate} = \frac{\text{Thickness of deposited film}}{\text{Deposition time}}$$

Wet Etch Rate

$$\text{Wet Etch Rate} = \frac{\text{Thickness change after etch}}{\text{Etch time}}$$

$$\text{Wet etch rate ratio} = \frac{\text{Thickness change of the CVD film}}{\text{Thickness change of the thermal oxide film}}$$

Uniformity

- Multi-point measurement
- Definition
- Average: $\bar{x} = \dfrac{x_1 + x_2 + x_3 + \cdots + x_N}{N}$
- Standard deviation:

$$s = \sqrt{\frac{(x_1 - \bar{x})^2 + (x_2 - \bar{x})^2 + (x_3 - \bar{x})^2 + \cdots + (x_N - \bar{x})^2}{N - 1}}$$

- Standard deviation non-uniformity: $s/\bar{x}$

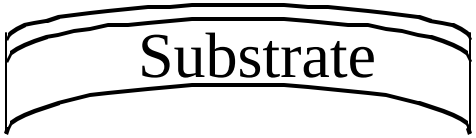
Stress

- Mismatch between different materials
- Two kinds of stresses, intrinsic and extrinsic
- Intrinsic stress develops during the film nucleation and growth process.
- The extrinsic stress results from differences in the coefficients of thermal expansion
- Tensile stress: cracking film if too high
- Compressive stress: hillock if too strong

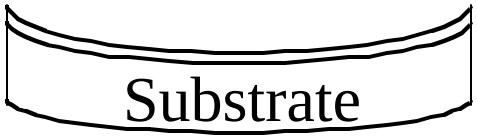
Film Stress

Bare Wafer

After Thin Film Deposition

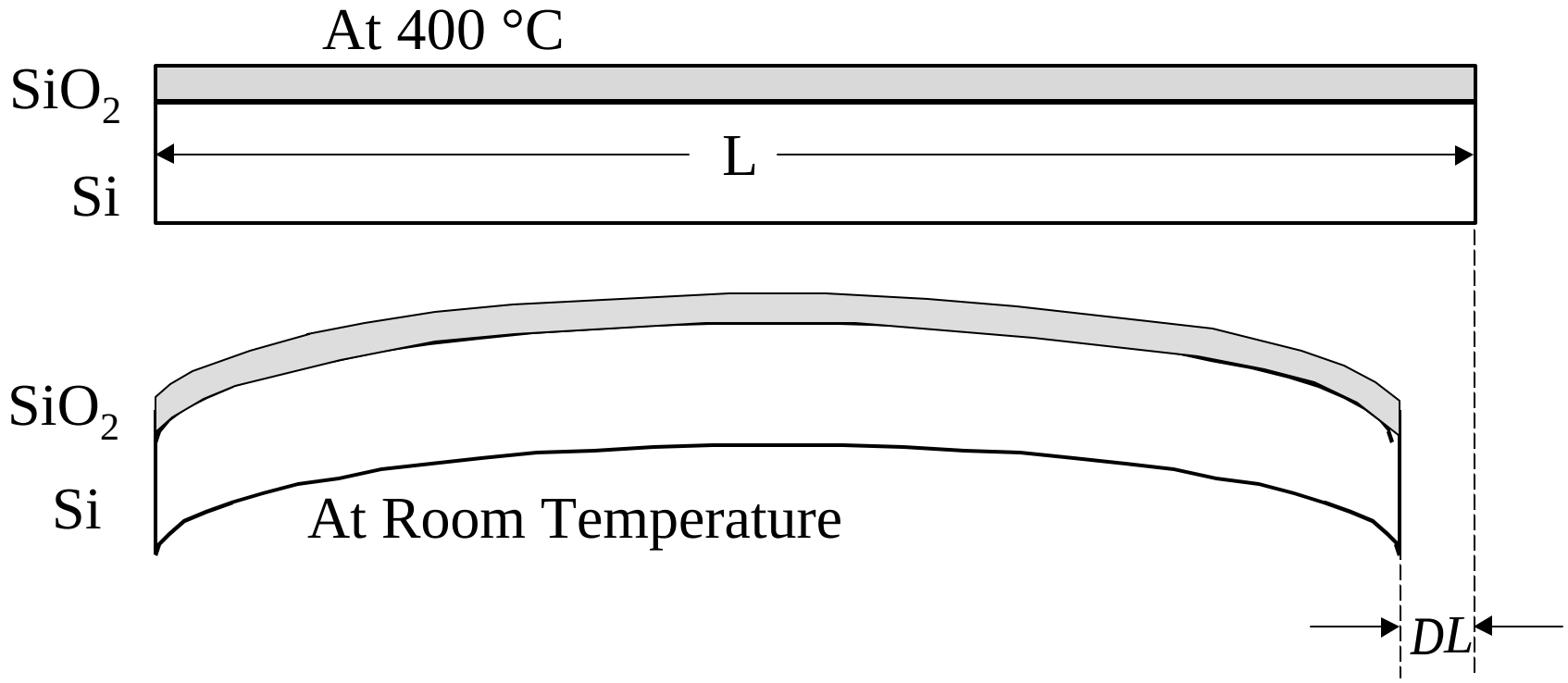


Compressive Stress
Negative curvature



Tensile Stress
Positive curvature

Illustration of Thermal Stress



$$DL = a\ DT\ L$$

Coefficients of Thermal Expansion

$$\alpha(SiO_2) = 0.5\times10^{-6}\ ^\circ C^{-1}$$

$$\alpha(Si) = 2.5\times10^{-6}\ ^\circ C^{-1}$$

$$\alpha(Si_3N_4) = 2.8\times10^{-6}\ ^\circ C^{-1}$$

$$\alpha(W) = 4.5\times10^{-6}\ ^\circ C^{-1}$$

$$\alpha(Al) = 23.2\times10^{-6}\ ^\circ C^{-1}$$

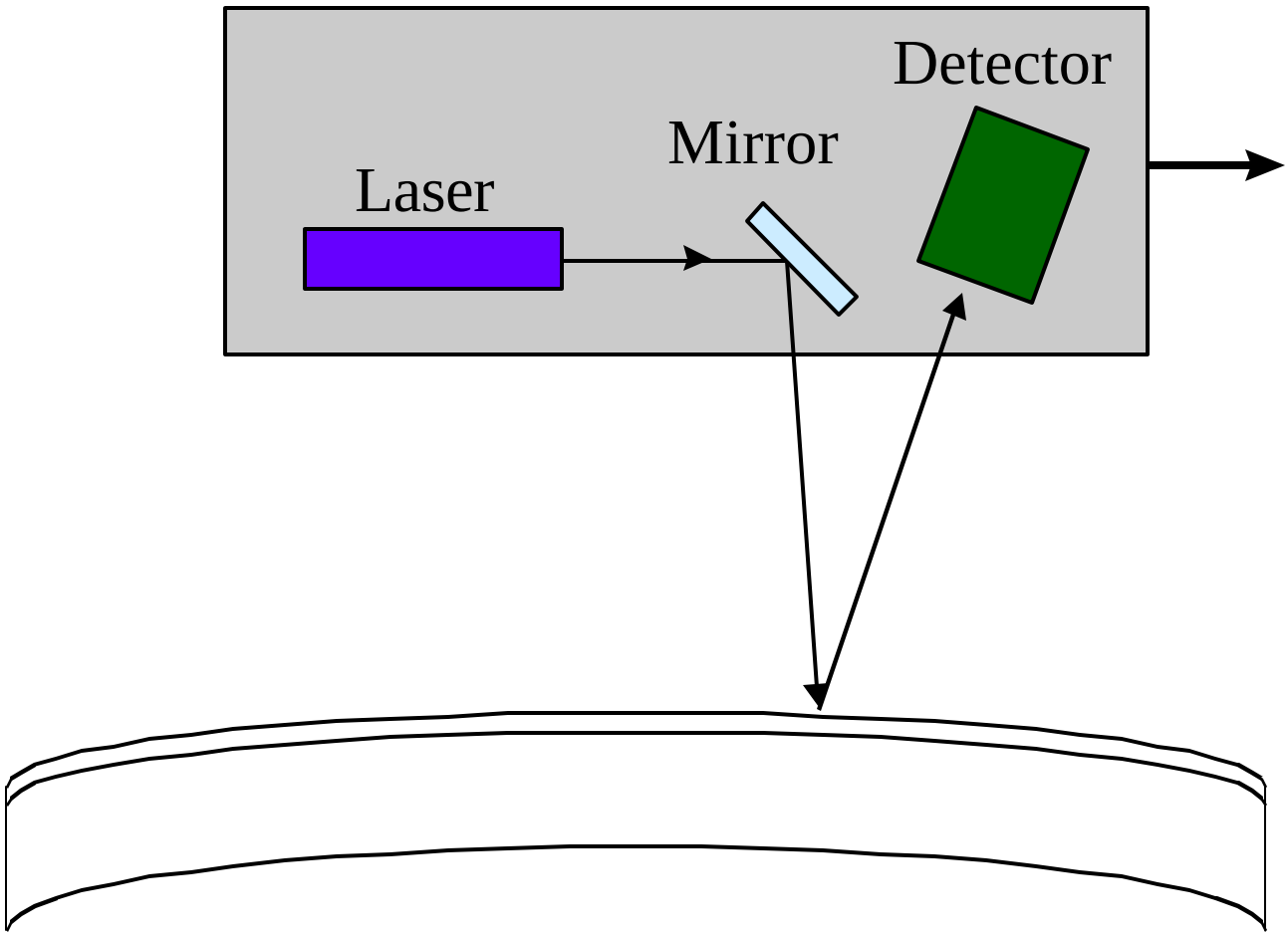
Stress Measurement

$$s = \frac{E}{1-n}\frac{h^2}{6t}\left(\frac{1}{R_2} - \frac{1}{R_1}\right)$$

Wafer curvature change before and after thin film deposition

Laser beam scans wafer surface, reflection light indicates the wafer curvature

Stress Measurement



Dielectric CVD Processes

- Thermal Silane CVD Process
- Thermal TEOS CVD Process
- PECVD Silane Processes
- PECVD TEOS Processes
- Dielectric Etchback Processes
- O_3-TEOS Processes
- Spin-on Glass
- High Density Plasma CVD

Thermal Silane CVD Process

- Silane has been commonly used for silicon dioxide deposition with both APCVD and LPCVD process

$$SiH_4 + 2\ O_2 \xrightarrow{\text{heat}} SiO_2 + 2\ H_2O$$

- APCVD normally uses diluted silane (3% in nitrogen) and LPCVD uses pure silane
- Not commonly used in the advanced fab

Thermal TEOS CVD Process

- TEOS: physisorption, high surface mobility
- TEOS film has better step coverage
- LPCVD TEOS dissociates at high temp:

$$Si(OC2H5)_4 \xrightarrow{700\ ^\circ C} SiO_2 + \text{volatile organics}$$

- BPSG with TMB and TMP for PMD
- Temperature is too high for IMD

PECVD Silane Processes

- Silane and N_2O (laughing gas)
- Dissociation in plasma form SiH_2 and O
- Radicals react rapidly to form silicon oxide

$$SiH_4 + N_2O \xrightarrow[\text{heat}]{\text{plasma}} SiO_xH_y + H_2O + N_2 + NH_3 + \ldots$$

- Overflow N_2O, using SiH_4 flow to control deposition rate

Question

- Can we overflow silane and use nitrous oxide flow rate to controlled deposition rate?

Answer

- Theoretically we can, but practically no one should even try this
- It is very dangerous and not cost effective
- Overflowing silane will create a big safety hazard: fire and explosion
- Silane is more expensive than nitrous oxide

Passivation: Silicon Nitride

- Barrier layer for moisture and mobile ions
- The PECVD nitride
  - Low deposition temperature (<450ºC)
  - High deposition rate
  - Silane, ammonia, and nitrogen

$$SiH_4 + N_2 + NH_3 \xrightarrow[\text{heat}]{\text{plasma}} SiN_xH_y + H_2 + N_2 + NH_3 + \ldots$$

- Requires good step coverage, high dep. rate, good uniformity, and stress control

Passivation Dielectric Deposition

- Stabilization 1 (stabilize pressure)
- Oxide deposition (stress buffer for nitride)
- Pump
- Stabilization 2 (stabilize pressure)
- Nitride deposition (passivation layer)
- Plasma purging (eliminate SiH_4)
- Pump

EPROM Passivation Dielectric

- Need UV transparent passivation layer
- UV light can erase EPROM memory
- Oxynitride (SiO_xN_y) is commonly used
- Source gases: SiH_4, N_2, NH_3, and N_2O

$$SiH_4 + N_2 + NH_3 + N_2O \xrightarrow[\text{heat}]{\text{plasma}} SiO_xN_y + H_2O + N_2 + \ldots$$

- Properties in between oxide and nitride
  - UV transparent, and a fairly good barrier layer

PMD Barrier Layer

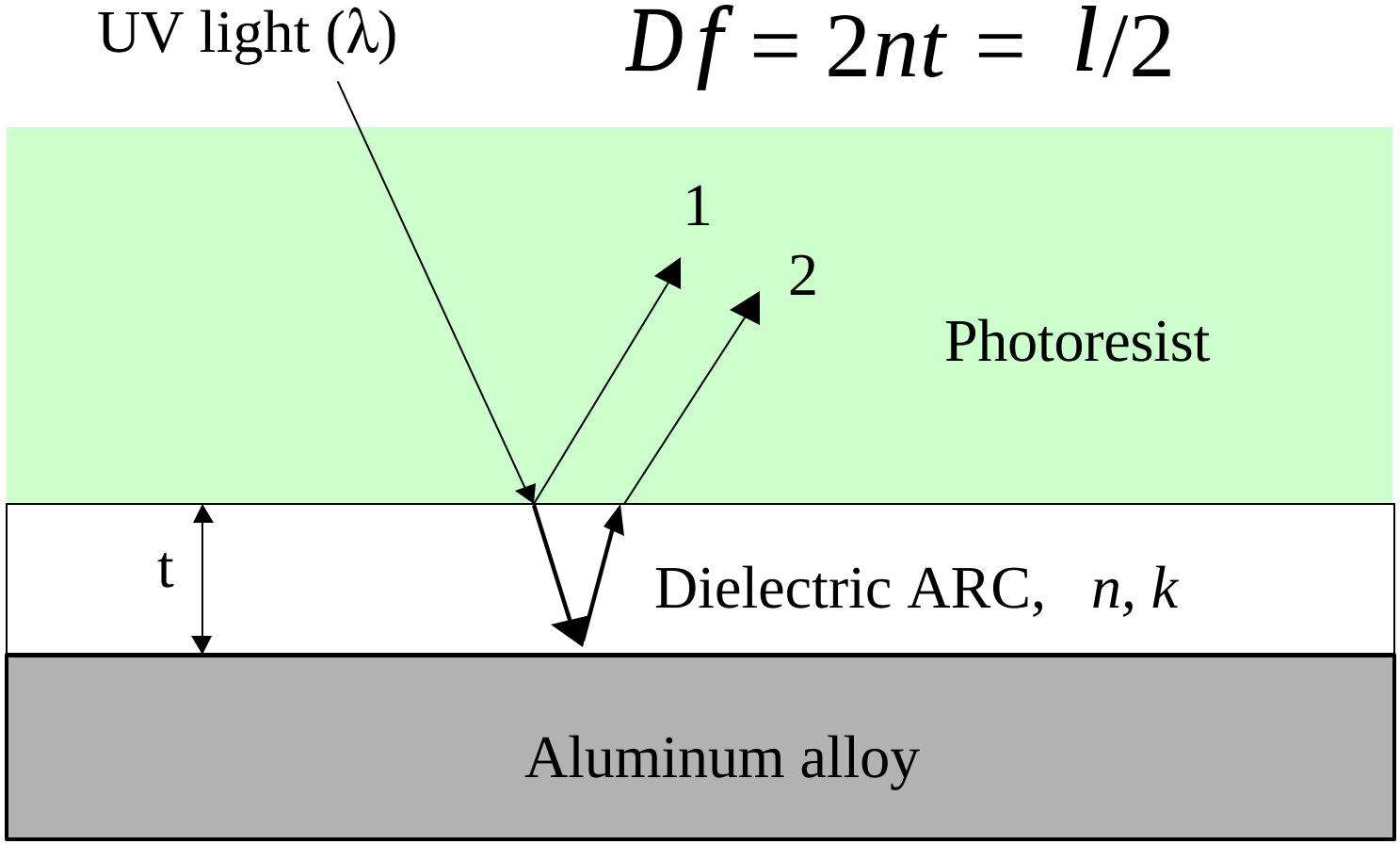
- PSG or BPSG need a diffusion barrier layer
  - USG (need 1000 Å)
  - LPCVD nitride at ~700 ºC (~ 300 Å)
  - PECVD nitride at <550 ºC (< 200 Å)
- At higher temperature, PECVD nitride film has higher deposition rate, lower hydrogen concentration, and better film quality
- Possible in future: remote plasma CVD

Dielectric Anti-Reflective Coating

- High resolution for photolithography
- ARC layer is required to reduce the reflection
- Metallic ARC: TiN, 30% to 40% reflection
- No longer good enough for < 0.25 μm
- Dielectric ARC layer is used
  - Spin-on before photoresist coating
  - CVD

Dielectric Anti-Reflective Coating

$$D f = 2nt = l/2$$



Dielectric ARC

- PECVD silane process
- N_2O as oxygen and nitrogen source

$$SiH_4 + N_2O + He \xrightarrow[\text{heat}]{\text{plasma}} SiO_xN_y + H_2O + N_2 + NH_3 + He + \cdots$$

PE-TEOS

- Most widely used dielectric CVD process
- Fast
- Good uniformity
- Good step coverage

- Mainly used for IMD

PE-TEOS

- USG process

$$Si(OC_2H_5)_4 + O_2 \xrightarrow[400\ ^oC]{Plasma} SiO_2 + \text{other volatiles}$$

- FGS process

$$FSi(OC_2H_5)_3 + Si(OC_2H_5)_4 + O_2 \xrightarrow[heat]{plasma} SiO_xF_y + \text{other volatile (FSG)}$$

(FTES) (TEOS)

FSG Process Trends

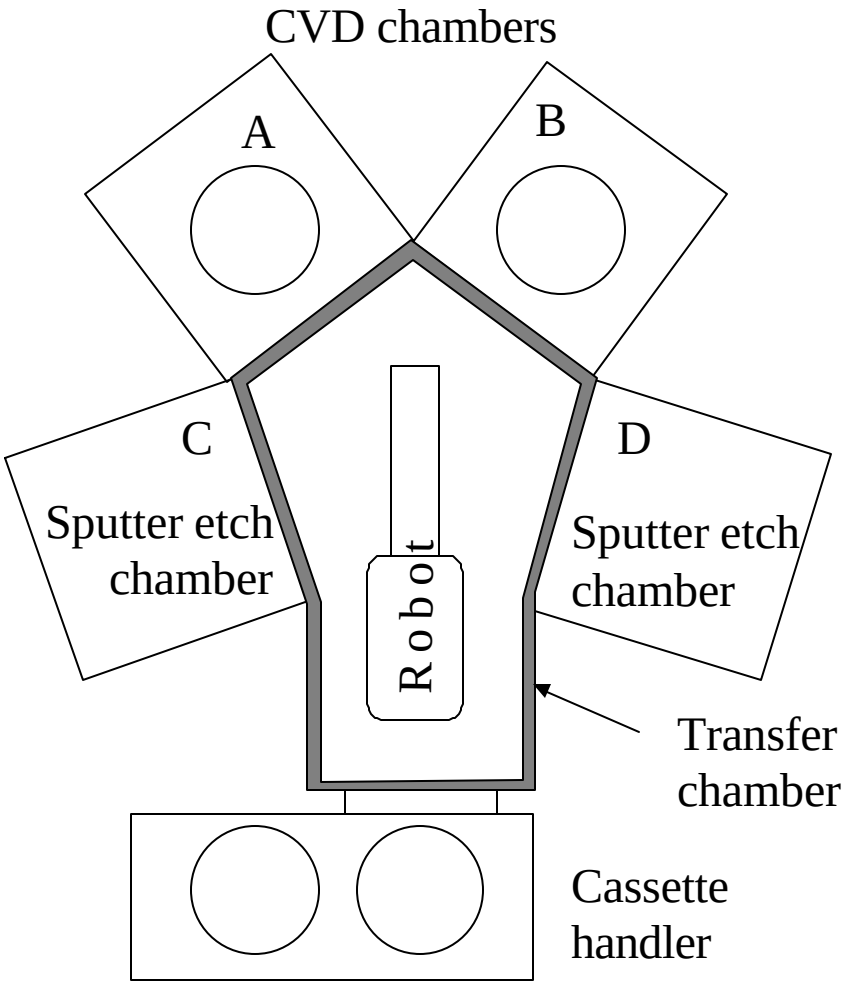
SiO_2	SiO_xF_y (FSG)	SiF_4
solid	solid	gas
$k = 3.9$	$3.8 < k < 3.2$	$k \sim 1$

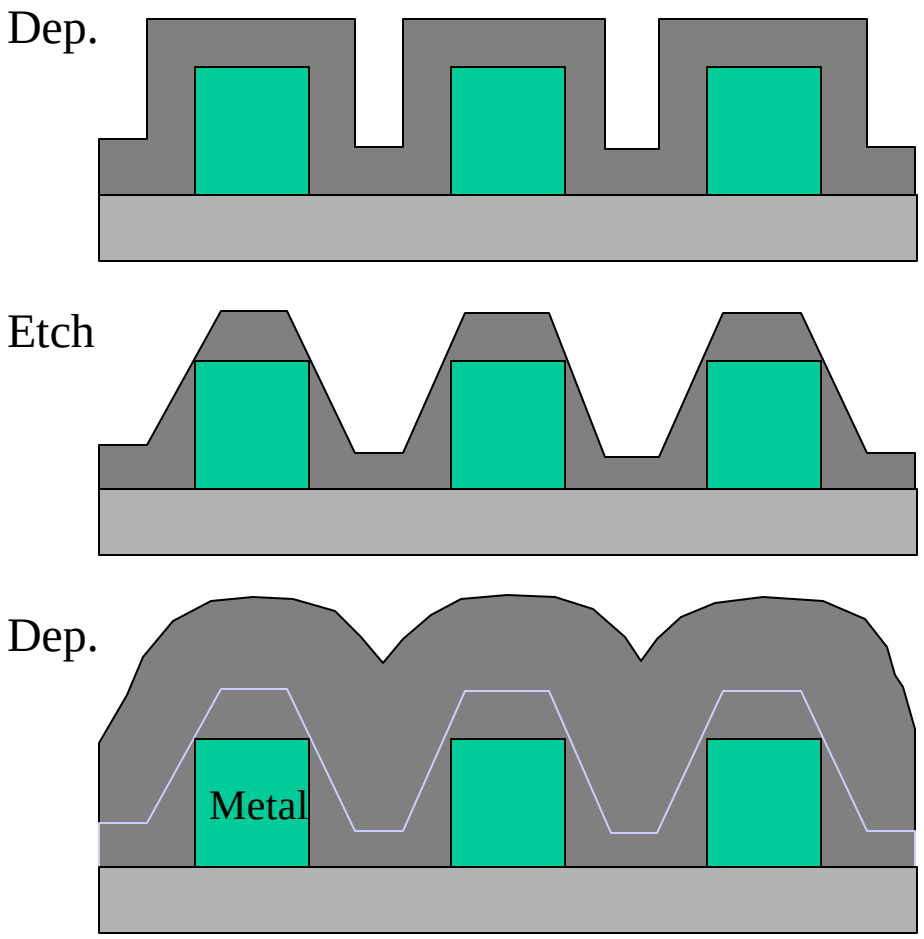
higher k less F ⟵ more F ⟶ lower k, F outgassing

Dielectric Etchback Processes

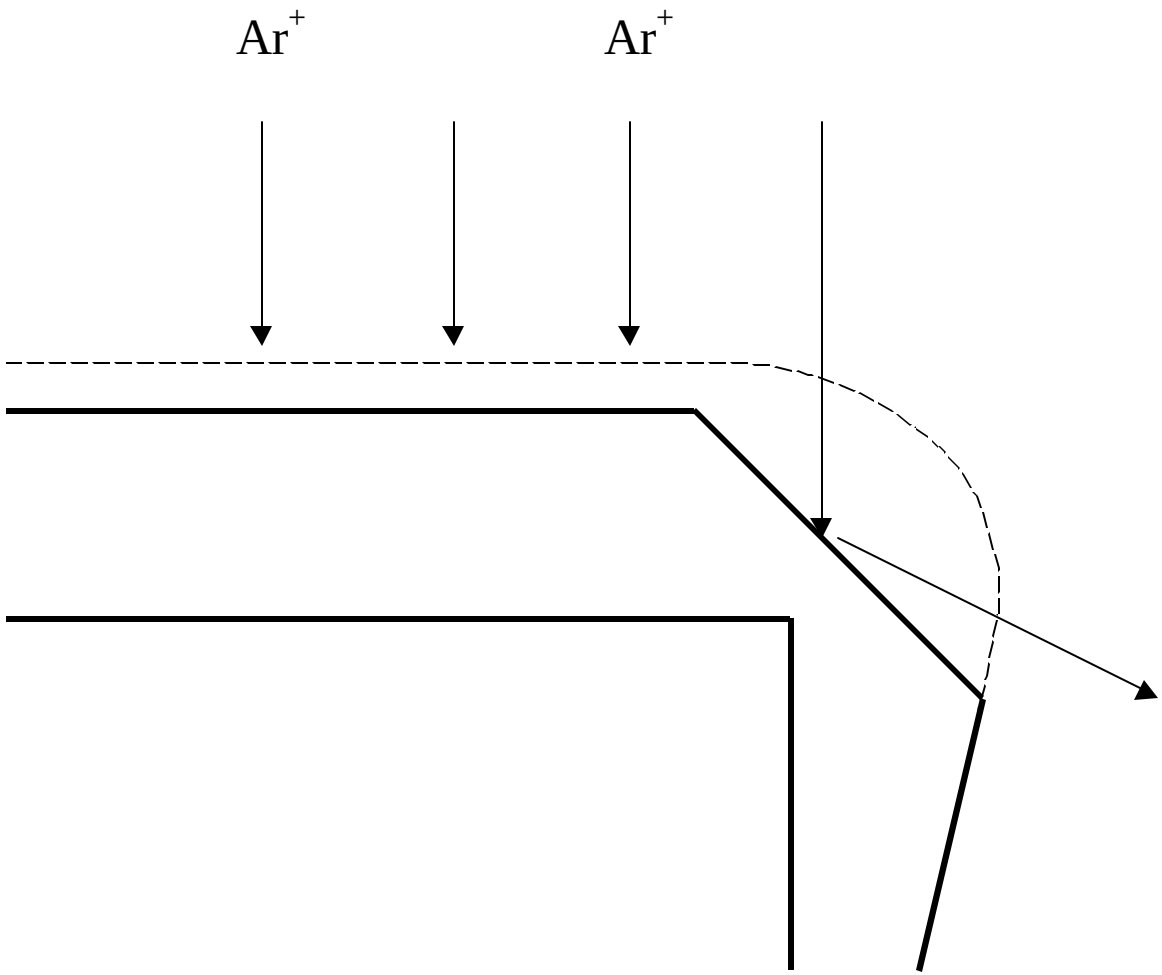
- Gap fill and planarization
- Performed in thin film bay with DCVD
- Cluster tool
- In-situ dep/etch/dep process

In-situ Dep/Etch/Dep Process





Sputtering Corner Chopping



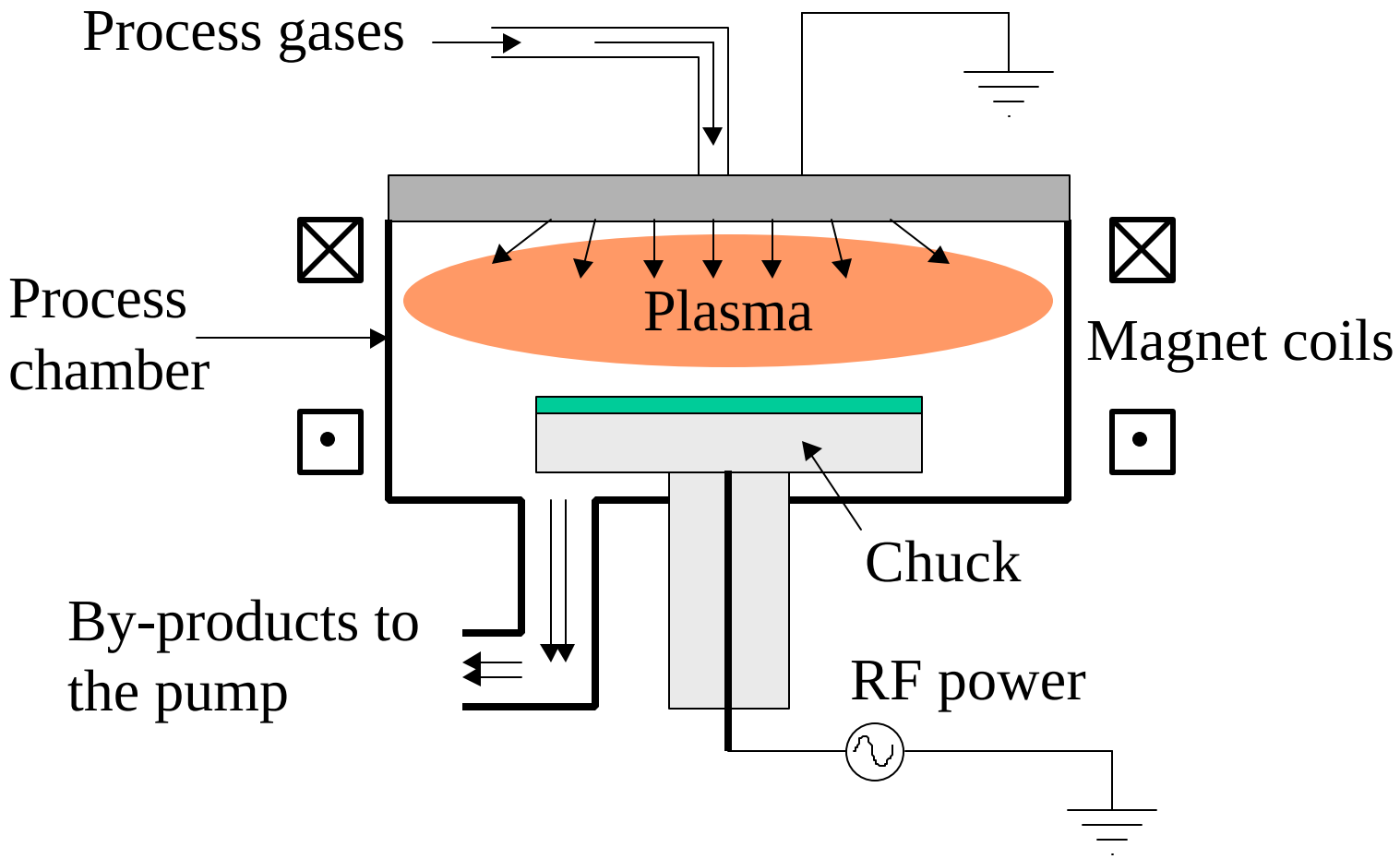
Question

- Why does sputtering etch process usually use argon as the process gas?

Answer

- It is inert, heavy, and relative inexpensive
- The atomic weight of argon is 40, compared with silicon's 28 and helium's 4
- Argon is the third most abundant element in earth atmosphere (~ 1%) only after nitrogen (78%) and oxygen (20%)
- Can be purified directly from condensed air

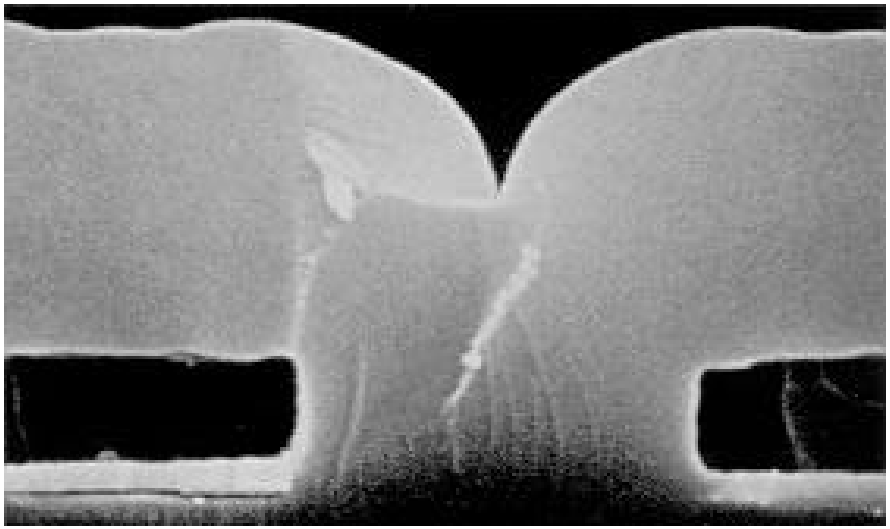
Schematic of Sputtering Etch Chamber



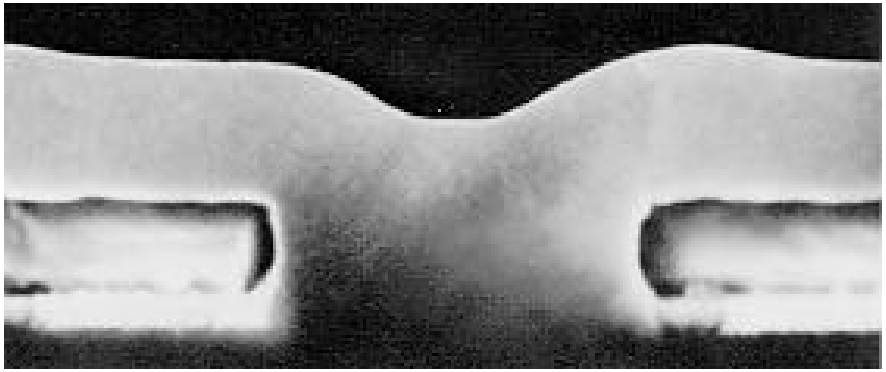
Reactive Etch Back

- CF_4 and O_2
- Heavy bombardment with chemical reaction
- Applications
  - Planarize dielectric surface
  - SOG etch back

Reactive Etch Back Planarization



2 μm PE-TEOS oxide deposition



1 μm planarization etchback

O_3-TEOS Processes

- Ozone is a very unstable molecule,

$$O_3 \rightarrow O_2 + O$$

- At 400 °C, half-lifetime of O_3: < 1ms
- Used as carrier of free oxygen radicals
- Ozone reacts with TEOS form silicon oxide
- Excellent conformality and gap fill capability
- Sub-micron IC chip applications
- APCVD and SA-CVD

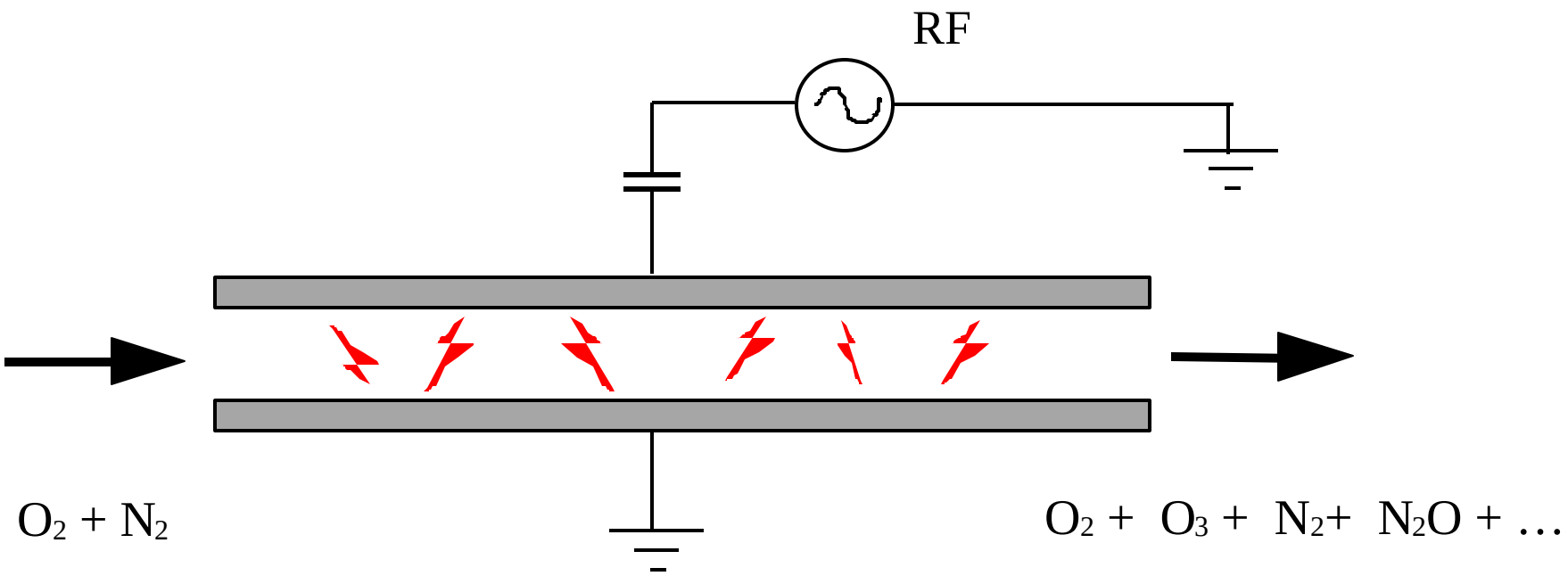
Ozone Generation

Lighting, corona discharge

$$O_2 \xrightarrow{\text{plasma}} O + O$$

$$O + O_2 + M \rightarrow O_3 + M \ (M = O_2, N_2, Ar, He, \text{etc.})$$

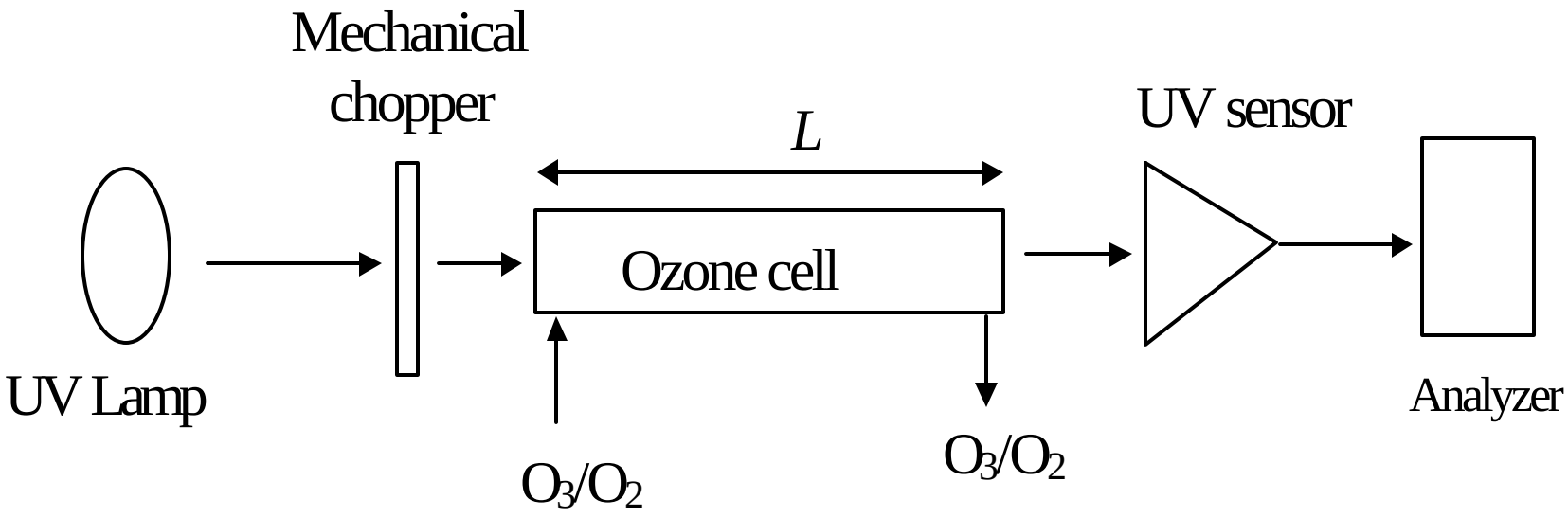
Illustration of Ozonator



Ozone Concentration Monitoring

Monitored by UV absorption (Beer-Lambert law):

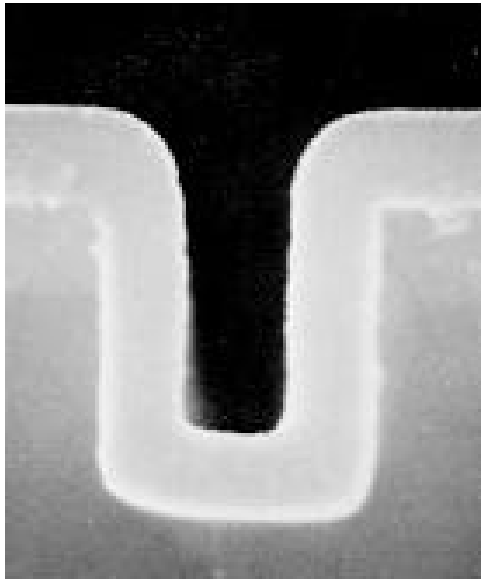
$$I = I_0 \, exp(-XCL)$$



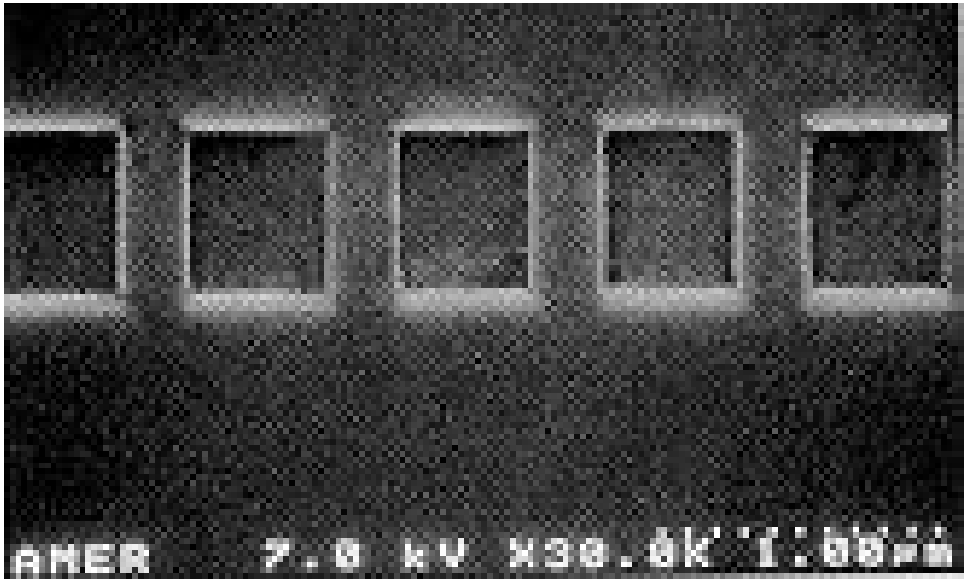
O_3-TEOS USG Process

- $TEOS + O_3 \xrightarrow[\text{heat}]{} SiO_2 + \text{volatile organics}$
- Main applications
  - STI (higher temperature, ~ 550 °C)
  - IMD (~ 400 °C)

O_3-TEOS USG



Step coverage



Gap fill

O_3-TEOS BPSG and PSG Process

$$O_3 \rightarrow O_2 + O$$

$$O + TEB + TEPO + TEOS \xrightarrow[\text{heat}]{} BPSG + \text{volatile organics}$$

$$O + TEPO + TEOS \xrightarrow[\text{heat}]{} PSG + \text{volatile organics}$$

- Main application
  - PMD

O_3-TEOS BPSG

O_3-TEOS BPSG

Barrier Nitride

Silicide

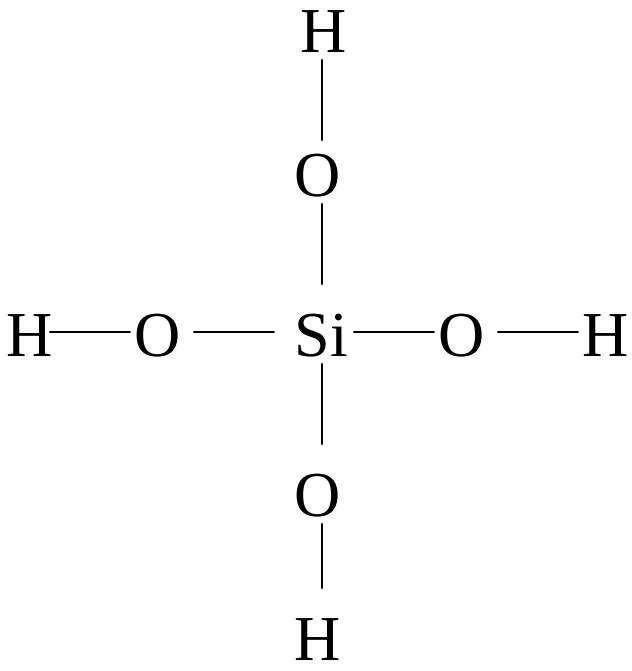
Poly Si

SACVD BPSG for 0.25 μm gap and 4:1 A/R.

Spin-on Glass (SOG)

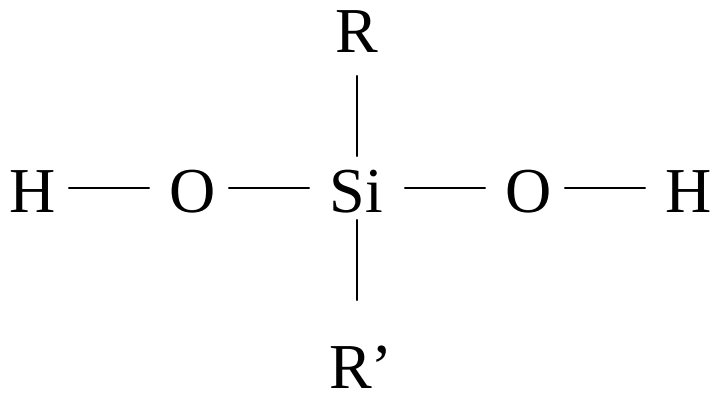
- Similar to PR coating and baking process
- People in fab like familiar technologies
- IMD gap fill and planarization
- Two kinds of spin-on glass:
  - Silicate
  - Siloxane

Spin-on Glass: Silicate and Siloxane



$Si(OH)_4$

Silicate

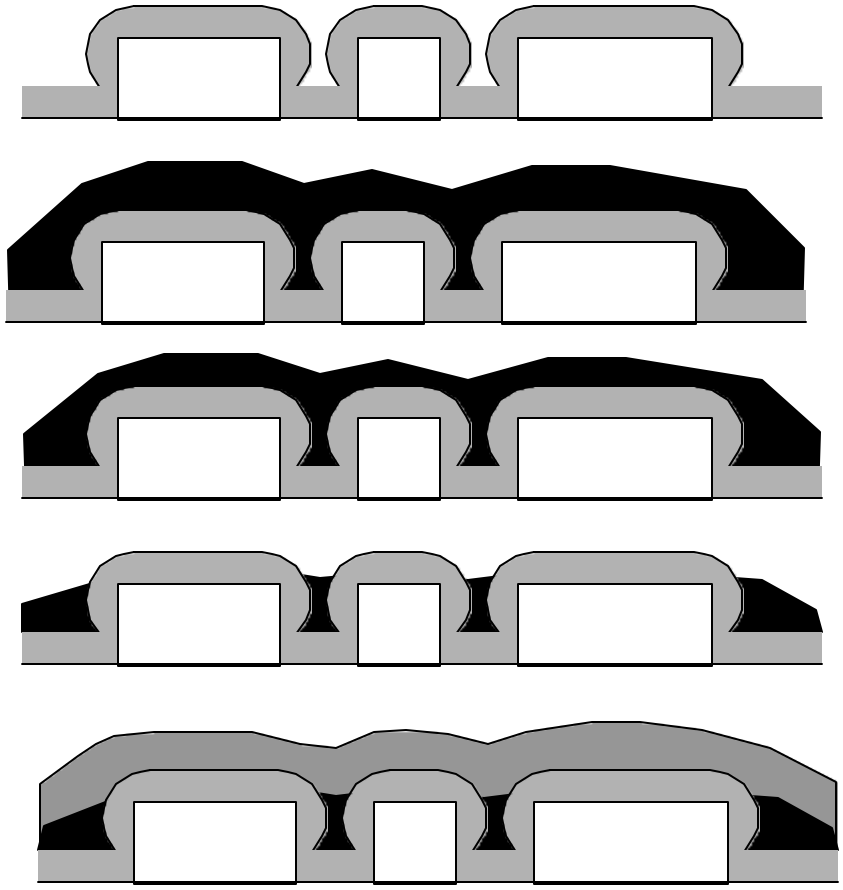


$R = CH_3$, R' = R or OH

$R_nSi(OH)_{4-n}$, n = 1, 2

Siloxane

Spin-on Glass Process Steps



PECVD USG barrier layer

Spin-on glass

SOG cure

SOG etchback

PECVD USG cap

High-Density Plasma CVD

- Dep/etch/dep gap fill needs two chambers
- Narrower gaps may need more dep/etch cycles to fill
- A tool can deposit and sputtering etch simultaneously would be greatly helpful
- The solution: HDP-CVD

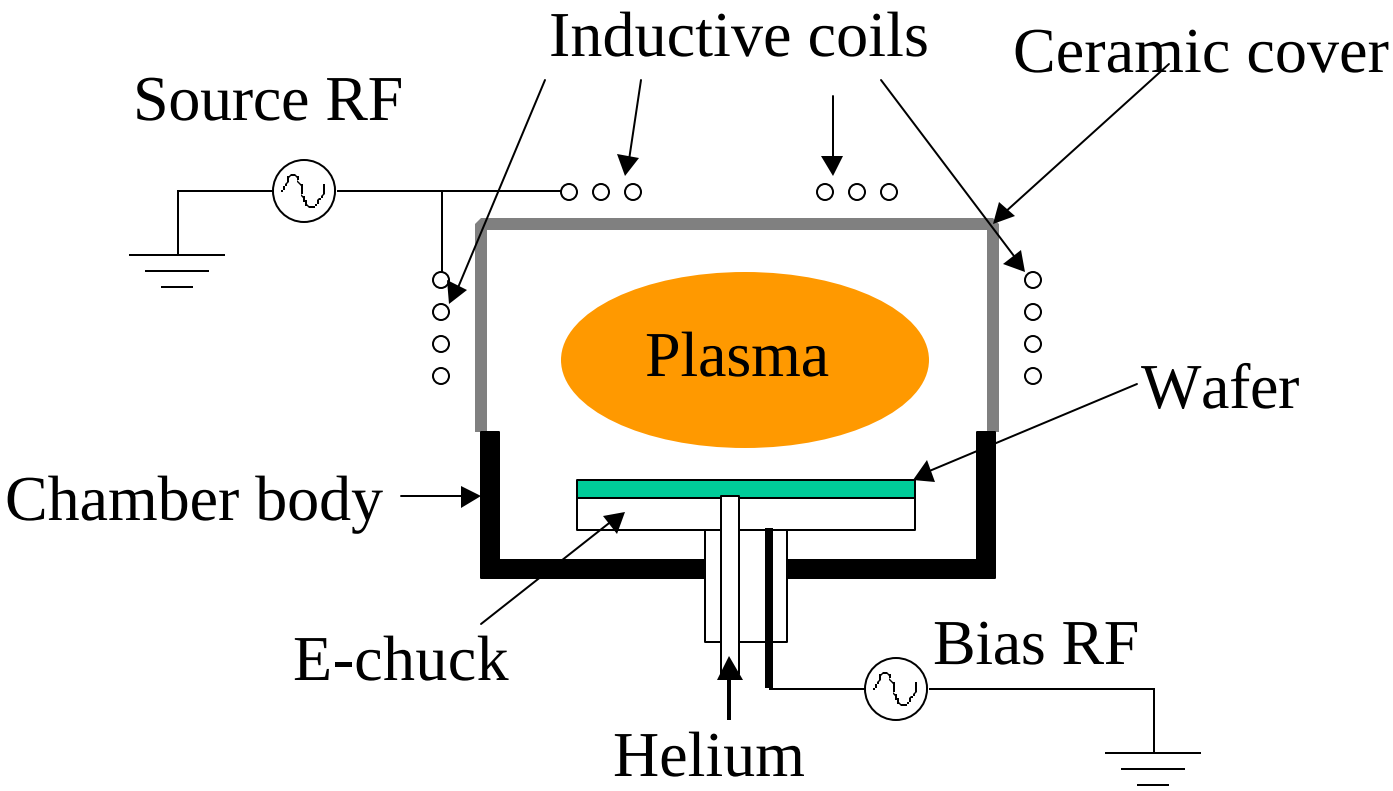
Question

- With the feature size shrinking, metal line width and gap between metal lines becomes smaller. However the metal line height doesn't shrink accordingly, which causes larger gap aspect ratio.
- Why doesn’t shrink metal line height accordingly to keep the same aspect ratio and easier for dielectric gap fill?

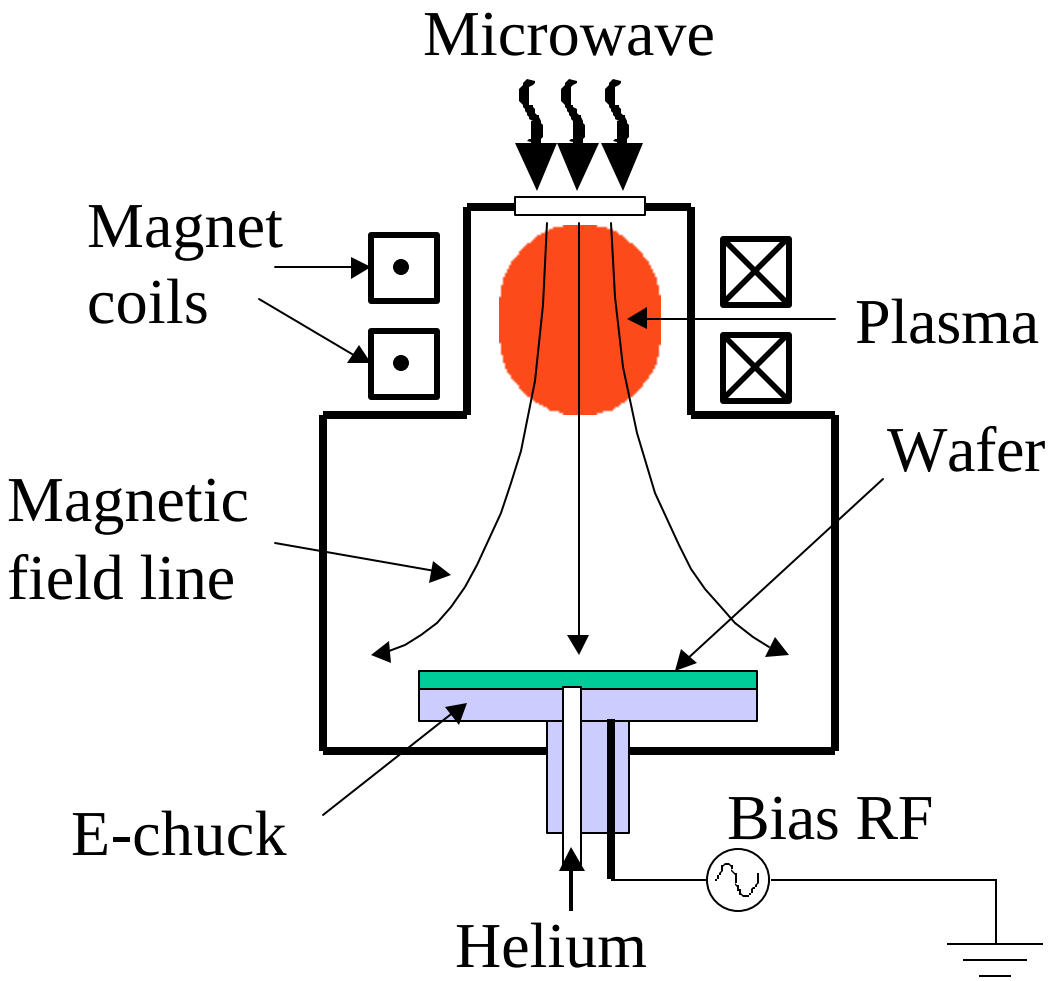
Answer

- Metal line resistance $R = r\ l/wh$.
- If h also reduces accordingly to l and w, resistance will increase accordingly
- Therefore, line has to keep the same height

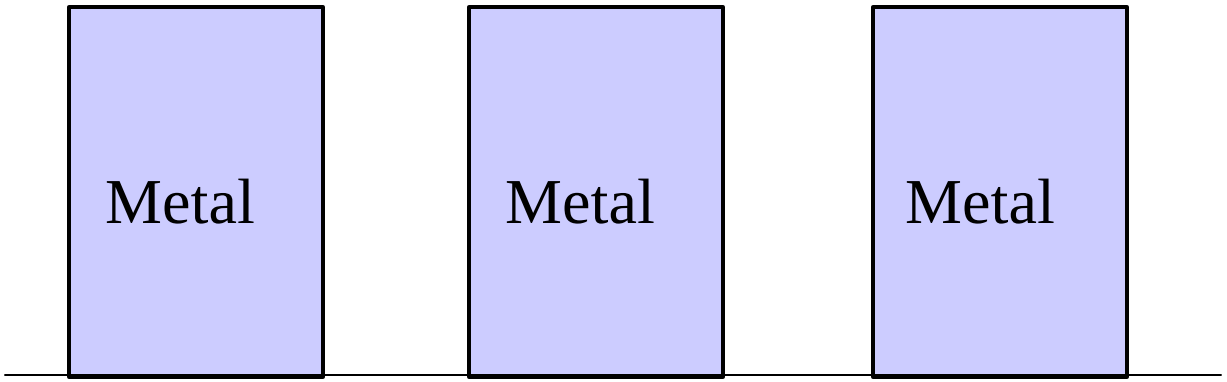
Inductively Coupled Plasma Chamber



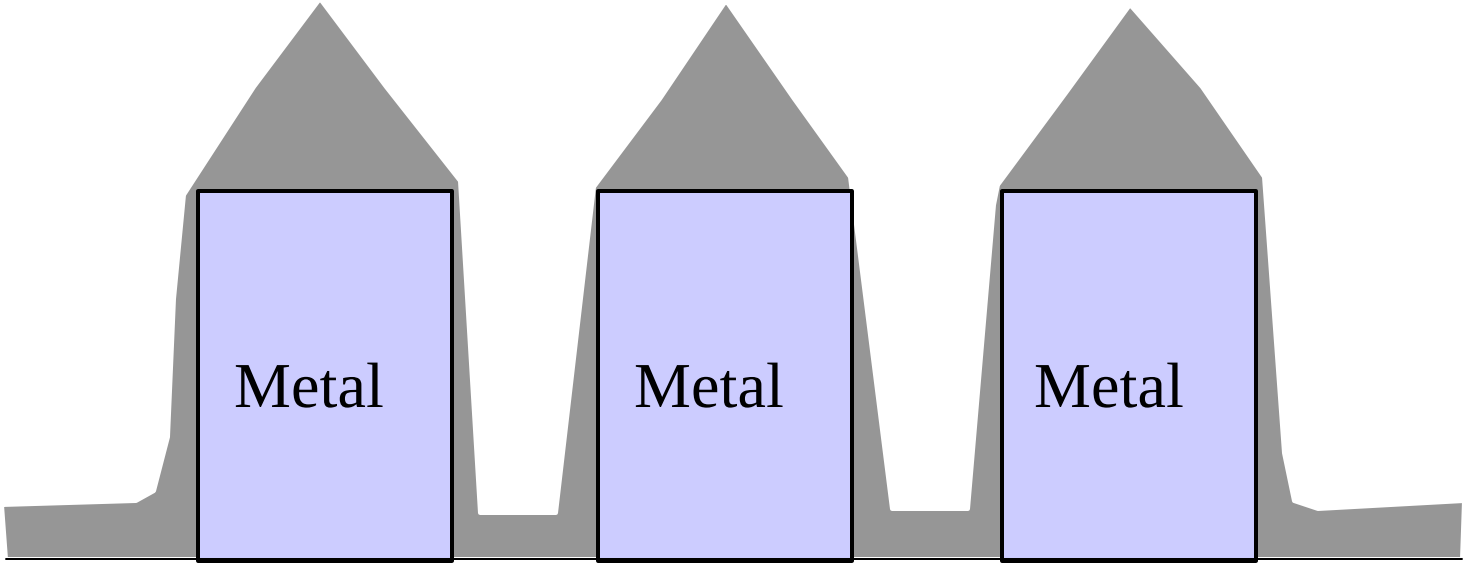
ECR Chamber


Microwave
Magnet coils
Plasma
Wafer
Magnetic field line
E-chuck
Bias RF
Helium

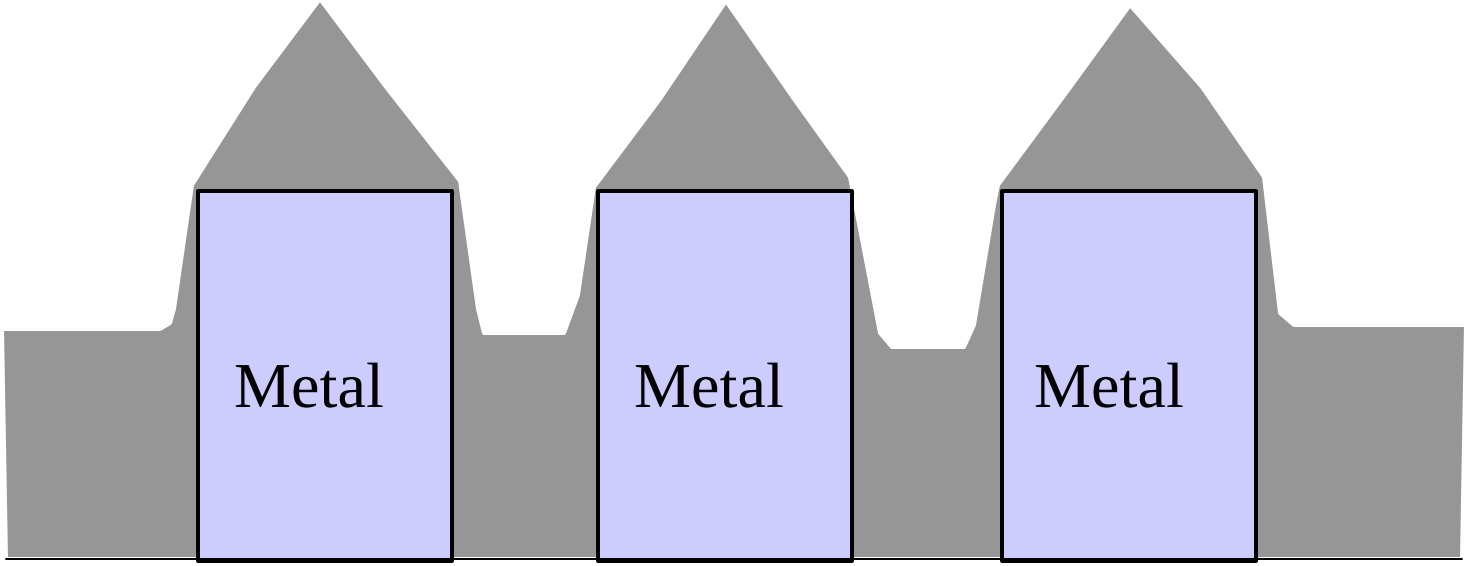
HDP-CVD, IMD Application



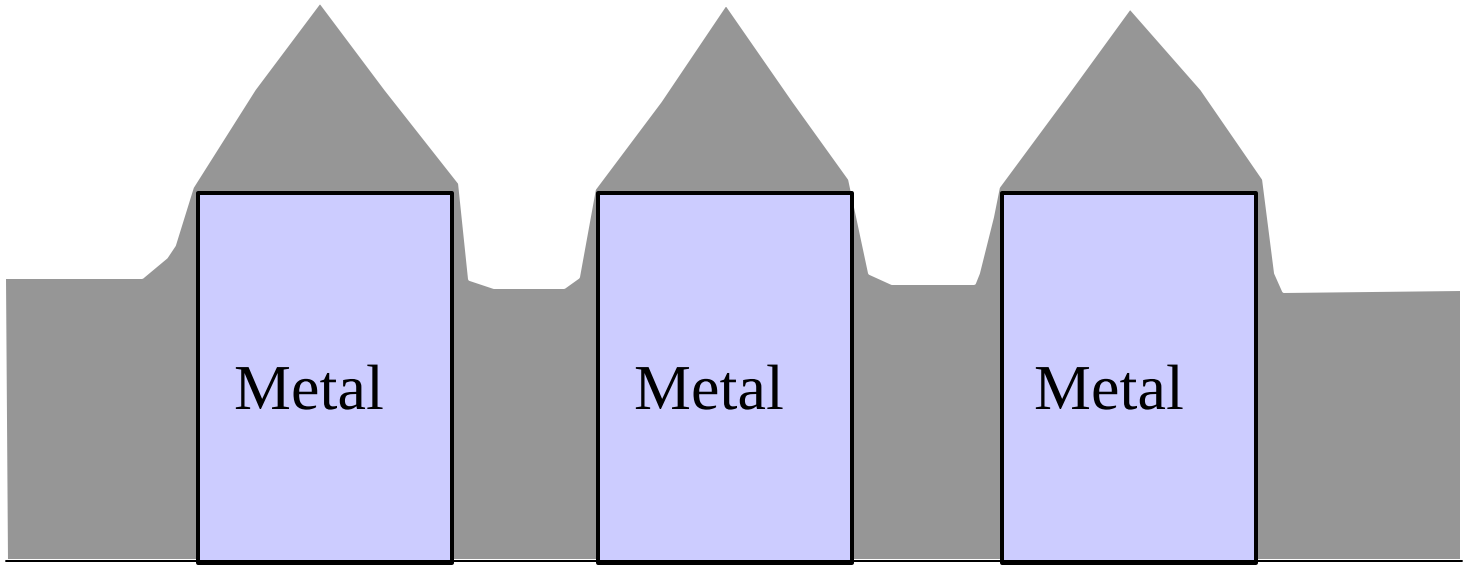
HDP-CVD, Deposition



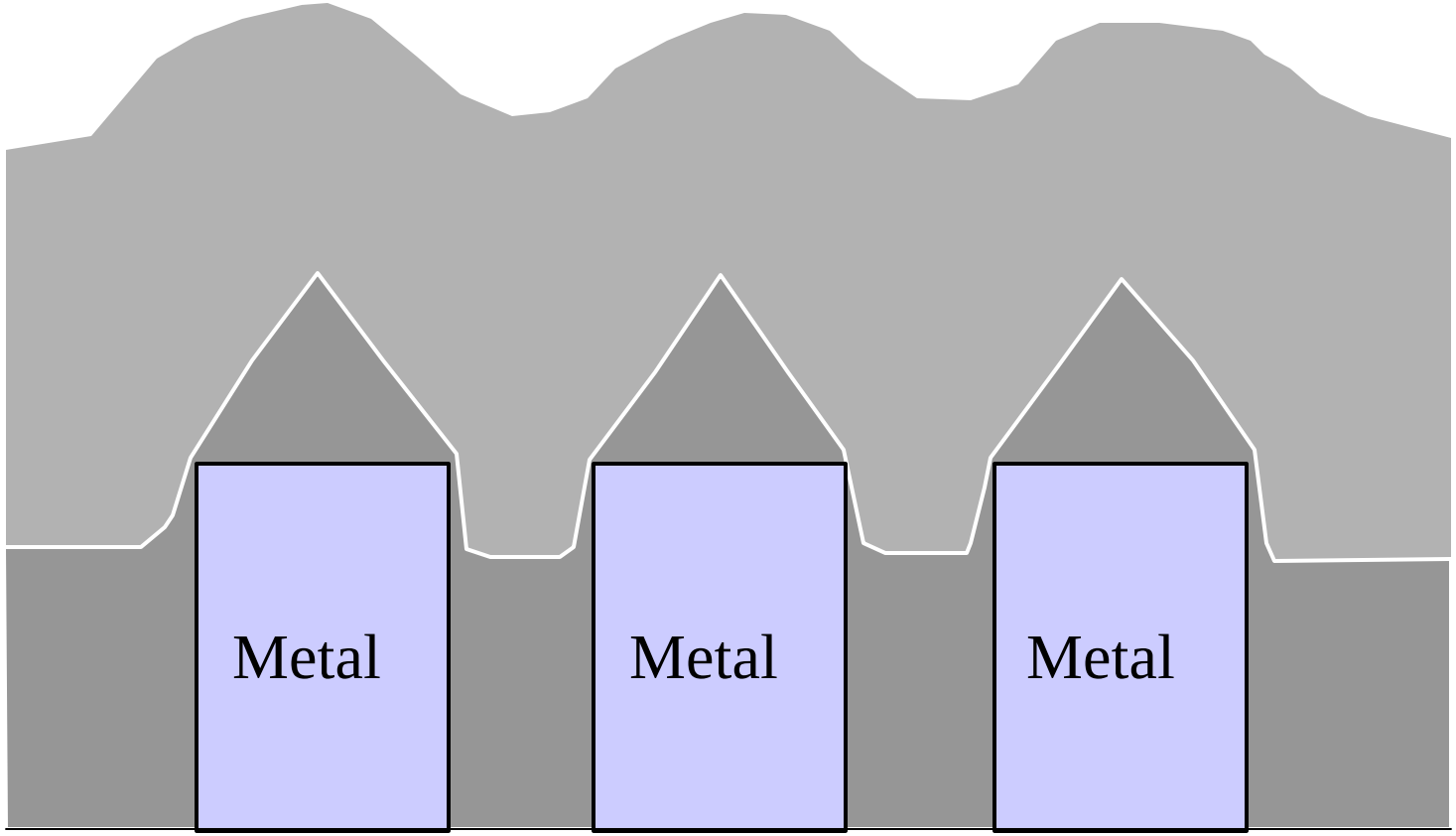
HDP-CVD, Deposition



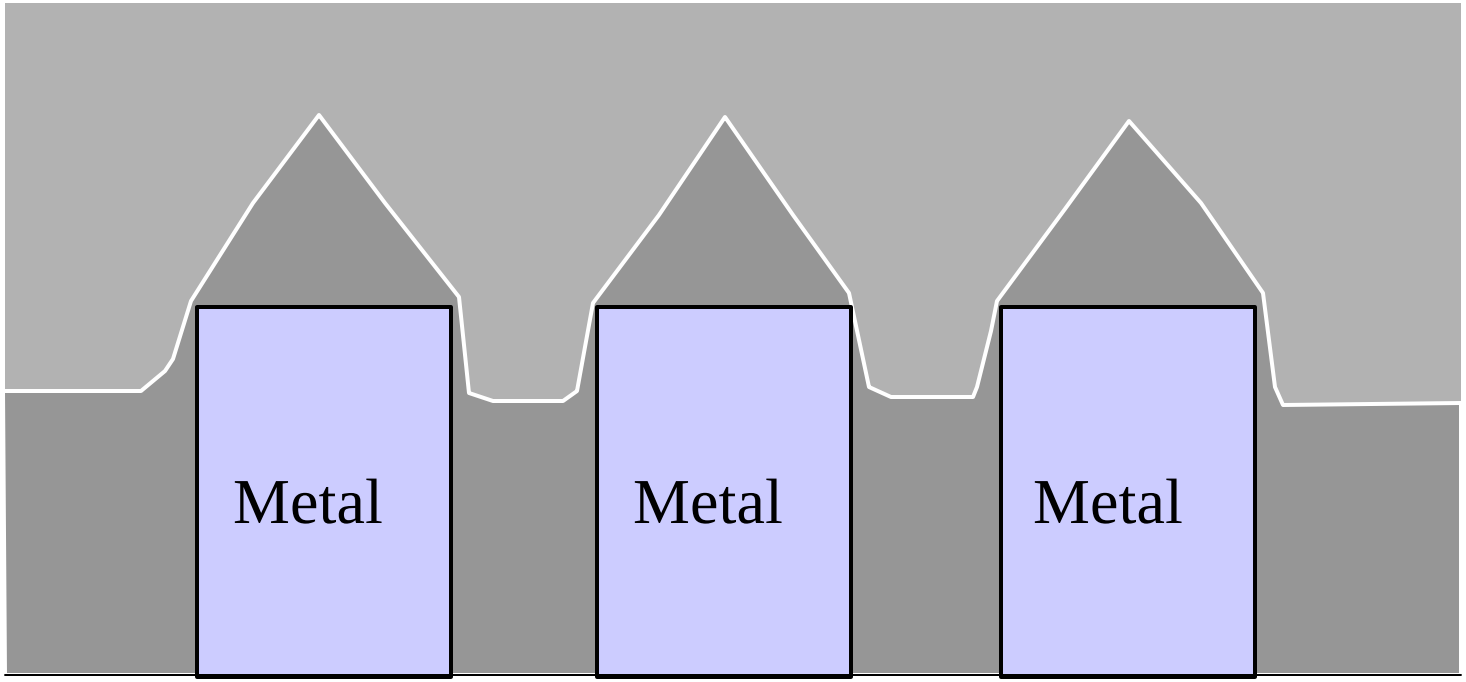
HDP-CVD, Deposition



PE-TEOS Deposition



Oxide CMP



HDP-CVD Processes

- For IMD Applications
- USG $SiH_4 + O_2 + Ar \rightarrow USG + H_2O + Ar + \ldots$
- FSG $SiH_4 + SiF_4 + O_2 + Ar \rightarrow FSG + volatiles$
- For PMD Applications
- PSG $SiH_4 + PH_3 + O_2 + Ar \rightarrow PSG + volatiles$

Question

- Why is silane instead of TEOS used as the silicon source gas for the HDP CVD oxide process?

Answer

- For HDP CVD processes, step coverage is no longer an important factor for the gap fill
- Heavy ion bombardment always keeps gap tapered and deposition is bottom up.
- Using silane can save the costs and hassles related with vapor delivery system of the liquid TEOS source.

Dielectric CVD Chamber Clean

- During dielectric CVD process, dielectric thin film will be deposited on everything inside chamber
- Need to routinely clean the chamber to prevent particulate contamination problems.
- For DCVD, more time for clean than dep.
- RF plasma clean and remote plasma clean

RF Plasma Clean

- Plasma clean process remove dielectric film on the process kits and chamber wall
- Fluorocarbon such as CF_4, C_2F_6 and C_3F_8
- In some case NF_3 is also used
- In plasma, fluorocarbon will be dissociated
- Free fluorine, F, will be generated
- F removes silicon oxide and silicon nitride

RF Clean Chemistry

$$CF_4 \xrightarrow{\text{plasma}} CF_3 + F$$

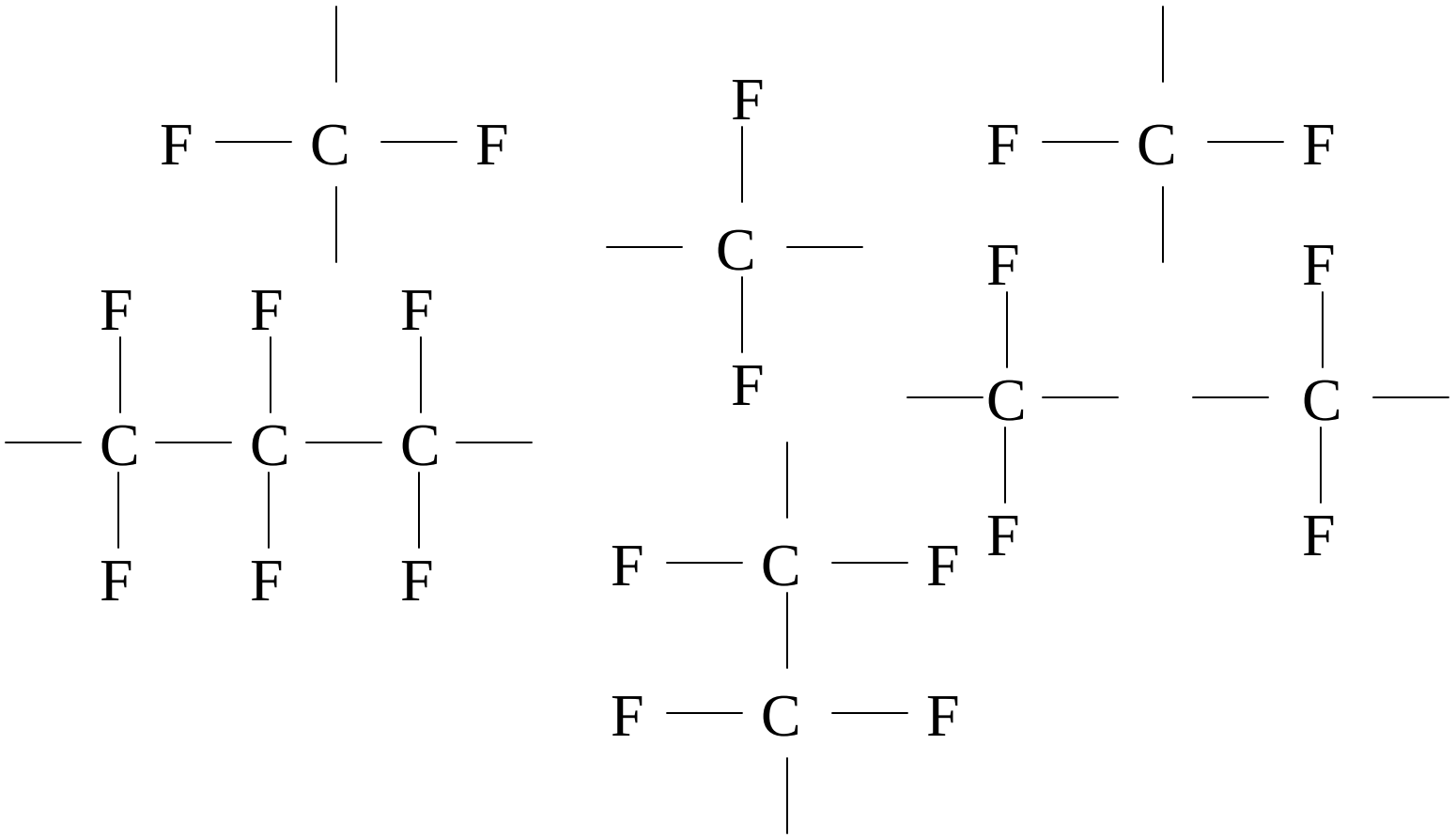
$$F + SiO_2 \xrightarrow[\text{heat}]{\text{plasma}} SiF_4 + O$$

$$F + Si_3N_4 \xrightarrow[\text{heat}]{\text{plasma}} SiF_4 + N$$

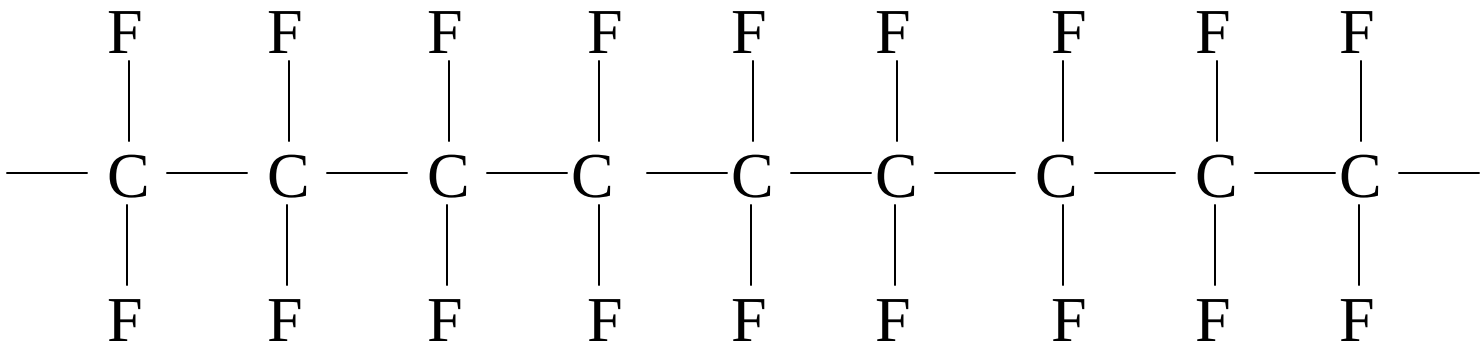
RF Clean Chemistry

- In plasma clean processes, oxygen source gases such as N_2O and O_2 are used with fluorocarbon to react with carbon and free more fluorine radicals
- Increase F/C ratio, keep it > 2
- Prevent carbon fluoride polymerization, and increases the clean efficiency

CF_2 and Reconnection



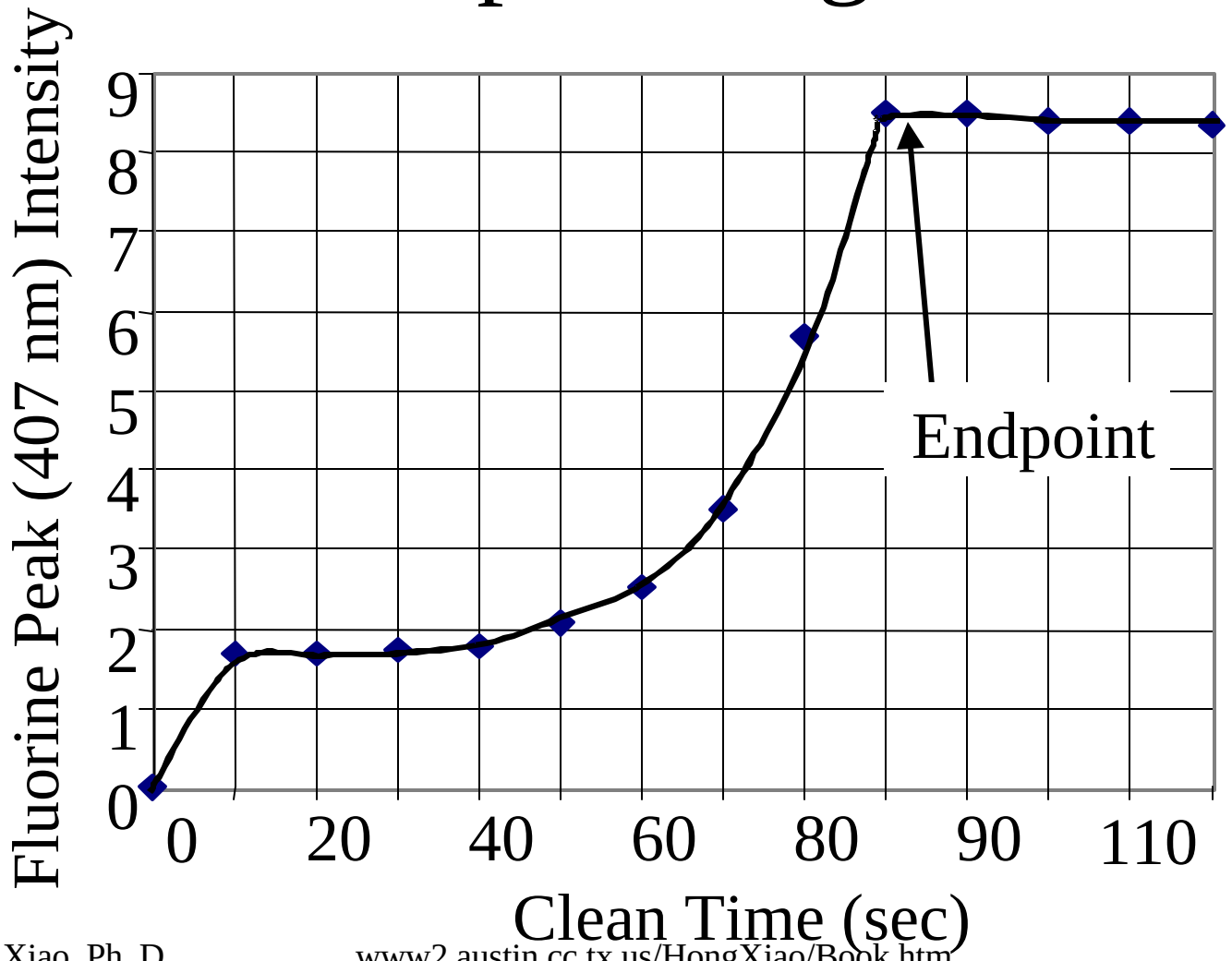
Polymerization, Teflon Deposition



RF Clean Endpoint

- Excitation-relaxation cause glow
- Different gases have different colors of light
- Information of chemical components in plasma
- Monitor line emission to control clean process

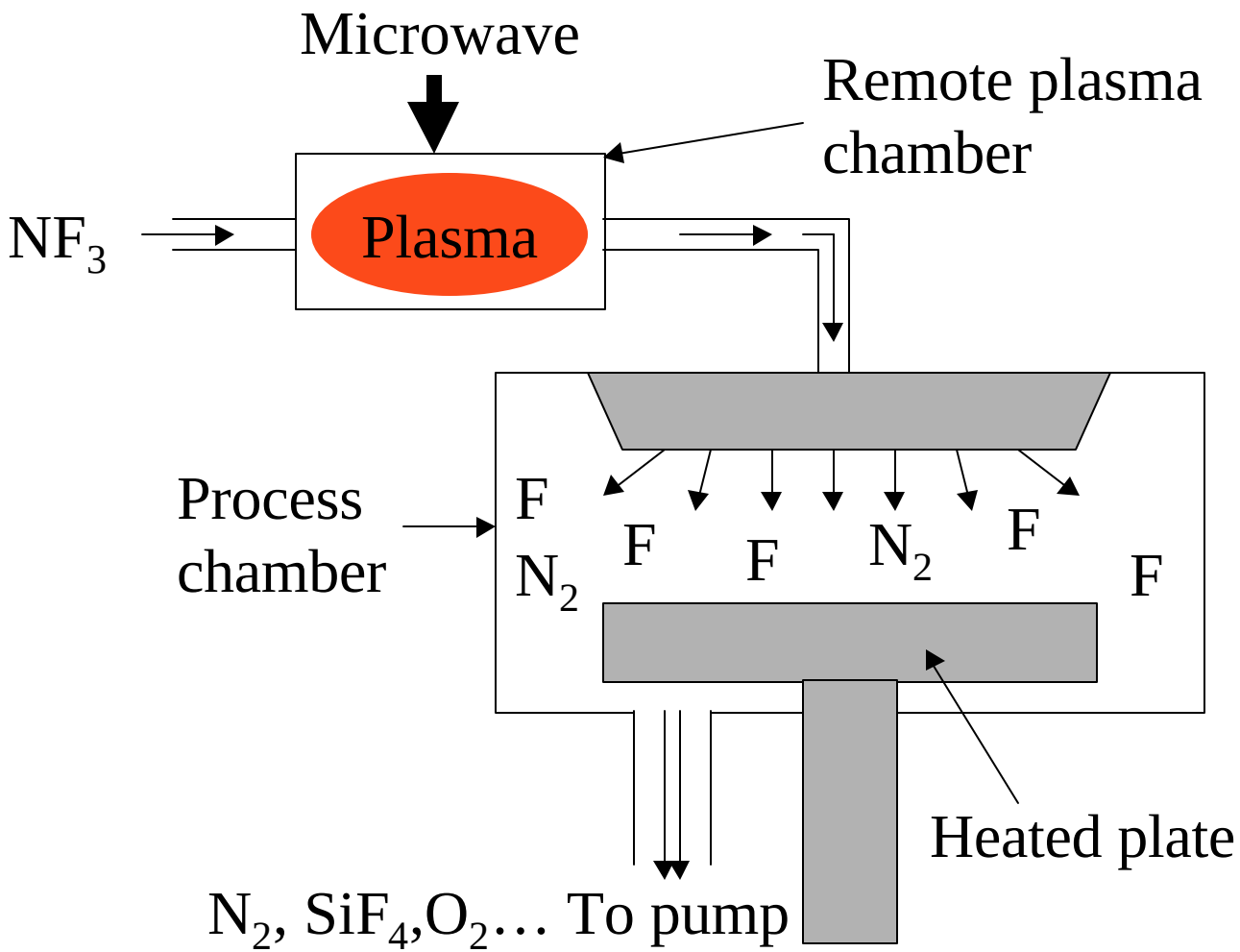
Endpoint Signal



Remote Plasma Clean

- RF Plasma clean
  - Ion bombardment
  - Cause damage on chamber parts
- Remote plasma clean
  - No ion bombardment
  - More gentle on chamber parts
  - Longer part lifetime
  - Less “green house” gas emission

Illustration of Remote Plasma Clean



Remote Plasma Clean

- Microwave (MW) power, NF_3 as fluorine source
- 99% of NF_3 dissociated in MW plasma
- Free fluorine reacts with the film in chamber
  - No plasma inside process chamber
  - No ion bombardment
  - Prolongs their lifetime
- Disadvantages:
  - Less maturity, higher cost, and using NF_3
  - Can not use optical endpoint system, may need FTIR system to achieve the automatic process endpoint.

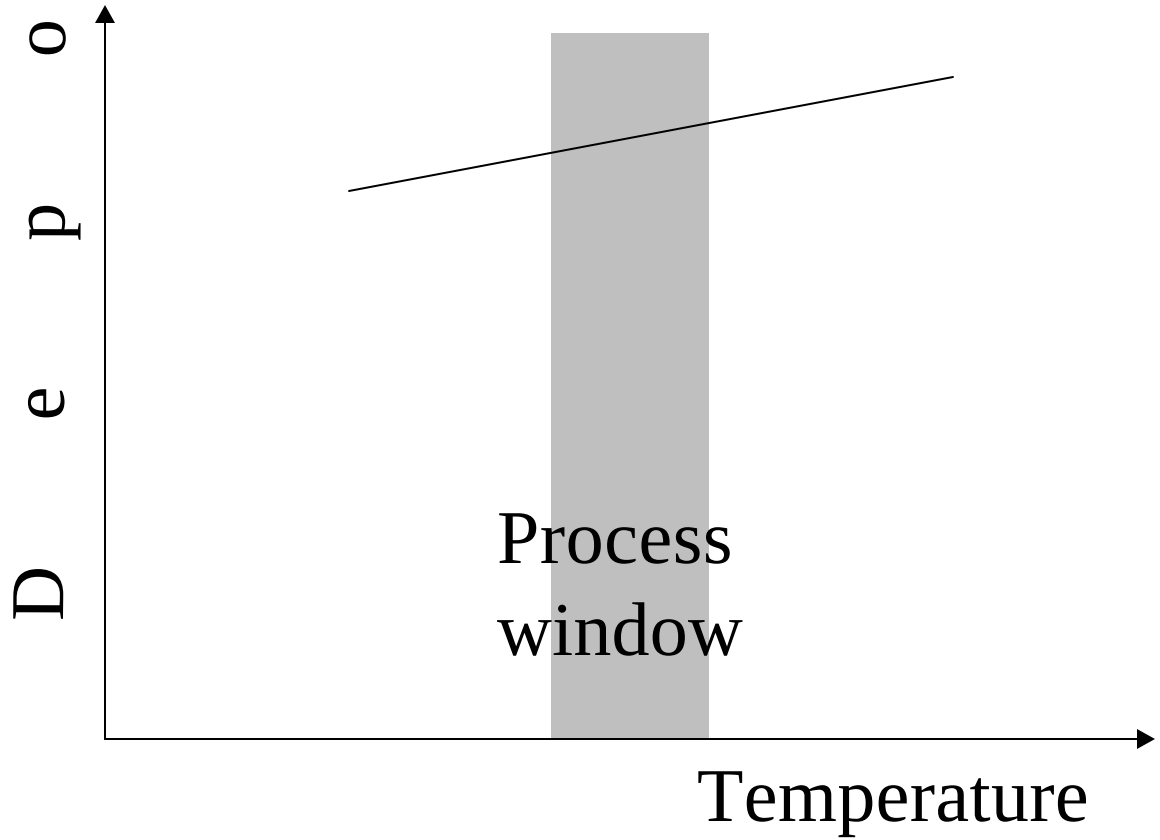
Process Trends and Troubleshooting

- Process response to input parameters change
- Help to determine the root cause if some wrong

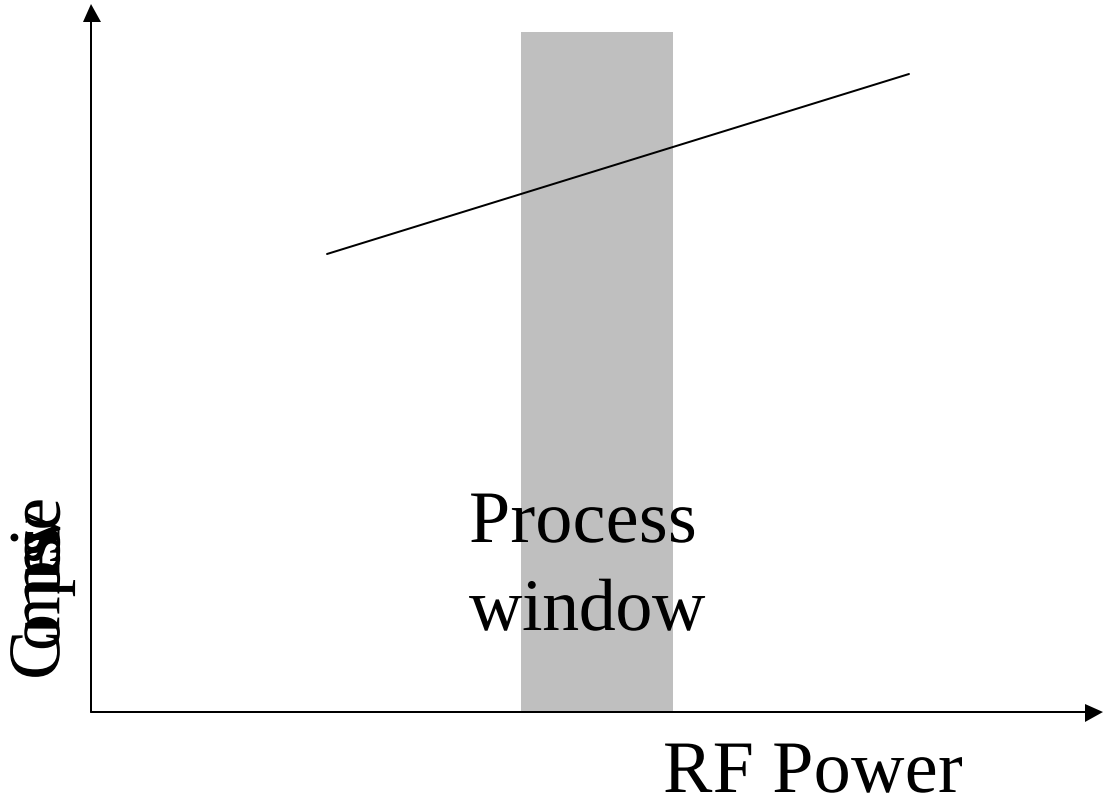
Silane PECVD Process Trends

- Increasing temperature increases deposition rate
  - Higher diffusion rate of precursors in boundary layer
- Increasing temperature improves deposited step coverage and film quality
- PMD uses a higher temperature
- IMD and PD, normally not exceed 400 ºC

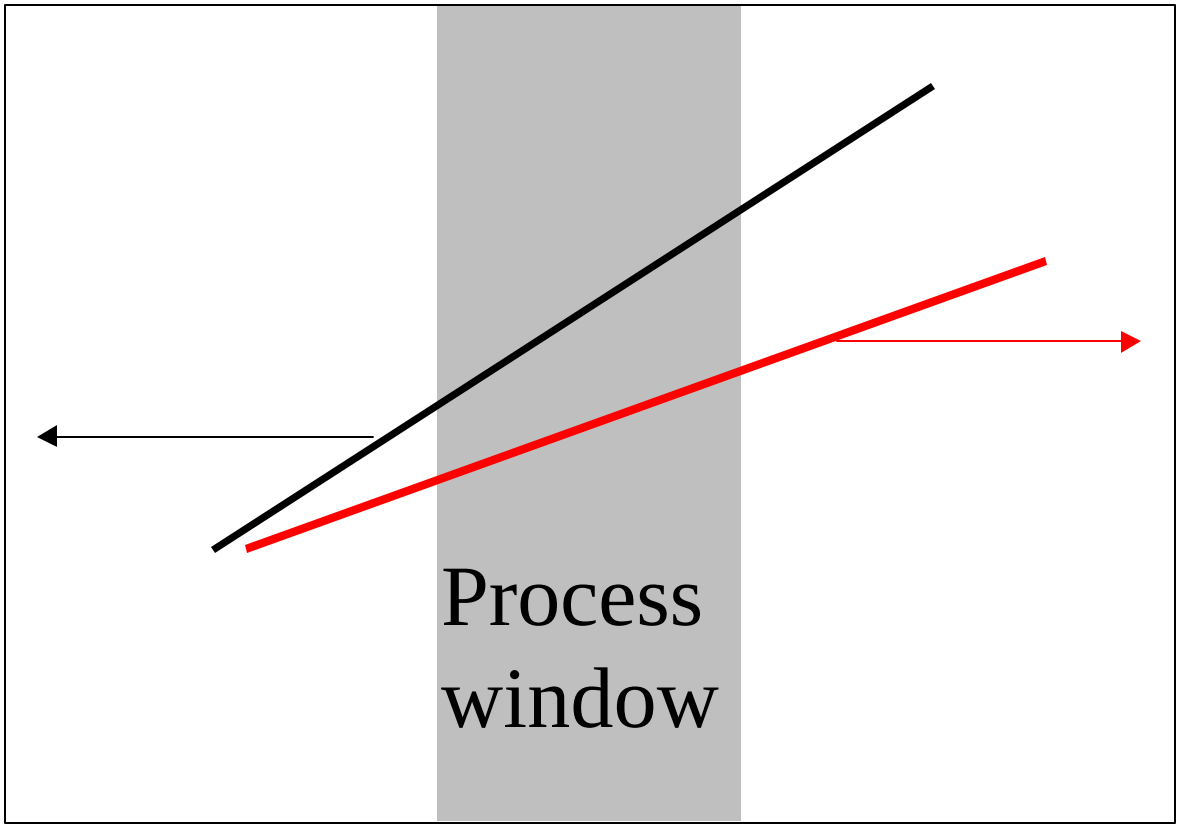
Deposition Rate and Temperature



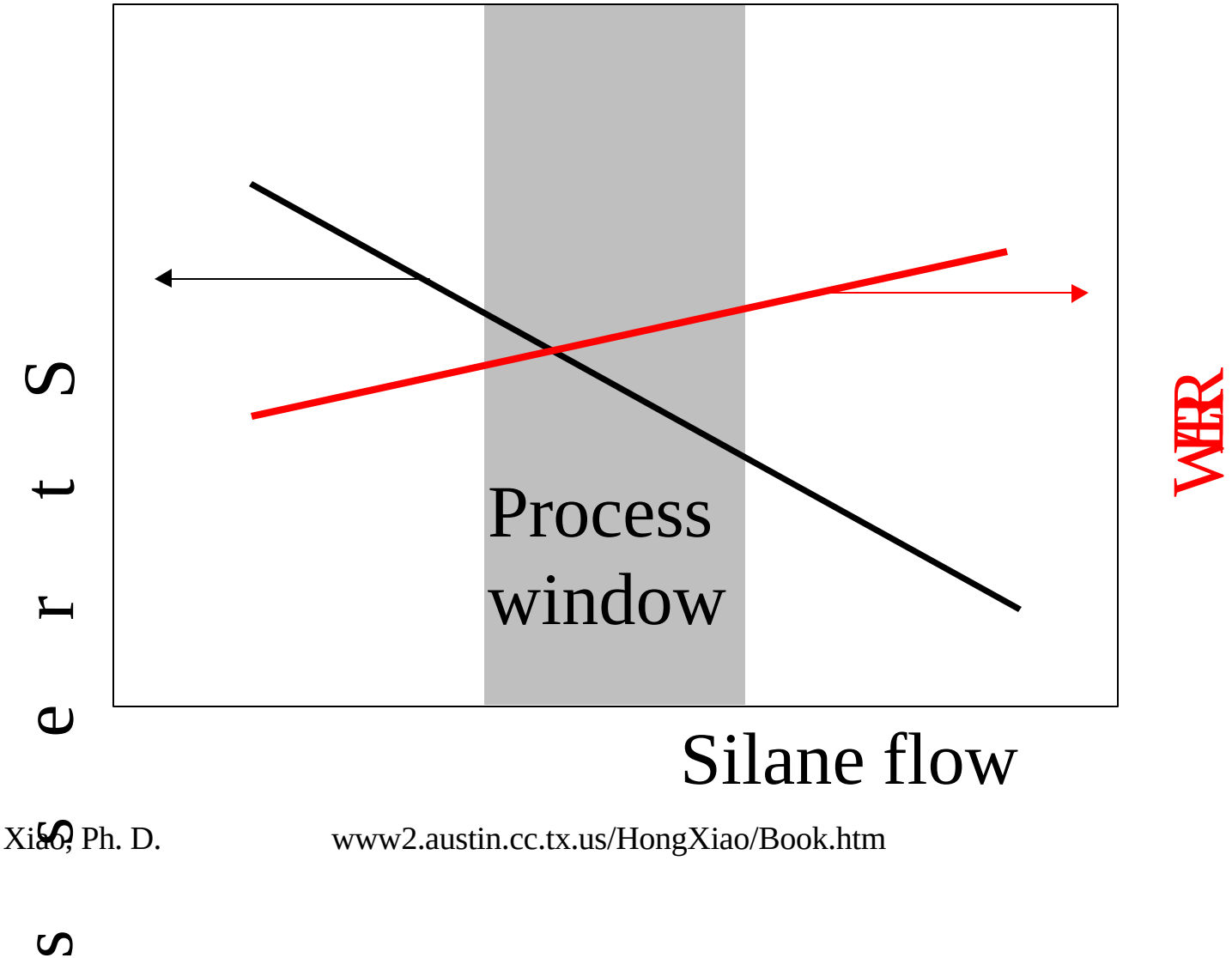
Stress and RF Power



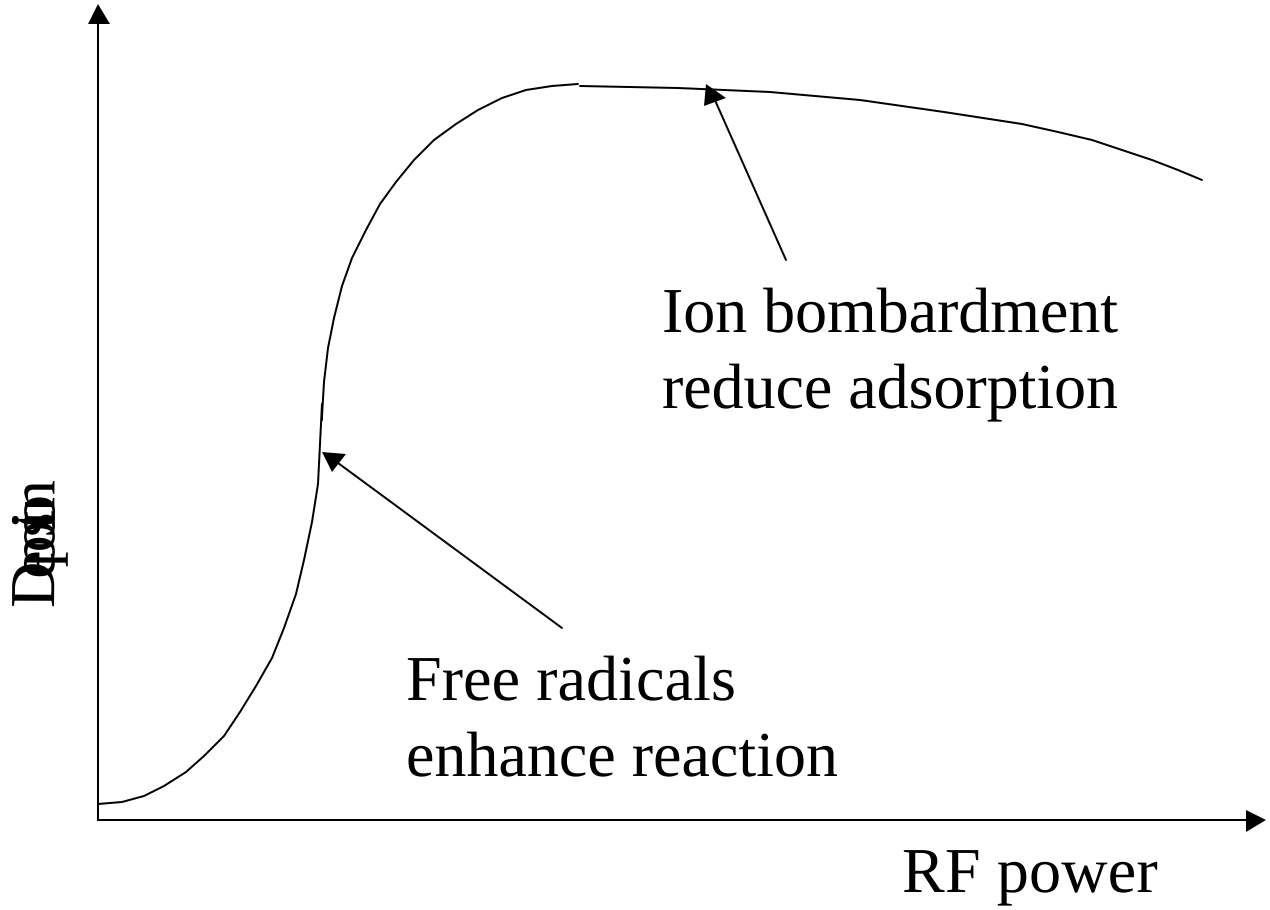
Silane PECVD Process Trends



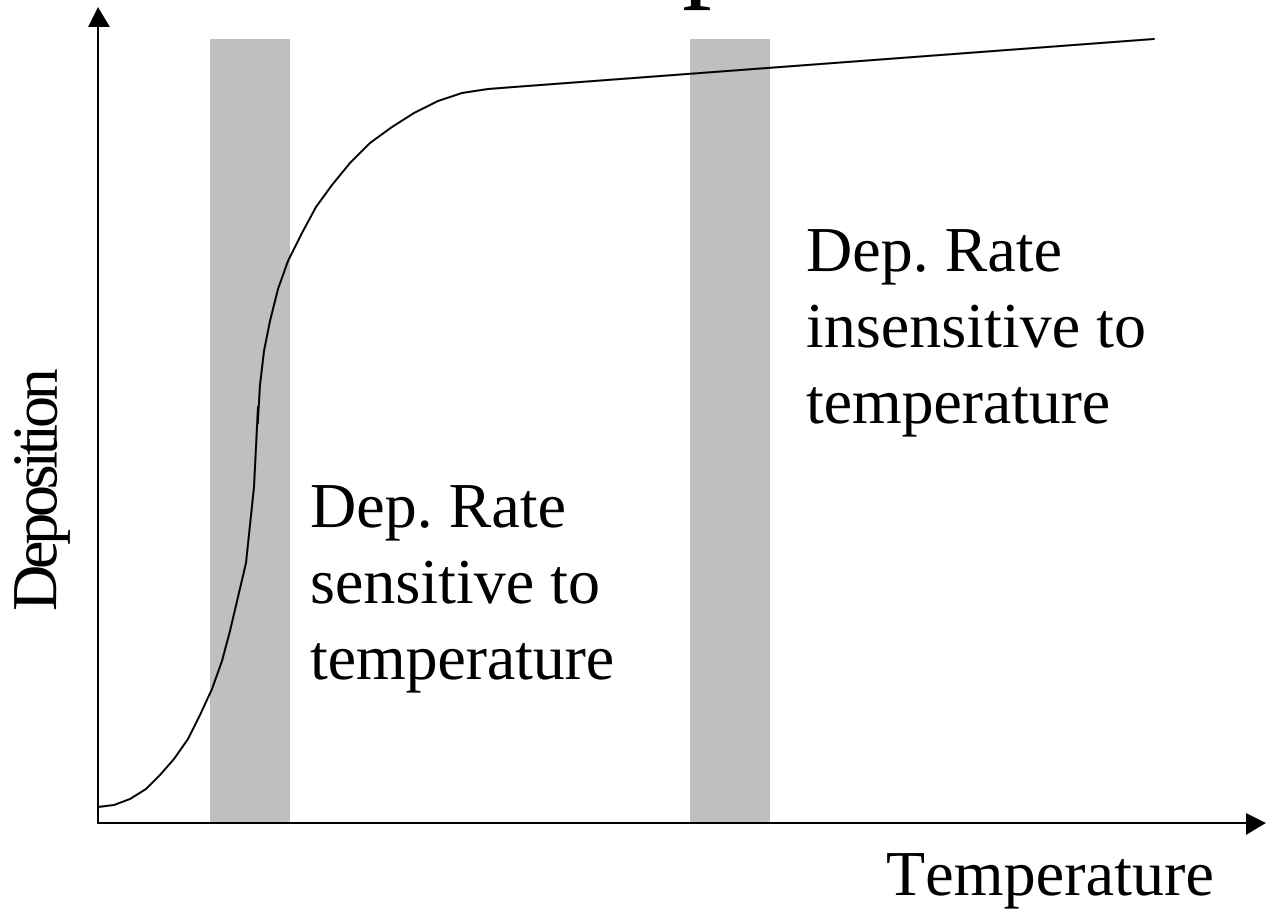
Silane PECVD Process Trends



Relationship of Deposition Rate and RF Power



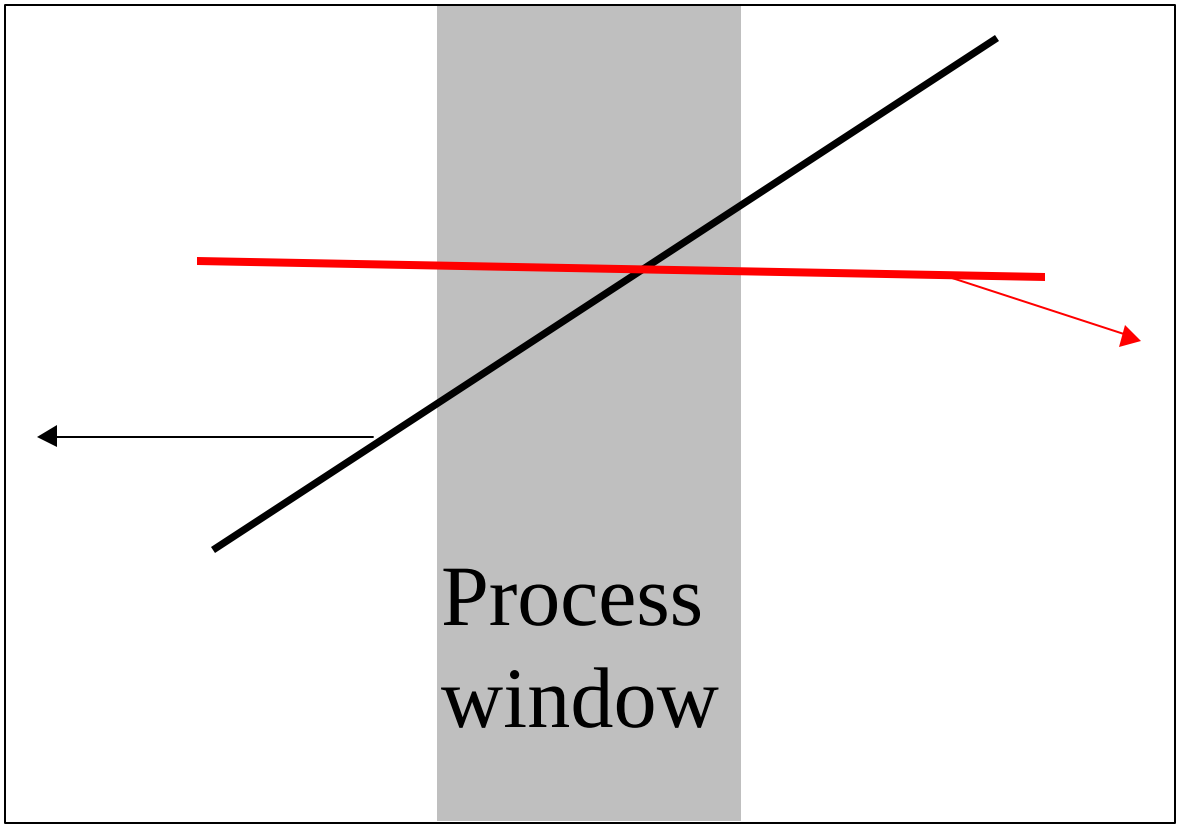
Relationship of Deposition Rate and Temperature



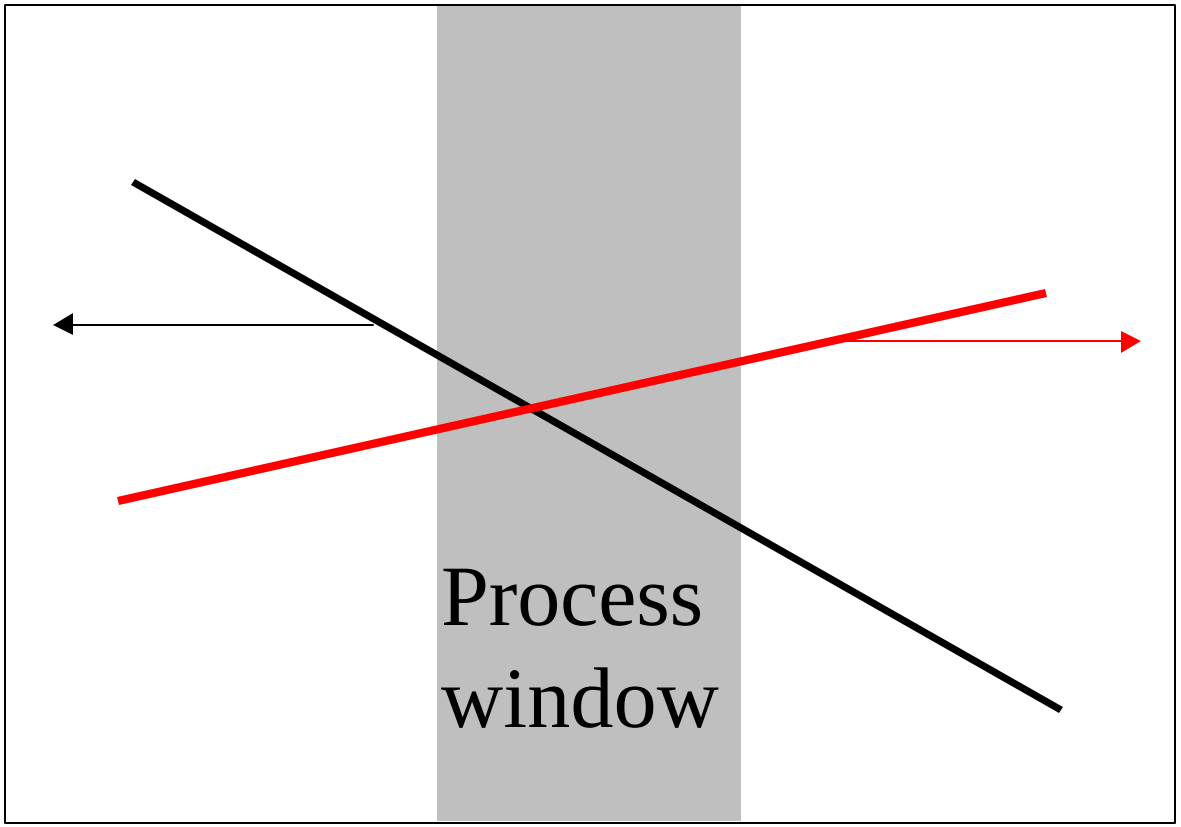
PE-TEOS Trends

- RF power↑: dep rate↑↓, compressive stress↑
  - In process window, dep rate go down
- Temperature↑: dep rate↑↓
  - In process window, dep rare go down
- TEOS flow↑: dep rate↑, compressive stress↓

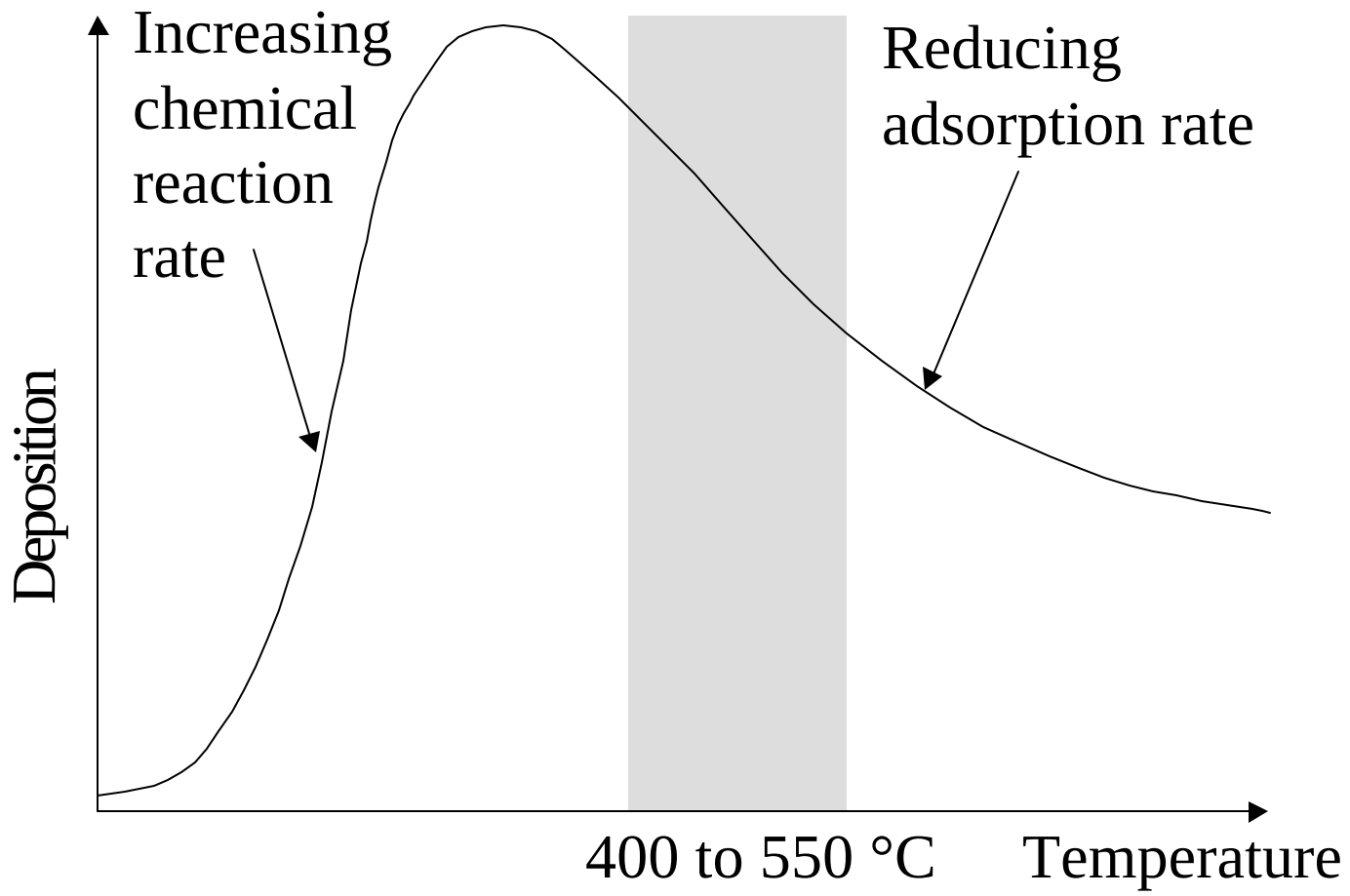
PE-TEOS Trends: TEOS Flow Rate



PE-TEOS Trends: TEOS Flow Rate



PE-TEOS Trends: Temperature



O_3-TEOS Trends

- Temperature↑: dep rate↑↓
  - In process window, dep rare go down
- TEOS flow↑: dep rate↑

Question

- For both PE- and O_3- TEOS processes, the maximum deposition rate can be achieved at about 250 ºC. Why do the IMD TEOS processes normally operate about 400 ºC and PMD and STI processes deposited even higher temperature (~ 550 ºC)?

Answer

- At higher deposition temperature, film quality is higher and step coverage is better

Troubleshooting

- Learned from hand-on experience
- Sudden process change, either suddenly goes wrong, or gradually goes wrong and suddenly comes back,
- Someone should check what has changed between good process and the bad process, or vice versa.

Troubleshooting

- Check metrology tool first and make sure the right recipe is used.
- If one measure PE-TEOS film with nitride recipe, measured thickness would be significantly thinner
- If nothing is wrong with metrology tool, then check whether the process recipe has been changed.

Troubleshooting

- Process always has problems at end of shift
- Someone should work cross shifts to find out what had been changed during shift change
- Something must be changed that put the process back to normal at the beginning of the next shift
- It most likely is the source of problems as the process gradually goes wrong at end of the shift

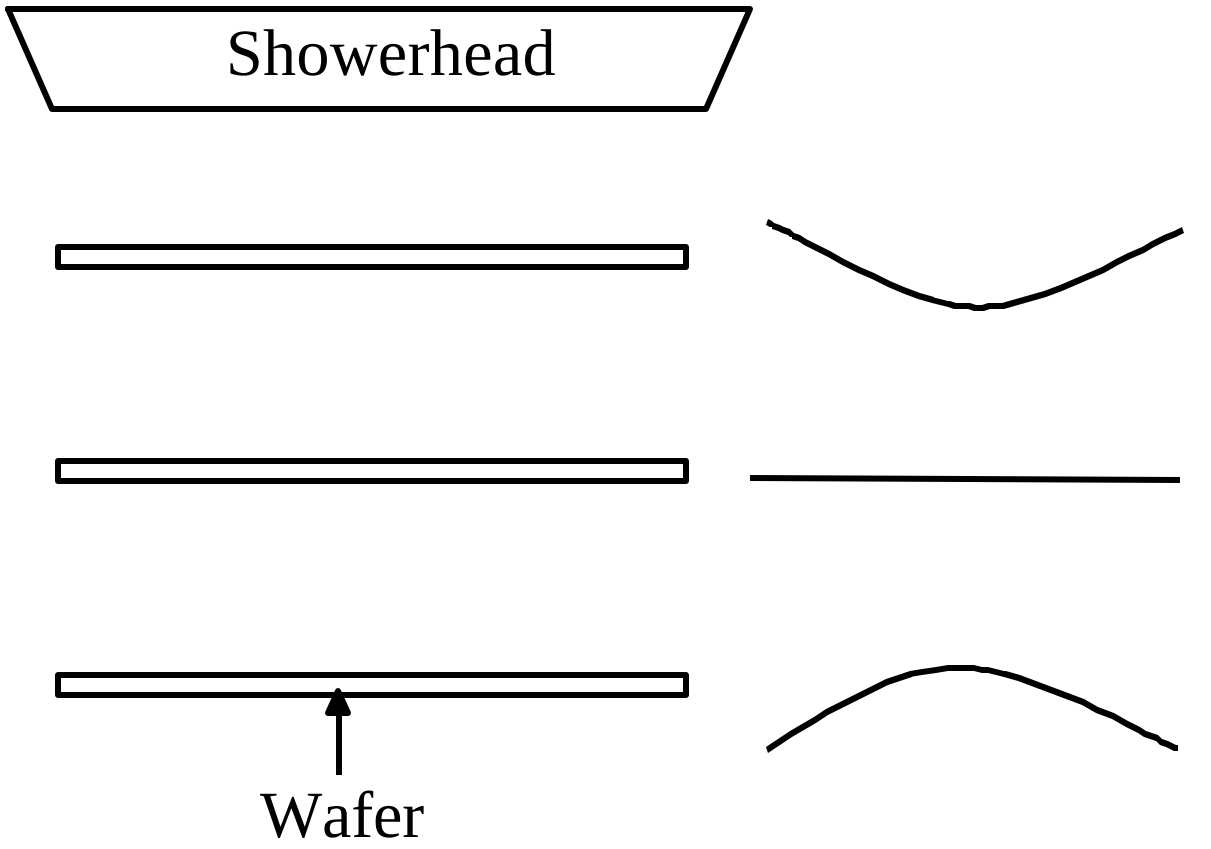
Troubleshooting

- Most dielectric CVD processes operate in mass-transport-limited regime
- Deposition rate is mainly determined by gas flow rate, usually silane and TEOS flow rate
- Very likely that deposition rate problems are related with silane or TEOS flow rate
- Mass flow controller and liquid flow controller

Troubleshooting: Non-uniformity

- Uniformity is determined by flow pattern
- If non-uniformity pattern is center symmetric
  - Adjusted spacing of the wafer and showerhead
  - Or changing the carrier gas flow rate
    - Helium flow for TEOS processes
    - Nitrogen flow for nitride process

Spacing and Film Profile



Smaller spacing
Higher dep. rate
Center thin profile

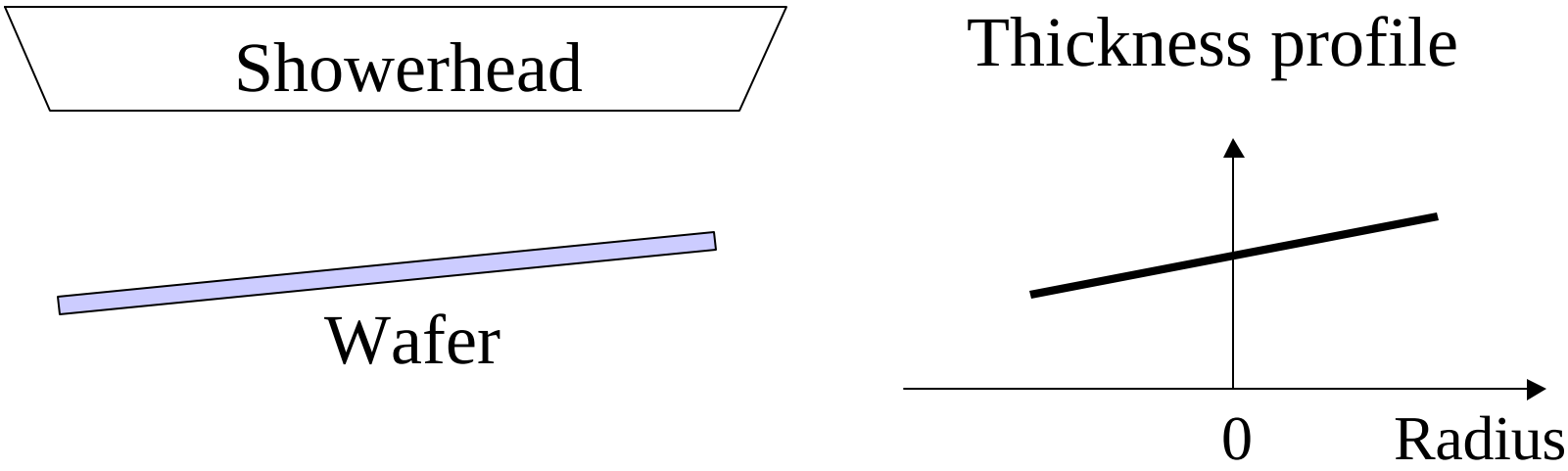
Normal spacing
Normal dep. rate
Normal profile

Larger spacing
Lower dep. rate
Center thick profile

Troubleshooting: Non-uniformity

- If the non-uniformity is side-to-side
- Check wafer leveling or centering
- Leak check of slip valve of the chamber

Leveling and Side-to-side Profile



Future Trends

- HDP-CVD USG for STI
- Nitride or O_3-TEOS oxide for sidewall spacer
- PECVD or RPCVD for PMD barrier nitride
- HDP-CVD PSG for PMD
- CMP for planarization
- Low-κ dielectric for IMD
- Silicon oxide/nitride as passivation dielectric

Future Trends

- High-κ gate dielectric
- Possible candidates: TiO_2, Ta_2O_5, and HfO_2
- CVD and RTA

Future Trends: Low-κ Dielectrics

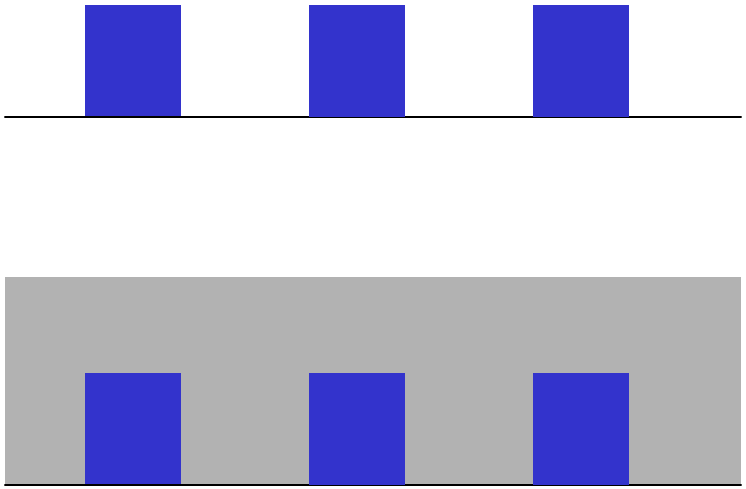
- Need to reduce *RC* time delay
  - low-κ reduces *C* and copper reduces *R*
- Require high thermal stability, high thermal conductivity, and process integration capability
  - CVD
    - CSG (C_xSi_yO, κ ~ 2.5 - 3.0) and α-CF (C_xF_y, κ ~ 2.5 – 2.7)
  - Spin-on dielectrics (SOD)
    - Hydrogen silsequioxane (HSQ, κ ~ 3.0),
    - Porous SOD such as xerogels (κ ~ 2.0 - 2.5)

Future Trends: Low-κ Dielectrics

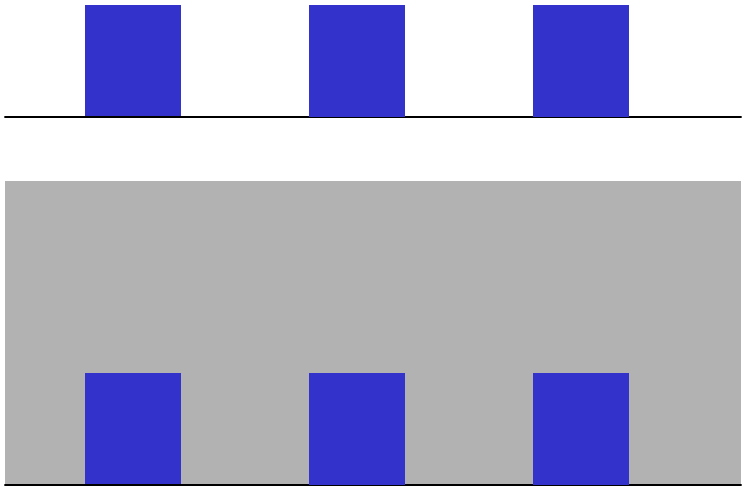
- Damascene process
- Copper metallization

- No gap fill, no planarization problem
- Main challenge: Integrate low-κ with copper metallization

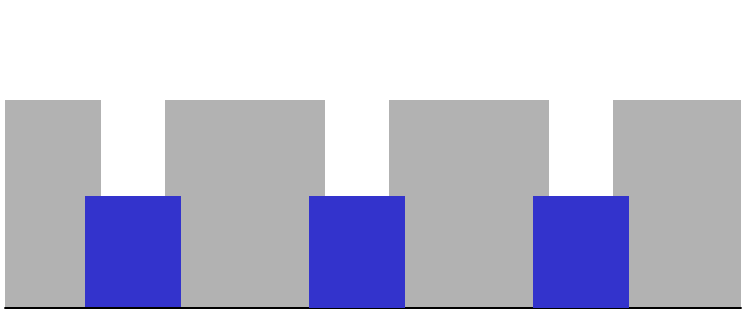
Interconnection Processes



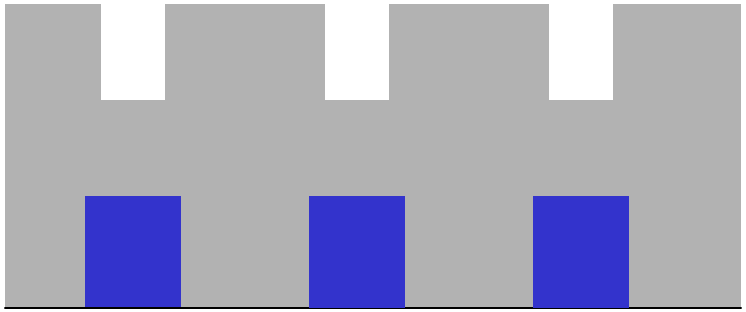
Dielectric deposition/planarization



Dielectric deposition/planarization

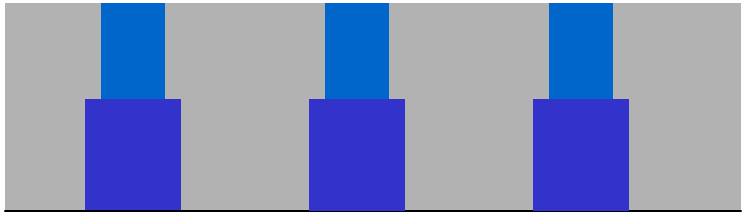


Via etch

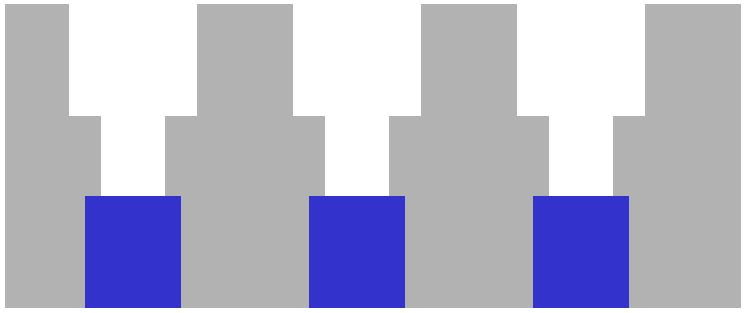


Via etch

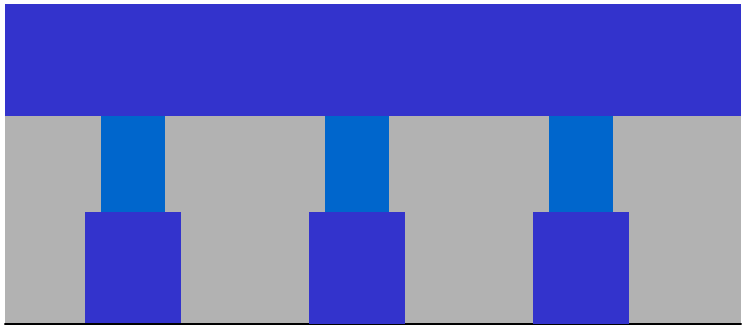
Interconnection Processes



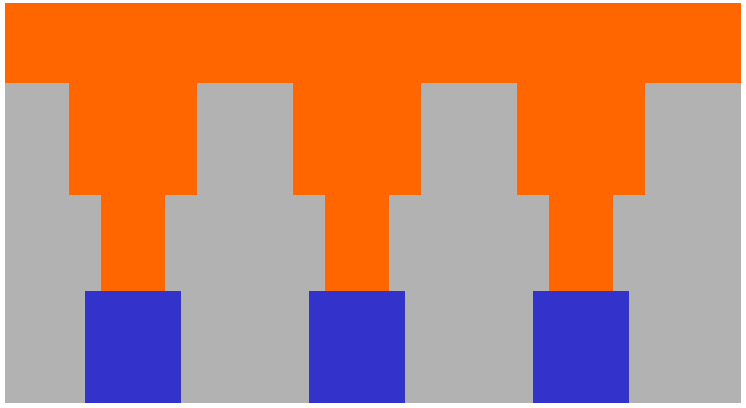
Via fill and polish



Trench etch

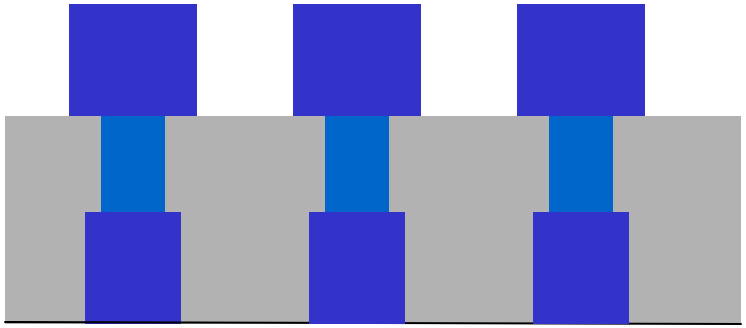


Metal deposition

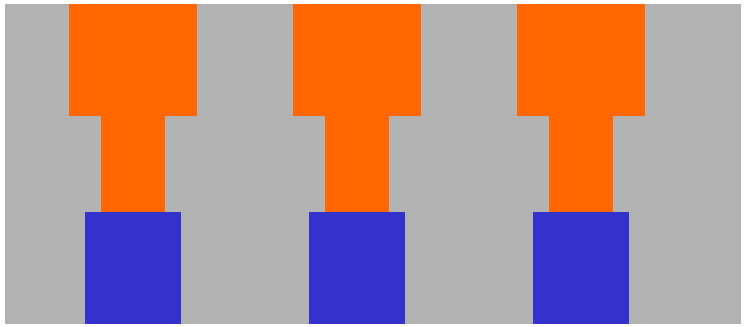


Metal deposition

Interconnection Processes



Metal etch



Metal polish

Summary

- Applications of dielectric thin film are STI, sidewall spacer, PMD, IMD and PD, in which IMD application is the dominant one

- Silicon oxide and silicon nitride are the two most commonly used dielectric materials

Summary

- Basic CVD process sequence: introducing precursor, precursor diffusion and adsorption, chemical reaction, gaseous byproducts desorption and diffusion
- Surface-reaction-limited regime
- Mass-transport-limited (MTL) regime
  - Most dielectric CVD reactors operate in MTL regime

Summary

- PMD uses PSG or BPSG, temperature are limited by thermal budget
- IMD mainly uses USG or FSG, temperature is limited by aluminum melting point
- PD usually uses both oxide and nitride

Summary

- Silane and TEOS are the two silicon sources for dielectric CVD processes
- O_2, N_2O, and O_3 are main oxygen precursors
- NH_3 and N_2 are the main nitrogen sources
- Fluorine chemistry is commonly used for dielectric CVD chamber dry clean
  - CF_4, C_2F_6, C_3F_8 and NF_3 are the most commonly used fluorine source gases

Summary

- Argon sputtering process is used for dep/etch/dep gap fill application
- CF_4/O_2 etchback is used for planarization
- Compressive stress (~100 MPa) is favored for the dielectric thin film

Summary

- HDP CVD
  - SiH_4 and O_2 to deposit oxide
  - Ar for sputtering
  - High aspect ratio gap fill
  - ICP and ECR: most commonly used HDP sources
- Low-κ and copper for future interconnection
- High-κ dielectric for gate or DRAM capacitor