Chapter 10
CVD and Dielectric Thin Film
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Objectives

- Identify at least four CVD applications
- Describe CVD process sequence
- List the two deposition regimes and describe their relation to temperature
- List two dielectric thin films
- Name the two most commonly used silicon precursors for dielectric CVD
CVD Oxide vs. Grown Oxide

- **SiO$_2$**
  - Grown film
  - Bare silicon

- **SiO$_2$**
  - Deposited film

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## CVD Oxide vs. Grown Oxide

<table>
<thead>
<tr>
<th>Grow</th>
<th>CVD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxygen is from gas phase</td>
<td>Both oxygen and silicon are from gas phase</td>
</tr>
<tr>
<td>Silicon from substrate</td>
<td>Deposit on substrate surface</td>
</tr>
<tr>
<td>Oxide grow into silicon</td>
<td>Lower temperature</td>
</tr>
<tr>
<td>Higher quality</td>
<td>Higher growth rate</td>
</tr>
</tbody>
</table>
Dielectric Thin Film Applications

- Multi-level metal interconnection
- CVD and SOG plus CVD dielectrics
- Shallow trench isolation (STI)
- Sidewall spacer for salicide, LDD, and the source/drain diffusion buffer
- The passivation dielectric (PD)
- Dielectric ARC for feature size < 0.25 µm
Dielectric Thin Film Applications

• Inter layer dielectric, or ILD, include PMD and IMD

• Pre-metal dielectric: PMD
  – normally PSG or BPSG
  – Temperature limited by thermal budget

• Inter-metal dielectric: IMD
  – USG or FSG
  – Normally deposited around 400 °C
Figure 10.2
Dielectric Processes

An N-layer metal interconnection IC chip with STI, the minimum number of dielectric process is:

\[
\text{Dielectric layer} = 1 + 1 + 1 + (N-1) + 1 = N + 3
\]

STI spacer PMD IMD PD
CVD

• Chemical Vapor Deposition

• Chemical gases or vapors react on the surface of solid, produce solid byproduct on the surface in the form of thin film. Other byproducts are volatile and leave the surface.
## CVD Applications

<table>
<thead>
<tr>
<th>FILMS</th>
<th>PRECURSORS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Semiconductor</strong></td>
<td></td>
</tr>
<tr>
<td>Si (poly)</td>
<td>SiH₄ (silane)</td>
</tr>
<tr>
<td>Si (epi)</td>
<td>SiCl₂H₂ (DCS)</td>
</tr>
<tr>
<td></td>
<td>SiCl₃H (TCS)</td>
</tr>
<tr>
<td></td>
<td>SiCl₄ (Siltet)</td>
</tr>
<tr>
<td></td>
<td>LPCVD</td>
</tr>
<tr>
<td></td>
<td>SiH₄, O₂</td>
</tr>
<tr>
<td></td>
<td>SiO₂ (glass)</td>
</tr>
<tr>
<td></td>
<td>PECVD</td>
</tr>
<tr>
<td></td>
<td>SiH₄, N₂O</td>
</tr>
<tr>
<td></td>
<td>PECVD</td>
</tr>
<tr>
<td></td>
<td>Si(OC₂H₅)₄ (TEOS), O₂</td>
</tr>
<tr>
<td><strong>Dielectrics</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LPCVD</td>
</tr>
<tr>
<td></td>
<td>TEOS</td>
</tr>
<tr>
<td></td>
<td>APCVD &amp; SACVD™</td>
</tr>
<tr>
<td></td>
<td>TEOS, O₃ (ozone)</td>
</tr>
<tr>
<td>Oxynitride</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SiH₄, N₂O, N₂, NH₃</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PECVD</td>
</tr>
<tr>
<td></td>
<td>SiH₄, N₂, NH₃</td>
</tr>
<tr>
<td></td>
<td>LPCVD</td>
</tr>
<tr>
<td></td>
<td>SiH₄, N₂, NH₃</td>
</tr>
<tr>
<td></td>
<td>LPCVD</td>
</tr>
<tr>
<td></td>
<td>C₈H₂₂N₂Si (BTBAS)</td>
</tr>
<tr>
<td><strong>Conductors</strong></td>
<td></td>
</tr>
<tr>
<td>W (Tungsten)</td>
<td>WF₆ (Tungsten hexafluoride), SiH₄, H₂</td>
</tr>
<tr>
<td>WSi₂</td>
<td>WF₆ (Tungsten hexafluoride), SiH₄, H₂</td>
</tr>
<tr>
<td>TiN</td>
<td>Ti[N (CH₃)₂]₄ (TDMAT)</td>
</tr>
<tr>
<td>Ti</td>
<td>TiCl₄</td>
</tr>
<tr>
<td>Cu</td>
<td></td>
</tr>
</tbody>
</table>

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CVD

- Gas or vapor phase precursors are introduced into the reactor
- Precursors across the boundary layer and reach the surface
- Precursors adsorb on the substrate surface
- Adsorbed precursors migrate on the substrate surface
- Chemical reaction on the substrate surface
- Solid byproducts form nuclei on the substrate surface
- Nuclei grow into islands
- Islands merge into the continuous thin film
- Other gaseous byproducts desorb from the substrate surface
- Gaseous byproducts diffuse across the boundary layer
- Gaseous byproducts flow out of the reactor.
Figure 10.3

- Precursors
- Showerhead
- Forced convection region
- Boundary layer
- Pedestal
- Wafer
- Byproducts
- Reactants
Deposition Process

- Precursor arrives surface
- Migrate on the surface
- React on the surface
- Nucleation: Island formation
Deposition Process

Islands grow

Islands grow, cross-section

Islands merge

Continuous thin film
CVD Processes

• APCVD
• LPCVD
• PECVD
Atmospheric Pressure CVD

- CVD process taking place at atmospheric pressure
- APCVD process has been used to deposit silicon oxide and silicon nitride
- APCVD O$_3$-TEOS oxide process is widely used in the semiconductor industry, especially in STI and PMD applications
- Conveyor belt system with in-situ belt clean
APCVD Reactor

N₂  Process Gas  N₂

Wafers

Heater

Belt Clean Station  Exhaust  Conveyor Belt
Question

• A semiconductor manufacturer has its R&D lab on the coast near sea level and one of its manufacturing fabs on a high altitude plateau. It was found that the APCVD processes developed in the R&D lab couldn’t directly apply in that particular fab. Why?
Answer

• On a high-altitude plateau, the atmospheric pressure is significantly lower than at sea level. Because earlier APCVD reactor didn’t have a pressure-control system, a process that worked fine in the R&D lab at sea level might not work well in the high altitude fab because of pressure difference
LPCVD

• Longer MFP
• Good step coverage & uniformity
• Vertical loading of wafer
• Fewer particles and increased productivity
• Less dependence on gas flow
• Vertical and horizontal furnace
Horizontal Conduction-Convection-heated LPCVD

• Adaptation of horizontal tube furnace
  – Low pressure: from 0.25 to 2 Torr
  – Used mainly for polysilicon, silicon dioxide and silicon nitride films
  – Can process 200 wafers per batch
LPCVD System

- Loading Door
- Process Gas Inlet
- Temperature
- Distance
- Pressure Sensor
- Heating Coils
- Wafers
- Wafer Boat
- Center Zone
- Flat Zone
- To Pump
- Quartz Tube
PECVD

- Developed when silicon nitride replaced silicon dioxide for passivation layer.

- High deposition rate at relatively low temp.
- RF induces plasma field in deposition gas
- Stress control by RF
- Chamber plasma clean.
Plasma Enhanced CVD System

- Process gases
- Process chamber
- Wafer
- RF power
- Plasma
- By-products to the pump
- Heated plate

By-products to the pump
Step Coverage

• A measurement of the deposited film reproducing the slope of a step on the substrate surface
• One of the most important specifications
  – Sidewall step coverage
  – Bottom step coverage
  – Conformality
  – Overhang
Step Coverage and Conformity

Sidewall step coverage = \( \frac{b}{a} \)  
Bottom step coverage = \( \frac{d}{a} \)

Conformity = \( \frac{b}{c} \)  
Overhang = \( \frac{c - b}{b} \)

Aspect ratio = \( \frac{h}{w} \)
Factors Affect Step Coverage

- Arriving angle of precursor
- Surface mobility of adsorbed precursor
Arriving Angles

180°  270°  90°
Arriving Angle

- Corner A: 270°, corner C: 90°
- More precursors at corner A
- More deposition
- Form the overhang
- Overhang can cause voids or keyholes
Void Formation Process

Metal

Dielectric

Metal

Dielectric

Metal

Dielectric

Metal

Void

Dielectric
Control of Arriving Angle

- Changing pressure
- Tapering opening
Step Coverage, Pressure and Surface Mobility

- **APCVD**
  - No mobility

- **LPCVD**
  - No mobility

- High mobility
Arriving Angles, Contact Holes
Gap Fill

- Fill a gap without voids
- Voids: cause defect and reliability problems
- Deposition/Etchback/Deposition
  - Silane and PE-TEOS film
- Conformal deposition
  - $\text{O}_3$-TEOS and tungsten CVD
- High density plasma CVD
Gap Fill

• PMD: zero tolerance voids
  – Tungsten can be deposited into these voids
  – Causing shorts

• IMD: voids below metal may tolerable
  – reducing $\kappa$
  – process gas could come out later and cause reliability problem
Void in PMD

Top view

Before W CVD

Silicide

Void

Sidewall spacers

Contact

Silicide
Unwanted W Line Between Gates

Top view

Tungsten

After W CVD

Silicide

Sidewall spacers

W plug
Deposition/Etchback/Deposition

USG

Al·Cu

USG

Al·Cu

USG

Al·Cu

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Conformal Deposition Gap Fill
Conformal Deposition Gap Fill
Conformal Deposition Gap Fill
HDP CVD Gap Fill
Surface Adsorption

- Determine precursors surface mobility
- Affect step coverage and gap fill

- Physical adsorption (physisorption)
- Chemical adsorption (chemisorption)
Chemisorption

- Actual chemical bonds between surface atom and the adsorbed precursor molecule
- Bonding energy usually exceeding 2 eV
- Low surface mobility
- Ion bombardment with 10 to 20 eV energy in PECVD processes can cause some surface migration of chemisorbed precursors
Physisorption

- Weak bond between surface and precursor
- Bonding energy usually less than 0.5 eV
  - Hydrogen bonding
  - Van der Waals forces
- Ion bombardment and thermal energy at 400 °C can cause migration of physisorbed precursors
- High surface mobility
Adsorptions

Distance from surface

Bonding energy

Chemisorbed precursor

Physisorbed precursor

Substrate Surface

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Dielectric CVD Precursors

- Silane ($\text{SiH}_4$)
- TEOS (tetra-ethyl-oxy-silane, $\text{Si(OC}_2\text{H}_5)_4$)
CVD Precursor: Silane

• Dielectric CVD
  – PECVD passivation dielectric depositions
  – PMD barrier nitride layer
  – Dielectric anti reflective coating (DARC)
  – High density plasma CVD oxide processes

• LPCVD poly-Si and silicon nitride

• Metal CVD
  – W CVD process for nucleation step
  – Silicon source for WSi$_x$ deposition
Dielectric CVD Precursor: Silane

- Pyrophoric (ignite itself), explosive, and toxic
- Open silane line without thoroughly purging can cause fire or minor explosion and dust line
Structure of Silane Molecule

![Structure of Silane Molecule](image-url)
CVD Precursor Adsorption: Silane

- Silane molecule is perfectly symmetrical
- Neither chemisorb nor physisorb
- Fragments of silane, SiH$_3$, SiH$_2$, or SiH, can easily form chemical bonds with surface
- Low surface mobility, overhangs and poor step coverage
CVD Precursor Adsorption: TEOS

- TEOS (tetra-ethyl-oxy-silane, Si(OC₂H₅)₄)
- Big organic molecule
- TEOS molecule is not perfectly symmetric
- Can form hydrogen bond and physisorb
- High surface mobility
- Good step coverage, conformality, and gap fill
- Widely used for oxide deposition
TEOS Molecule
TEOS Applications

- STI, sidewall spacer, PMD, and IMD
- Most dielectric CVD processes are TEOS based oxide processes
TEOS Vapor Pressure

Vapor Pressure (Torr)

Temperature (°C)

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TEOS Delivery

• A liquid at room temperature with boiling point at the sea level is 168 °C
  – As a reference, boiling point of water (H₂O) at sea level is 100 °C
• Need delivery system to send its vapor to process chamber
• Boiler, bubbler, and injection systems
Boiler System

Heated gas line

MFC

Process chamber

Heated foreline

Pump

TEOS

Thermostatic oven
Bubbler System

Carrier gas → MFC → MFM → Process chamber

Liquid TEOS

Thermostatic oven

Heated gas line

Carrier gas bubbles

Pump
Injection System

Pressurize gas

LFC

MFC

Injection valve

Process chamber

Liquid TEOS

Heated gas line, TEOS vapor and carrier gas

Carrier gas

Pump

Liquid TEOS flow

Injection System
Sticking Coefficient

- The probability that precursor atom forms chemical bond with surface atom in one collision
- Can be calculated by comparing the calculated deposition rate with 100% sticking coefficient and the measured actual deposition rate
## Sticking Coefficient

<table>
<thead>
<tr>
<th>Precursors</th>
<th>Sticking Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiH(_4)</td>
<td>(3 \times 10^{-4}) to (3 \times 10^{-5})</td>
</tr>
<tr>
<td>SiH(_3)</td>
<td>0.04 to 0.08</td>
</tr>
<tr>
<td>SiH(_2)</td>
<td>0.15</td>
</tr>
<tr>
<td>SiH</td>
<td>0.94</td>
</tr>
<tr>
<td>TEOS</td>
<td>(10^3)</td>
</tr>
<tr>
<td>WF(_6)</td>
<td>(10^{-4})</td>
</tr>
</tbody>
</table>
Step Coverage of TEOS and Silane Oxide

TEOS

Silane
Question

• Why don’t people apply TEOS as the silicon source gas for the silicon nitride deposition to get better step coverage for the nitride film
Answer

• In the TEOS molecule, the silicon atom is bonded with four oxygen atoms. It is almost impossible to strip all oxygen atoms and have silicon bonded only with nitrogen. Therefore, TEOS is mainly used for the oxide deposition and the nitride deposition normally uses silane as the silicon source gas.
Chemical Reaction Rate

\[ C.R. = A \exp \left(-\frac{E_a}{kT}\right) \]
Deposition Regimes

- Mass-transport-limited regime
- Surface-reaction-limited regime
- Gas-phase-nucleation regime

\[ \text{Slope} = \frac{-E_a}{k} \]
Surface-Reaction-Limited Regime

• Chemical reaction rate can’t match precursor diffusion and adsorption rates; precursors pile up on the substrate surface and wait their turn to react.

\[ D.R. = C.R. \ [B] [C] \ [\] \ldots \]

• Deposition rate is very sensitive to temperature
Mass-Transport-Limited Regime

- When the surface chemical reaction rate is high enough, the chemical precursors react immediately when they adsorb on the substrate surface.
- \( \text{Deposition rate} = D \frac{dn}{dx} [B] [C] [\ldots] \)
- Deposition rate is insensitive to temperature
- Mainly controlled by gas flow rates
Deposition Rate Regimes

Deposition rate

Dep. rate sensitive to temperature

Dep. rate insensitive to temperature

Temperature
CVD Reactor Deposition Regime

• Most single wafer process reactors are designed in mass-transport-limited regime
• It is easier to control the gas flow rate
• Plasma or unstable chemicals such as ozone are used to achieve mass-transport-limited-regime at relatively low temperature
Applications of Dielectric Thin film

- Shallow trench isolation (STI, USG)
- Sidewall Spacer (USG)
- Pre-metal dielectric (PMD, PSG or BPSG)
- Inter-metal dielectric (IMD, USG or FSG)
- Anti-reflection coating (ARC, SiON)
- Passivation dielectric (PD, Oxide/Nitride)
## Dielectric CVD, Oxide and Nitride

<table>
<thead>
<tr>
<th>Oxide (SiO$_2$)</th>
<th>Nitride (Si$_3$N$_4$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Similar dielectric strength, &gt; 1×10$^7$ V/cm</td>
<td>Similar dielectric strength, &gt; 1×10$^7$ V/cm</td>
</tr>
<tr>
<td>Lower dielectric constant, $\kappa = 3.9$</td>
<td>Higher dielectric constant, $\kappa = 7.0$</td>
</tr>
<tr>
<td>Not a good barrier for moisture and mobile ion (Na$^+$)</td>
<td>Good barrier for moisture and mobile ion (Na$^+$)</td>
</tr>
<tr>
<td>Transparent to UV</td>
<td>Conventional nitride opaque to UV</td>
</tr>
<tr>
<td>Can be doped with P and B</td>
<td></td>
</tr>
</tbody>
</table>
Shallow Trench Isolation (STI)

Grow pad oxide
Deposition nitride

Etch nitride, oxide and silicon

Grow barrier oxide
CVD USG trench fill

CMP USG
Anneal USG

Strip nitride and oxide

Si

USG

Si
Shallow Trench Isolation (STI)
Sidewall Spacer Formation

- Lightly doped drain (LDD)
- Self aligned silicide (Salicide)
PMD

• Doped oxide
• PSG or BPSG
• Phosphorus: gettering sodium and reduce flow temperature.
• Boron: further reduces flow temperature without excessive phosphorus
Sodium Ion Turn-on the MOSFET

Normal off

Turn on by Na⁺
PMD

- More phosphorus, lower reflow temperature
- >7wt% phosphorus, hygroscopic

\[ \text{P}_2\text{O}_5 + 3\text{H}_2\text{O} \rightarrow 2\text{H}_3\text{PO}_4 \]

- \(\text{H}_3\text{PO}_4\) etches aluminum causes metal corrosion
- Too much boron will cause crystallization of boric acid. \(\text{H}_3\text{BO}_3\).
- Limit, \(\text{P}\% + \text{B}\% < 10\%\)
Question

• Silicon nitride is a better sodium barrier layer than silicon oxide. Why don’t people just use nitride for PMD layer?
Answer

• Silicon nitride has higher dielectric constant
• Using nitride can cause longer $RC$ time delay and reduce circuit speed
• A thin layer of nitride (~ 200 Å) is commonly used as a diffusion barrier layer in the PMD application
• Prevent diffusion of phosphorus and boron from BPSG diffusing into source/drain
PSG Reflow at 1100 °C, N₂, 20 min.

Source: VLSI Technology, by S.M. Sze
Some Facts about Sodium

<table>
<thead>
<tr>
<th>Name</th>
<th>Sodium</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
<td>Na</td>
</tr>
<tr>
<td>Atomic number</td>
<td>11</td>
</tr>
<tr>
<td>Atomic weight</td>
<td>22.989770</td>
</tr>
<tr>
<td>Discoverer</td>
<td>Sir Humphrey Davy</td>
</tr>
<tr>
<td>Discovered at</td>
<td>England</td>
</tr>
<tr>
<td>Discovery date</td>
<td>1807</td>
</tr>
<tr>
<td>Origin of name</td>
<td>From the English word &quot;soda&quot; (the origin of the symbol Na comes from the Latin word &quot;natrium&quot;)</td>
</tr>
<tr>
<td>Density of solid</td>
<td>0.968 g/cm³</td>
</tr>
<tr>
<td>Molar volume</td>
<td>23.78 cm³</td>
</tr>
<tr>
<td>Velocity of sound</td>
<td>3200 m/sec</td>
</tr>
<tr>
<td>Electrical resistivity</td>
<td>4.7 μΩ·cm</td>
</tr>
<tr>
<td>Reflectivity</td>
<td>No data</td>
</tr>
<tr>
<td>Melting point</td>
<td>97.72 °C</td>
</tr>
<tr>
<td>Boiling point</td>
<td>882.85 °C</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>140 W m⁻¹K⁻¹</td>
</tr>
<tr>
<td>Coefficient of linear thermal expansion</td>
<td>$71\times10^{-6}$ K⁻¹</td>
</tr>
<tr>
<td>Applications</td>
<td>Major contaminant, needs to be strictly controlled</td>
</tr>
<tr>
<td>Main removal agent</td>
<td>HCl</td>
</tr>
<tr>
<td>Barrier materials used</td>
<td>Silicon nitride and PSG</td>
</tr>
</tbody>
</table>
4×4 BPSG Reflow at 850 °C, 30 Minutes in N\textsubscript{2} Ambient
# Development of PMD Processes

<table>
<thead>
<tr>
<th>Dimension</th>
<th>PMD</th>
<th>Planarization</th>
<th>Reflow temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt; 2 µm</td>
<td>PSG</td>
<td>Reflow</td>
<td>1100°C</td>
</tr>
<tr>
<td>2 - 0.35 µm</td>
<td>BPSG</td>
<td>Reflow</td>
<td>850 - 900°C</td>
</tr>
<tr>
<td>0.25 µm</td>
<td>BPSG</td>
<td>Reflow + CMP</td>
<td>750°C</td>
</tr>
<tr>
<td>0.18 µm</td>
<td>PSG</td>
<td>CMP</td>
<td>-</td>
</tr>
</tbody>
</table>
PMD Applications Roadmap

Feature Size (µm) 0.8 0.5 0.35 0.25 0.18
Wafer Size (mm) 150 200 300

- **O₃-TEOS BPSG**
  - Thermal Flow or RTP/CMP

- **APCVD Silane BPSG**
- **PE-TEOS BPSG**
- **LPCVD BPSG**
- **Thermal Flow**

- **O₃-TEOS PSG + PE-PSG**
  - CMP

- **HDP PSG + PE-PSG**
  - CMP

- **Low-k Dielectric**
  - CMP
IMD

- Inter-metal dielectric
- Undoped silicate glass (USG) or FSG
- SOG
- Gap fill and planarization
- Temperature limited by metal melting
  - Normally 400 °C
- PE-TEOS, O$_3$-TEOS, and HDP
TEOS

- Tetraethylorthosilicate, Si(OC₂H₅)₄
- Liquid silicon source
- Commonly used for SiO₂ deposition
- Good step coverage and gap fill
PE-TEOS

- Plasma-enhanced TEOS CVD processes
- TEOS and O\textsubscript{2}
- Most commonly used dielectric CVD process
- Deposit USG at \(\sim 400 \) °C
- Mainly for IMD
Spin-on Glass (SOG) Processes
PE-TEOS

- PE-TEOS
- Sputtering etchback
- PE-TEOS

Photo courtesy: Applied Materials
O$_3$-TEOS

• TEOS and Ozone

• O$_3$ $\rightarrow$ O$_2$ + O (half-life time: 86 hours at 22 °C, < 1ms at 400 °C)

• O + TEOS $\rightarrow$ USG + other volatile byproducts

• Excellent step coverage and gap fill.
• Applied for IMD and PMD
O$_3$-TEOS vs PE-TEOS

**PE-TEOS**

- Step coverage: 50%
- Conformality: 87.5%

**Ozone-TEOS**

- Step coverage: 90%
- Conformality: 100%
High Density Plasma CVD

• HDP-CVD: deposition and sputtering etch at the same time.
• USG for STI application
• USG and FSG for IMD applications
• PMD for PMD application
HDP-CVD, IMD Application
Oxide CMP
Passivation

- Nitride and oxide
- Nitride is very good barrier layer, oxide help nitride stick with metal
- Silane process
- \( \text{NH}_3, \ N_2 \) and nitrogen precursors, \( N_2O \) as oxygen precursor
- In-situ CVD process
Dielectric Thin Film Characteristics

• Refractive index
• Thickness
• Uniformity
• Stress
• Particles
Refractive Index

Refractive index, $n = \frac{\text{Speed of light in vacuum}}{\text{Speed of light in the film}}$
Refractive Index

Incident light

Vacuum

$\theta_1$

$\sin \theta_1 = \frac{n_2}{n_1} \sin \theta_2$

Film

$\theta_2$

Refractive light
Film Information from R.I.

- Oxygen rich
- Nitrogen rich
- Polysilicon

- Oxygen rich
- Nitrogen rich
- Si$_3$N$_4$

- Oxygen rich
- Nitrogen rich
- SiO$_2$

- Oxygen rich
- Nitrogen rich
- Oxynitride

- Oxygen rich
- Silicon rich

- Oxygen rich
- Silicon rich
Ellipsometry R.I. Measurement

Linearly Polarized Incident Light

Elliptically Polarized Reflected Light

n₁, k₁, t₁

n₂, k₂
Illustration of Prism Coupler

Laser light

Thin film

Substrate

Coupling head

Photo detector

$\theta$
Reflected Light Intensity vs. Incidence Angle

Reflected

Modes

20° 10° 0° -10° -20°
Metricon Model 2010 Prism Coupler
Comparison of the Two Methods

Ellipsometry

• Need know rough film thickness before hand
• Can measure thickness if R.I. is know

Prism coupler

• Need certain thickness of the film, > 3000 Å
• Can measure thickness if film thick enough to support enough modes
Thickness Measurement

• One of the most important measurements for dielectric thin film processes.

• Determines
  – Film deposition rate
  – Wet etch rate
  – Shrinkage
Dielectric Thin Film Thickness Measurement

Incident light

1

2

Human eye or photodetector

Dielectric film, $n(\lambda)$

Substrate

$t$
Dielectric Thin Film Thickness Measurement

- Different thickness has different color
- Tilting wafer also changes the color
Question

• If you see some beautiful color rings on a wafer with a CVD dielectric layer, what is your conclusion?
Answer

• Color change indicates the dielectric thin film thickness change, thus we know the film with the color rings must have problem with thickness uniformity, which is most likely caused by a non-uniform thin film deposition process.
Question

• Why does the thin film color change when one look at the wafer from different angle?
Answer

• When one looking at wafer from a different angle, phase shift will change, thus wavelength for constructive interference will change, which causes color change

• It is important to hold the wafer straight when using the color chart to measure film thickness

• Tilt wafer makes the film thickness thicker than it actually is
Spectroreflectometry

• Measure the reflected light intensity at different wavelengths
• Calculate thin film thickness from the relationship between reflected light intensity and wavelength.
• Photodetector is more sensitive than human eyes
• Spectroreflectometry can obtain much higher resolution and accuracy for the film thickness
Relation of Reflectance and Wavelength

\[ \frac{1}{\lambda_m} - \frac{1}{\lambda_{m+k}} = \frac{1}{2nt} \]
Spectroreflectometry System

- UV lamp
- Detectors
- Film
- Substrate
Question

- Many advance thin film thickness measurement tools allows user to choose the refractive index of the film. If someone mistakenly chooses the PE-TEOS USG film refractive index to measure $O_3$-TEOS USG films thickness, what will be the effect on the measurement result?
Answer

• Since the nt always coupled together
• A wrong n will cause wrong t measurement
• O$_3$-TEOS USG is a porous film and has a R.I., about 1.44
• Slightly lower than 1.46 of PE-TEOS USG
• Measured O$_3$-TEOS film thickness will be slightly thinner than its actual value
Deposition Rate

Deposition Rate = \frac{\text{Thickness of deposited film}}{\text{Deposition time}}
Wet Etch Rate

\[
\text{Wet Etch Rate} = \frac{\text{Thickness change after etch}}{\text{Etch time}}
\]

\[
\text{Wet etch rate ratio} = \frac{\text{Thickness change of the CVD film}}{\text{Thickness change of the thermal oxide film}}
\]
Uniformity

- Multi-point measurement
- Definition
- Average: \( \bar{x} = \frac{x_1 + x_2 + x_3 + \cdots + x_N}{N} \)
- Standard deviation:

\[
\sigma = \sqrt{\frac{(x_1 - \bar{x})^2 + (x_2 - \bar{x})^2 + (x_3 - \bar{x})^2 + \cdots + (x_N - \bar{x})^2}{N - 1}}
\]

- Standard deviation non-uniformity: \( \sigma/\bar{x} \)

Hong Xiao, Ph. D.  
www2.austin.cc.tx.us/HongXiao/Book.htm
Stress

• Mismatch between different materials
• Two kinds of stresses, intrinsic and extrinsic
• Intrinsic stress develops during the film nucleation and growth process.
• The extrinsic stress results from differences in the coefficients of thermal expansion
• Tensile stress: cracking film if too high
• Compressive stress: hillock if too strong
Film Stress

Bare Wafer                      After Thin Film Deposition

Substrate                       Substrate

Compressive Stress
Negative curvature

Tensile Stress
Positive curvature
Illustration of Thermal Stress

At 400 °C

SiO₂

Si

L

At Room Temperature

ΔL = α ΔT L
Coefficients of Thermal Expansion

\[ \alpha(\text{SiO}_2) = 0.5 \times 10^{-6} \, ^\circ\text{C}^{-1} \]
\[ \alpha(\text{Si}) = 2.5 \times 10^{-6} \, ^\circ\text{C}^{-1} \]
\[ \alpha(\text{Si}_3\text{N}_4) = 2.8 \times 10^{-6} \, ^\circ\text{C}^{-1} \]
\[ \alpha(\text{W}) = 4.5 \times 10^{-6} \, ^\circ\text{C}^{-1} \]
\[ \alpha(\text{Al}) = 23.2 \times 10^{-6} \, ^\circ\text{C}^{-1} \]
Stress Measurement

\[ \sigma = \frac{E}{1-\nu} \frac{h^2}{6t} \left( \frac{1}{R_2} - \frac{1}{R_1} \right) \]

Wafer curvature change before and after thin film deposition

Laser beam scans wafer surface, reflection light indicates the wafer curvature
Stress Measurement

Diagram showing a laser, mirror, and detector setup for stress measurement.
Dielectric CVD Processes

• Thermal Silane CVD Process
• Thermal TEOS CVD Process
• PECVD Silane Processes
• PECVD TEOS Processes
• Dielectric Etchback Processes
• $\text{O}_3$-TEOS Processes
• Spin-on Glass
• High Density Plasma CVD
Thermal Silane CVD Process

• Silane has been commonly used for silicon dioxide deposition with both APCVD and LPCVD process

\[
\text{heat} \\
\text{SiH}_4 + 2 \text{O}_2 \rightarrow \text{SiO}_2 + 2 \text{H}_2\text{O}
\]

• APCVD normally uses diluted silane (3% in nitrogen) and LPCVD uses pure silane

• Not commonly used in the advanced fab
Thermal TEOS CVD Process

- TEOS: physisorption, high surface mobility
- TEOS film has better step coverage
- LPCVD TEOS dissociates at high temp: $700 \, ^\circ C$
  \[ \text{Si(OC2H5)}_4 \rightarrow \text{SiO}_2 + \text{volatile organics} \]
- BPSG with TMB and TMP for PMD
- Temperature is too high for IMD
PECVD Silane Processes

- Silane and N\textsubscript{2}O (laughing gas)
- Dissociation in plasma form SiH\textsubscript{2} and O
- Radicals react rapidly to form silicon oxide

\[
\text{plasma} \\
\text{SiH}_4 + \text{N}_2\text{O} \rightarrow \text{SiO}_x\text{H}_y + \text{H}_2\text{O} + \text{N}_2 + \text{NH}_3 + \ldots
\]

heat

- Overflow N\textsubscript{2}O, using SiH\textsubscript{4} flow to control deposition rate
Question

- Can we overflow silane and use nitrous oxide flow rate to controlled deposition rate?
Answer

• Theoretically we can, but practically no one should even try this
• It is very dangerous and not cost effective
• Overflowing silane will create a big safety hazard: fire and explosion
• Silane is more expensive than nitrous oxide
Passivation: Silicon Nitride

- Barrier layer for moisture and mobile ions
- The PECVD nitride
  - Low deposition temperature (<450°C)
  - High deposition rate
  - Silane, ammonia, and nitrogen plasma
    
    \[ \text{SiH}_4 + \text{N}_2 + \text{NH}_3 \rightarrow \text{SiN}_x\text{H}_y + \text{H}_2 + \text{N}_2 + \text{NH}_3 + \ldots \]  
    
  heat
- Requires good step coverage, high dep. rate, good uniformity, and stress control
Passivation Dielectric Deposition

- Stabilization 1 (stabilize pressure)
- Oxide deposition (stress buffer for nitride)
- Pump
- Stabilization 2 (stabilize pressure)
- Nitride deposition (passivation layer)
- Plasma purging (eliminate SiH$_4$)
- Pump
EPROM Passivation Dielectric

- Need UV transparent passivation layer
- UV light can erase EPROM memory
- Oxynitride ($\text{SiO}_x\text{N}_y$) is commonly used
- Source gases: $\text{SiH}_4$, $\text{N}_2$, $\text{NH}_3$, and $\text{N}_2\text{O}$

\[ \text{SiH}_4 + \text{N}_2 + \text{NH}_3 + \text{N}_2\text{O} \rightarrow \text{SiO}_x\text{N}_y + \text{H}_2\text{O} + \text{N}_2 + \ldots \]

- Properties in between oxide and nitride
  - UV transparent, and a fairly good barrier layer
PMD Barrier Layer

• PSG or BPSG need a diffusion barrier layer
  – USG (need 1000 Å)
  – LPCVD nitride at ~700 °C (~ 300 Å)
  – PECVD nitride at <550 °C (< 200 Å)

• At higher temperature, PECVD nitride film has higher deposition rate, lower hydrogen concentration, and better film quality

• Possible in future: remote plasma CVD
Dielectric Anti-Reflective Coating

• High resolution for photolithography
• ARC layer is required to reduce the reflection
• Metallic ARC: TiN, 30% to 40% reflection
• No longer good enough for < 0.25 μm
• Dielectric ARC layer is used
  – Spin-on before photoresist coating
  – CVD
Dielectric Anti-Reflective Coating

\[ \Delta \phi = 2nt = \frac{\lambda}{2} \]

UV light (\(\lambda\))

1. Photoresist

2. Dielectric ARC, \(n, k\)

3. Aluminum alloy

\(t\)
Dielectric ARC

• PECVD silane process
• N$_2$O as oxygen and nitrogen source

\[
\text{plasma} \quad \text{SiH}_4 + \text{N}_2\text{O} + \text{He} \quad \rightarrow \quad \text{SiO}_x\text{N}_y + \text{H}_2\text{O} + \text{N}_2 + \text{NH}_3 + \text{He} + \cdots
\]

\[
\text{heat}
\]
PE-TEOS

- Most widely used dielectric CVD process
- Fast
- Good uniformity
- Good step coverage
- Mainly used for IMD
PE-TEOS

• USG process

Plasma

\[
\text{Si(OC}_2\text{H}_5)_4 + \text{O}_2 \rightarrow \text{SiO}_2 + \text{other volatiles}
\]

400 °C

• FGS process

plasma

\[
\text{FSi(OC}_2\text{H}_5)_3 + \text{Si(OC}_2\text{H}_5)_4 + \text{O}_2 \rightarrow \text{SiO}_x\text{F}_y + \text{other volatile}
\]

(FTES) (TEOS) heat (FSG)
FSG Process Trends

<table>
<thead>
<tr>
<th>SiO₂</th>
<th>SiOₓFᵧ (FSG)</th>
<th>SiF₄</th>
</tr>
</thead>
<tbody>
<tr>
<td>solid</td>
<td>solid</td>
<td>gas</td>
</tr>
</tbody>
</table>

κ = 3.9  
3.8 < κ < 3.2  
κ~ 1

higher \(k\)  
less F  
more F  
lower \(k\), F outgassing

Hong Xiao, Ph. D.  
www2.austin.cc.tx.us/HongXiao/Book.htm
Dielectric Etchback Processes

• Gap fill and planarization
• Performed in thin film bay with DCVD
• Cluster tool
• In-situ dep/etch/dep process
In-situ Dep/Etch/Dep Process

CVD chambers

A
B
C
D

Robot

Sputter etch chamber

Transfer chamber

Cassette handler

Dep.

Etch

Dep.

Metal
Sputtering Corner Chopping

\[ \text{Ar}^+ \quad \text{Ar}^+ \]
Question

• Why does sputtering etch process usually use argon as the process gas?
Answer

• It is inert, heavy, and relatively inexpensive
• The atomic weight of argon is 40, compared with silicon’s 28 and helium’s 4
• Argon is the third most abundant element in earth atmosphere (~ 1%) only after nitrogen (78%) and oxygen (20%)
• Can be purified directly from condensed air
Schematic of Sputtering Etch Chamber

- Process gases
- Process chamber
- Plasma
- Magnet coils
- Chuck
- RF power
- By-products to the pump
- By-products to the pump
Reactive Etch Back

• CF$_4$ and O$_2$
• Heavy bombardment with chemical reaction
• Applications
  – Planarize dielectric surface
  – SOG etch back
Reactive Etch Back Planarization

2 μm PE-TEOS oxide deposition

1 μm planarization etchback
O$_3$-TEOS Processes

• Ozone is a very unstable molecule,
  \[ \text{O}_3 \rightarrow \text{O}_2 + \text{O} \]
• At 400 °C, half-lifetime of O$_3$: < 1ms
• Used as carrier of free oxygen radicals
• Ozone reacts with TEOS form silicon oxide
• Excellent conformality and gap fill capability
• Sub-micron IC chip applications
• APCVD and SA-CVD
Ozone Generation

Lighting, corona discharge

\[ \text{plasma} \]

\[ O_2 \rightarrow O + O \]

\[ O + O_2 + M \rightarrow O_3 + M \ (M = O_2, N_2, \text{Ar}, \text{He}, \text{etc.}) \]
Illustration of Ozonator

\[ \text{O}_2 + \text{N}_2 \rightarrow \text{O}_2 + \text{O}_3 + \text{N}_2^+ + \text{N}_2\text{O} + \ldots \]
Ozone Concentration Monitoring

Monitored by UV absorption (Beer-Lambert law):

\[ I = I_0 \exp(-XCL) \]
O₃-TEOS USG Process

• TEOS + O₃ → SiO₂ + volatile organics

    heat

• Main applications
  – STI (higher temperature, ~ 550 °C)
  – IMD (~ 400 °C)
O$_3$-TEOS USG

Step coverage

Gap fill
O$_3$-TEOS BPSG and PSG Process

\[ \text{O}_3 \rightarrow \text{O}_2 + \text{O} \]

\[ \text{O} + \text{TEB} + \text{TEPO} + \text{TEOS} \rightarrow \text{BPSG} + \text{volatile organics} \]
heat

\[ \text{O} + \text{TEPO} + \text{TEOS} \rightarrow \text{PSG} + \text{volatile organics} \]
heat

• Main application
  – PMD
O$_3$-TEOS BPSG

SACVD BPSG for 0.25 µm gap and 4:1 A/R.
Spin-on Glass (SOG)

- Similar to PR coating and baking process
- People in fab like familiar technologies
- IMD gap fill and planarization
- Two kinds of spin-on glass:
  - Silicate
  - Siloxane
Spin-on Glass: Silicate and Siloxane

\[
\begin{align*}
\text{Si(OH)}_4 & \quad \text{Silicate} \\
\text{R} & \quad \text{R} = \text{CH}_3, \ R' = \text{R or OH}
\end{align*}
\]

\[
\begin{align*}
\text{R}_n\text{Si(OH)}_{4-n} & , \ n = 1, 2 \\
\text{Siloxane}
\end{align*}
\]
Spin-on Glass Process Steps

- PECVD USG barrier layer
- Spin-on glass
- SOG cure
- SOG etchback
- PECVD USG cap
High-Density Plasma CVD

• Dep/etch/dep gap fill needs two chambers
• Narrower gaps may need more dep/etch cycles to fill
• A tool can deposit and sputtering etch simultaneously would be greatly helpful
• The solution: HDP-CVD
Question

• With the feature size shrinking, metal line width and gap between metal lines becomes smaller. However the metal line height doesn't shrink accordingly, which causes larger gap aspect ratio.

• Why doesn’t shrink metal line height accordingly to keep the same aspect ratio and easier for dielectric gap fill?
Answer

• Metal line resistance $R = \rho \, l/wh$.
• If $h$ also reduces accordingly to $l$ and $w$, resistance will increase accordingly.
• Therefore, line has to keep the same height.
Inductively Coupled Plasma Chamber

- Source RF
- Inductive coils
- Ceramic cover
- Chamber body
- Plasma
- Wafer
- E-chuck
- Helium
- Bias RF
ECR Chamber

- **Microwave**
- **Plasma**
- **Magnet coils**
- **Magnetic field line**
- **Wafer**
- **E-chuck**
- **Bias RF**
- **Helium**
HDP-CVD, IMD Application

Metal Metal Metal
HDP-CVD, Deposition

Metal  Metal  Metal
HDP-CVD, Deposition
HDP-CVD, Deposition
PE-TEOS Deposition
Oxide CMP

Metal

Metal

Metal
HDP-CVD Processes

- For IMD Applications
  - USG: \[ \text{SiH}_4 + \text{O}_2 + \text{Ar} \rightarrow \text{USG} + \text{H}_2\text{O} + \text{Ar} + \ldots \]
  - FSG: \[ \text{SiH}_4 + \text{SiF}_4 + \text{O}_2 + \text{Ar} \rightarrow \text{FSG} + \text{volatiles} \]

- For PMD Applications
  - PSG: \[ \text{SiH}_4 + \text{PH}_3 + \text{O}_2 + \text{Ar} \rightarrow \text{PSG} + \text{volatiles} \]
Question

• Why is silane instead of TEOS used as the silicon source gas for the HDP CVD oxide process?
Answer

- For HDP CVD processes, step coverage is no longer an important factor for the gap fill.
- Heavy ion bombardment always keeps gap tapered and deposition is bottom up.
- Using silane can save the costs and hassles related with vapor delivery system of the liquid TEOS source.
Dielectric CVD Chamber Clean

• During dielectric CVD process, dielectric thin film will be deposited on everything inside chamber
• Need to routinely clean the chamber to prevent particulate contamination problems.
• For DCVD, more time for clean than dep.
• RF plasma clean and remote plasma clean
RF Plasma Clean

- Plasma clean process remove dielectric film on the process kits and chamber wall
- Fluorocarbon such as CF$_4$, C$_2$F$_6$ and C$_3$F$_8$
- In some case NF$_3$ is also used
- In plasma, fluorocarbon will be dissociated
- Free fluorine, F, will be generated
- F removes silicon oxide and silicon nitride
RF Clean Chemistry

plasma

\[
\text{CF}_4 \rightarrow \text{CF}_3 + \text{F}
\]

plasma

\[
\text{F} + \text{SiO}_2 \rightarrow \text{SiF}_4 + \text{O}
\]

heat

plasma

\[
\text{F} + \text{Si}_3\text{N}_4 \rightarrow \text{SiF}_4 + \text{N}
\]

heat
RF Clean Chemistry

• In plasma clean processes, oxygen source gases such as N$_2$O and O$_2$ are used with fluorocarbon to react with carbon and free more fluorine radicals
• Increase F/C ratio, keep it > 2
• Prevent carbon fluoride polymerization, and increases the clean efficiency
CF$_2$ and Reconnection
Polymerization, Teflon Deposition
RF Clean Endpoint

- Excitation-relaxation cause glow
- Different gases have different colors of light
- Information of chemical components in plasma
- Monitor line emission to control clean process
Endpoint Signal

Fluorine Peak (407 nm) Intensity

Clean Time (sec)

Endpoint
Remote Plasma Clean

• RF Plasma clean
  – Ion bombardment
  – Cause damage on chamber parts

• Remote plasma clean
  – No ion bombardment
  – More gentle on chamber parts
  – Longer part lifetime
  – Less “green house” gas emission
Illustration of Remote Plasma Clean

Microwave

Remote plasma chamber

NF$_3$ → Plasma → Remote plasma chamber

Process chamber

F F F N$_2$ F F N$_2$ F

N$_2$, SiF$_4$, O$_2$… To pump

Heated plate
Remote Plasma Clean

- Microwave (MW) power, NF₃ as fluorine source
- 99% of NF₃ dissociated in MW plasma
- Free fluorine reacts with the film in chamber
  - No plasma inside process chamber
  - No ion bombardment
  - Prolongs their lifetime

- Disadvantages:
  - Less maturity, higher cost, and using NF₃
  - Can not use optical endpoint system, may need FTIR system to achieve the automatic process endpoint.
Process Trends and Troubleshooting

• Process response to input parameters change
• Help to determine the root cause if some wrong
Silane PECVD Process Trends

• Increasing temperature increases deposition rate
  – Higher diffusion rate of precursors in boundary layer
• Increasing temperature improves deposited step coverage and film quality
• PMD uses a higher temperature
• IMD and PD, normally not exceed 400 °C
Deposition Rate and Temperature

![Graph showing deposition rate and temperature with a process window shaded.](#)
Stress and RF Power

Graph showing the relationship between compressive stress and RF power, with a shaded process window.
Silane PECVD Process Trends

Silane flow

Process window
Silane PECVD Process Trends

![Graph showing process window and silane flow trends]
Relationship of Deposition Rate and RF Power

Free radicals enhance reaction

Ion bombardment reduce adsorption

Deposition Rate

RF power
Relationship of Deposition Rate and Temperature

Deposition Rate

Deposition

Temperature

Dep. Rate sensitive to temperature

Dep. Rate insensitive to temperature
PE-TEOS Trends

• RF power $\uparrow$: dep rate $\uparrow\downarrow$, compressive stress $\uparrow$
  – In process window, dep rate go down
• Temperature $\uparrow$: dep rate $\uparrow\downarrow$
  – In process window, dep rare go down
• TEOS flow $\uparrow$: dep rate $\uparrow$, compressive stress $\downarrow$
PE-TEOS Trends: TEOS Flow Rate
PE-TEOS Trends: TEOS Flow Rate
PE-TEOS Trends: Temperature

Increasing chemical reaction rate

Reducing adsorption rate

Temperature

400 to 550 °C
O$_3$-TEOS Trends

- Temperature↑: dep rate↑↓
  - In process window, dep rate go down
- TEOS flow↑: dep rate↑
Question

- For both PE- and O$_3$- TEOS processes, the maximum deposition rate can be achieved at about 250 °C. Why do the IMD TEOS processes normally operate about 400 °C and PMD and STI processes deposited even higher temperature (~ 550 °C)?
Answer

- At higher deposition temperature, film quality is higher and step coverage is better
Troubleshooting

• Learned from hand-on experience
• Sudden process change, either suddenly goes wrong, or gradually goes wrong and suddenly comes back,
• Someone should check what has changed between good process and the bad process, or vice versa.
Troubleshooting

• Check metrology tool first and make sure the right recipe is used.
• If one measure PE-TEOS film with nitride recipe, measured thickness would be significantly thinner.
• If nothing is wrong with metrology tool, then check whether the process recipe has been changed.
Troubleshooting

• Process always has problems at end of shift
• Someone should work cross shifts to find out what had been changed during shift change
• Something must be changed that put the process back to normal at the beginning of the next shift
• It most likely is the source of problems as the process gradually goes wrong at end of the shift
Troubleshooting

- Most dielectric CVD processes operate in mass-transport-limited regime
- Deposition rate is mainly determined by gas flow rate, usually silane and TEOS flow rate
- Very likely that deposition rate problems are related with silane or TEOS flow rate
- Mass flow controller and liquid flow controller
Troubleshooting: Non-uniformity

- Uniformity is determined by flow pattern
- If non-uniformity pattern is center symmetric
  - Adjusted spacing of the wafer and showerhead
  - Or changing the carrier gas flow rate
    - Helium flow for TEOS processes
    - Nitrogen flow for nitride process
Spacing and Film Profile

Smaller spacing
Higher dep. rate
Center thin profile

Normal spacing
Normal dep. rate
Normal profile

Larger spacing
Lower dep. rate
Center thick profile
Troubleshooting: Non-uniformity

• If the non-uniformity is side-to-side
• Check wafer leveling or centering
• Leak check of slip valve of the chamber
Leveling and Side-to-side Profile

![Diagram showing leveling and side-to-side profile](image-url)
Future Trends

- HDP-CVD USG for STI
- Nitride or $O_3$-TEOS oxide for sidewall spacer
- PECVD or RPCVD for PMD barrier nitride
- HDP-CVD PSG for PMD
- CMP for planarization
- Low-$\kappa$ dielectric for IMD
- Silicon oxide/nitride as passivation dielectric
Future Trends

• High-κ gate dielectric
• Possible candidates: TiO$_2$, Ta$_2$O$_5$, and HfO$_2$
• CVD and RTA
Future Trends: Low-\(\kappa\) Dielectrics

• Need to reduce \(RC\) time delay
  – low-\(\kappa\) reduces \(C\) and copper reduces \(R\)
• Require high thermal stability, high thermal conductivity, and process integration capability
  – CVD
    • CSG \((C_xSi_yO, \kappa \sim 2.5 - 3.0)\) and \(\alpha\)-CF \((C_xF_y, \kappa \sim 2.5 - 2.7)\)
  – Spin-on dielectrics (SOD)
    • Hydrogen silsequioxane (HSQ, \(\kappa \sim 3.0\)),
    • Porous SOD such as xerogels \((\kappa \sim 2.0 - 2.5)\)
Future Trends: Low-\(\kappa\) Dielectrics

- Damascene process
- Copper metallization
- No gap fill, no planarization problem
- Main challenge: Integrate low-\(\kappa\) with copper metallization
Interconnection Processes

Dielectric deposition/planarization

Via etch

Dielectric deposition/planarization

Via etch
Interconnection Processes

Via fill and polish

Trench etch

Metal deposition

Metal deposition
Interconnection Processes

Metal etch

Metal polish
Summary

• Applications of dielectric thin film are STI, sidewall spacer, PMD, IMD and PD, in which IMD application is the dominant one.

• Silicon oxide and silicon nitride are the two most commonly used dielectric materials.
Summary

• Basic CVD process sequence: introducing precursor, precursor diffusion and adsorption, chemical reaction, gaseous byproducts desorption and diffusion

• Surface-reaction-limited regime

• Mass-transport-limited (MTL) regime
  – Most dielectric CVD reactors operate in MTL regime
Summary

• PMD uses PSG or BPSG, temperature are limited by thermal budget

• IMD mainly uses USG or FSG, temperature is limited by aluminum melting point

• PD usually uses both oxide and nitride
Summary

• Silane and TEOS are the two silicon sources for dielectric CVD processes
• O$_2$, N$_2$O, and O$_3$ are main oxygen precursors
• NH$_3$ and N$_2$ are the main nitrogen sources
• Fluorine chemistry is commonly used for dielectric CVD chamber dry clean
  – CF$_4$, C$_2$F$_6$, C$_3$F$_8$ and NF$_3$ are the most commonly used fluorine source gases
Summary

• Argon sputtering process is used for dep/etch/dep gap fill application
• CF$_4$/O$_2$ etchback is used for planarization
• Compressive stress (~100 MPa) is favored for the dielectric thin film
Summary

• HDP CVD
  – SiH$_4$ and O$_2$ to deposit oxide
  – Ar for sputtering
  – High aspect ratio gap fill
  – ICP and ECR: most commonly used HDP sources

• Low-κ and copper for future interconnection

• High-κ dielectric for gate or DRAM capacitor