Chapter 11
Metallization

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www2.austin.cc.tx.us/HongXiao/Book.htm
Objectives

- Explain device application of metallization
- List three most commonly used metals
- List three different metallization methods
- Describe the sputtering process
- Explain the purpose of high vacuum in metal deposition processes
Metallization

- Definition
- Applications
- PVD vs. CVD
- Methods
- Vacuum
- Metals
- Processes
- Future Trends
Metallization

• Processes that deposit metal thin film on wafer surface.
Applications

• Interconnection
• Gate and electrodes
• Micro-mirror
• Fuse
CMOS: Standard Metallization

- P-wafer
- N-Well
- P-Well
- STI
- n
- n+
- p
- p+
- Metal 1, Al•Cu
- Ti/TiN
- TiN, ARC
- TiSi₂
- BPSG
- W
- P-epi
- P-wafer
Applications: Interconnection
Applications: Interconnection

- Dominate the metallization processes
- Al-Cu alloy is most commonly used
- W plug, technology of 80s and 90s
- Ti, welding layer
- TiN, barrier, adhesion and ARC layers
- The future is --- Cu!
Copper Metallization

Ti/TiN  SiN  CoSi₂  Ta or TaN

M1  Cu  FSG  Cu  Cu

PSG  FSG

n⁺  W  p⁺  p⁺

STI  n⁺  USG  P-Well  N-Well

P-Epi  P-Wafer
Wafer Process Flow

Materials

Wafers

Masks

Design

IC Fab

Metalization

CMP

Dielectric deposition

Thermal Processes

Implant PR strip

Etch PR strip

Photo-lithography

Wafers Process Flow

Test

Packaging

Final Test
Applications: Gate and Electrode

- Al gate and electrode
- Polysilicon replace Al as gate material
- Silicide
  - WSi$_2$
  - TiSi$_2$
  - CoSi$_2$, MoSi$_2$, TaSi$_2$, ...
- Pt, Au, ... as electrode for DRAM capacitors
Q & A

• Can we reduce all dimensions of metal interconnection line at the same ratio?

• $R = \rho \frac{l}{wh}$. When we shrink all dimensions (length $l$, width $w$, and height $h$) accordingly to the shrinking of the device feature size, resistance $R$ increases,

• Slower circuit and more power consumption
Applications: Micro-mirror

- Digital projection display
- Aluminum-Titanium Alloy
- Small grain, high reflectivity
- “Home Theater”
Applications: Fuse

- For programmable read-only memory (PROM)
- High current generates heat which melt thin Al line and open the circuit
- Polysilicon also being used as fuse materials
Conducting Thin Films
Conducting Thin Films

- Polysilicon
- Silicides
- Aluminum alloy
- Titanium
- Titanium Nitride
- Tungsten
- Copper
- Tantalum
Polysilicon

- Gates and local interconnections
- Replaced aluminum since mid-1970s
- High temperature stability
  - Required for post implantation anneal process
  - Al gate can not use form self-aligned source/drain
- Heavily doped
- LPCVD in furnace
Silicide

- Much lower resistivity than polysilicon
- TiSi$_2$, WSi$_2$, and CoSi$_2$ are commonly used
Salicide

• TiSi$_2$ and CoSi$_2$
  – Argon sputtering removes the native oxide
  – Ti or Co deposition
  – Annealing process forms silicide
  – Ti or Co don’t react with SiO$_2$, silicide is formed at where silicon contacts with Ti or Co
  – Wet strips unreacted Ti or Co
  – Optional second anneal to increase conductivity
Self-aligned Titanium Silicide Formation

Titanium deposition

Silicide annealing

Titanium wet striping

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Tungsten Silicide

• Thermal CVD process
  – WF$_6$ as the tungsten precursor
  – SiH$_4$ as the silicon precursor.

• Polycide stack is etched
  – Fluorine chemistry etches WSi$_x$
  – Chlorine chemistry etches polysilicon

• Photoresist stripping

• RTA increases grain size and conductivity
Aluminum

• Most commonly used metal

• The fourth best conducting metal
  – Silver 1.6 $\mu\Omega\cdot$cm
  – Copper 1.7 $\mu\Omega\cdot$cm
  – Gold silver 2.2 $\mu\Omega\cdot$cm
  – Aluminum 2.65 $\mu\Omega\cdot$cm

• It was used for gate before mid-1970
Aluminum-Silicon Alloy

- Al make direct contact with Si at source/drain
- Si dissolves in Al and Al diffuses into Si
- Junction spike
  - Aluminum spikes punctuate doped junction
  - Short source/drain with the substrate
- ~1% of Si in Al saturates it
- Thermal anneal at 400 °C to form Si-Al alloy at the silicon-aluminum interface
Junction Spike

![Diagram of a junction spike with Al, SiO₂, and n-type silicon layers.](image-url)
Electromigration

- Aluminum is a polycrystalline material
- Many mono-crystalline grains
- Current flows through an aluminum line
- Electrons constantly bombards the grains
- Smaller grains will start to move
- This effect is called electromigration
Electromigration

• Electromigration tear the metal line apart
• Higher current density in the remaining line
  – Aggravates the electron bombardment
  – Causes further aluminum grain migration
  – Eventually will break of the metal line
• Affect the IC chip reliability
• Aluminum wires: fire hazard of old houses
Electromigration Prevention

• When a small percent of copper is alloyed with aluminum, electromigration resistance of aluminum significantly improved

• Copper serves as “glue” between the aluminum grains and prevent them from migrating due to the electron bombardment

• Al-Si-Cu alloy was used

• Al-Cu (0.5%) is very commonly
Aluminum Alloy Deposition

- PVD
  - Sputtering
  - Evaporation
    - Thermal
    - Electron beam
- CVD
  - Dimethylaluminum hydride [DMAH, Al(CH₃)₂H]
  - Thermal process
PVD vs. CVD

- CVD: Chemical reaction on the surface
- PVD: No chemical reaction on the surface

- CVD: Better step coverage (50% to ~100%) and gap fill capability
- PVD: Poor step coverage (~ 15%) and gap fill capability
PVD vs. CVD

• PVD: higher quality, purer deposited film, higher conductivity, easy to deposit alloys

• CVD: always has impurity in the film, lower conductivity, hard to deposit alloys
## Some Facts About Aluminum

<table>
<thead>
<tr>
<th>Name</th>
<th>Aluminum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
<td>Al</td>
</tr>
<tr>
<td>Atomic number</td>
<td>13</td>
</tr>
<tr>
<td>Atomic weight</td>
<td>26.981538</td>
</tr>
<tr>
<td>Discoverer</td>
<td>Hans Christian Oersted</td>
</tr>
<tr>
<td>Discovered at</td>
<td>Denmark</td>
</tr>
<tr>
<td>Discovery date</td>
<td>1825</td>
</tr>
<tr>
<td>Origin of name</td>
<td>From the Latin word &quot;alumen&quot; meaning &quot;alum&quot;</td>
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<td>Density of solid</td>
<td>2.70 g/cm$^3$</td>
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<tr>
<td>Molar volume</td>
<td>10.00 cm$^3$</td>
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<tr>
<td>Velocity of sound</td>
<td>5100 m/sec</td>
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<tr>
<td>Hardness</td>
<td>2.75</td>
</tr>
<tr>
<td>Electrical resistivity</td>
<td>2.65 $\mu$Ω cm</td>
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<tr>
<td>Reflectivity</td>
<td>71%</td>
</tr>
<tr>
<td>Melting point</td>
<td>660 °C</td>
</tr>
<tr>
<td>Boiling point</td>
<td>2519 °C</td>
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<tr>
<td>Thermal conductivity</td>
<td>235 W m$^{-1}$ K$^{-1}$</td>
</tr>
<tr>
<td>Coefficient of linear thermal expansion</td>
<td>23.1 $10^{-6}$ K$^{-1}$</td>
</tr>
<tr>
<td>Etchants (wet)</td>
<td>H$_3$PO$_4$, HNO$_4$, CH$_3$COOH</td>
</tr>
<tr>
<td>Etchants (dry)</td>
<td>Cl$_2$, BCl$_3$</td>
</tr>
<tr>
<td>CVD Precursor</td>
<td>Al(CH$_3$)$_2$H</td>
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</table>

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Titanium

• Applications
  – Silicide formation
  – Titanium nitridation
  – Wetting layer
  – Welding layer
Welding Layer

• Reduce contact resistance.
  – Titanium scavenges oxygen atoms
  – Prevent forming high resistivity $\text{WO}_4$ and $\text{Al}_2\text{O}_3$.

• Use with TiN as diffusion barrier layer
  – Prevent tungsten from diffusing into substrate
Applications of Titanium

\[ \text{Al-Cu} \quad \text{Ti} \quad \text{W} \quad \text{PSG} \quad \text{Ti} \]

\[ \text{TiSi}_2 \quad n^+ \]
# Some Face About Titanium

<table>
<thead>
<tr>
<th>Name</th>
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</tr>
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<tbody>
<tr>
<td>Symbol</td>
<td>Ti</td>
</tr>
<tr>
<td>Atomic number</td>
<td>22</td>
</tr>
<tr>
<td>Atomic weight</td>
<td>47.867</td>
</tr>
<tr>
<td>Discoverer</td>
<td>William Gregor</td>
</tr>
<tr>
<td>Discovered at</td>
<td>England</td>
</tr>
<tr>
<td>Discovery date</td>
<td>1791</td>
</tr>
<tr>
<td>Origin of name</td>
<td>Named after the &quot;Titans&quot;, (the sons of the Earth goddess in Greek mythology)</td>
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<tr>
<td>Density of solid</td>
<td>4.507 g/cm³</td>
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<tr>
<td>Molar volume</td>
<td>10.64 cm³</td>
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<td>Velocity of sound</td>
<td>4140 m/sec</td>
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<td>Hardness</td>
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<td>40 µΩ cm</td>
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<tr>
<td>Melting point</td>
<td>1668 °C</td>
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<td>Boiling point</td>
<td>3287 °C</td>
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<tr>
<td>Thermal conductivity</td>
<td>22 W m⁻¹ K⁻¹</td>
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<td>Coefficient of linear thermal expansion</td>
<td>8.6 10⁻⁶ K⁻¹</td>
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<td>Etchants (wet)</td>
<td>H₂O₂, H₂SO₄</td>
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<tr>
<td>Etchants (dry)</td>
<td>Cl₂, NF₃</td>
</tr>
<tr>
<td>CVD Precursor</td>
<td>TiCl₄</td>
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</table>

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Titanium Nitride

• Barrier layer
  – prevents tungsten diffusion

• Adhesion layer
  – help tungsten to stick on silicon oxide surface

• Anti-reflection coating (ARC)
  – reduce reflection and improve photolithography resolution in metal patterning process
  – prevent hillock and control electromigration

• Both PVD and CVD
Titanium Nitride PVD

• Barrier layer, adhesion layer and ARC
• Reactive sputtering a Ti target with Ar and N\textsubscript{2}
  – N\textsubscript{2} molecules dissociate in plasma
  – Nitrogen free radials (N)
  – N reacts with Ti and form TiN layer on Ti surface
  – Ar ions sputter TiN off and deposit them on the wafer surface
Titanium Nitride CVD

• Barrier layer and adhesion layer
• Better step coverage than PVD
• Metal organic process (MOCVD)
  – ~350 °C
  – TDMAT, Ti[N(CH₃)₂]₄
  – Via application
Titanium Nitridation

- Titanium PVD
- Nitridation of titanium surface with ammonia
- Rapid thermal process
Tungsten

- Metal plug in contact and via holes
- contact holes become smaller and narrower
- PVD Al alloy: bad step coverage and void
- CVD W: excellent step coverage and gap fill
- higher resistivity: 8.0 to 12 $\mu\Omega\cdot cm$ compare to PVD Al alloy (2.9 to 3.3 $\mu\Omega\cdot cm$)
- only used for local interconnections and plugs
Evolution of Contact Processes

Widely tapered contact hole, PVD metal fill

Narrow contact hole, void with PVD metal fill

Narrow contact hole, WCVD for tungsten plug

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Tungsten CVD

- WF$_6$ as the tungsten precursor
- React with SiH$_4$ to form nucleation layer
- React with H$_2$ for bulk tungsten deposition
- Needed a TiN layer to adhere on oxide
## Some Facts About Tungsten

<table>
<thead>
<tr>
<th>Name</th>
<th>Tungsten</th>
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<tr>
<td>Symbol</td>
<td>W</td>
</tr>
<tr>
<td>Atomic number</td>
<td>74</td>
</tr>
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<td>Atomic weight</td>
<td>183.84</td>
</tr>
<tr>
<td>Discoverer</td>
<td>Fausto and Juan Jose de Elhuyar</td>
</tr>
<tr>
<td>Discovered at</td>
<td>Spain</td>
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<td>1783</td>
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<tr>
<td>Origin of name</td>
<td>From the Swedish words &quot;tung sten&quot; meaning &quot;heavy stone&quot;. W comes from &quot;wolfram&quot;, named after the tungsten mineral wolframite.</td>
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<tr>
<td>Density of solid</td>
<td>19.25 g/cm³</td>
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<td>Molar volume</td>
<td>9.47 cm³</td>
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<td>Hardness</td>
<td>7.5</td>
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<td>Reflectivity</td>
<td>62%</td>
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<td>Electrical resistivity</td>
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<td>Etchants (wet)</td>
<td>KH₂PO₄, KOH, and K₃Fe(CN)₆; boiling H₂O</td>
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<td>Etchants (dry)</td>
<td>SF₆, NF₃, CF₄, etc.</td>
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<td>CVD Precursor</td>
<td>WF₆</td>
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W Plug and TiN/Ti Barrier/Adhesion Layer

- Tungsten
- TiN/Ti
- Oxide
Copper

- Low resistivity ($1.7 \ \mu \Omega \cdot \text{cm}$),
  - lower power consumption and higher IC speed
- High electromigration resistance
  - better reliability
- Poor adhesion with silicon dioxide
- Highly diffusive, heavy metal contamination
- Very hard to dry etch
  - copper-halogen have very low volatility
Copper Deposition

- PVD of seed layer
- ECP or CVD bulk layer
- Thermal anneal after bulk copper deposition
  - increase the grain size
  - improving conductivity
# Some Facts About Copper

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<td>Symbol</td>
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<td>29</td>
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<tr>
<td>Atomic weight</td>
<td>63.546</td>
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<tr>
<td>Discoverer</td>
<td>Copper had been used by human being since ancient time, long before any written history.</td>
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<td>Discovered at</td>
<td></td>
</tr>
<tr>
<td>Discovery date</td>
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<tr>
<td>Origin of name</td>
<td>From the Latin word &quot;cuprum&quot; meaning the island of &quot;Cyprus&quot;</td>
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<td>Density of solid</td>
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<td>Molar volume</td>
<td>7.11 cm$^3$</td>
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<td>Etchants (wet)</td>
<td>HNO$_4$, HCl, H$_2$SO$_4$</td>
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<tr>
<td>Etchants (dry)</td>
<td>Cl$_2$, needs low pressure and high temperature (hfac)Cu(tmvs)</td>
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Tantalum

• Barrier layer
• Prevent copper diffusion
• Sputtering deposition
### Some Facts About Tantalum

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<td>Ta</td>
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<td><strong>Atomic weight</strong></td>
<td>180.9479</td>
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<tr>
<td><strong>Discoverer</strong></td>
<td>Anders Ekeberg</td>
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<tr>
<td><strong>Discovered at</strong></td>
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<td><strong>Origin of name</strong></td>
<td>From the Greek word &quot;Tantalos&quot; meaning &quot;father of Niobe&quot; due it close relation to niobium in the Periodic Table</td>
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<td><strong>Molar volume</strong></td>
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<td><strong>Velocity of sound</strong></td>
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<td><strong>Hardness</strong></td>
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<td><strong>Thermal conductivity</strong></td>
<td>57.5 W m⁻¹ K⁻¹</td>
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<tr>
<td><strong>Coefficient of linear thermal expansion</strong></td>
<td>6.3×10⁻⁶ K⁻¹</td>
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</table>
Cobalt

• Mainly used for cobalt silicide (CoSi$_2$).
• Normally deposited with a sputtering process
Cobalt Silicide

- Titanium silicide grain size: ~ 0.2 µm
- Can’t be used for 0.18 mm gate
- Cobalt silicide will be used
- Salicide process
Cobalt Silicide: Process

- Pre-deposition argon sputtering clean
- Cobalt sputtering deposition
- First anneal, 600 °C
  \[ \text{Co} + \text{Si} \rightarrow \text{CoSi} \]
- Strip Unreacted cobalt
- Second anneal, 700 °C
  \[ \text{Co} + \text{Si} \rightarrow \text{CoSi}_2 \]
# Some Facts About Cobalt

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
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<tr>
<td>Name</td>
<td>Tantalum</td>
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<tr>
<td>Symbol</td>
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<tr>
<td>Atomic number</td>
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<tr>
<td>Atomic weight</td>
<td>180.9479</td>
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<tr>
<td>Discoverer</td>
<td>Georg Brandt</td>
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<td>Discovered at</td>
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<td>1735</td>
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<td>From the German word &quot;kobald&quot; meaning &quot;goblin&quot; or evil spirit</td>
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<td>Hardness</td>
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<td>Boiling point</td>
<td>3200 K or 2927 °C</td>
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<td>Thermal conductivity</td>
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<tr>
<td>Coefficient of linear thermal expansion</td>
<td>13.0×10⁻⁶ K⁻¹</td>
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Metal Thin Film Characteristics
Metal Thin Film Measurements

• Thickness.
• Stress
• Reflectivity
• Sheet resistance
Metal Thin Film Thickness

- TEM and SEM
- Profilometer
- 4-point probe
- XRF
- Acoustic measurement
TEM and SEM

- Cross section
- TEM: very thin film, few hundred Å
- SEM: film over thousand Å
Q & A

• Why is SEM photo is always in black and white?

• Intensity of the secondary electron emission
  – strong or weak signals
  – photo image: bright and dim, black and white

• SEM photo can be painted after it has been analyzed
Profilometer

- Thicker film (> 1000 Å),
- Patterned etch process prior to measurement
- Stylus probe senses and records microscopic surface profile
Schematic of Stylus Profilometer

Profile Signal  \[ \text{Film Thickness} \]
Four-point Probe

- Measure sheet resistance
- Commonly used to monitor the metal film thickness by assuming the resistivity of the metal film is a constant all over the wafer surface
Acoustic Measurement

• New technique
• Directly measure opaque thin film thickness
• Non-contact process, can be used for production wafer
Acoustic Measurement

- Laser shots on thin film surface
- Photo-detector measures reflected intensity
- 0.1 ps laser pulse heat the spot up 5 to 10 °C
- Thermal expansion causes a sound wave
- It propagates in the film and reflects at the interface of the different materials
- The echo causes reflectivity change when it reaches the thin film surface.
Acoustic Measurement

- Acoustic wave echoes back and forth in film
- The film thickness can be calculated by
  \[ d = \frac{V_s \Delta t}{2} \]
- \( V_s \) is speed of sound and \( \Delta t \) is time between reflectivity peaks
- The decay rate the echo is related to the film density.
- Multi-layer film thickness
Acoustic Method Measurement

\[ d = v_s \cdot \Delta t / 2 \]

Echoing acoustic wave

First echo
Second echo
Third echo

TiN
TEOS SiO₂
TiN Thickness

- $d = V_s \cdot \Delta t/2$
- Sound velocity in TiN film $V_s = 95 \text{ Å/ps}$
- $\Delta t \approx 25.8 \text{ ps}$
- $d = 1225 \text{ Å}$
Uniformity

• The uniformity, in fact it is non-uniformity, of the thickness, sheet resistance, and reflectivity are routinely measured during the process development and for the process maintenance.

• It can be calculated by measuring at multiple locations on a wafer
Mapping Patterns for Uniformity Measurement
Uniformity

• Most commonly used non-uniformity definition: 49-point, $3\sigma$ standard deviation
• Clearly define non-uniformity
  – For the same set of data, different definitions causes different results
• 5-point and 9-point are commonly used in production
Stress

• Caused by mismatching between film and substrate
• Compressive and tensile
• High compressive stress causes hillocks
  – short metal wires between different layers
• High tensile stress causes cracks or peels
Compressive Stress Causes Hillock

Force

Metal

Substrate

Force
Tensile Stress Causes Crack
Favorable Stress

- Aluminum has higher thermal expansion rate than silicon
  \[ \alpha_{\text{Al}} = 23.6 \times 10^{-6} \text{ K}^{-1}, \quad \alpha_{\text{Si}} = 2.6 \times 10^{-6} \text{ K}^{-1} \]
- It favors tensile stress at room temperature
- Stress becomes less tensile when wafer is heated up later
  - metal annealing (~ 450 °C)
  - dielectric deposition (~ 400 °C)
Q & A

• Why does silicon oxide film favor compressive stress at room temperature?

• Silicon oxide has lower thermal expansion rate \( (\alpha_{\text{SiO}_2} = 0.5 \times 10^{-6} \text{ K}^{-1}) \) than the silicon

• If it has tensile stress at room temperature, it will become more tensile when the wafer is heated up in later processes
Reflectivity

- Reflectivity change indicates drift of process
- A function of film grain size and surface smoothness
- Larger grain size film has lower reflectivity
- Smoother metal surface has higher reflectivity
- Easy, quick and non-destructive
- Frequently performed in semiconductor fabs
Sheet Resistance

- 4-point probe
- Widely used to determine film thickness
- Assuming resistivity is the same on wafer
- Faster and cheaper than the profilometer, SEM, and acoustic measurement
Sheet Resistance

- Sheet resistance \((R_s)\) is a defined parameter

\[ R_s = \frac{\rho}{t} \]

- By measuring \(R_s\), one can calculate film resistivity \((\rho)\) if film thickness \(t\) is known, or film thickness if its resistivity is known.
Resistance of a Metal Line

\[ R = \rho \frac{L}{A} \]

- \( R \) = Resistance
- \( \rho \) = Resistivity
- \( L \) = Length
- \( A \) = Area of line cross-section

Hong Xiao, Ph. D.  
www2.austin.cc.tx.us/HongXiao/Book.htm
Sheet Resistance Concepts

Apply current $I$ and measure voltage $V$,
Resistance: $R = \frac{V}{I} = \rho \frac{L}{(wt)}$
For a square sheet, $L = w$, so $R = \frac{\rho}{t} = R_s$
Unit of $R_s$: ohms per square ($\Omega/\square$)
Sheet Resistance
Sheet Resistance

Are you sure their resistance is the same?

\[ R_s = \rho / t \]
Sheet Resistance

For this two conducting lines patterned from the same metal thin film with the same length-to-width ratios, are their line resistance the same?

Yes.
Four-point Probe

• Commonly used tool for sheet resistance
• A current is applied between two pins and voltage is measured between other two pins
  – If current $I$ is between $P_1$ and $P_4$, $R_s = 4.53 \frac{V}{I}$, $V$ is voltage between $P_2$ and $P_3$
  – If current $I$ is between $P_1$ and $P_3$, $R_s = 5.75 \frac{V}{I}$, $V$ is voltage between $R_2$ and $R_4$
• Both configurations are used in measurement
Four-Point Probe Measurement

**Diagram:**

- **I** represents the current source.
- **V** represents the voltage measurement.
- **P<sub>1</sub>**, **P<sub>2</sub>**, **P<sub>3</sub>**, and **P<sub>4</sub>** are the probe points.
- **S<sub>1</sub>**, **S<sub>2</sub>**, and **S<sub>3</sub>** are the distances between the probes.

**Layer Structure:**

- **Film** is the layer above the substrate.
- **Substrate** is the layer beneath the film.
Metal CVD

• Widely used to deposit metal
• Good step coverage and gap fill capability
  – can fill tiny contact holes to make connections between metal layers.
• Poorer quality and higher resistivity than PVD metal thin films.
  – Used for plugs and local interconnections
  – Not applied for global interconnections
Metal CVD Chamber

Process Gases

RF Power

Process Chamber

Wafer

Heated plate

To pump
Metal CVD

• W, WSi$_x$, Ti, and TiN
• Thermal process, heat provides free energy needed for the chemical reaction
• RF system is used for plasma dry clean of the process chamber
Metal CVD Process Steps

- Wafer into the chamber
- Slip valve closes
- Set up pressure and temperature, with secondary process gas(es)
- All process gases flow in, start deposition
- Termination of the main process gas. Secondary process gas(es) remain on
- Termination of all process gases
- Purge chamber with nitrogen
- Slip valve opens and robot pull wafer out
Metal CVD Chamber Clean Steps

• Chamber pumps down
• Set up pressure and temperature
• RF turns on. Start plasma and clean process
• RF turns off. Chamber is purged
• Set up pressure and temperature, with secondary process gas(es)
• Flows main process gas to deposit the seasoning layer
• Terminate the main process gas
• Terminate all process gases
• Purge chamber with nitrogen
• Chamber is ready for the next deposition
Vertical and Tapered Contact Holes

Area = A

A << B

Area = B

Straight Sidewall

Tapered Sidewall
Tungsten CVD Basics

Tungsten source gas: tungsten hexafluoride (WF$_6$)

Additional reactant: hydrogen (H$_2$)

Temperature: 400 - 475 °C

Step Coverage is 100 %
Typical W CVD Process

- Wafer transferred to chamber
- Pressure and gas flows ($H_2$, $SiH_4$) established
- Nucleation takes place (silane reduction of $WF_6$)
- Pressure and gas flows changed for bulk deposit
- Bulk deposit takes place ($H_2$ reduction of $WF_6$)
- Chamber pumped and purged
- Wafer transferred out of chamber
W CVD Reactions

Nucleation on silicon
\[ 2 \text{WF}_6 + 3 \text{ Si} \rightarrow 2 \text{ W} (s) + 3 \text{ SiF}_4 \]

Nucleation on glue layer
\[ 2 \text{WF}_6 + 3 \text{ SiH}_4 \rightarrow 2 \text{ W} (s) + 3 \text{ SiF}_4 + 6 \text{ H}_2 \]

Bulk deposit
\[ \text{WF}_6 + 3 \text{ H}_2 \rightarrow \text{ W} (s) + 6 \text{ HF} \]

WF$_6$ reaction with moisture
\[ \text{WF}_6 + 3 \text{ H}_2\text{O} \rightarrow \text{WO}_3 + 6 \text{ HF} \]
Tungsten Seed and Bulk Layers

- Tungsten seed layer
- Ti/TiN barrier & adhesion layer
- Bulk tungsten layer
Tungsten Silicide

- CVD and RTP
- WF$_6$ and SiH$_4$ as CVD source gases
- Anneal after gate etch
- Less popular than TiS$_2$ due to higher resistivity
Tungsten Silicide

- Sate and local interconnection applications
- Silicon sources: SiH$_4$ and SiH$_2$Cl$_2$ (DCS)
- Tungsten precursor is WF$_6$
- SiH$_4$/WF$_6$: lower temperature, ~ 400 °C,
- DCS/WF$_6$: higher temperature, ~ 575 °C
Tungsten Silicide: CVD

300 to 400 °C

\[
WF_6 + 2 \text{SiH}_4 \rightarrow \text{WSi}_2 + 6 \text{HF} + \text{H}_2
\]

• Wider process window, more matured process

500 to 600 °C

\[
WF_6 + 3.5 \text{SiH}_2\text{Cl}_2 \rightarrow \text{WSi}_2 + 1.5 \text{SiF}_4 + 7 \text{HCl}
\]

• Better step coverage
• Less fluorine integration
Silane-Based $\text{WSi}_x$

$$\text{WF}_6 + 2 \text{SiH}_4 \rightarrow \text{WSi}_2(\text{s}) + 6 \text{HF} + \text{H}_2$$

- Very similar to the nucleation step of the tungsten CVD process.
- Different flow rate ratio of $\text{SiH}_4/\text{WF}_6$
  - lower than 3:1, tungsten deposition
  - larger than 10:1 tungsten silicide deposition
DCS-Based $\text{WSi}_x$

$$2 \text{WF}_6 + 7 \text{SiH}_2\text{Cl}_2 \rightarrow 2 \text{WSi}_2 + 3 \text{SiF}_4 + 14 \text{HCl}$$

• Requires higher deposition temperature,
• Higher deposition rate
• Better step coverage
• Lower fluorine concentration
• Less tensile stress
  – less film peeling and cracking
Titanium CVD

- High temperature (~ 600 °C)
- CVD Ti can react with Si to form TiSi$_2$ simultaneously during the Ti deposition

\[
\text{TiCl}_4 + 2 \text{H}_2 \rightarrow \text{Ti} + 4 \text{HCl} \\
\text{Ti} + \text{Si} \rightarrow \text{TiSi}_2
\]
Titanium Nitride CVD

- Barrier/glue layer for the tungsten plug
- Better sidewall step coverage
- A thin layer of (~200 Å) usually is applied for the contact/via holes after PVD Ti and TiN deposition
CVD PVD and CVD TiN Layers

PVD TiN Layer

CVD TiN Layer

Ti Layer

Metal

Oxide
CVD TiN

• Inorganic chemistry: TiCl$_4$ and NH$_3$ at 400 to 700 °C:
  
  \[ 6\text{TiCl}_4 + 8 \text{NH}_3 \rightarrow 6 \text{TiN} + 24 \text{HCl} + \text{N}_2 \]

• MOCVD at 350 °C and 300 mTorr:
  
  \[ \text{Ti[N(CH}_3\text{)}_2\text{]}_4 \rightarrow \text{TiN} + \text{organics} \]
CVD Aluminum

• R&D to replace tungsten plug
• Dimethylaluminum hydride (DMAH), $\text{Al(\text{CH}_3)_2\text{H}}$
• At about 350 °C, DMAH dissociates and deposits aluminum
  $$\text{Al(\text{CH}_3)_2\text{H}} \rightarrow \text{Al} + \text{volatile organics}$$
• Difficult to incorporate ~1% Cu needed for electromigration resistance
Cluster Tool, Aluminum CVD/PVD

Transfer Chamber

Pre-clean Ti/TiN PVD

TiN CVD

Al CVD

Wafer Loading

Wafer Unloading

Cooldown Al-Cu PVD
Aluminum CVD/PVD

• Ti/TiN barrier/glue layer deposition
• Al CVD via fill, Al alloy PVD, TiN PVD
  – No need for W and W etch back

• Not a matured technology
• Hard to compete with copper metallization
Physical Vapor Deposition
PVD

- Vaporizing solid materials
- Heating or sputtering
- Condensing vapor on the substrate surface
- Very important part of metallization
PVD vs. CVD

- PVD Start with P
- CVD Start with C
PVD vs. CVD: Sources

• PVD  Solid materials
• CVD  Gases or vapors
CVD vs. PVD

Precursor Gases → Heated Susceptor → Chemical Reaction → Deposited Film → Wafer

Target → Plasma
PVD Methods

• Evaporation
• Sputtering
PVD Methods: Evaporation

- Filaments
- Flash hot plate
- Electron beam
Thermal Evaporator

Aluminum Charge

Aluminum Vapor

10^{-6} Torr

To Pump

High Current Source

Wafers
Electron Beam Evaporator

Aluminum Charge

Aluminum Vapor

Electron Beam

Wafers

$10^{-6}$ Torr

To Pump

Power Supply

Hong Xiao, Ph. D.  www2.austin.cc.tx.us/HongXiao/Book.htm
PVD Methods: Sputtering

- DC Diode
- RF Diode
- Magnetron
Sputtering

Momentum transfer will dislodge surface atoms off
DC Diode Sputtering

- Target
- Argon Plasma
- Wafer Chuck
- Metal film
- Wafer
Schematic of Magnetron Sputtering

Magnets

Target

Higher plasma density

Magnetic field line

Erosion groove
Magnetron Sputtering

• Most widely used PVD system
• More sputter from grove
• Better uniformity cross wafer
PVD Chamber with Shield

- Shield, Liner
- Wafer
- Target
- Wafer Chuck
Applications of Argon

• Sputtering deposition

• Sputtering etch
  – pre-clean to remove native oxide before metal deposition
  – Taper opening for dielectric gap fill

• Patterned etch
  – dielectric to enhance bombardment and damaging effect
Properties of Argon

• Inert
• Relatively heavy
• Abundance
  – about 1% in atmosphere
  – low cost
Some Facts About Argon

<table>
<thead>
<tr>
<th>Name</th>
<th>Argon</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
<td>Ar</td>
</tr>
<tr>
<td>Atomic number</td>
<td>18</td>
</tr>
<tr>
<td>Atomic weight</td>
<td>39.948</td>
</tr>
<tr>
<td>Discoverer</td>
<td>Sir William Ramsay, Lord Rayleigh</td>
</tr>
<tr>
<td>Discovered at</td>
<td>Scotland</td>
</tr>
<tr>
<td>Discovery date</td>
<td>1894</td>
</tr>
<tr>
<td>Origin of name</td>
<td>From the Greek word &quot;argos&quot; meaning &quot;inactive&quot;</td>
</tr>
<tr>
<td>Molar volume</td>
<td>22.56 cm(^3)</td>
</tr>
<tr>
<td>Speed of sound</td>
<td>319 m /sec</td>
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<tr>
<td>Refractive index</td>
<td>1.000281</td>
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<tr>
<td>Electrical resistivity</td>
<td>N/A</td>
</tr>
<tr>
<td>Melting point</td>
<td>-189.2 °C</td>
</tr>
<tr>
<td>Boiling point</td>
<td>-185.7 °C</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>0.01772 W m(^{-1}) K(^{-1})</td>
</tr>
</tbody>
</table>
# Sputtering vs. Evaporator

<table>
<thead>
<tr>
<th>Sputtering</th>
<th>Evaporator</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Purer film</td>
<td>• More impurities</td>
</tr>
<tr>
<td>• Better uniformity</td>
<td>• Batch process</td>
</tr>
<tr>
<td>• Single wafer, better process control</td>
<td>• Cheaper tool</td>
</tr>
<tr>
<td>• Larger size wafer</td>
<td></td>
</tr>
</tbody>
</table>

Hong Xiao, Ph. D.  
www2.austin.cc.tx.us/HongXiao/Book.htm
PVD Vacuum Requirement

• Residue gases on the vacuum chamber wall
  – $\text{H}_2\text{O}$, …

• Water can react with Al to form $\text{Al}_2\text{O}_3$

• Affects conductivity of interconnections

• Only way to get rid of $\text{H}_2\text{O}$: reach ultra high vacuum, $10^{-9}$ Torr
PVD Vacuum Requirement

• Cluster tool
• Staged vacuum
• Loading station: $10^{-6}$ Torr
• Transfer chamber: $10^{-7}$ to $10^{-8}$ Torr
• Deposition chamber: $10^{-9}$ Torr
PVD Vacuum: Pumps

- Wet pump (oil diffusion pump): atm to $10^{-3}$ Torr, phasing out from fabs.
- Rough pump: atm to $10^{-5}$ Torr
- Turbo pump: $10^{-2}$ to $10^{-7}$ Torr
- Cryo pump: to $10^{-10}$ Torr
- Ion pump: to $10^{-11}$ Torr
Endura® PVD System

PVD Target

PVD Chamber

CVD Chamber
Contact/Via Process

- Degas
- Pre-clean
- Ti PVD
- TiN PVD
- TiN CVD
- $N_2-H_2$ plasma treatment
- W CVD
Aluminum Interconnection Process

- Degas
- Pre-clean
- Ti PVD
- Al-Cu PVD
- TiN PVD
Copper Interconnection Process

• Degas
• Pre-clean
• Ta PVD
• Cu seed PVD
Degas

- Heat wafer to drive away gases and moisture on wafer surface
- Outgassing can cause contamination and high resistivity of deposited metal film
Pre-clean

• Remove the native oxide
• Reduce the contact resistance
• Sputtering with argon ions
• RF plasma
Pre-clean Process

Argon Plasma

Metal

Native Oxide

Ar$^+$
Titanium PVD

- Reduce contact resistance
- Larger grain size with low resistivity
- Wafer normally is heated to about 350 °C during the deposition process to
- Improve the surface mobility
- Improve step coverage
Collimated Sputtering

• Used for Ti and TiN deposition
• Collimator allows metal atoms or molecules to move mainly in vertical direction
• Reach the bottom of narrow contact/via holes
• Improves bottom step coverage
Collimated Sputtering

- Target
- Plasma
- Collimator
- Film
- Via holes
- Magnets
Metal Plasma System

• Ti, TiN, Ta, and TaN deposition
• Ionize metal atoms through inductive coupling of RF power in the RF coil
• Positive metal ions impact with the negatively charged wafer surface vertically
• Improving bottom step coverage
• Reduce contact resistance
Ionized Metal Plasma

Target

Inductive Coils

Plasma

Via Hole

RF
Titanium Nitride PVD

- Reactive sputtering process
- Ar and \( \text{N}_2 \)
- \( \text{N}_2 \) molecules dissociate in plasma
- Free nitrogen radicals react with Ti to form a thin layer of TiN on target surface.
- Argon ions sputter the TiN from the target surface and deposit it on the wafer surface
Three Applications of TiN

- TiN ARC, PVD
- TiN, PVD
- TiN glue layer, PVD & CVD

Diagram showing layers of materials:
- TiSi₂
- n⁺
- PSG
- W
- Al-Cu
- TiN glue layer, PVD & CVD
- TiN, PVD
- TiN ARC, PVD
Al-Cu PVD

- Ultra high vacuum to remove moisture and achieve low film resistivity.
- Cluster tool with staged vacuum
- dry pumps, turbo pumps and cryopump
- A cryopump can help a PVD chamber to reach up to $10^{-10}$ Torr base pressure by freezing the residue gases in a frozen trap
Al-Cu PVD

- Standard process and hot aluminum process
- Standard process: Al-Cu over tungsten plug after Ti and TiN deposition
- Normally deposit at ~ 200 °C
- Smaller grain size, easier to etch
- Metal annealing to form larger grain size
  - lower resistivity
  - high EMR
Al-Cu PVD

- Hot aluminum process
- fill contact and via holes, reduces contact resistance
- Several process steps:
  - Ti deposition
  - Al-Cu seed layer is deposited at low <200°C
  - Bulk Al-Cu layer is deposited at higher temperatures (450°C to 500°C)
Copper Metallization
Copper

- Better conductor than aluminum
- Higher speed and less power consumption
- Higher electromigration resistance
- *Diffusing freely in silicon and silicon dioxide, causing heavy metal contamination, need diffusion barrier layer*
- *Hard to dry etch, no simple gaseous chemical compounds*
Copper

- Damascene process with CMP
- Ta and/or TaN as barrier layer
- Start using in IC fabrication
Copper

• Pre-deposition clean
• PVD barrier layer (Ta or TaN, or both)
• PVD copper seed layer
• Electrochemical plating bulk copper layer

• Thermal anneal to improve conductivity
Etch trenches and via holes
Tantalum Barrier Layer and Copper Seed Layer Deposition
Electrochemical Plating Copper
CMP Copper and Tantalum, CVD Nitride
Pre-clean

• Argon sputtering pre-deposition clean
  – Commonly used
  – Possible copper contamination due to sputtering

• Chemical pre-clean
  – $\text{H}_2$ and He plasma
  – H radicals react with $\text{CuO}_2$
    \[
    4 \text{H} + \text{CuO}_2 \rightarrow \text{Cu} + 2 \text{H}_2\text{O}
    \]}
Barrier Layer

- Copper diffusion into silicon can cause device damaging
- Need barrier layer
- Ti, TiN, Ta, TaN, W, WN,
- Few hundred Å Ta is commonly used
- Combination of Ta and TaN in near future
Copper Seed Layer

- PVD copper layer (500 to 2000 Å)
- Nucleation sites for bulk copper grain and film formation.
- Without seed layer
  - No deposition
  - or deposition with very poor quality and uniformity
Copper Seed Layer

- Copper vapor can be easily ionized
- Low pressure, long MFP
- Copper ions throw into via and trench
  - good step coverage and smooth film surface
- Very narrow via hole, PVD copper will be in trouble due to its poor step coverage
- CVD copper process may be needed
Electrochemical Plating (ECP)

- Old technology
- Still used in hardware, glass, auto, and electronics industries.
- Recently introduced in IC industry
- Bulk copper deposition
- Low-temperature process
- Compatible with low-κ polymeric dielectric
Electrochemical Plating (ECP)

- CuSO$_4$ solution
- Copper anode
- Wafer with copper seed layer as cathode
- Fixed electric current
- Cu$^{2+}$ ion diffuse and deposit on wafer
Copper Electrochemical Plating

Anode, Cu

Solution with CuSO$_4$

Wafer holder, plastic

Conducting ring, cathode

Wafer

Current

Cu$^{2+}$

Copper film

Cu$^{2+}$

Cu$^{2+}$

Cu$^{2+}$
Via and Trench Fill

- To achieve better gap-fill, pulse current with large forward amperage and small reversed amperage is used.
- Reversed current removes copper, which reduces overhang of the gap.
- Similar to dep/etch/dep process
- Additives reduces deposition on the corner to improve the via fill capability
Electrochemical Plating Via Fill

![Diagram showing electrochemical plating process with copper ions (Cu²⁺) diffusing into a tantalum layer through a solution containing CuSO₄. The diagram illustrates the movement of copper ions into the USG layers.](image-url)
Copper CVD

- bis-hexafluoroacetyl-acetonate copper, or Cu(hfac)$_2$

\[
\text{Cu(hfac)$_2$ + H}_2 \rightarrow \text{Cu} + 2 \text{H(hfac)}
\]

- 350 to 450 °C
- Too high for polymeric low-κ dielectric
$\text{Cu}^{\text{II}}(\text{hfac})_2$
Copper CVD

• Organiometallic compound
• Cu(hfac)(tmvs): $C_{10}H_{13}CuF_6O_2Si$

$$2 \text{Cu(hfac)(tmvs)} \rightarrow \text{Cu} + \text{Cu(hfac)}_2 + 2 \text{tmvs}$$

• Thermal process $\sim 175 \, ^\circ\text{C}$, 1 to 3 Torr
• Excellent step coverage and gap fill capability
Copper CVD

• Cu(hfac)(vtms) process is the more promising copper CVD process.
• Tough competition from the production-proven copper ECP process
• PVD/CVD copper seed layer deposition
Summary

- Mainly application: interconnection
- CVD (W, TiN, Ti) and PVD (Al-Cu, Ti, TiN)
- Al-Cu alloy is still dominant
- Need UHV for Al-Cu PVD
- W used as plug
- Ti used as welding layer
- TiN: barrier, adhesion and ARC layers
- The future: Cu and Ta/TaN