Bipolar Transistors - Part 2

Chapter 5 of Physics of Semiconductor Devices

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Outline

1. 5.3 Microwave Characteristics
   - Cutoff Frequency
   - Small-Signal Characterization
   - Switching Characterisitcs
   - Device Geometry and Performance
2. 5.4 Related Device Structures
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   - Graded-Base Bipolar Transistor
   - Hot-Electron Transistor

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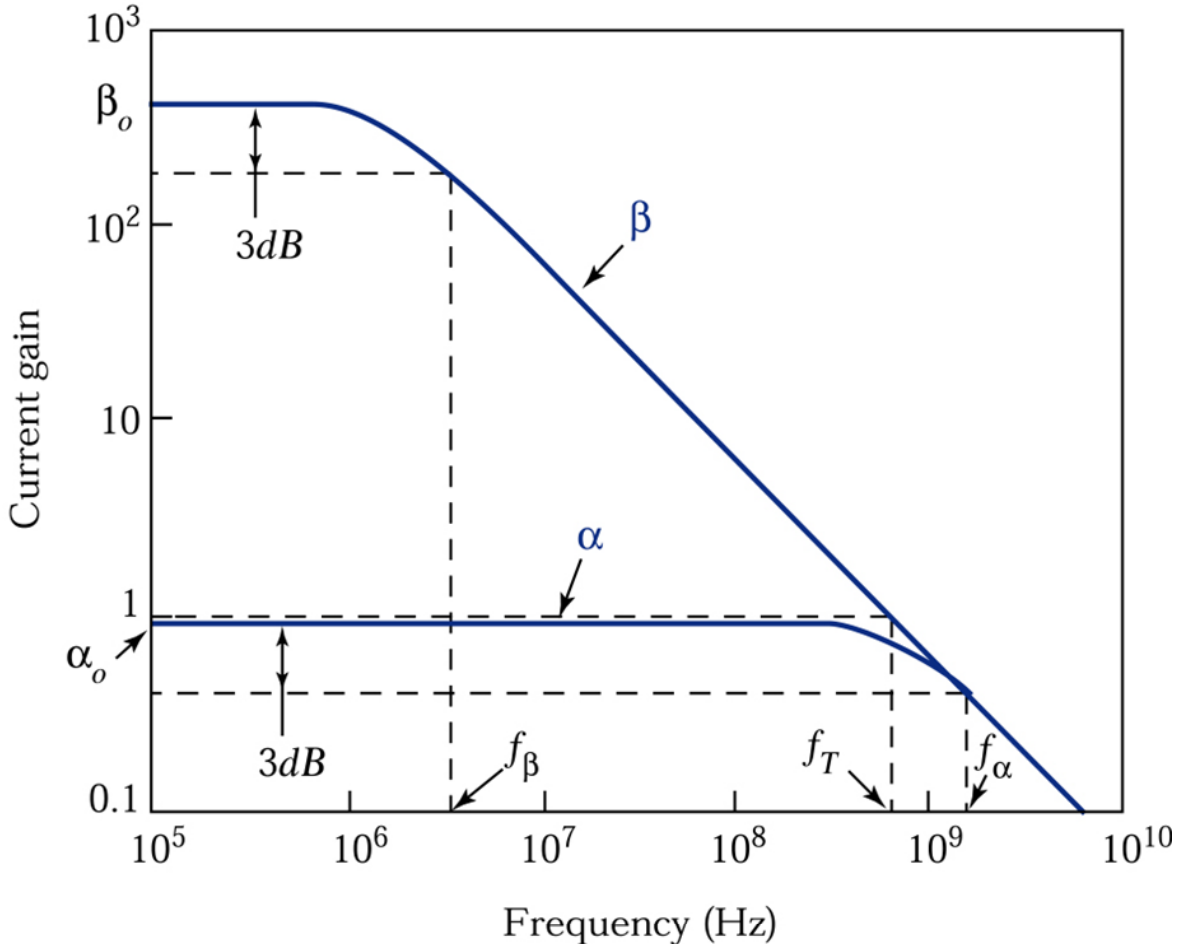
5.3 Microwave Characteristics

High g_m = high current drive = high speed circuits

1. Microwave transistors
   - Operation with small signal amplification
2. Switching transistors
   - Operation with large-signal transient process (switching between on and off state)
   - E.g. digital circuits

Cutoff Frequency, f_T

The frequency at which the small signal common-emitter current gain is unity: $\beta \equiv h_{fe} \equiv \frac{dI_C}{dI_B}$ = 1 = 0 dB



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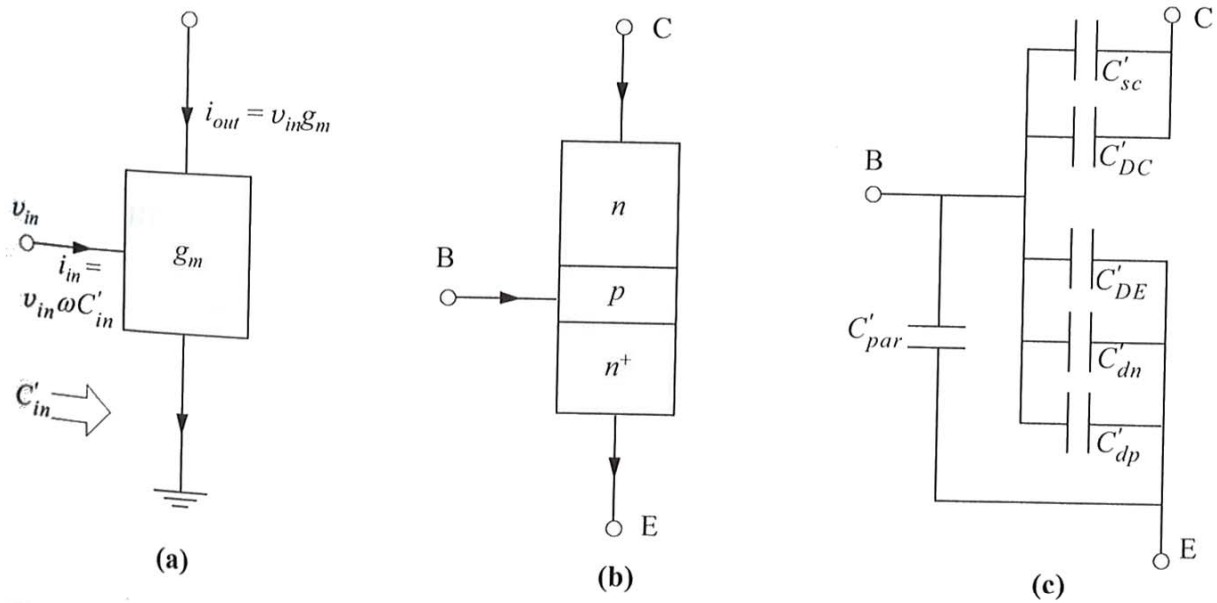
Cutoff Frequency, f_T



$$C'_{in} = C'_{par} + C'_{in} + C'_{dn} + C'_{dp} + C'_{DE} + C'_{DC} + C'_{sc}$$

- C'_{par}: Parasitic capacitance
- C'_{dn}: Diffusion capacitance due to electrons (into base)
- C'_{dp}: Diffusion capacitance due to holes (into emitter)
- C'_{DE}: Emitter-base depletion capacitance
- C'_{DC}: Collector-base depletion capacitance
- C'_{sc}: Space-charge capacitance in collector, due to injected electrons

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Cutoff Frequency, f_T

$$f_T = \frac{g_m}{2\pi C'_{in}} = \frac{1}{2\pi\Sigma(C'/g_m)} = \frac{1}{2\pi\Sigma\tau}$$

$\tau = C'/g_m$: the time constant of the delay due to each capacitance (or the time required to charge each capacitance)

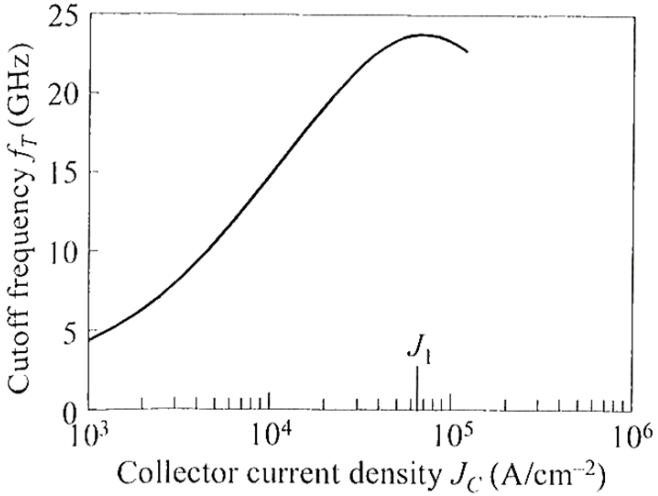
$\tau = R_C C'_{DC}$: the time constant in the collector terminal, where R_C is the total collector resistance

$$f_T = \{2\pi[\underbrace{\frac{kT(C'_{par} + C'_{DE} + C'_{DC})}{qI_C}}_{\text{Decrease with current}} + \frac{W^2}{\eta D_n} + \frac{W_E W}{\theta D_n} + \frac{W_{DC}}{2\nu_s} + R_C C'_{DC}]\}^{-1}$$

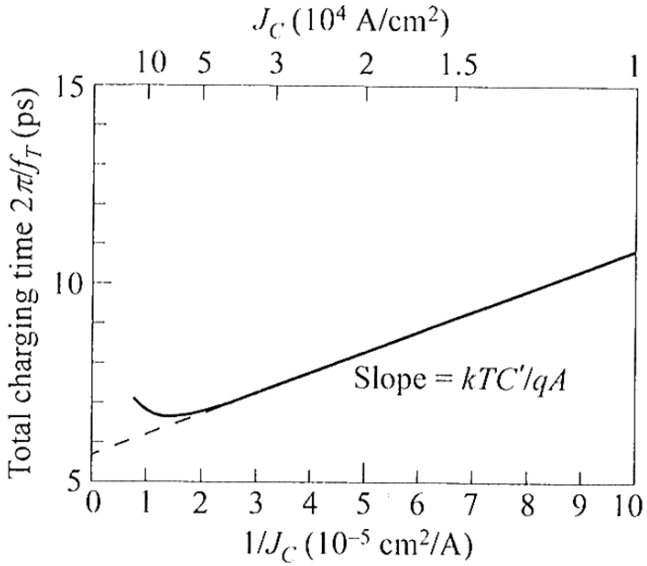
For high-frequency applications, a bipolar transistor should:

- Operate at high current (but less than regime of undesirable high-current effects, e.g. Kirk effect)
- Have a very narrow base thickness
- Have a very narrow collector depletion region

Cutoff Frequency, f_T



(a)



(b)

- At low current densities, f_T increases with J_C. In this regime the collector current is carried mainly by the drift component
- J_1 is the current at which the largest uniform electric field can exist, where $\mathcal{E}_C = (\phi_{bi} + V_{CB})/W_C$
- At $J_1 = \frac{q\mu_n N_C(\phi_{bi}+V_{CB})}{W_C}$, f_T reaches its maximum. Beyond J_1, the current cannot be carried totally by the drift component throughout the collector epitaxial region.

Small-Signal Characterization, Figures of Merit

Power gain, G_p: the ratio of power delivered to the load over the maximum available power to the network.

Stability factor, K: indicates where a transistor will oscillate upon applying a combination of passive load and source impedance with no external feedback.

$$K: \begin{cases} > 1 & \text{the device is unconditionally stable (will not oscillate)} \\ < 1 & \text{the device is potentially unstable} \end{cases}$$

Maximum available power gain, G_{pmax}: the power gain which can be realised by a particular transistor without external feedback

Unilateral gain, U: the forward power gain in a feedback amplifier with its reverse power gain set to zero by adjusting a lossless reciprocal feedback network around the transistor

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Small-Signal Characterization, Figures of Merit

Maximum frequency of oscillation, f_{max}: the frequency at which the unilateral gain becomes unity

Noise figure, NF: the ratio of total mean-square noise voltage at the output of the transistor to mean-square noise voltage at the output resulting from thermal noise in the source resistance

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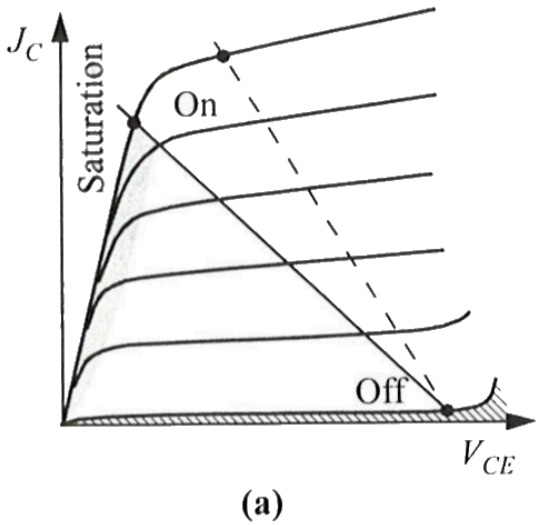
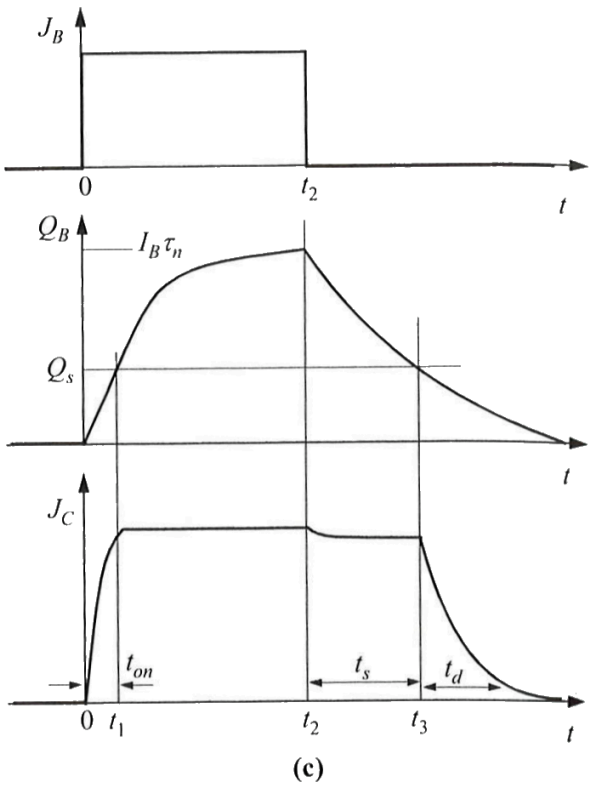
Switching Characteristics



(a)

- A switching transistor is designed to function as a switch
- The state switches from high-impedance (*off*) condition to low-impedance (*on*) condition in a very short time
- Large signal operation
- E.g. digital circuits
- Usually ”on” $\longrightarrow$ saturation

Switching Characteristics



(c)

- In saturation, Q_B rises due to an applied I_B without increasing I_C
- The change of Q_B gives rise the the transient response
- After the time t_{on}, the steady-state value of Q_B:
  $Q_B = J_B\tau_n[1 - exp\frac{-t}{\tau_n}]$
  $t_{on} = \tau_n ln\left[\frac{1}{1-(Q_s/J_B\tau_n)}\right]$, $Q_s = \frac{J_C W^2}{2D_n}$
- At t_2, I_B is turned off and Q_B decays with time constant τ_n.
- The storage time t_s is the time interval for Q_B to decay from $J_B\tau_n$ to Q_s
  $t_s = \tau_n ln\left(\frac{J_B\tau_n}{Q_s}\right)$
- After t_3, J_C decreases with time constant τ_n
- The sum of t_s and the delay time t_d is the total turn-off time, which limits the switching speed in digital circuits

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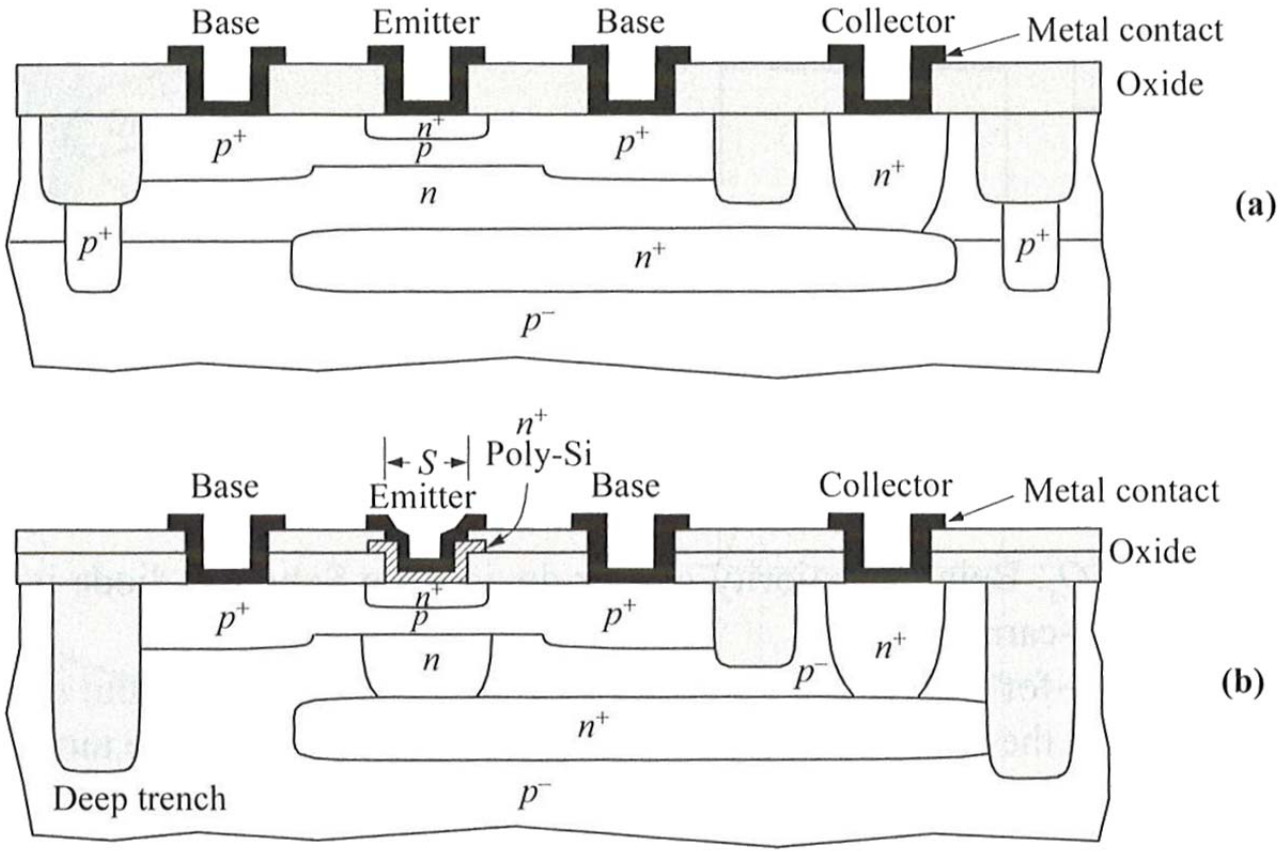
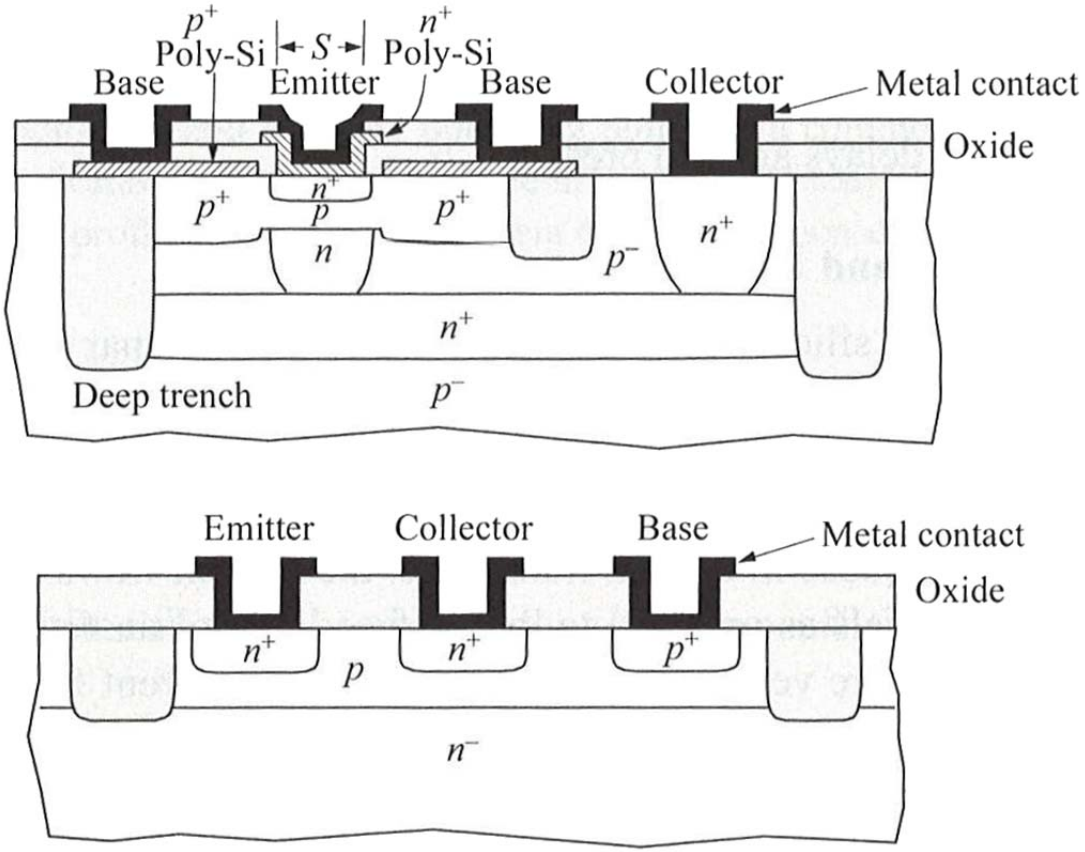
Device Geometry and Performance



Cross-sections of silicon bipolar transistors: (a) Conventional structure. (b) Modern single-poly structure with deep trench isolation.

Device Geometry and Performance



Cross-sections of silicon bipolar transistors: (c) Modern double-poly self-aligned structure. (d) Low-performance lateral structure.

5.4 Related Device Structures

1. Power Transistor
2. Basic Circuit Logics

Power Transistor

- Designed for power amplification or power switching
  - Must handle high voltages and/or large currents
  - Tradeoff between power and speed
    $\rightarrow$ Power usually proportional to $1/f^2$
- A Safe Operating Area (SOA) defines the collector load lines and bias conditions which safeguard a transistor from the effects described in the next few slides

High-Voltage Limit: HV operation limited by breakdown, typically valued at the off state (i.e. V_{BCE0})

- Voltage range can be extended by degrading the current gain

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Power Transistor

High-Current Effects: Several undesirable effects:

- Base widening due to the Kirk Effect
- Current crowding toward the boundary of the emitter due to the intrinsic base resistance
- In order to obtain high breakdown voltage, must reduce the collector doping N_C
  $\rightarrow$ Low N_C 1) exacerbates the Kirk effect and 2) induces region of quasi-saturation due to conductivity modulation in the collector (injected electron density higher than the collector doping)

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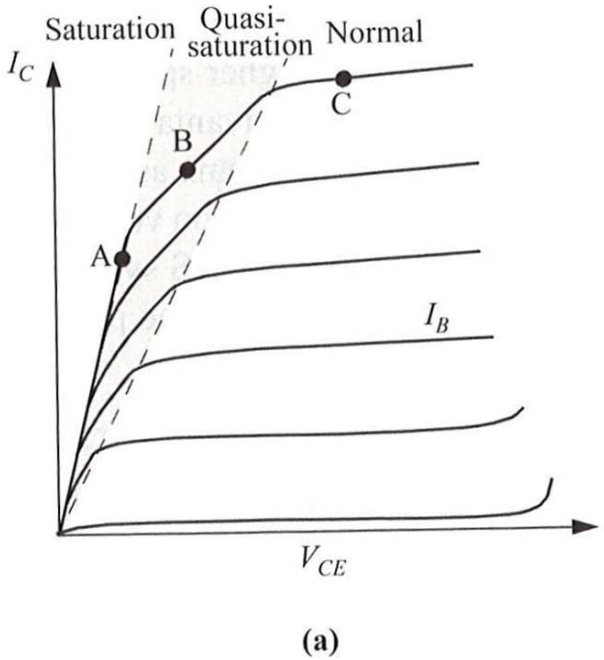
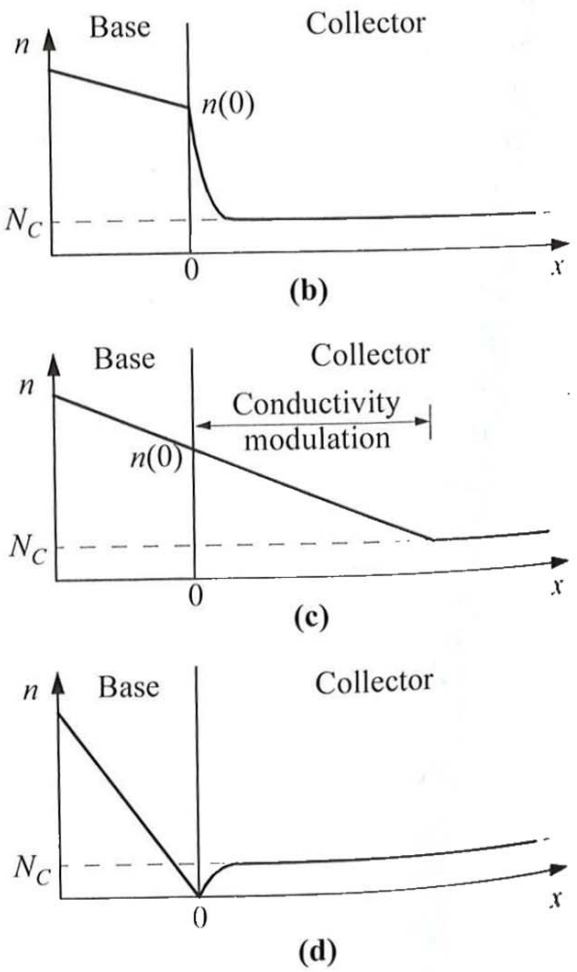
Power Transistor





(a) Common-emitter I-V characteristics showing quasi-saturation at high current and low V_{CE}. Electron-concentration profiles corresponding to (b) saturation mode (Point-A), (c) quasi-saturation mode (Point-B), and (d) normal mode (Point-C).

Power Transistor

Thermal Runaway: Local catastrophic damage due to positive feedback from raised transistor currents (from elevated temperatures due to power dissipation)

- Performance can be improved by:
  - Encapsulation and packaging with thermal conduction to sink heat
  - Enforce even distribution of current across the entire device area by segmenting the total emitter area into smaller parallel interdigits and adding an emitter resistor over each device to limit undesired current increase
    $\rightarrow$ Stabilizing resistors or emitter ballasting resistors

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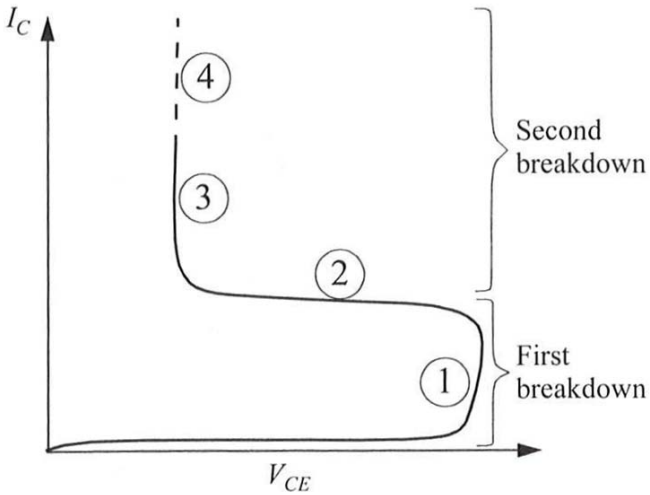
Power Transistor

Second Breakdown: An abrupt decrease in device voltage with a simultaneous internal constriction of current



- The device must be operated within a certain safe region to avoid permanent damage
- The avalanche breakdown (first breakdown) occurs when the applied emitter-collector voltage reaches V_{BCE0}
- Second breakdown occurs as the voltage increases further

- In real applications, power devices are often under transient biases $\rightarrow$ High power is dissipated only momentarily
- Higher power can be applied for a short time before destruction occurs (depends on device parameters, e.g. doping concentrations, and geometries, which affect the heat sink efficiency)

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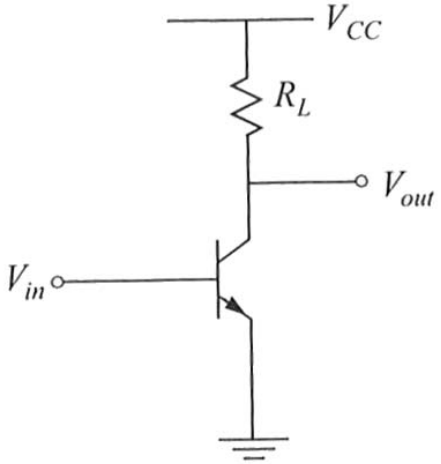
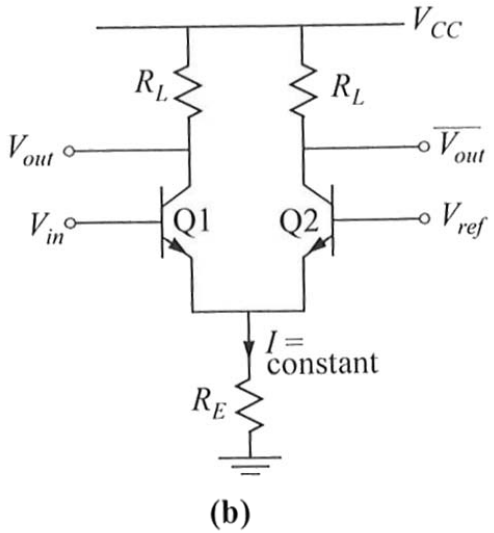
Basic Circuit Logics



(a)

- Basic inverter configuration: input = high $\rightarrow$ Transistor is on
  - High I_C develops and IR drop across the load resistor R_L, pulling output low
- Advantage over FETs: high transconductance of bipolar transistors $\rightarrow$ high speed
- Disadvantage: delay when switching in and out of saturation

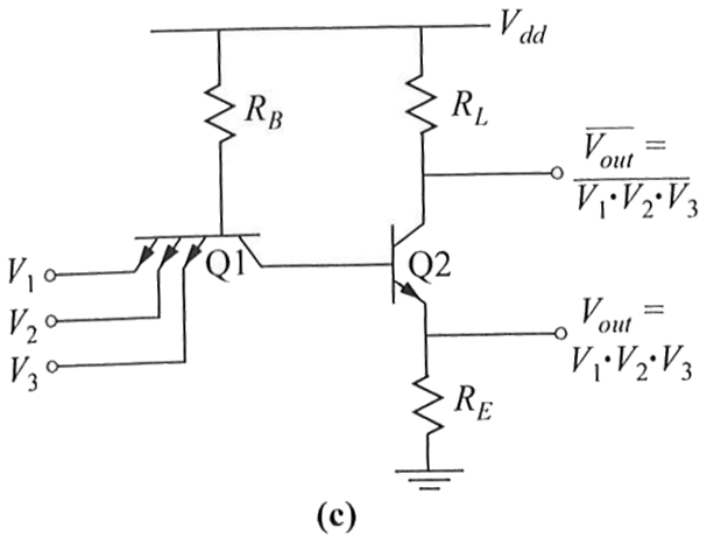
Emitter-Coupled Logic, ECL



- High-speed/high performance circuit, at the expense of high power dissipation
- Transistors arranged and biased such that they never operate in saturation mode (for speed)
- Reference transistor $Q2$ biased with fixed reference base voltage

- Current I through R_E held constant
  - Constant I shared between $Q1$ and $Q2$, which are coupled by the emitter resistance R_E
- When $Q1$ is on ($V_{in} > V_{ref}$), it steers current away from $Q2$, which raises the output $\bar{V}_{out}$
- ECL provides two complementary outputs

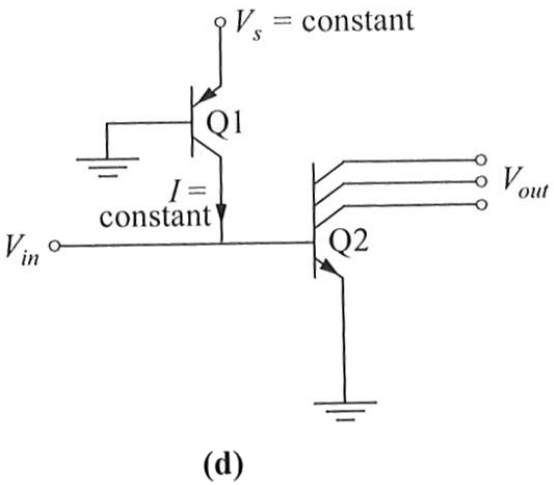
Transistor, Transistor Logic, TCL



- Multiple input gates per transistor
  $\rightarrow$ Suitable for dense circuits
- Transistor $Q1$ has multiple emitter inputs and implements an AND function
- Transistor $Q2$ is an emitter follower for the lower V_{out} and an inverter for the upper V_{out}

- TTL is designed for speed
  - When $Q2$ is turned off from saturation, the base charge is drained quickly as collector current through $Q1$

Integrated-Injection Logic, IIL



- Used in IC logic and memories
- Complementary bipolar transistors, i.e. both $n-p-n$ and $p-n-p$
- The structure incorporates a lateral $p-n-p$ transistor
- The p-collector is merged with the base of the vertical $n-p-n$ transistor

- Note: no resistor is needed
- The circuit is closely packed and does not need isolation between transistors
  $\rightarrow$ Ease of layout
  $\rightarrow$ High packing density
- The $p-n-p$ lateral transistor $Q1$ acts as a current source which injects current into the base of $Q2$
- $Q2$ has multiple collector output contacts

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BiCMOS

- Bipolar transistors have many strong points
  - High g_m
    $\longrightarrow$ High speed digital circuits
    $\longrightarrow$ High analog gain
  - Turn-on voltage of a $p-n$ junction is more controllable than the threshold voltage of a MOSFET
- BiCMOS circuits utilise both bipolar transistors and complementary MOSFETs (CMOS) for optimum design

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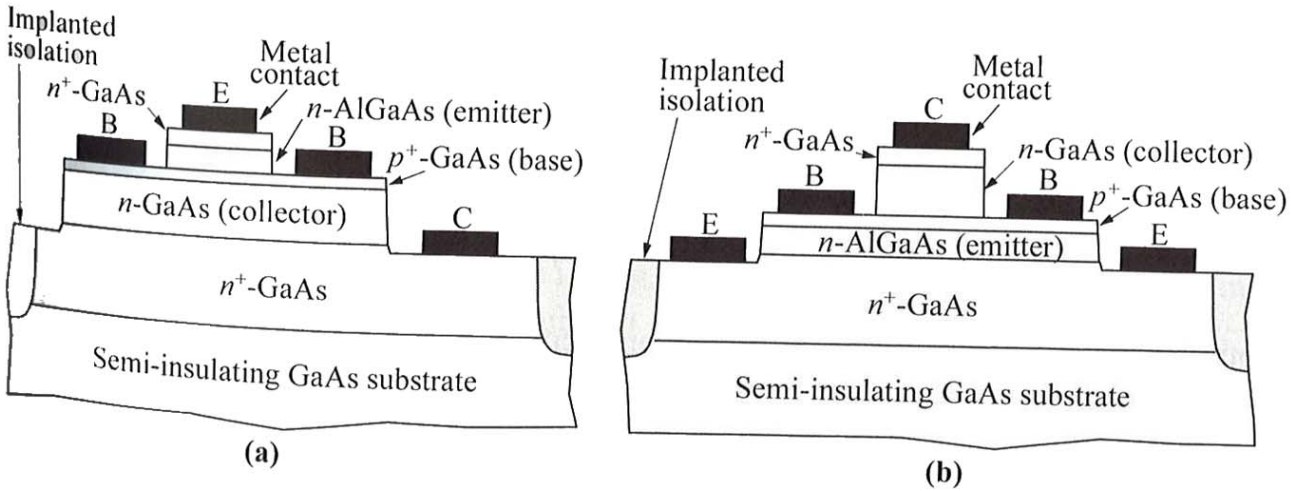
5.5 Heterojunction Bipolar Transistor

- Current gain in a bipolar transistors comes from the injection efficiency of the emitter-base junction
  - Gain determined by ratio of emitter doping to base doping
- An HBT incorporates a heterojunction as the E-B junction, with a larger bandgap in the emitter
  → Improved injection efficiency
  → Much larger current gain
- However, gain isn't everything...



(a) Typical structure of an HBT.

(b) Special structure using collector-up to minimize the collector capacitance.

Heterojunction Bipolar Transistor, HBT

- Extra gain can be traded off for other improvements
- In an HBT, the base doping can be higher than the emitter doping, but still maintain a reasonable gain
- High base doping:
  1. Lowers the base resistance, which improves f_{max} and current crowding
  2. Improves the Early voltage and reduces high-current effects
- Lower emitter doping:
  1. Reduced bandgap narrowing and reduced C_{BE}
  2. Larger built-in potential
- HBTs are mostly fabricated on III-V compound semiconductors which are capable of providing a semi-insulating substrate $\rightarrow$ Reduces parasitic capacitance and greatly improves the speed performance
- Current gain:

$$\frac{J_n}{J_p}\Big|_{HBT} = \left(\frac{n_{iB}^2}{n_{iE}^2}\right)\frac{J_n}{J_p}\Big|_{homojunction}$$
$$= \left[exp\left(\frac{\Delta Eg}{kT}\right)\right]\frac{J_n}{J_p}\Big|_{homojunction}$$

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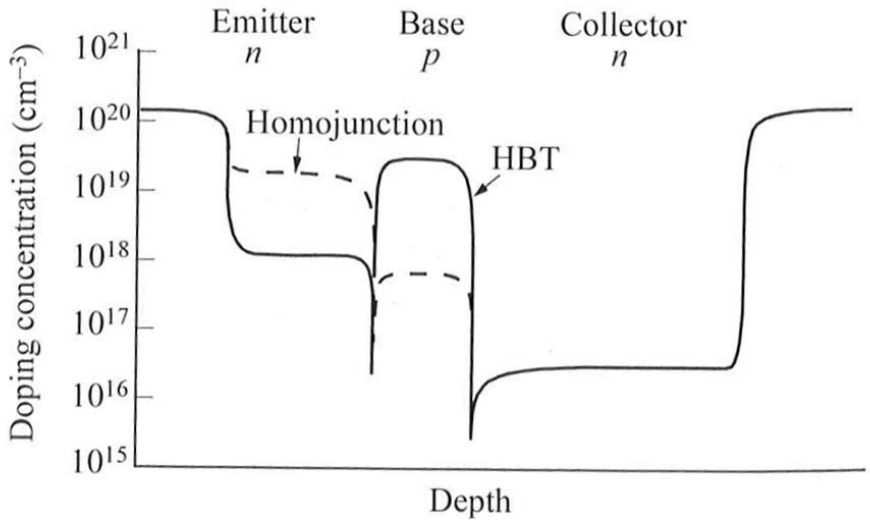
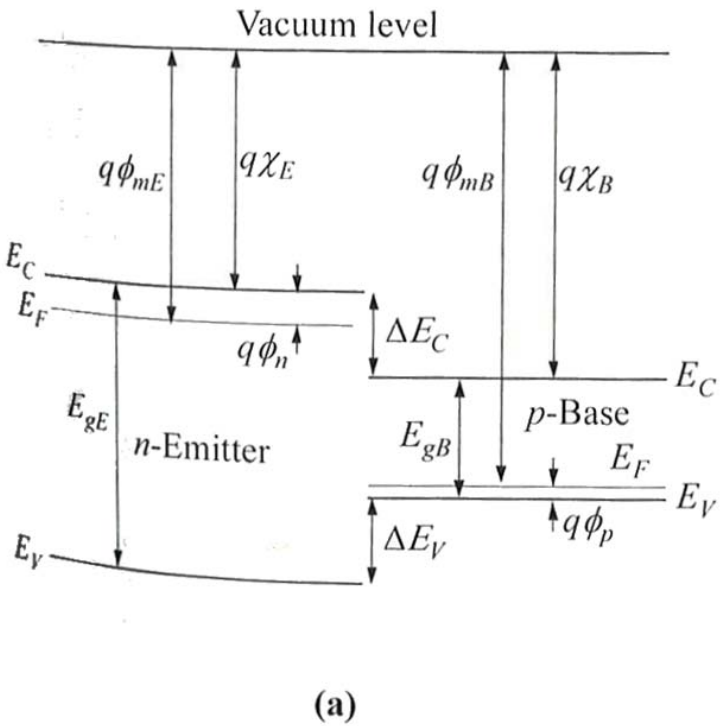

Emitter
n
Base
p
Collector
n
Homojunction
HBT
Doping concentration (cm⁻³)
10²¹
10²⁰
10¹⁹
10¹⁸
10¹⁷
10¹⁶
10¹⁵
Depth


Vacuum level
qφmE
qχE
qφmB
qχB
EC
EF
qφn
ΔEC
EC
EgE
n-Emitter
EgB
p-Base
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EV
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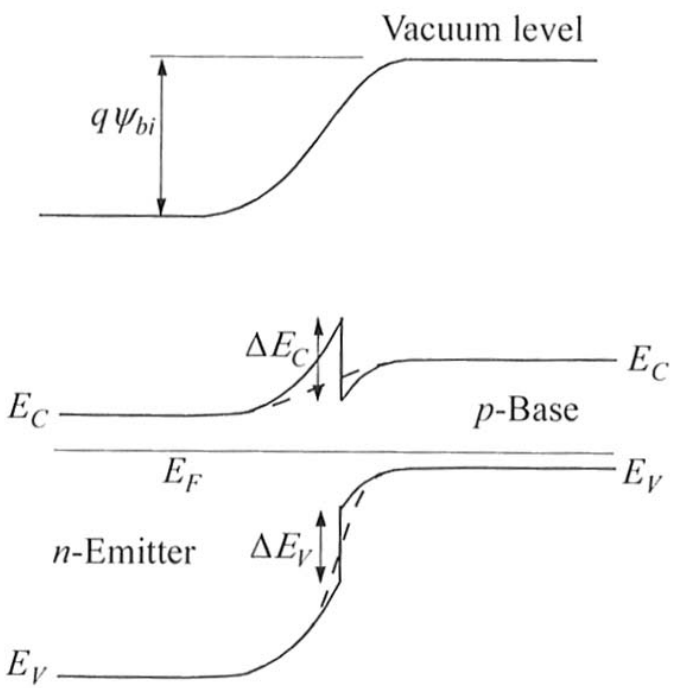
qφp
EV

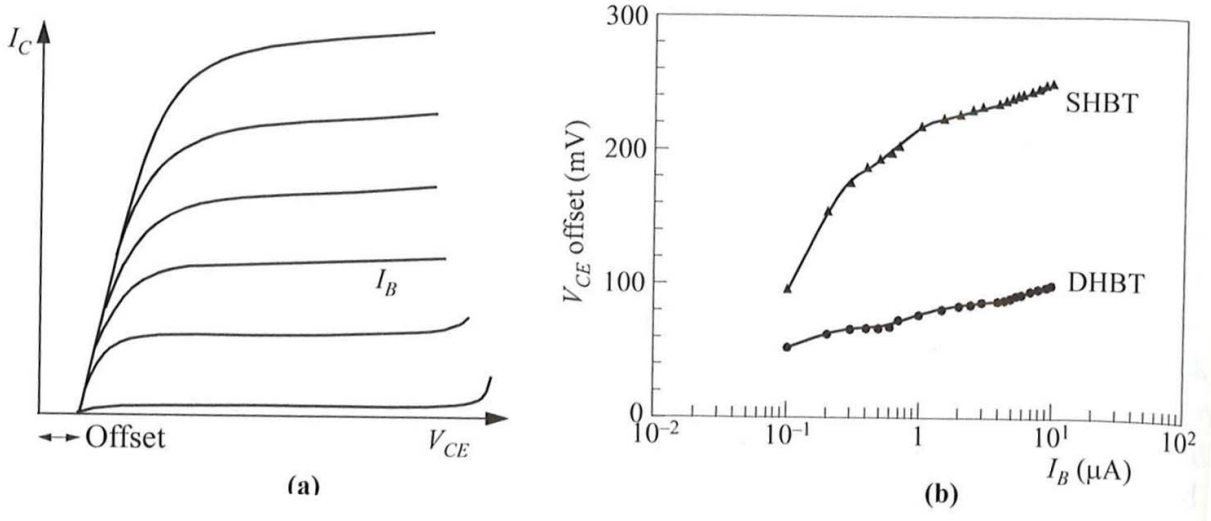
(a)


Vacuum level
qψbi
ΔEC
EC
EC
p-Base
EF
EV
n-Emitter
ΔEV
EV

(b)

Double-Heterojunction Bipolar Transistor, DHBT

- One drawback of HBT is V_{offset} in the common-emitter configuration
  - V_{offset} is because, in the low V_{CE} region (i.e. saturation) both the base-emitter and the base-collector junctions are under forward bias
  - In an HBT, the base-emitter current is suppressed, so the base-collector current contributes to a negative collector terminal current



Double-Heterojunction Bipolar Transistor, DHBT

- A double-heterojunction bipolar transistor (DHBT) eliminates this drawback by adding a second heterojunction as the base-collector junction
- Other advantages of DHBT:
  1. Higher breakdown voltage from a large collector bandgap
  2. The high-bangap collector reduces the injection of holes from the base to the collector in the saturation mode
     $\rightarrow$ Reduces the minority charge
  3. if the collector doping is made higher, it can also reduce high-current effects (e.g. Kirk effect and quasi-saturation)

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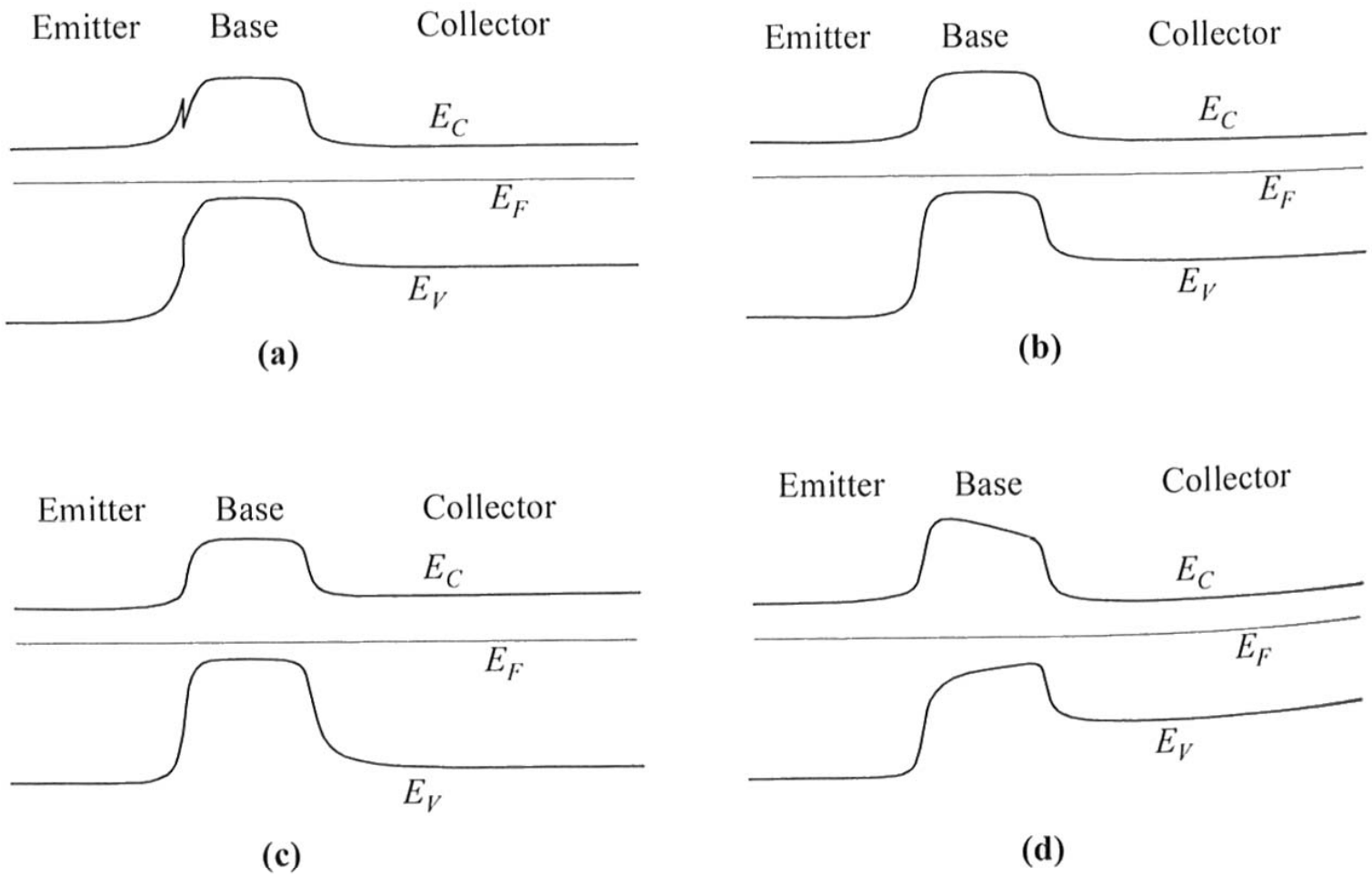
Graded-Base Bipolar Transistor



Energy-band diagrams for (a) abrupt HBT, (b) graded HBT, (c) graded DHBT, and (d) graded-base bipolar transistor.

Graded-Base Bipolar Transistor

- A graded HBT is an HBT in which the composition if varied slowly within the depletion region (note: the gain improvement is determined by the total change in bandgap, ΔE_g)
- In a graded-base bipolar transistor, the composition is changed gradually within the neutral base region, rather than in the junctions (different function than HBT)
  - The composition grading creates a quasi-field to assist the drift of electrons
- Advantages of graded-base bipolar transistor:
  1. Higher electron current and current gain
  2. Reduced base charging time for higher f_T
  3. Increased Early voltage

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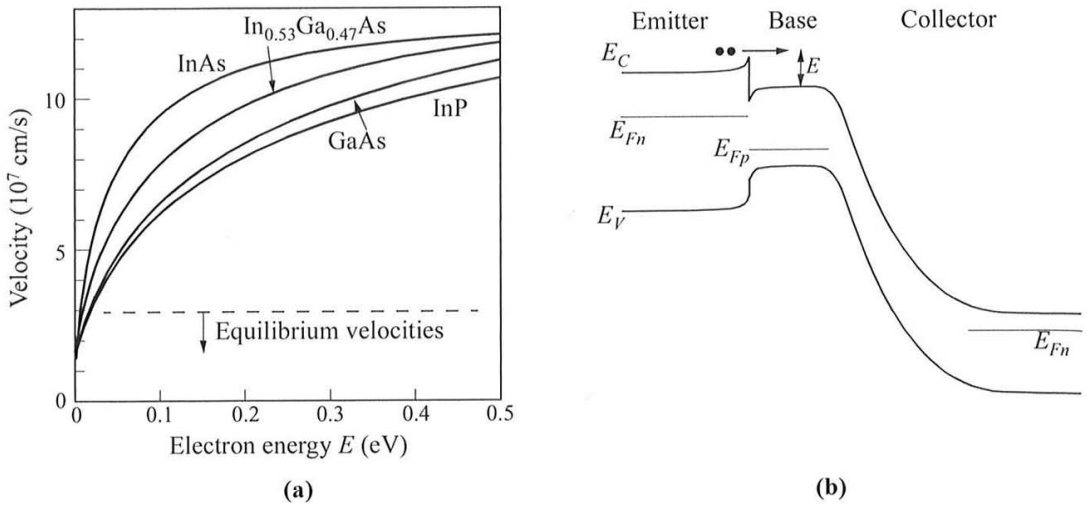
Hot-Electron Transistor

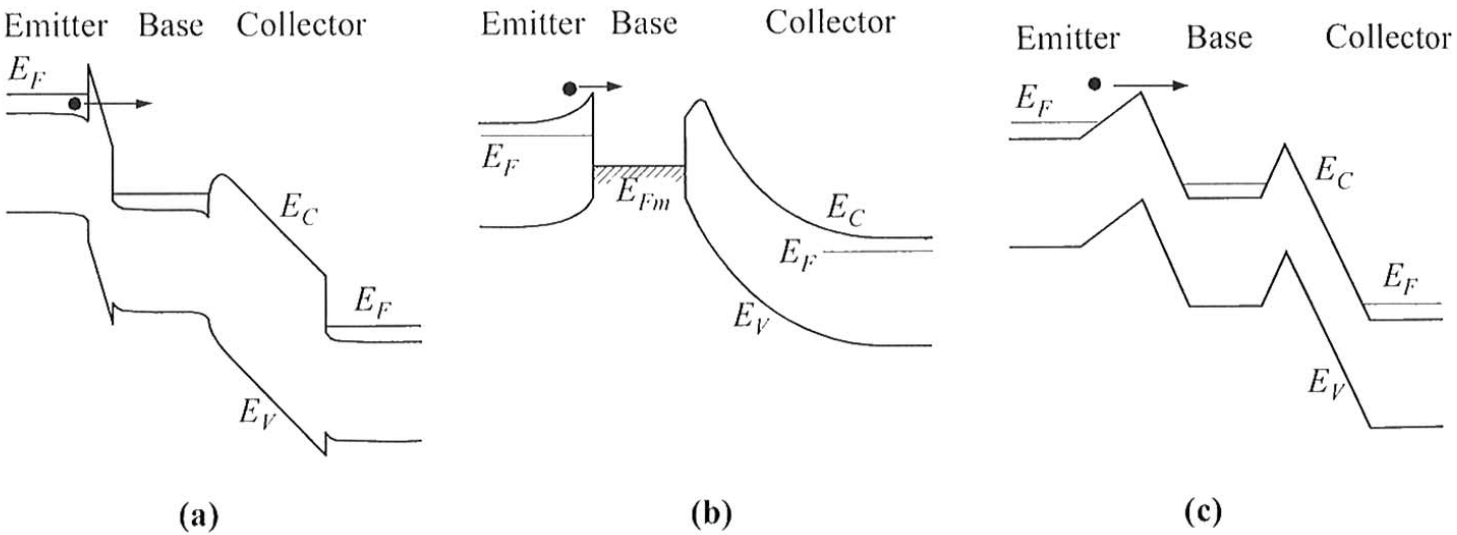
- A hot electron is an electron with energy more than a few kT above the Fermi energy
  → The electron is not in thermal equilibrium → Extra kinetic energy → higher velocity → larger current



(a) Electron group velocities as a function of energy above the conduction band.

(b) Energy-band diagram of hot-electron based on an abrupt HBT.

Hot-Electron Transistor



Other forms of hot-electron transistors. Hot electrons from: (a) tunneling through a barrier, (b) thermionic emission over a Schottky barrier, and (c) over a planar-doped barrier.

- The speed advantage of a hot-electron transistor has not been demonstrated
- It has been used as a spectrometer to study the properties of hot carriers as a function of their energy