Metal-Oxide-Semiconductor Field-Effect Transistor, Part II

Erik Fröjdh

Section 6.4-6.8 Physics of Semiconductor Devices, Sze

Mid Sweden University

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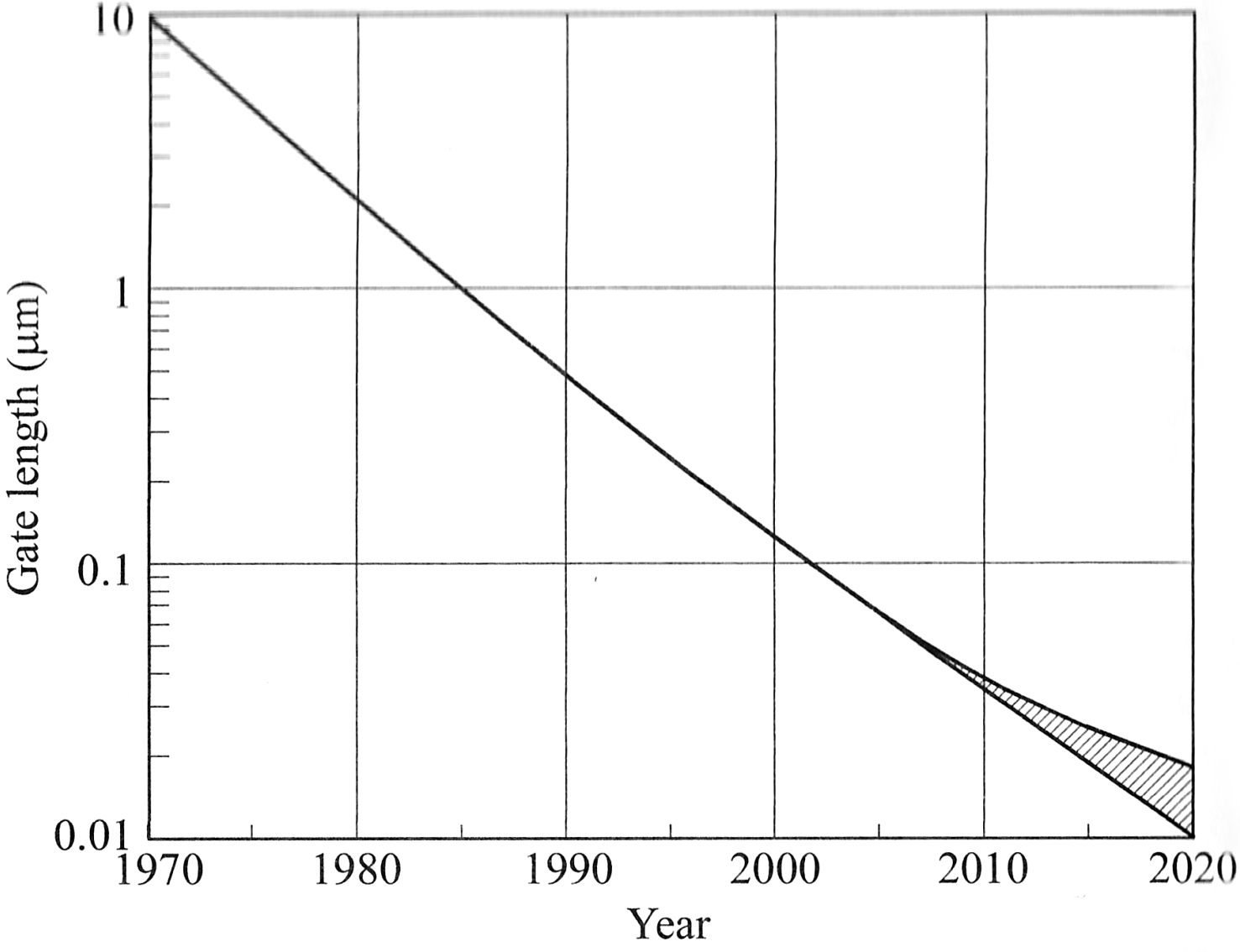
Outline

- Introduction and motivation
- Device scaling and short channel effects
- MOSFET structures
- Memory devices
- Single Electron Transistor


10
1
0.1
0.01
Gate length (μm)
1970
1980
1990
2000
2010
2020
Year

Device scaling

- Several interconnected parameters
  - Smaller channel length $\rightarrow$depletion width of source and drain causes punch through
  - Needs higher channel doping $\rightarrow$ Higher channel doping increases threshold voltage.
  - Requires thinner gate oxide.
- Production issues
- Quantum mechanical effects
  - Fundamental physical limits

Charge Sharing from Source/Drain

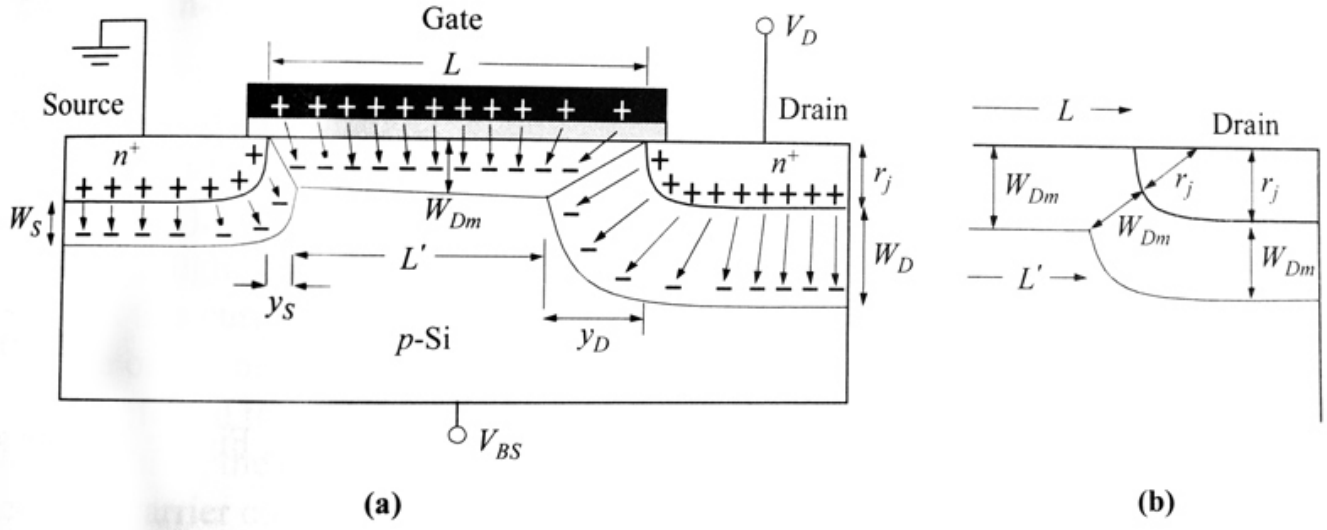


Fig. 26 Charge-conservation model for (a) $V_D > 0$, and (b) $V_D = 0$ where $W_D \approx W_S \approx W_{Dm}$. (After Ref. 47.)

- $\Delta V_T = \frac{qN_A W_{Dm} r_j}{2C_{OX} L}[(\sqrt{1 + \frac{2y_s}{r_j}} - 1) + (\sqrt{1 + \frac{2y_D}{r_j}} - 1)]$
  (Ekv 100)

Charge Sharing from Source/Drain

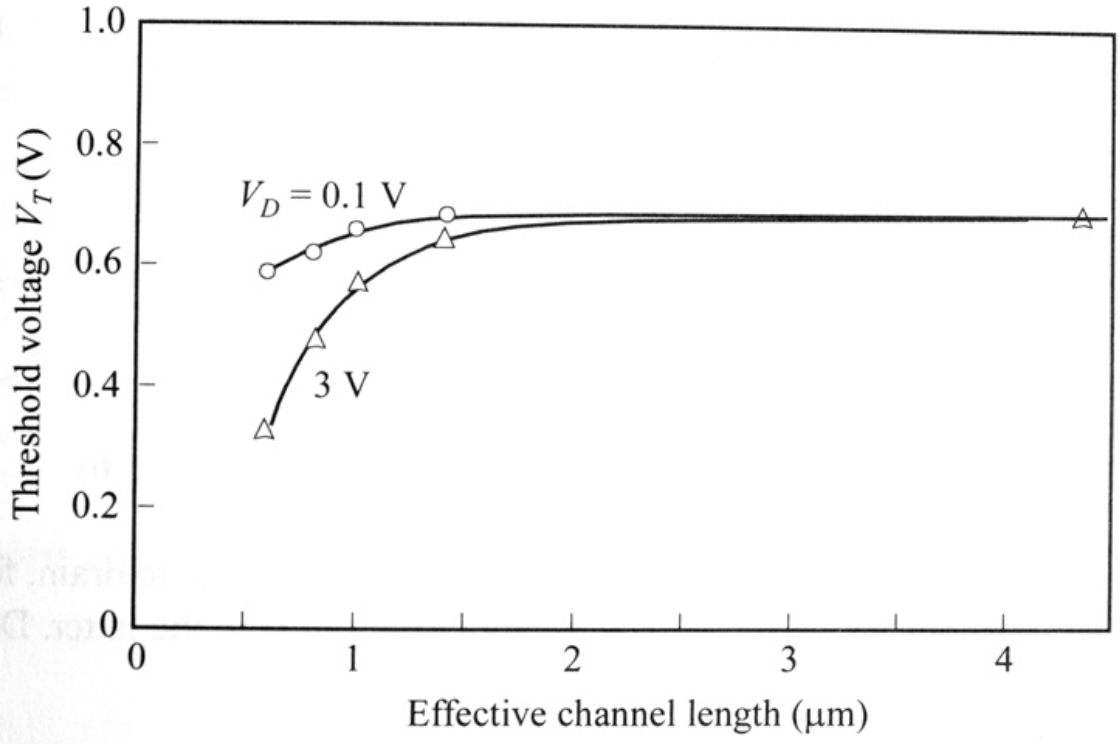


Fig. 27 Dependence of threshold voltage on channel length and drain bias. (After Ref. 49.)

Drain Induced Barrier Lowering

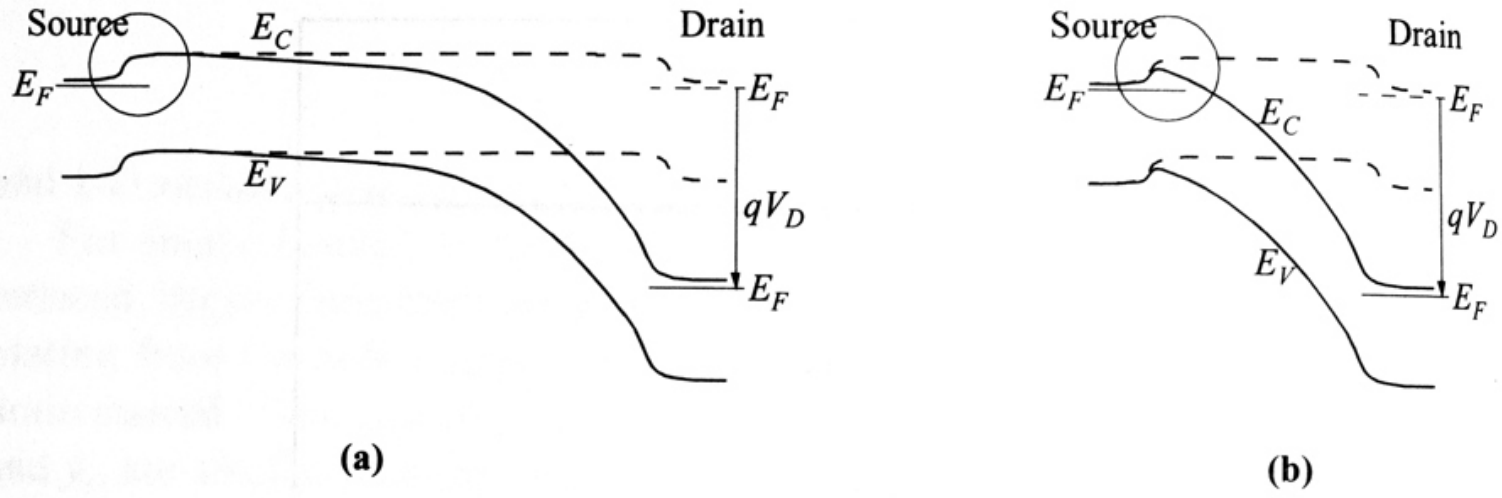


Fig. 28 Energy-band diagram at the semiconductor surface from source to drain, for (a) long-channel and (b) short-channel MOSFETs, showing the DIBL effect in the latter. Dashed lines $V_D = 0$. Solid lines $V_D > 0$.

Multiplication and oxide relaiability

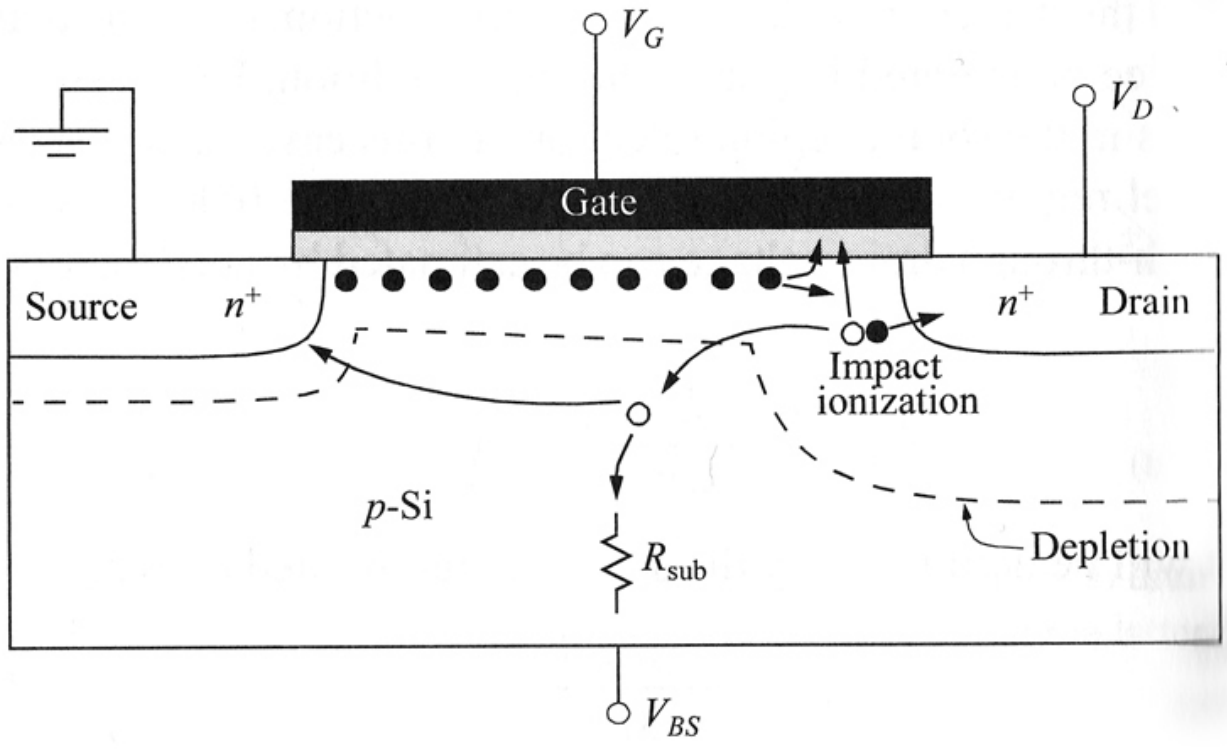


Fig. 30 Current components of a MOSFET under high fields.

Channel Doping Profile

- Peak level slightly below the semiconductor surface
- Ion implantation using several doses and energies

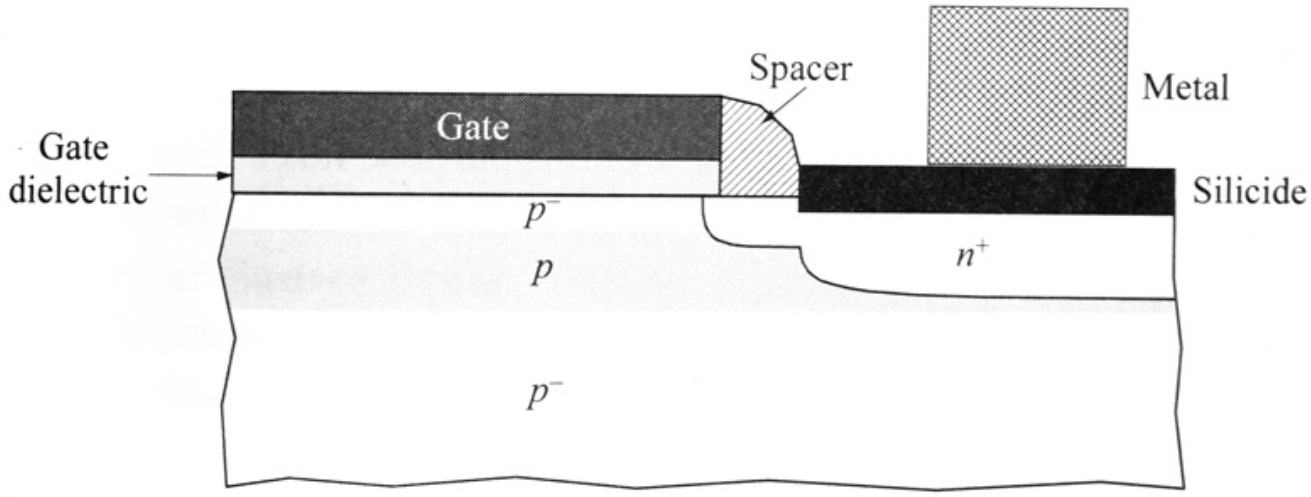


Fig. 32 High-performance MOSFET planar structure with a retrograde channel doping profile, two-step source/drain junction, and self-aligned silicide source/drain contact.

Gate Stack

- Thin gate oxides (¡2nm)
  - Controlling thickness
  - Tunneling
- Replace SiO_2 with other dielectrica
  - EOT$=t \cdot K_{SiO_2}/K$
- Al_2O_3, HFO_2, ZrO_2, Y_2O_3, La_2O_3, Ta_2O_5,
- K$=$ 9 ... 30, K_{SiO_2}=3,9
- $K_{TiO_2} \sim 80 \rightarrow EOT_2nm$=40nm

Other structures

- Schottky Barrier Source/Drain
- Raised Source/Drain
- Silicon on insulation
- Thin-Film Transistor (TFT)

Schottky Barrier Source/Drain

- pn-junction replaced by a Schotty Barrier contact
- Junction depth effectivley zero
- No need for high temperature impant.
- Possible to use semiconductors as CdS where is is difficult to form pn-junctions
- Disadvatages: High seriers resistance, Metal contacts need to be extended under gate.

Raised Source/Drain

- Minimize junction depth to control short channel effects
- Difficult to control contour and oxide thickness for submicron devices
- Oxide charging due to more hot carrier injection

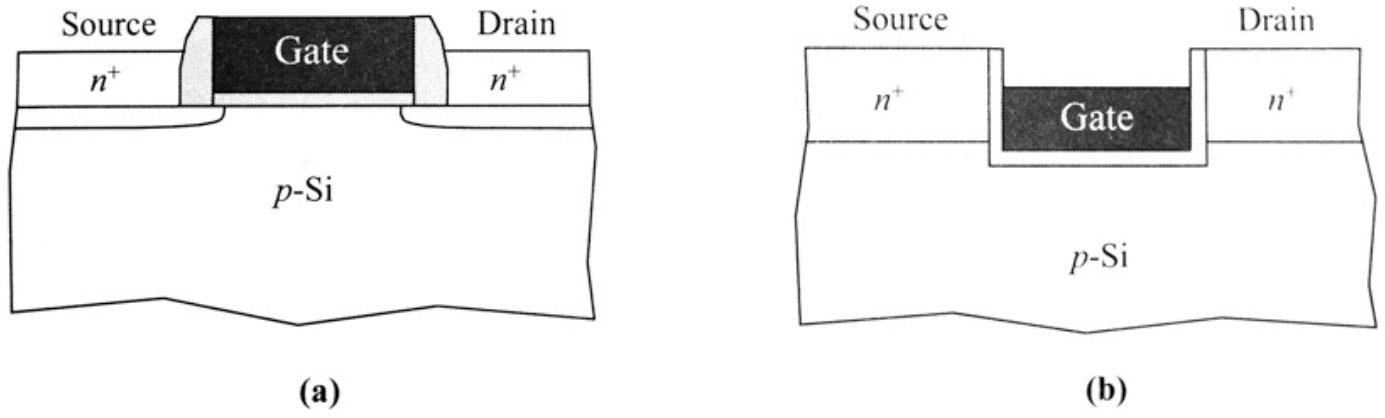
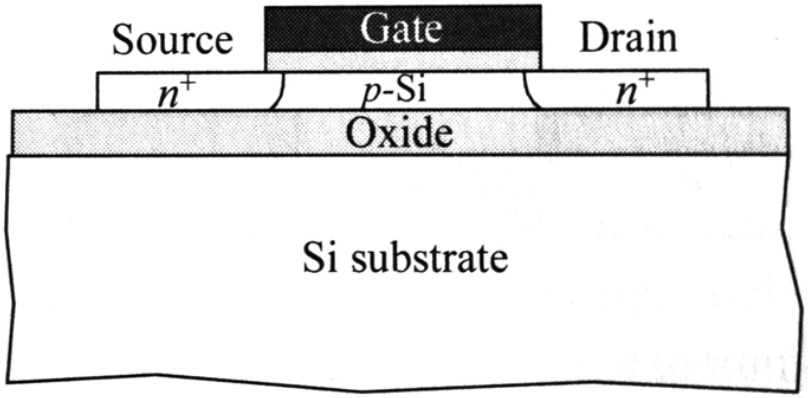


Fig. 36 Means to reduce source/drain junction depth and series resistance. (a) Raised source/drain. (b) Recessed channel.

Silicon on Insulator (SOI)

- Normaly silicon on silicon-oxide
- Thin body removes most of the problems with punch through. Allows channel to be doped more lightly.
- Device insulation possible by removing surrounding thin film.



(a)

Fig. 37 (a) Typical structure of MOSFET on SOI (After Ref. 66.)

Thin-Film Transistor (TFT)

- Similar structure to SOI but with a deposited amorphous thin film.
- More defects than single crystal semiconductors
- Limited current due to low mobility.
- Main application is for large area or flexible substrate is needed.

Memory Devices

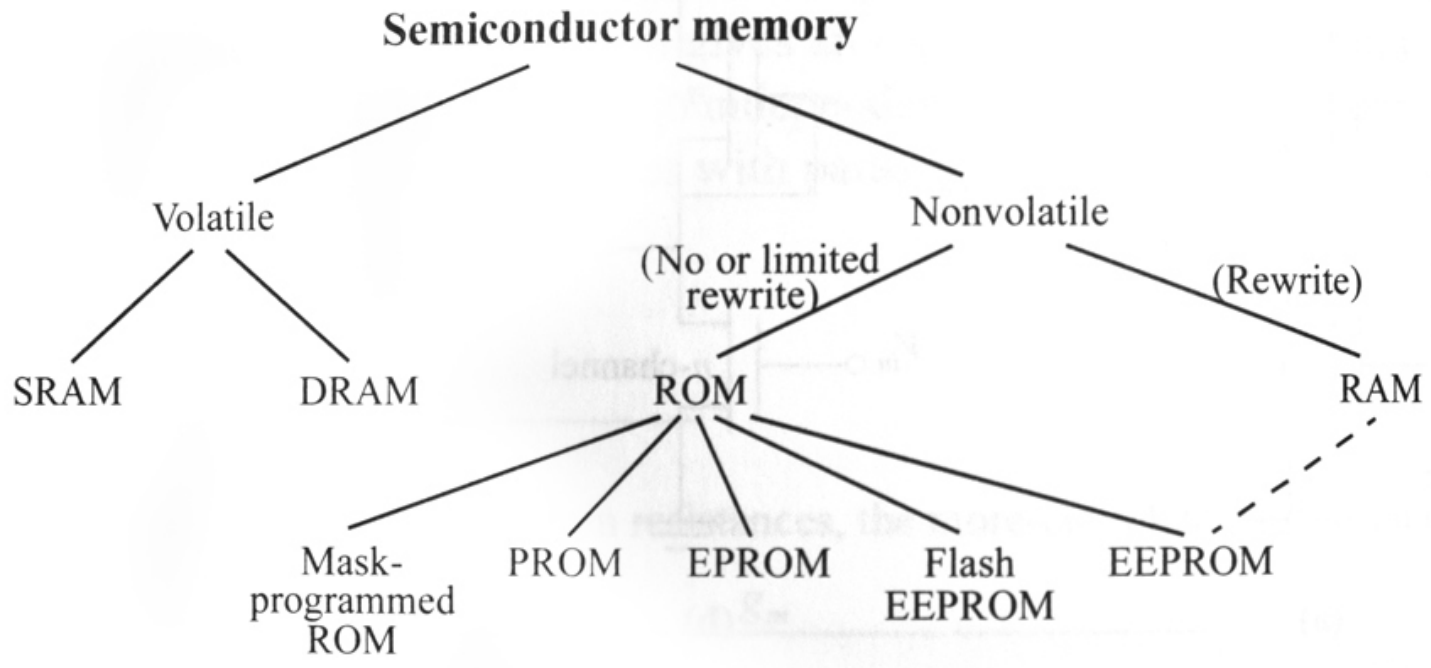


Fig. 43 Classification of semiconductor memories.

Floating Gate Devices

- Programmed by hot-carrier injection or Fowler-Nordheim tunneling
- $t_R = \frac{ln(2)}{v \cdot exp(q\phi_B/kT)}$ Eq 122

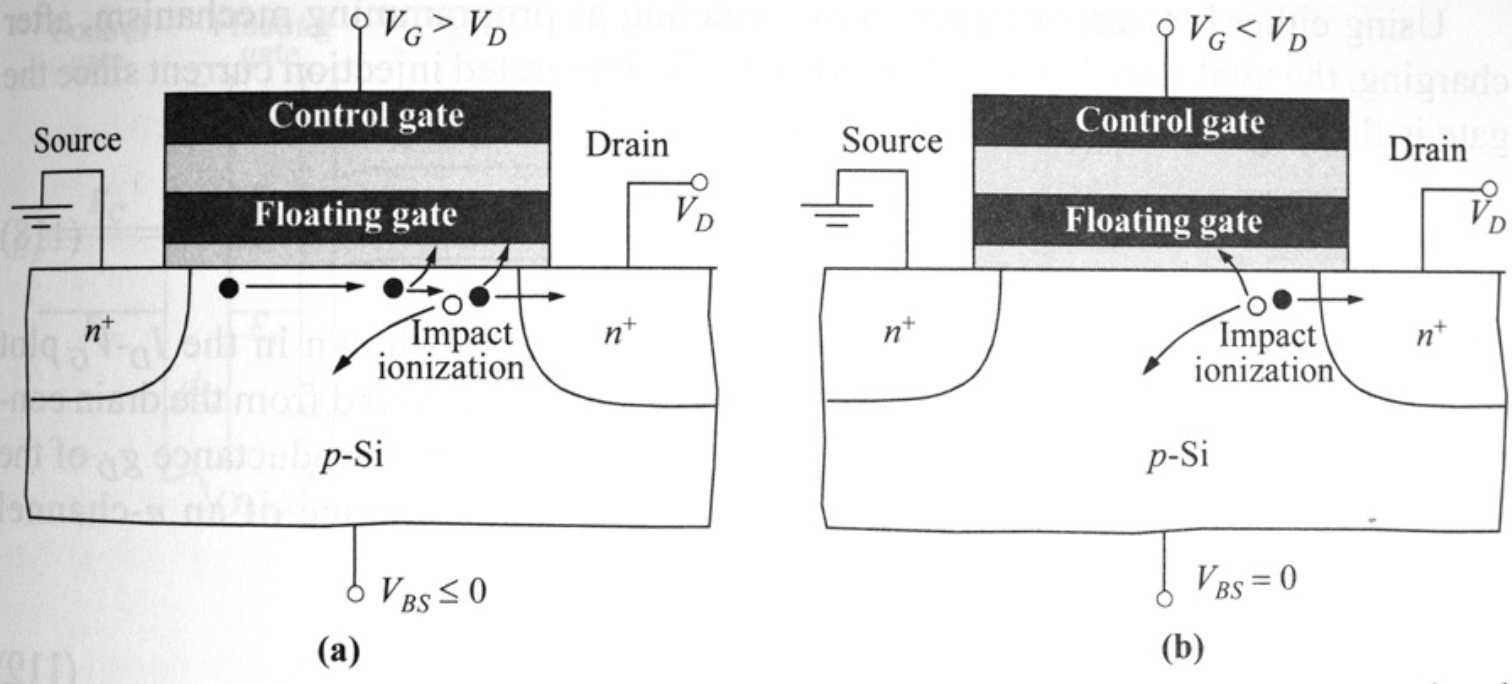


Fig. 45 Charging of the floating gate by hot carriers. (a) Hot electrons from channel and impact ionization. (b) Hot holes from drain avalanche. Note difference in gate bias between the two figures.

Floating Gate Devices

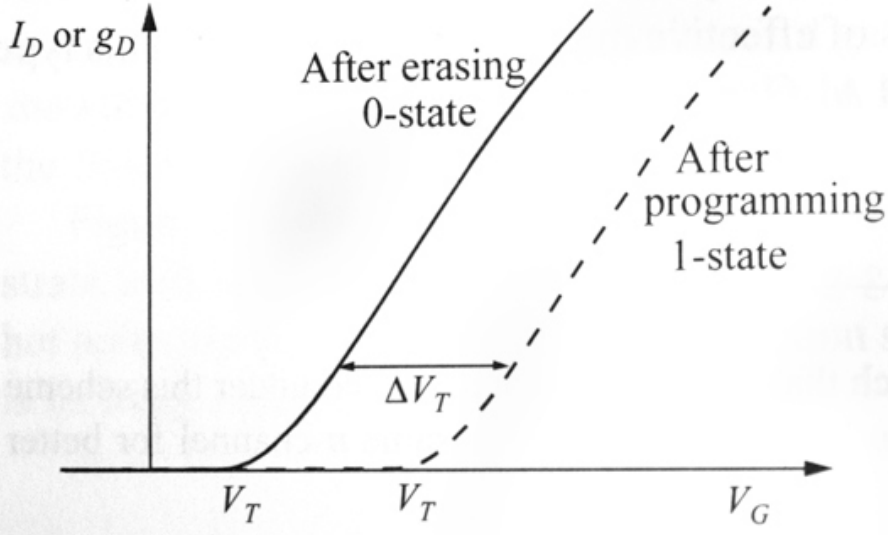


Fig. 46 Drain-current characteristics of a stacked-gate *n*-channel memory transistor, showing the change of threshold voltage after erasing and programming.

Floating Gate Devices

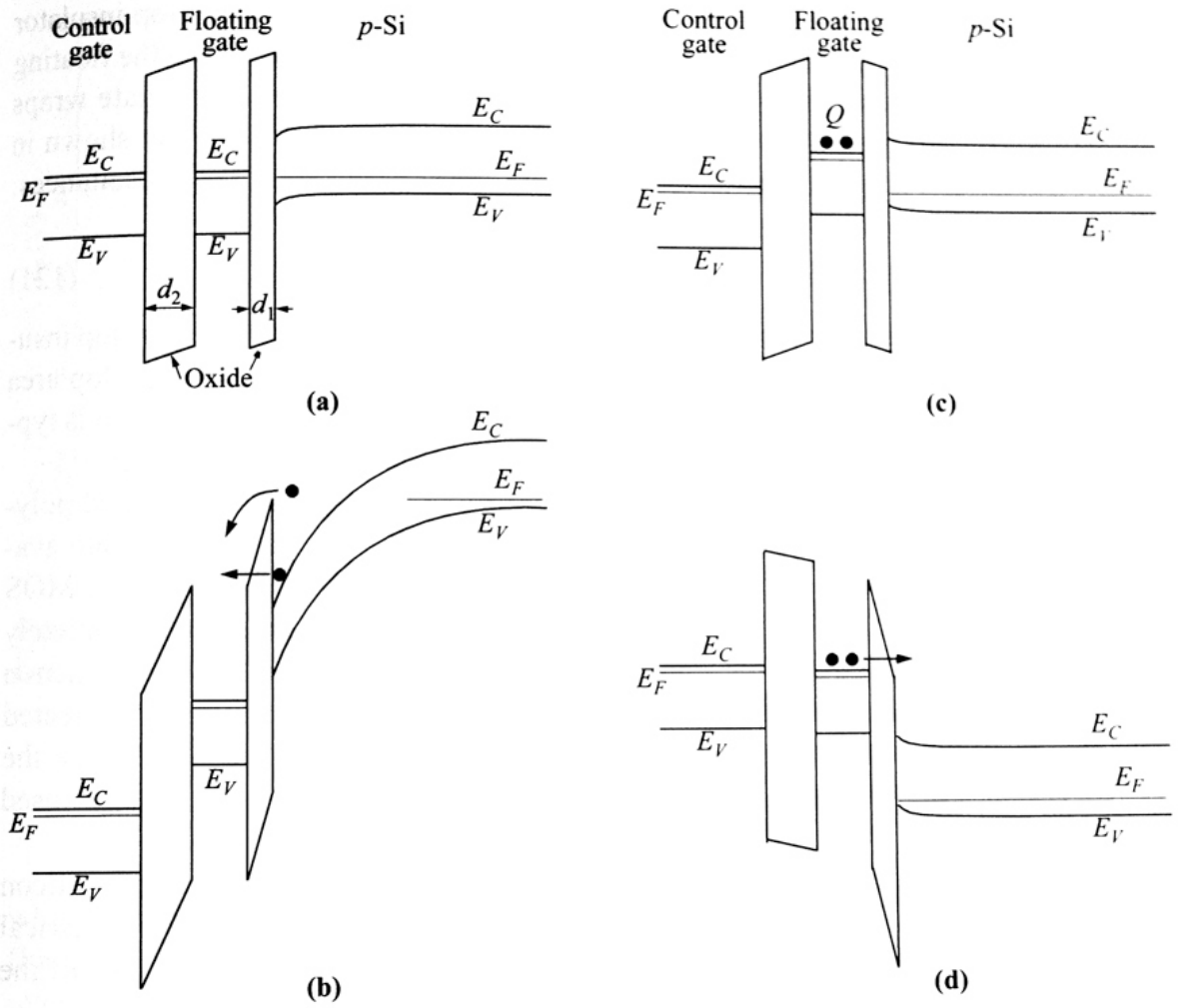


Fig. 47 Energy-band diagrams for a stacked-gate memory transistor at different stages of operation. (a) Initial stage. (b) Charging by hot electrons or electron tunneling. (c) After charging, the floating-gate having charge Q (negative) is at higher potential and V_T is increased. (d) Erasing by electron tunneling.

Charge Trapping Devices

- Metal nitride oxide silicon transistor (MNOS)
- Silicon Nitride layer used to trap charge
- Programming speed largley affected by oxide thickness
- Radiation hard
-

Charge Trapping Devices

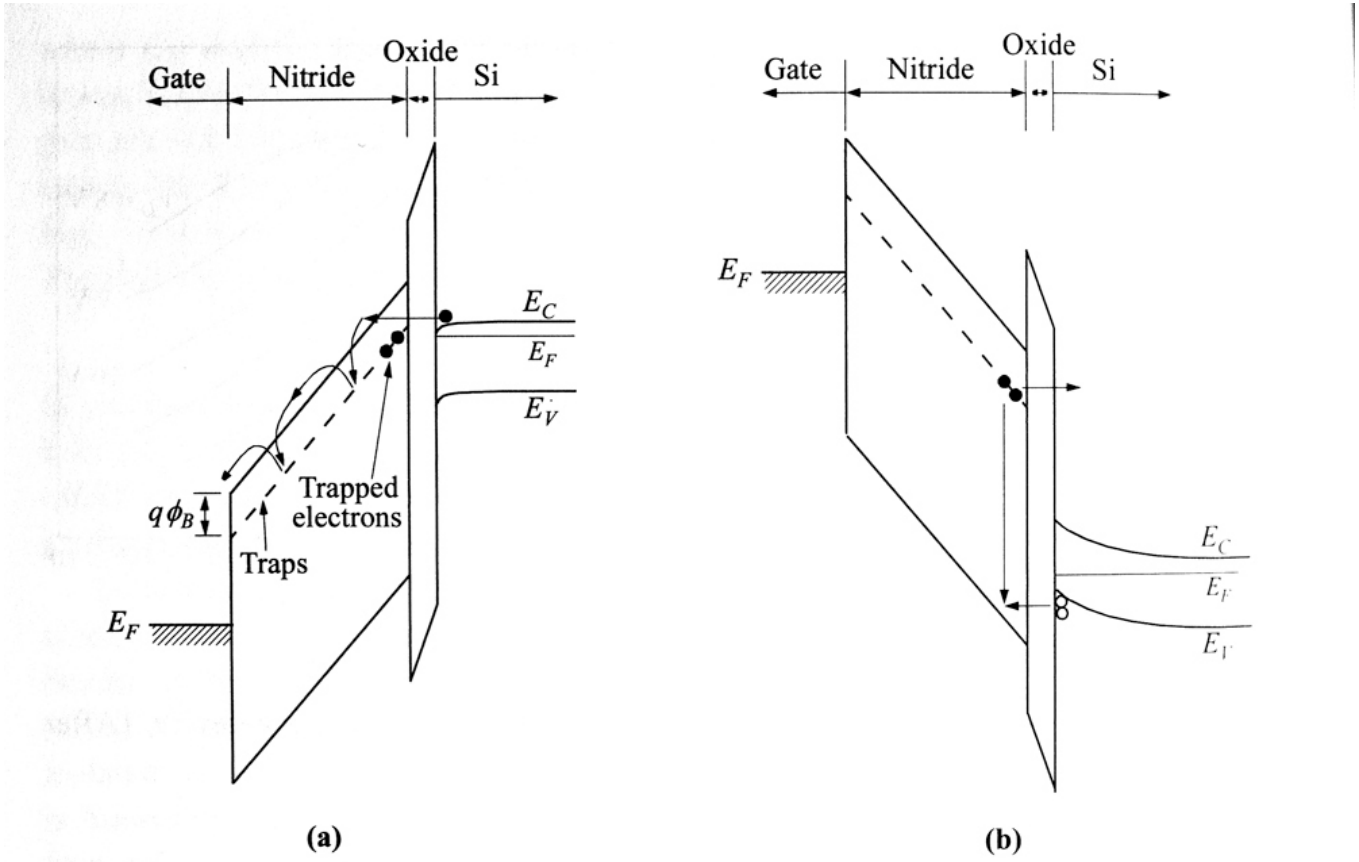
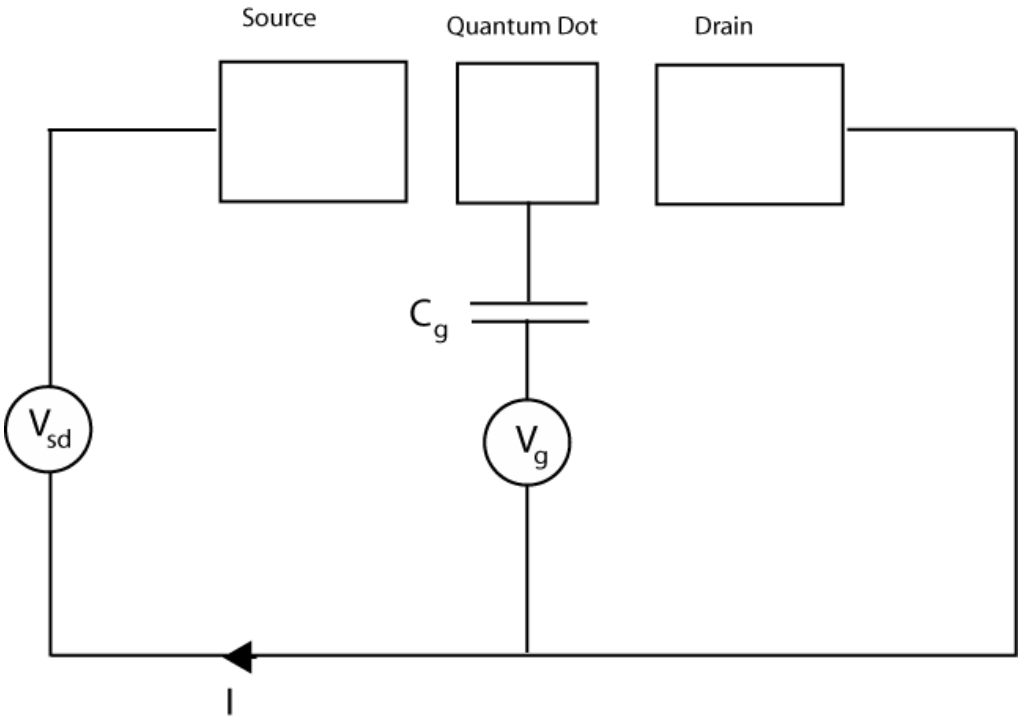


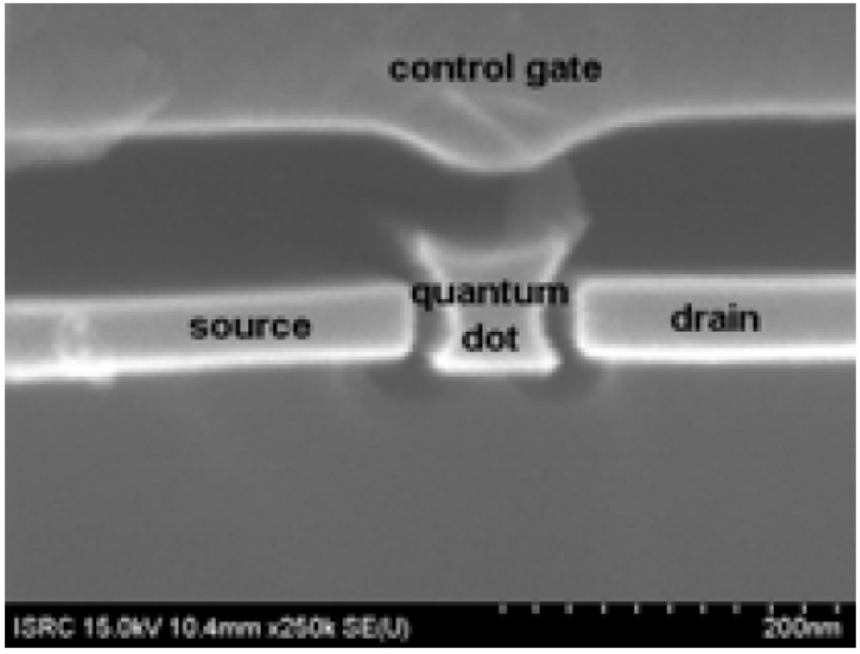
Fig. 51 Rewriting of MNOS memory. (a) Programming: electrons tunnel through oxide and are trapped in the nitride. (b) Erasing: holes tunnel through oxide to neutralize the trapped electrons, and tunneling of trapped electrons.

Single Electron Transistor (SET)



- $V = \frac{e}{2C_{dot}}$
- $E_C = \frac{e^2}{C_{dot}} >> k_B T$
- $R_t >> \frac{h}{e^1}$

SET Operation



SEM image of a SET [1]

- $E_C \sim 100 k_B T$
- Voltage Logic
  - Power dissipation $10^{-7} W/transistor$ $\rightarrow 10\text{kW/cm}^2$!
- Charge State Logic