Flip Chip on FPC

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Small form-factor and additional functionality are increasingly important for the increased penetration of information devices such as mobile phones and portable computers. As a result, the use of high density component assembly technology is important to maximize component assembly on a minimum amount of circuit board area. Flip-chip (F/C) bonding technology is commonly used, not only for capacitors and resistors, but also for 'bare die' IC's directly attached to PCBs.

Fujikura has established the design and manufacturing technology for high-density circuits with flat planar topography to improve the assembly process. We have developed a new flexible printed circuit (FPC) that is suitable for F/C technology, including ACF bonding techniques. Flip-chip on FPC will contribute to the required form-factor reductions with increased functionality of electronic devices.

1. Introduction

According to small form-factor and additional functionality of today's electronic devices, it is required to increase the density of component assembly on printed circuit boards. Based on this requirement, the assembly form of semiconductor devices is changing from the packaged IC molded by resin, e.g. QFP (quad flat package), BGA (ball grid array), to bare die bonding directly assembled on to a substrate. Within Fujikura, we have established in mass production COF (chip-on-film) assembly technology that assembles the IC bare die onto FPC (flexible printed circuit) by W/B (wire bonding). However, in response to the current requirements of reduced space (where W/B method is impossible), increased IC pin numbers and faster assembly, we paid close attention to F/C (flip-chip) assembly and have developed the F/C assembly technology onto FPC. F/C assembly on FPC with the advantages of being thin, light weight and flexible, is an essential technology for applications that require a smaller form-factor and additional functionality, e.g. HDD, camera, video camcorder, etc.

2. Outline of F/C Assembly

F/C assembly technology has the following merits when compared to conventional technology.

(1) Elimination of the fan-out area from IC die pads by mold package or W/B with the result that the assembly area can be reduced to 10~30% compared with QFP.

(2) Signal transmission paths are reduced to a minimum and the parasitic capacitance is eliminated, which may be generated by Au wire loop, resulting in reduced noise and cross-talk of the IC when operated by a high-speed clock frequency.

(3) High tact-up of assembling will be expected due to the gang bonding between the IC and substrate compare with wire bonding depends on pin number.

But on the other hand, assembled substrate is required that fine pitch circuit which is the same as the I/O terminal pitch of IC die, furthermore, it is required that high-density circuit patterning, high coplanarity enough to gang bonding. To achieve F/C assembly many methods have been proposed including C4 (Controlled Collapse Chip Connection)[1] using solder bump, SBB (Stud Bump Bonding)[2] using Au bump and conductive resin. However, ACF (Anisotropic Conductive Film) [3] has been selected as it is appropriate for fine pitch circuitry and high productivity. ACF consists of an epoxy resin (binder) and conductive particles (filler) whose diameter is approximately several micrometers, which are dispersed in the binder. The common types of conductive particles used are metal (Ni, Ag) or a resin ball plated by Ni/Au.

The process flow of the ACF method of F/C assembly is shown in Fig. 1 The hardened ACF takes up conductivity, insulation and adhesion which are inserted between die and substrate (Fig. 2).

3. Evaluation of F/C Assembly

3.1 F/C Assembly on FPC

For the F/C assembly onto FPC, the following are required:

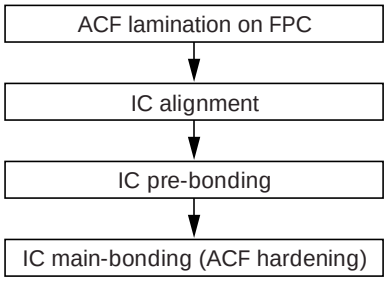


Fig. 1. Manufacturing Flow of ACF Method (F/C bonding).

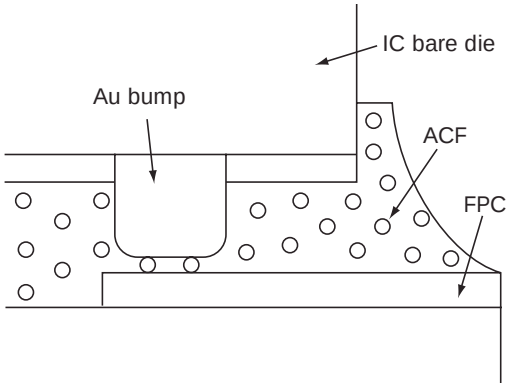


Fig. 2. Cross Sectional View of F/C bonding by ACF.

(1) Fine pitch and high-density circuit patterning FPC corresponding to the I/O terminal pitch of the IC
(2) Co-planarity of bump height for the electric connection
(3) Co-planarity of bump connection area (bonding pad) of the FPC

As a result a test element grid (TEG) with a minimum pitch 120μm (line/space=80/40) was produced, and we confirmed technical points. Fig. 3 shows our TEG pattern where we can measure the conductivity and insulation resistance between adjacent terminals. The main specification of TEG is shown in Table 1.

3.1.1 FPC Substrate

For F/C connection the aim of circuit formation is not only to achieve a finer pitch but also to achieve a wider top of the FPC conductor with high accuracy. Usually the FPC circuit is formed by the subtractive method which is influenced by the etch factor, therefore the cross-section of the circuit is trapezoidal with the base as its widest point. For F/C assembly, it is important to produce a circuit that has enough insulation resistance between adjacent circuits, a fine circuit pitch and a conductor with a wide top, i.e. produce a trapezoid with a small aspect ratio (degrees). Therefore, we produced a circuit with a minimum pitch of 120μm using new materials and manufacturing equipment compatible to fine pitch circuit production. A metal stiffener was attached to the reverse side so as to avoid curvature of the substrate thereby achieving co-planarity and size stability.

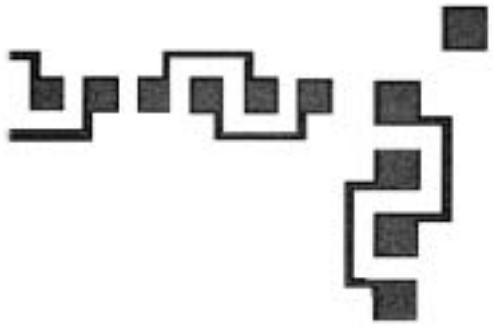


Fig. 3. Circuit Pattern of TEG Die.

Table 1. Specification of TEG

Assembled substrate	Au plated FPC
Conductor thickness	18μm
Terminal pitch	120μm [L/S=80/40]
Bump material	Au
Bump diameter	80μm
Bump height	50μm

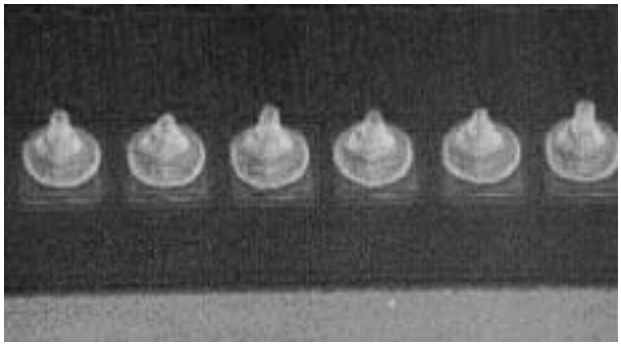


Fig. 4. SEM Image of Gold Stud Bump (×150).

3.1.2 Bump Forming

The bumps, which become the connector, formed stud bump using wire bonder.

The method used is to form an Au ball by arc discharge on the tip of an Au wire like W/B, the Au ball is then bonded on an Al pad of the IC chip metallically by heat and ultrasonic and finally the wire tip is cut and bump surface is leveled to the same height. As the deviation of this bump height and volume is related to the reliability of the electrical and mechanical connection, it is important to form a bump with uniform shape at all terminals. We researched the condition of bump formation with the correct height, which can absorb co-planarity of FPC, and having the required adhesive properties without peeling out of the IC pads. A SEM photograph of an Au stud bump (approximately 80μm diameter and 50μm height) is shown in Fig. 4 and the deviation of the bump share strength is shown in Fig. 5.

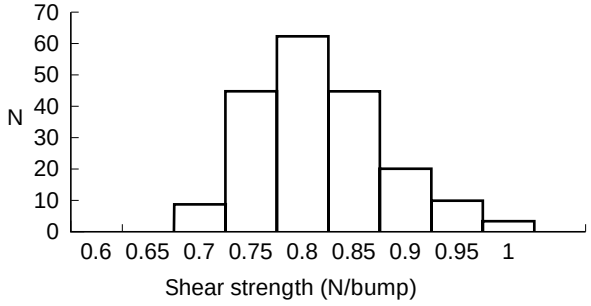
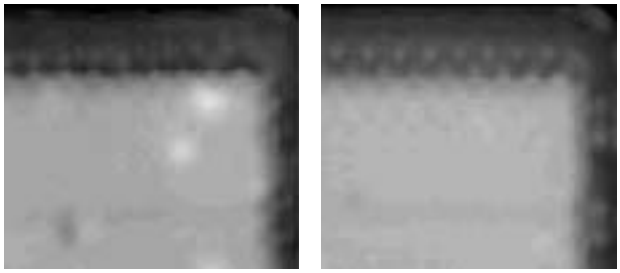


Fig. 5. Deviation of Shear Strength of Gold Stud Bump.



(a) Including void (NG) (b) Void-less (Good)

Fig. 6. Scanning Acoustic Tomograph Image of Voids in ACF.

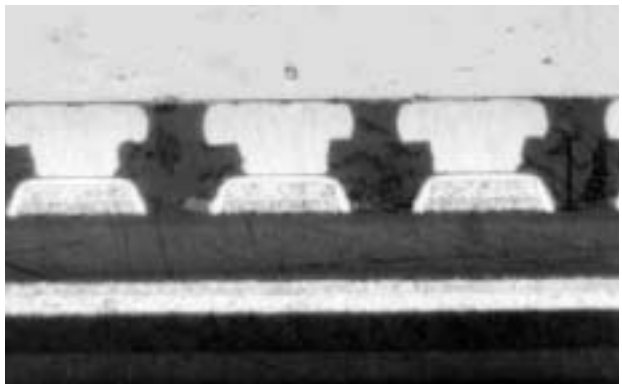


Fig. 7. Cross Sectional Photograph of F/C Connection.

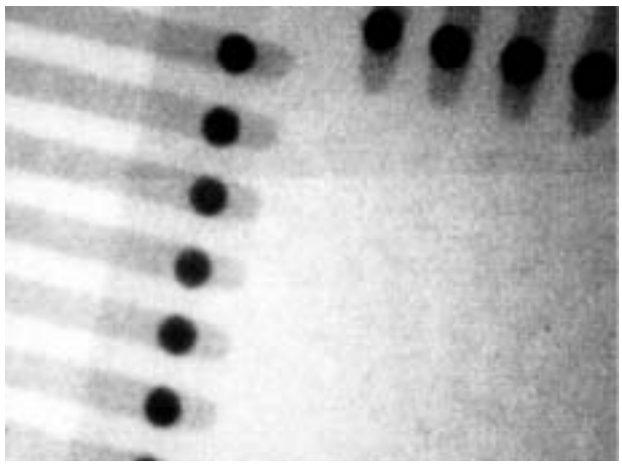


Fig. 8. X-ray Image of F/C Connection.

3.2 Assembly Condition

ACF is a heat-hardening material and has been selected due to the excellent adhesive properties with polyimide, the base material of FPCs. It is necessary to determine the condition of ACF hardening as voids (air bubbles), as shown in Fig. 6, or peeling off at the die-ACF boundary can occur resulting in an inferior product due to humidity absorption. Another critical element is the bonding pressure. If the pressure is too high, the FPC's electrode is deformed and an open circuit occurs or the die-edge contacts with the FPC's electrode resulting in a short circuit. The correct conditions were determined to absorb deviation of bump height. A cross-sectional photograph of the bump bonding part under the appropriate assembly condition is shown in Fig. 7 and an X-ray photograph is shown in Fig. 8.

3.3 Reliability Test

The F/C assembly using the ACF method was subjected to 3 areas of stress to determine the reliability of the assembly. The test conditions for the reliability test are shown in Table 2. All tests were passed; no problems were found.

Table 2. Condition of Reliability Test

Heat schock test	–40/125°C, 30min/30min
Migration test	85°C, 85%RH, 5V
Pressure cooker test	121°C, 2atm, 95%RH

3.3.1 Heat Shock Test

In this method, the bonding is took up by gluing of among organic materials and there is concern that there may be poor adhesion between the ACF resin and FPC substrate when subjected to thermal stress due to repeated expansion and shrinkage. After 1,000 cycles in the condition of the general semiconductor device, we are able to confirm sufficient durability based on the increase in conductive resistance of approximately 10% as shown in Fig. 9.

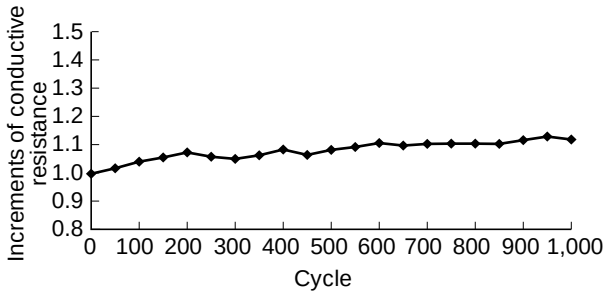


Fig. 9. Result of Heat Shock Test.

3.3.2 Migration Test

In ACF the conductive particle is dispersed within the insulation resin and migration of the conductive filler in ACF may occur with a bias voltage. The test results of an in-situ measurement by 100V bias voltage are shown in Fig. 10. Using 40μm of minimum gaps, the minimum insulation resistance was $1\times10^{8}\Omega$ after 1,000 hours, confirming the general durability.

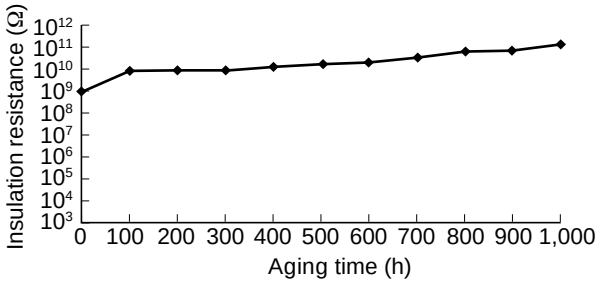


Fig. 10. Result of High Temperature High Humidity Bias Test.

3.3.3 Pressure Cooker Test (PCT)

In PCT, which is an accelerated degradation test, it is to determine the destruction of the electric connection by absorption and degradation of resin under the high pressure, high temperature and high humidity. We tested to 200 hours under the conditions shown in Table 2, but no failures were detected in any of the samples, confirming the durability. However, we can confirm that the sample of the hardening worse ACF or including void such as Fig. 6 results in an open circuit after less than 100 hours.

4. Sample Making by Functional IC

Production of samples using actual IC dies based on the results of TEG.

4.1 IC Assembly for LCD (Liquid Crystal Display) Driver

An LCD driver IC is assembled using stud bump in the same way as the TEG, with F/C assembly using the ACF method. For FPC, to realize W-side FPC patterning with high density and fine pitch circuit forming, a special thin w-side copper foil is used with laser via hole and thin copper plating. The cross-sectional photograph is shown in Fig. 11. To keep the co-planarity of the assembling area, an Al stiffener is located on the reverse side, and moreover capacitors and resistors are assembled as shown in Fig. 12. We are able to confirm that it is possible for the LCD to illuminate.

5. Technical Problem in the Future

In this time, we are able to confirm the practicality of F/C assembling on FPC with ICs of low voltage and low current driving, e.g. LCD. However, in the future it appears that the die's internal frequency will increase to several GHz, therefore it becomes more important to consider the heat dispersion property from internal dies with high voltage, high current driving. In case of F/C assembly, most of the heat occurs from the reverse side of the die, where is exposed to air, so it is important that the characteristic of radiation from there. We think the radiation structure and understand further the characteristics

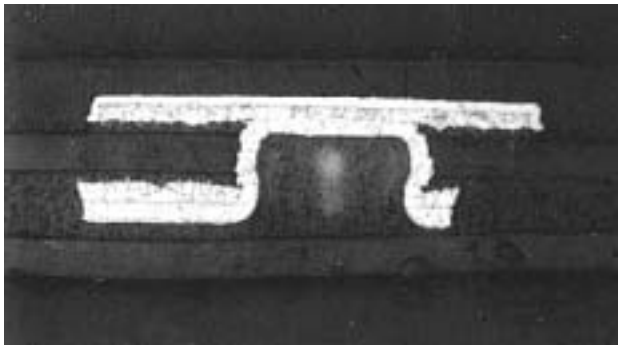


Fig. 11. Cross Sectional Photograph of Laser Via Hole Connection.

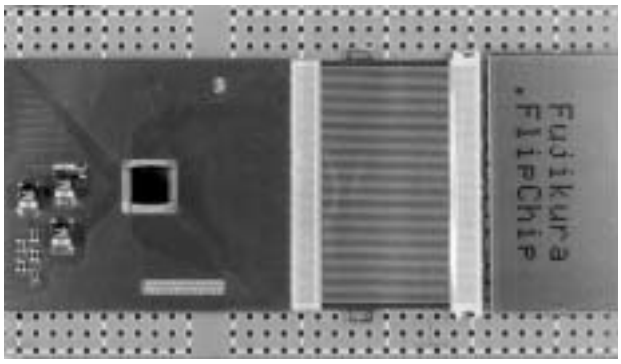


Fig. 12. F/C Assembling Module Sample (Liquid Crystal Display Panel).

of the organic material such as the ACF resin and also the FPC substrate when subjected high temperature, we need to expand the applications.

6. Conclusion

We have developed F/C assembly using the ACF method on FPC which become thin, light weight and flexible and we have established fine circuit production technology corresponding to the I/O pitch of the IC. We are able to confirm that it is possible to maintain its assembly position on the substrate with no curve, expansion and shrinkage, and possible to assemble with an electrically connection. Also, we have confirmed that it clears a general environment test (heat shock test, high temperature and high humidity bias test, PCT test). In the future, we plan to put an emphasis on the characteristic based on conditions of the electronic equipment applications.

References

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