Fundamental of IC assembly

Chapter 9
Outline

• IC assembly technologies (Ch. 9)
  – Wire bonding (WB)
  – Tape automated bonding (TAB)
  – Flip chip (FC) processing
Remember the . . .
What is IC assembly?

IC assembly is the first step (after wafer singulation into individual die) enabling the IC to be packaged, involving:

1. Metallurgical bonding to IC bond pad (Al);
2. Metallurgical bonding to package bond pad;
3. Electrical connection between these two.
IC assembly requirements

The IC assembly method should provide the following:

- Acceptable electrical properties, including capacitance resistance and inductance.
- Low cost manufacturing solutions
- High through-put manufacturing capability
- High reliability
- Repairability or replaceability
Chip to Package
Interconnection Techniques

**Wirebond**
- Epoxy
- Active face
- Adhesive
- Wire
- Pad
- CHIP

**TAB**
- Inner Lead Bond Encapsulation
- TAB Beam Lead
- Active Face
- Bumps
- UNDERFILL
- CHIP

**Flip Chip**
- Active Face
- UNDERFILL
- CHIP

**Two options:**
- Ball bonding
- Wedge bonding

**Two options:**
- Face up chip
- Face down chip

**Three options:**
- Metallurgical bond
- Metallurgical and adhesive bond
- Adhesive bond
IC interconnection technologies

• Wire Bonding
  – The chip is attached to the substrate with the bonding pads facing away from the substrate.
  – Connecting wires (bond wires) made of Au or Al are then attached by welding on the chip pads, pulled to the substrate pads and again attached by welding.

• Tape Automated Bonding
  – The chip is attached to a polyimide tape prepared with Cu conductors.
  – The Cu wires are attached to the pre-bumped chip by thermo-compression bonding.

• Flip Chip
  – The chip is placed upside down on the substrate, which have the same pattern as the chip.
  – This technique requires the formation of bumps onto the chip pads (solder alloy balls, copper bumps, adhesives).
Wire bonding
Wire bonding

Thermosonic gold ball bonding is currently the most widely used bonding technique, primarily because it is faster than ultrasonic aluminum bonding.

Chip interconnection using wirebonding technology (courtesy of Saab Microwave Systems AB).
Wire bonding

- **Ball bonding**
  - 95% of all wire bonding
  - Wire: normally Au
  - Controlled capillary bonding force <100g
  - Thermosonic welding technique:
    - Moderate temperatures 150-200°C
    - Ultrasonic excitation (capillary and wire) 60-120KHz
  - Full bond cycle can be <20 ms per bond
  - Round capillary bonding tool (major advantage)

- **Wedge bonding**
  - Finest pitch bonding capabilities
  - Higher yield compared to ball bonding
  - Wire: normally Al
  - Controlled wedge bonding force
  - Thermosonic welding technique:
    - Moderate wire temperature (for Au, 125-150°C)
    - Ultrasonic excitation (capillary and wire) 60-120KHz
  - Full bond cycle can be <80 ms per bond
Thermosonic Ball Bonding Process
## Wire bonding: bond shape

**Ball bond (after APROVA Bonding tool).**

**Wedge bond (after K&S Micro-Swiss).**

<table>
<thead>
<tr>
<th>Wire bonding</th>
<th>Bonding technique</th>
<th>Bonding tool</th>
<th>Wire</th>
<th>Pad</th>
<th>Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ball bond</td>
<td>Thermo compression, T/C</td>
<td>Capillar</td>
<td>Au</td>
<td>Al, Au</td>
<td>10 wires/sec</td>
</tr>
<tr>
<td></td>
<td>Thermosonic, T/S</td>
<td></td>
<td></td>
<td></td>
<td>(T/S)</td>
</tr>
<tr>
<td>Wedge bond</td>
<td>Thermosonic, T/S</td>
<td>Wedge</td>
<td>Au, Al</td>
<td>Al, Au</td>
<td>4 wires/sec</td>
</tr>
<tr>
<td></td>
<td>Ultrasonic, U/S</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</table>
Wire bonding

Wire bonding is an electrical interconnection technique using thin wire and a combination of heat, pressure and/or ultrasonic energy.

<table>
<thead>
<tr>
<th>Wire bonding</th>
<th>Pressure</th>
<th>Temperature [°C]</th>
<th>Ultrasonic energy</th>
<th>Wire</th>
<th>Pad</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermo-compression</td>
<td>High</td>
<td>300-500</td>
<td>No</td>
<td>Au</td>
<td>Al, Au</td>
</tr>
<tr>
<td>Ultrasonic</td>
<td>Low</td>
<td>25</td>
<td>Yes</td>
<td>Au, Al</td>
<td>Al, Au</td>
</tr>
<tr>
<td>Thermosonic</td>
<td>Low</td>
<td>100-150</td>
<td>Yes</td>
<td>Au</td>
<td>Al, Au</td>
</tr>
</tbody>
</table>

Once the ball bond is made on the device, the wire may be moved in any direction without stress on the wire, which greatly facilitates automatic wire bonding, as the movement need only be in the $x$ and $y$ directions.
Wire bonding: cost

• *The main cost of wire bonding method includes:*
  – Wire bonder.
  – Die attach equipment.
  – Support equipment, such as wire pull and shear stations, plasma etchers, as well as storage facilities.
  – Materials including tool, wire, die attach materials.
  – Engineering.

• *Wire bonding is a low cost process since:*
  – No chip modification is needed.
  – Equipment has an established base of competitive development.
Wire bonding: advantages

- Highly flexible process
- Low defect rates (high yield)
- High reliability interconnection structures
- Very large infrastructure
- Rapid advances in equipment, tools and materials technology
Wire bonding: disadvantages

• For the application of wire bonding method, *terminals of chips have to be arranged at the periphery of the chips*,
  – =>difficult for high I/O (>500) interconnections.

• *Large bonding pads* (~100 µm) and large bonding pitch in (~200 µm),

• Requires *relatively large quantities of Au*,

• Low production rate (point-to-point processing),

• Relatively poor electrical performance (*long chip-to-package interconnection lengths*)

• Variations in bond geometry,

• Robustness and reliability problems brought about by environmental conditions.
Tape Automated Bonding

TAB
Tape Automated bonding (TAB)

*TAB is an approach to (very) fine pitch interconnection of a chip to a lead-frame*

Tape-automated bonded die with a bare chip placed on the tape and connected to an interconnection pattern (Courtesy of Westinghouse ESG).
Typical TAB Process

a) Inner Lead Bonding

b) Outer Lead Bonding
Typical TAB Fabrication Process

1. Wafer Bumping
2. Wafer Dicing
3. Fabricate Tape (Multi-Layer)
4. Align Chip and Tape
5. Inner Lead Bonding
6. Testing
7. Encapsulation
8. Singulation
9. Test/Burn-in
10. Lead Forming
11. Outer Lead Bonding

Diagram details:
- Polymer Tape
- Outer Lead Bonding Leads
- Test Pads
- Circuit Traces
- Sprocket Holes for Fixturing and Automation
- Inner Lead Bonding to Chip I/O Pad
TAB: some advantages

- smaller **bonding pad** and **pitch** compared to wire bonding technology,
- decrease in the quantity of gold used for bonding,
- reduction of variations in bond geometry,
- increase in production rate because of area or `gang' bonding,
- improved electrical performance (noise and frequency),
- lower labor costs (more automatic),
- higher I/O counts (up to 1000),
- lighter weight,
- greater densities are achievable,
- the chip can be attached in a face-up or face-down configuration.
TAB: some disadvantages

- Process inflexibility
  - due to hard tooling requirements.

- Relatively little production infrastructure,

- Large capital equipment investment required,

- Time and cost of designing and fabricating the tape,
  - each die must have its own tape patterned for its bonding configuration.

- Limited to high-volume production applications.
Flip chip
Flip Chip Interconnect System
Advantages of Flip Chip

1. **Smaller size and more I/Os**: Smaller IC footprint, reduced height and weight.
2. **Improved performance**: Short interconnect delivers reduced signal inductance, resistance and capacitance, small electrical delays, good high frequency characteristics, thermal path from the back side of the die.
3. **Improved reliability**: Epoxy underfill in large chips ensures high reliability.
4. **Improved thermal capabilities**: Because flip chips are not encapsulated, the back side of the chip can be used for efficient cooling.
5. **Low cost**: Batch bumping process, cost of bumping decreases, cost reductions in the underfill-process.
Disadvantages of Flip Chip

1. Difficult testing of bare dies.
2. Limited availability of bumped chips.
3. Challenge for PCB technology as pitches become very fine and bump counts are high.
4. For inspection of hidden joints an X-ray equipment is needed.
5. Weak process compatibility with SMT.
6. Handling of bare chips is difficult.
7. High assembly accuracy needed.
8. With present day materials underfilling process with a considerable curing time is needed.
9. Low reliability for some substrates.
10. Repairing is difficult or impossible.
Under Bump Metallization (UBM)

- **Structure:**
  - Adhesion layer: Cr, Ti, W, Ni
  - Barrier layer: Cr, W, Ti, TiW
  - Wetting layer: Cu
  - Oxidation layer: flash gold

- **Processes**
  - Evaporation
  - Sputtering
  - Plating
    - Electroless
    - Electrolytic
Flip Chip Bumps: solder bumps

- Processes to deposit solder bumps:
  - Evaporation
  - Electroplating
  - Screen-printing

- High temperature
  - Pb95-Sn3, Pb97-Sn3

- Moderate
  - Sn-Ag-Cu, Sn-Ag

- Low temperature
  - Sn63-Pb37

Typical Solder-bumped Area
Example of the UBM and solder bumping deposition process

1. Evaporate UBM & Solder Dam
2. Platten Plating Template Resist
3. Etch Solder Dam
4. Electroplate Solder
5. Strip Photoresist
6. Reflow
7. Etch Solder Dam & UBM
Flip chip process by solder joining

- **Die preparing:** testing, bumping, dicing
- **Substrate preparing:** flux application or solder paste printing
- **Pick, alignment and place**
- **Underfill dispensing**
- **Cleaning of flux residues** (optional)
- **Reflow soldering**
- **Underfill curing**

The low viscosity epoxy is drawn by capillary forces into the space between the chip and the substrate.

**Underfill application by dispensing**
Flip Chip Bumps: stud bumps

- **Plated:**
  - Au, AuSn, Ni, NiAu, NiCu

- **Wire stud:**
  - Au, Pb82-Sn2, Cu, Pd (thermo-sonic process using traditional wires of different materials)
Solder Interconnection Structures

a) Controlled Collapse
b) Solid State Bonding
c) Cap Reflow
Flip chip joining using adhesives

- Easy of processing
- Low curing temperatures
- ICA are pastes of polymer resin that are filled with conductive particles to a content that assures conductivity in all directions.
- ACA are pastes or films of thermoplastics or B-stage epoxies. They are filled with metal coated polymer spheres. Can be used for fine pitch.

**Isotropically conductive adhesive (ICA)**

**Anisotropically conductive adhesive (ACA)**
Conductive Adhesives

- Isotropic conductive adhesives (ICA)
- Anisotropic conductive adhesives (ACA)
- Non-conductive adhesives (NCA)

Flake-shaped and Ag powder filled epoxy resin

Polymer particles with Ni/Au

Bump

IC

Adhesive with conductive particles

Contact pads

Substrate
Schematic of Underfill Processing
Capillary Flow Underfill Processing
Schematic of Injection Underfill Processing
Compression Flow Underfill Process

Chip Placement Motion

Solder or Adhesive Bumps
Area Array Format

Circuit Traces

Flow Front

Polymer Underfill

Substrate
Flip Chip underfill equations

- Underfill time for Capillary flow:
  \[ t_{cap} = \frac{3\mu L^2}{\sigma h \cdot \cos(\alpha)} \]

- Underfill time for Injection flow:
  \[ t_{inj} = \frac{6\mu L^2}{(P_{inj} - P_{atm})h^2} \]

- Also Compression flow (or no-flow) underfill
Flip Chip reliability issues

- Die cracking (edge, centre, backside)
- Underfill cracking (bulk, fillet)
- Die/Underfill delaminations and void growth
- Solder migration (extruding into voids)
- Solder fatigue cracking
- Electrostatic Discharge (ESD) sensitivity
- Sensitivity to Alpha particle emission
Mean Time to Fatigue Failure as a Function of Thermal Coefficient of Expansion of Substrate
The Strain Reduction in Solder with Underfill

Approximate Strain (%)

Without underfill 5/95 Sn/Pb and 63/37 Sn/Pb solders
With underfill 5/95 Sn/Pb solder

with underfill-eutectic solder

Solder Composition

0% 25% 50% 75% 100%
63/37 63/37 63/37 63/37 63/37
Example of a Plastic Ball Grid Array (BGA) Package