Homework MKM105, 2013
Hand in your solutions latest 5/12, 18:00
Submit your solutions on the ping-pong website in pdf format. Name the file with your name.

Question 1

a) What are the main reasons to use underfill? (Give at least 4 different reasons).
b) Explain thoroughly the three underfill flow processes: capillary flow underfill, injection flow underfill and compression flow underfill.
Try to give at least 3 advantages and 3 disadvantages of each one of the processes.

Question 2

Ceramic capacitors are built with stacked plates, and the stacking effect is the same as adding an additional plate area for each element of the stack.
Consider a capacitor built with 40 stacked layers, each layer with an area of 1 cm2.
If the dielectric constant is 4000, and the thickness of the dielectric is 10 microns, what would the capacitance be?
If the layers are increased to 80, what is the capacitance?

Question 3

A perimeter PBGA package is assembled onto a FR-4 printed wiring board (PWB) and subjected to a temperature cycling between 0°C and 100°C.
The PBGA has a DNP of 17mm to the outermost solder joint and the solder height is 0,5mm. The CTE of the BT substrate is 15 ppm/°C and for the FR4 PCB the CTE is 18 ppm/°C. The effective CTE of the mould compound and silicon die may be assumed to be the same as the BT substrate.
Estimate the maximum shear strain range ($\Delta\gamma$) in the solder joint of the PBGA package.
What is your prediction on underfill time of a device if you:
a) raise the temperature
b) increase the filler content
c) shrink the die-substrate gap
d) add a surfactant in the underfill

Question 4

Flip chip production that has been in place for 30 years has always been on wafer. How is wafer-level packaging being developed differently today? (Explain the main differences between flip-chip and wafer-level packaging)