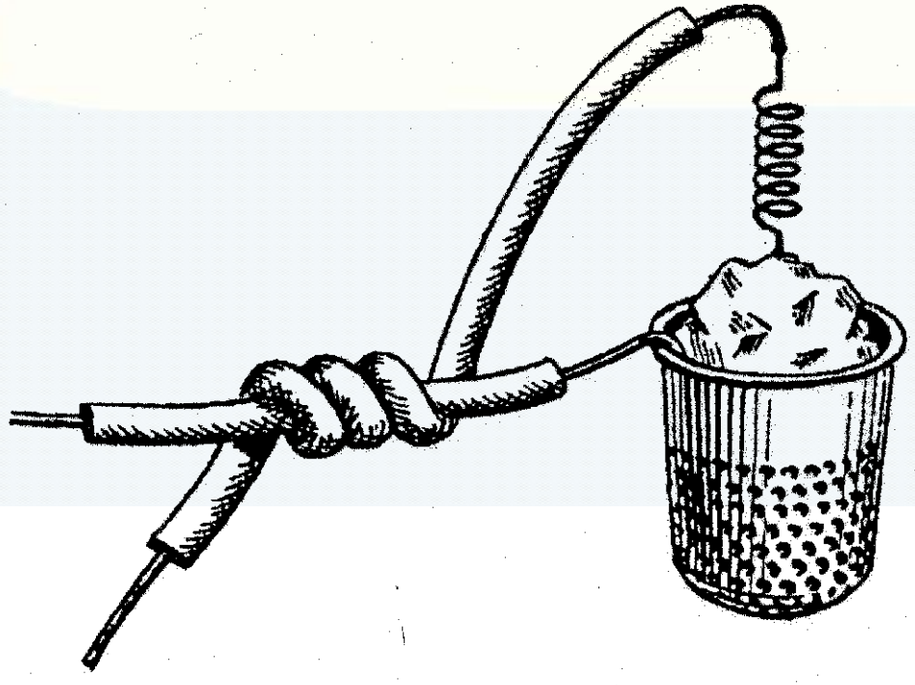
ELECTRONICS
Design Division

Introduction to Semiconductor Technology



Teacher, Göran Thungström

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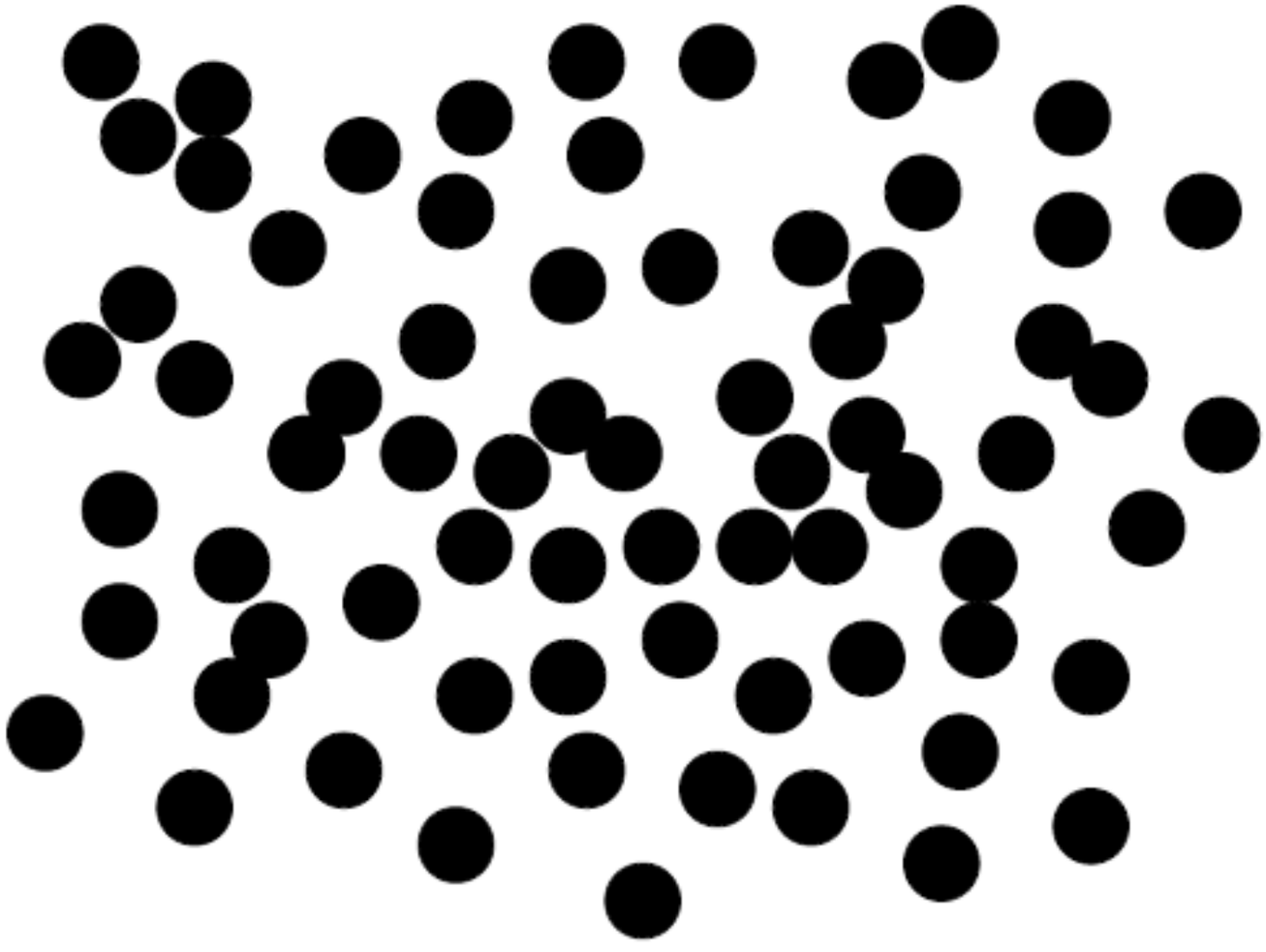
Outline

- Course planning
- Crystal Lattices
- Bulk Crystal Growth
- Epitaxial Growth

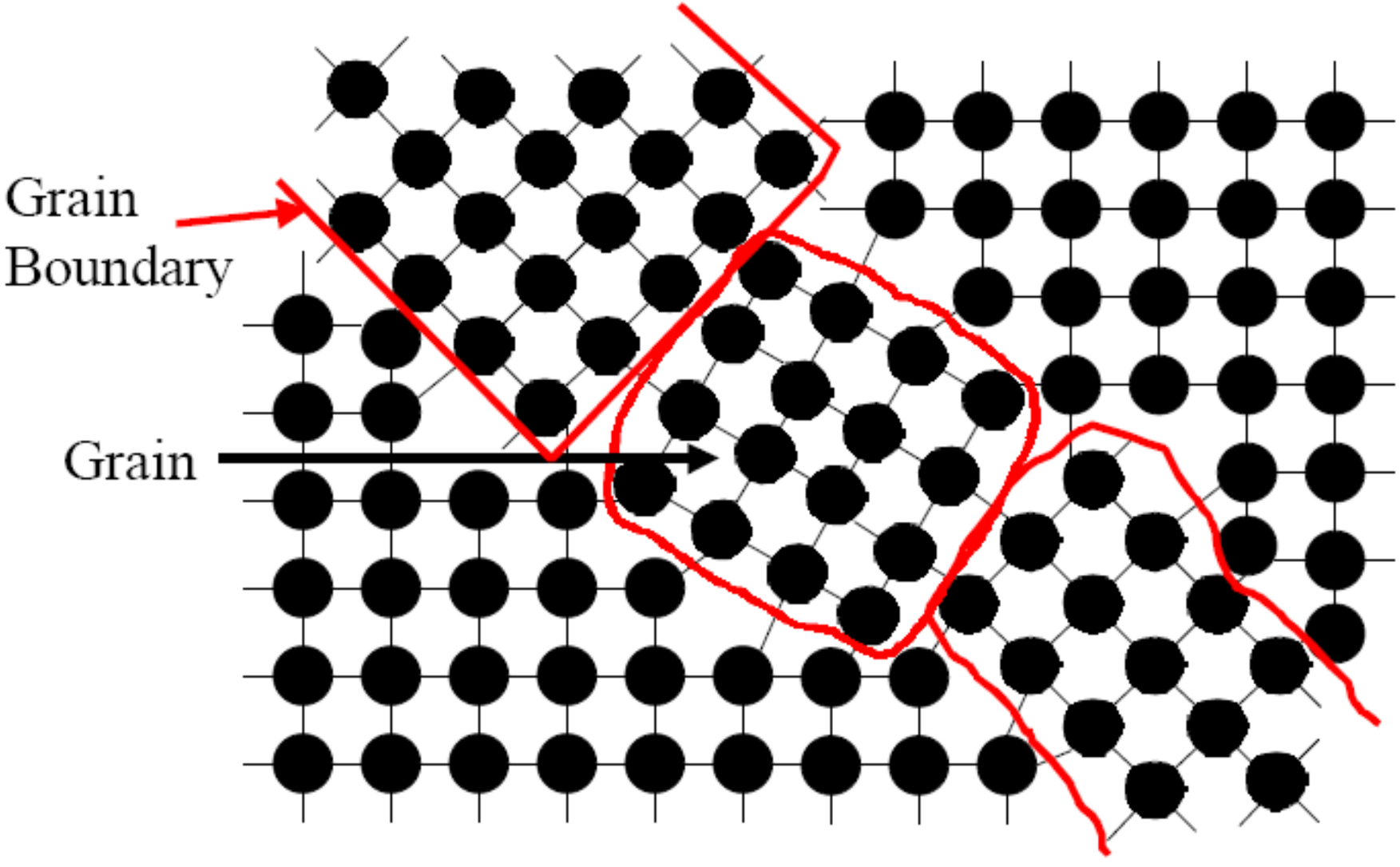
Course planning

- L1 Crystals and Manufacturing of Semiconductors
- L2 Atoms and Electrons
- L3 Energy Bands and Charge Carriers in Semiconductors
- L4 Excess Carriers in semiconductors
- L5 Junctions
- L6 Field–Effect transistors
- L7 Bipolar Junction Transistors
- L8 Optoelectronic Devices and Radiation detectors
- Chapter 9 and 10, Overview reading
- Laboratory work, Characterization of pn-junction
- Exercise, Selected problems from the book (“Solid state electronic devices”, 7e, ISBN 978-1-292-06055-2, Streetman)
- http://apachepersonal.miun.se/~gorthu/halvledare/

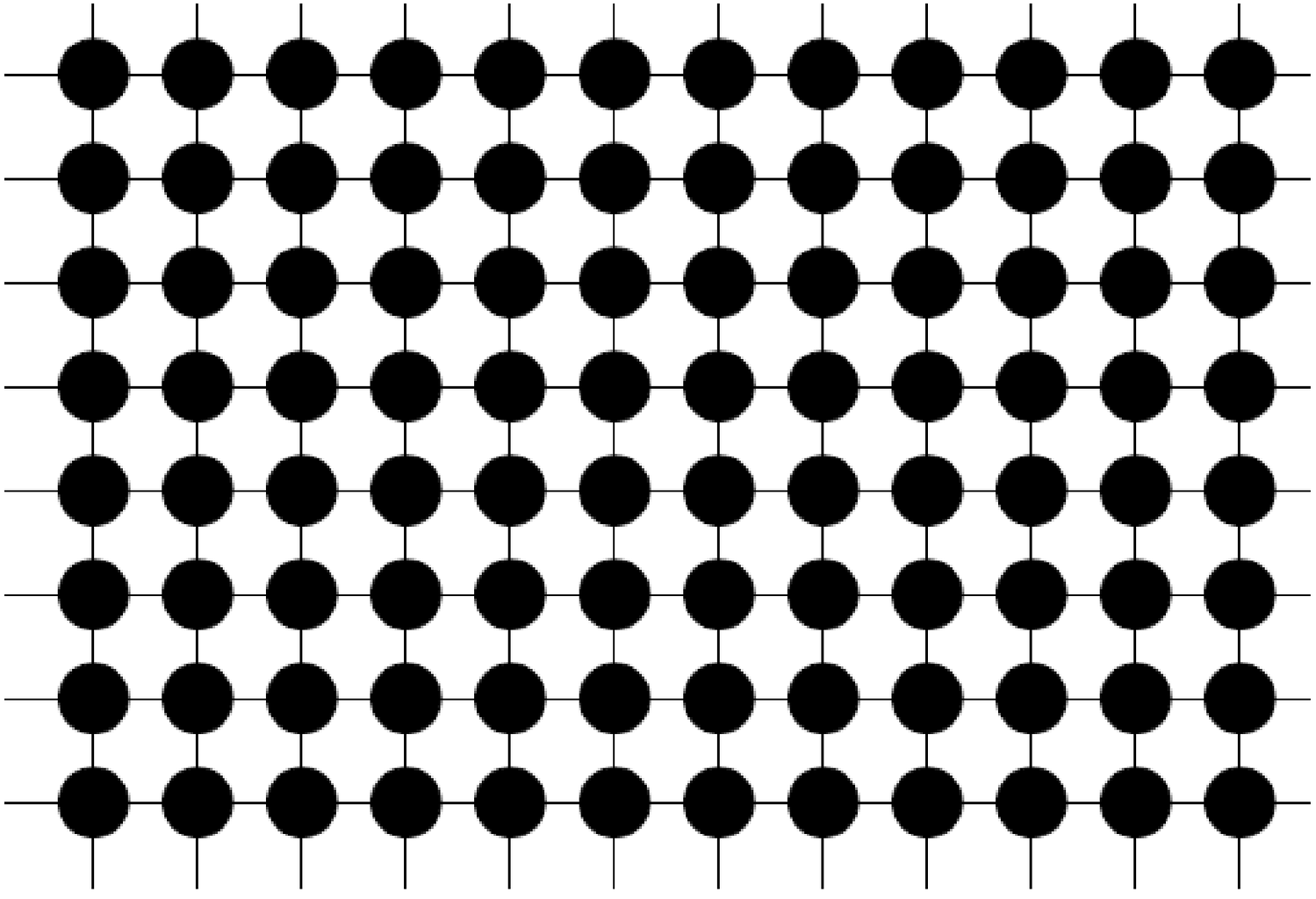
Amorphous Structure



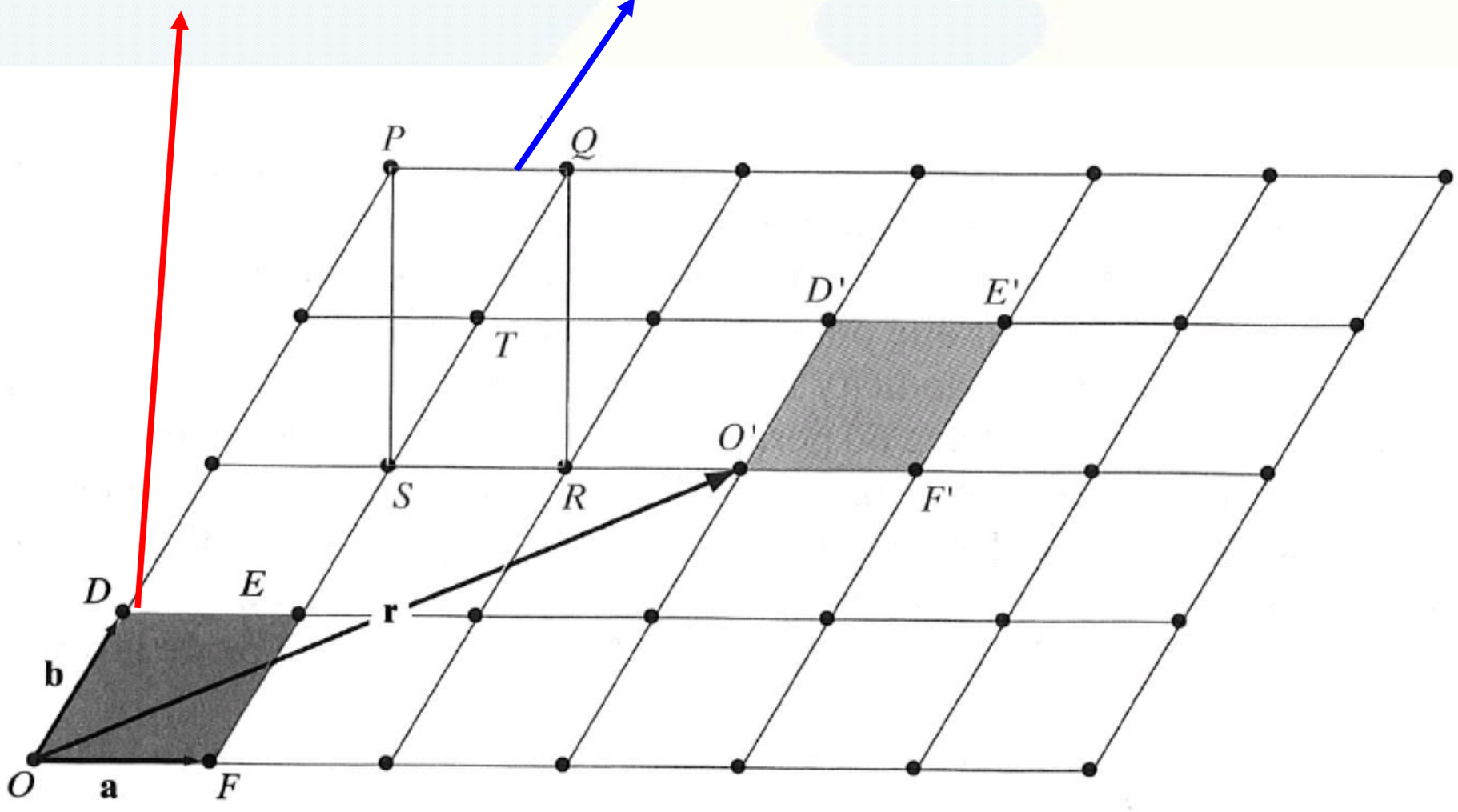
Polycrystalline Structure



Single Crystal Structure



Primitive cell, Unit cell (PQRS)



Translation of a primitive cell by **r**=3**a**+2**b**

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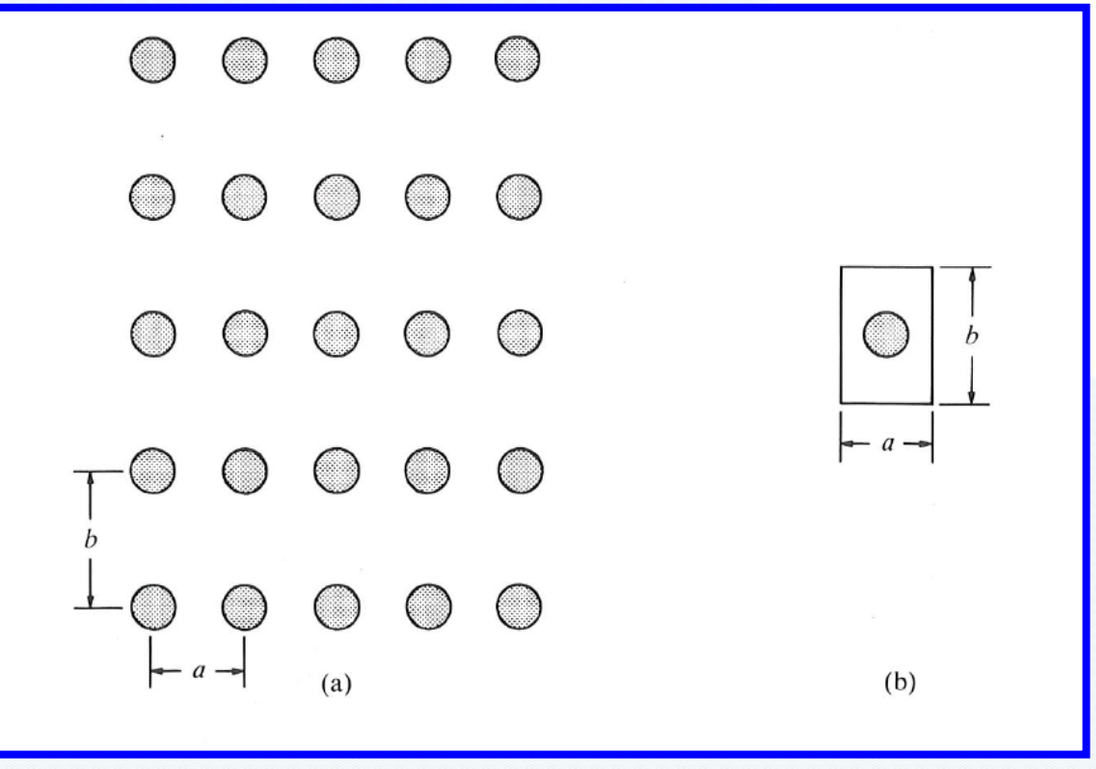
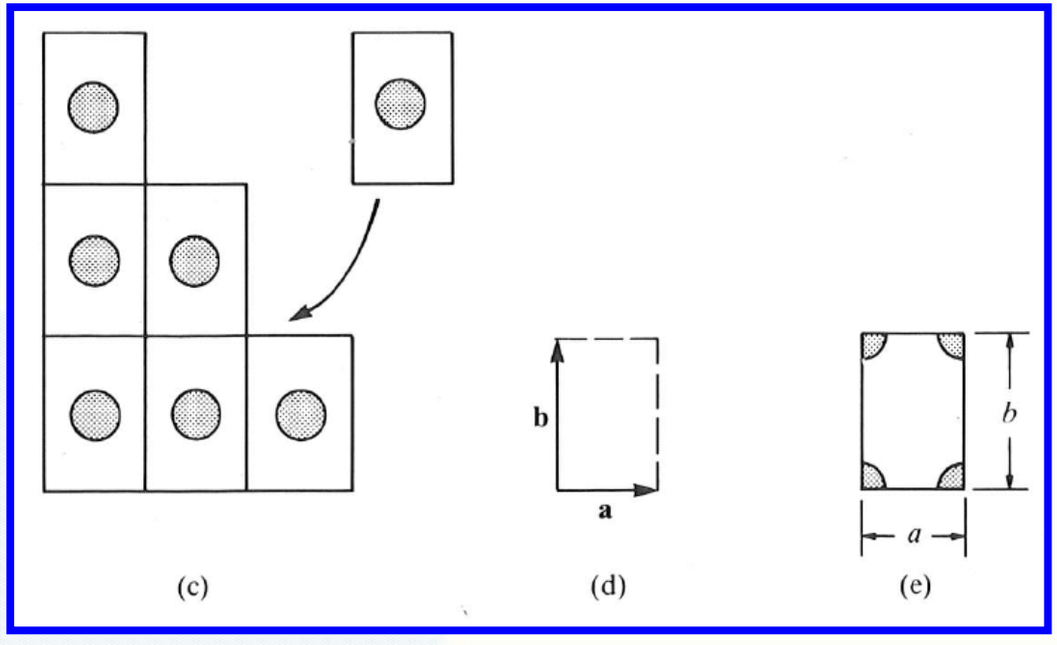
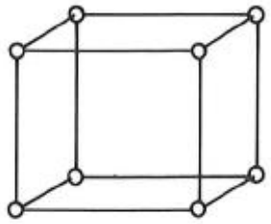
Unit cell

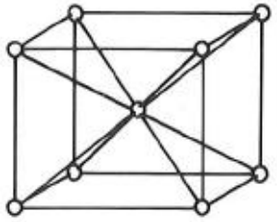




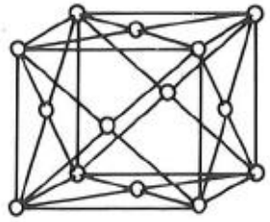
Possible unit cells (Bravais 1840)



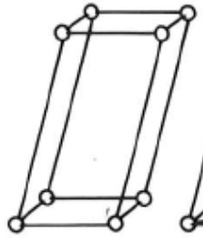
Simple cubic



Body-centered cubic

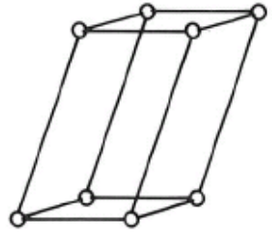


Face-centered cubic

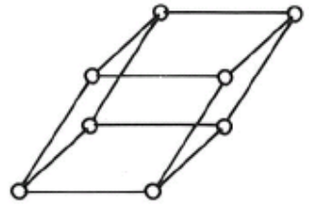


Simple monoclinic

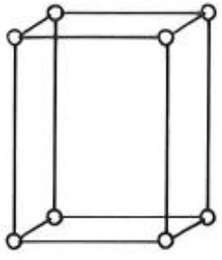
Base-centered monoclinic



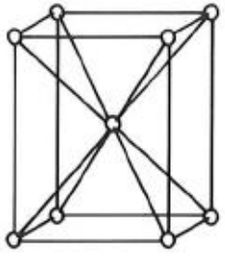
Triclinic



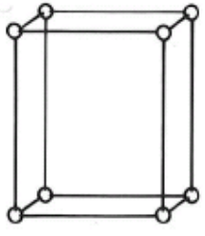
Trigonal



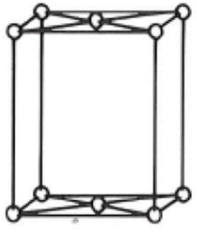
Simple tetragonal



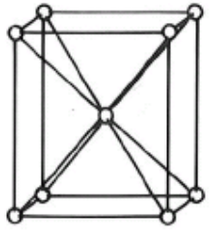
Body-centered tetragonal



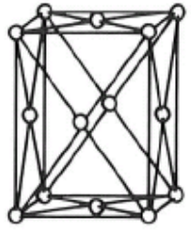
Simple orthorhombic



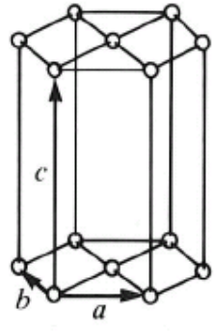
Base-centered orthorhombic



Body-centered orthorhombic



Face-centered orthorhombic



Hexagonal

Diamond and Zink-blende lattice structure

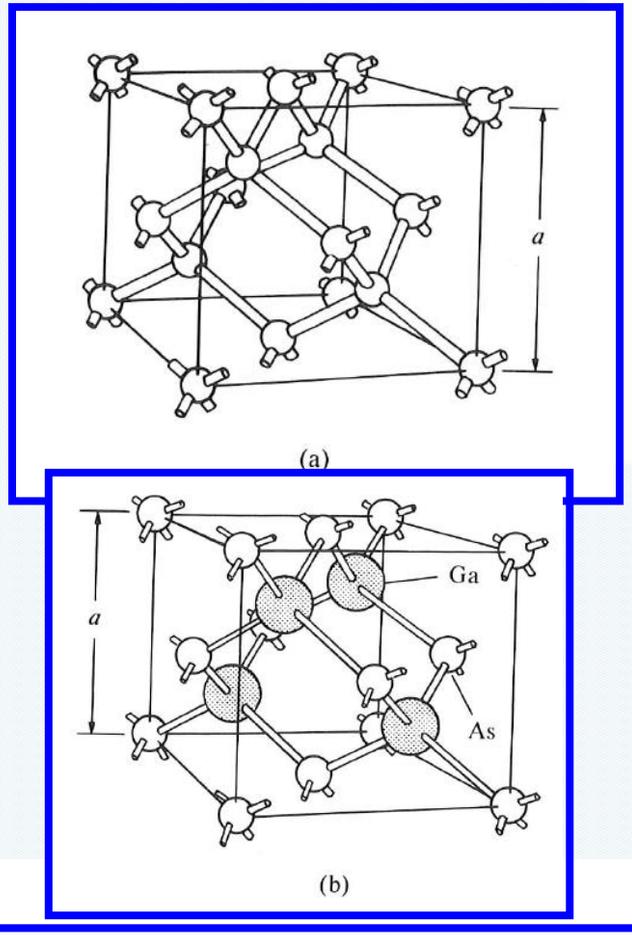


Fig. 1.5 (a) Diamond lattice unit cell. (b) Zincblende lattice unit cell (GaAs used for illustration). [(a) After Shockley;[5] (b) after Sze.[6] Reprinted with permission.]

Table 1.5 Crystal Structure and 300 °K Lattice Constants of Representative Materials (1 Å = 10^{-8} cm).

Semiconductor	Crystal Structure	Lattice Constant (Å)
Si	Diamond	5.43095
Ge	Diamond	5.64613
GaAs	Zincblende	5.6533
CdS	Zincblende	5.8320
	Wurtzite	$a = 4.16$, $c = 6.756$
PbS	Rock-Salt	5.9362

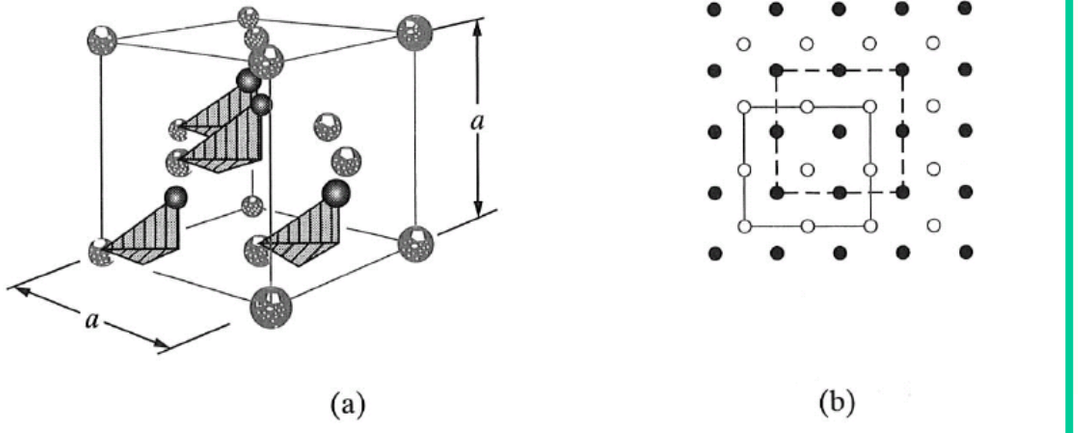


Figure 1–8
Diamond lattice structure: (a) a unit cell of the diamond lattice constructed by placing atoms $\frac{1}{4}, \frac{1}{4}, \frac{1}{4}$ from each atom in an fcc; (b) top view (along any ⟨100⟩ direction) of an extended diamond lattice. The colored circles indicate one fcc sublattice and the black circles indicate the interpenetrating fcc.

Miller index

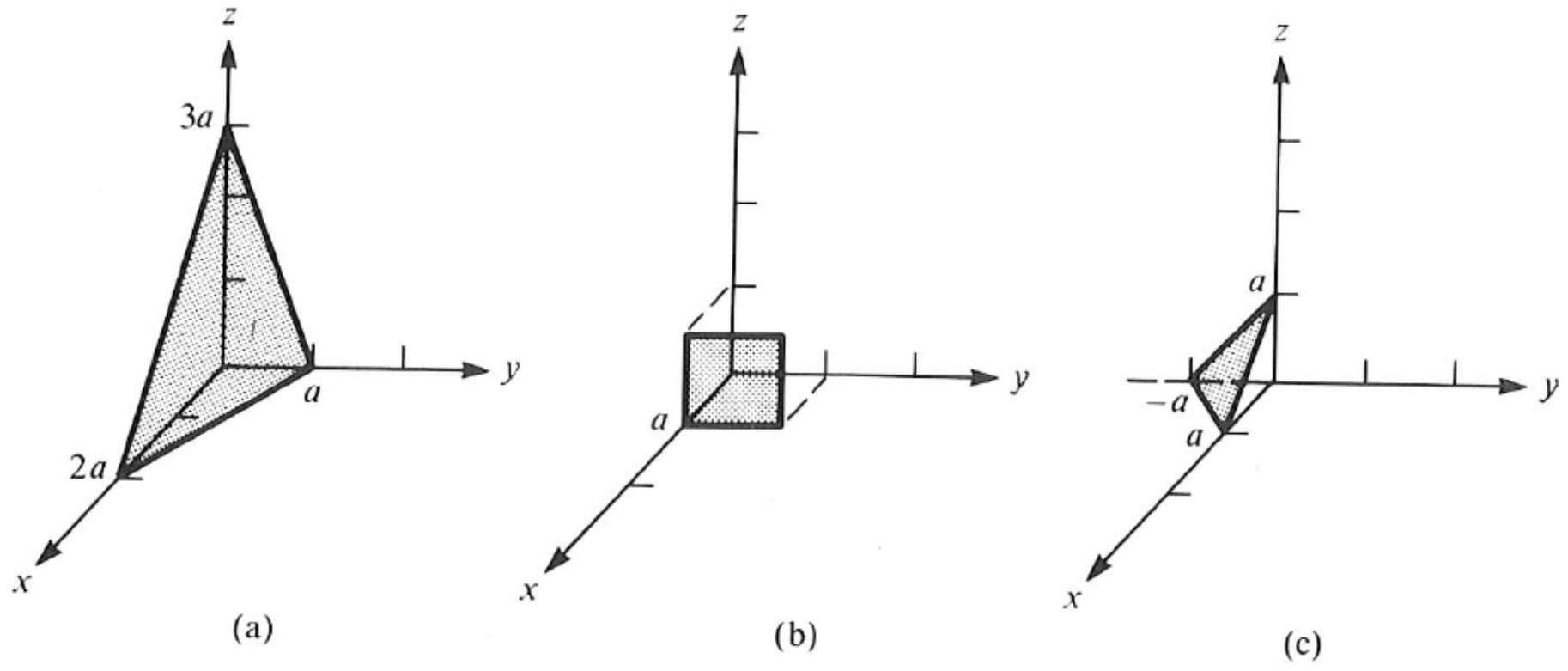


Fig. 1.7 Sample cubic crystal planes. (a) The (362) plane used in explaining the Miller indexing procedure. (b) The (100) plane. (c) The $(1\bar{1}1)$ plane.

Miller index

Indexing Procedure for Planes	Sample Implementation
(1) After setting up coordinate axes along the edges of the unit cell, note where the plane to be indexed intercepts the axes. Divide each intercept value by the unit cell length along the respective coordinate axis. Record the resulting normalized (pure-number) intercept set in the order x, y, z.	2, 1, 3
(2) Invert the intercept values — that is, form [1/intercept]s.	1/2, 1, 1/3
(3) Using an appropriate multiplier, convert the 1/intercept set to the smallest possible set of whole numbers.	3, 6, 2
(4) Enclose the whole-number set in curvilinear brackets.	(362)

Miller index

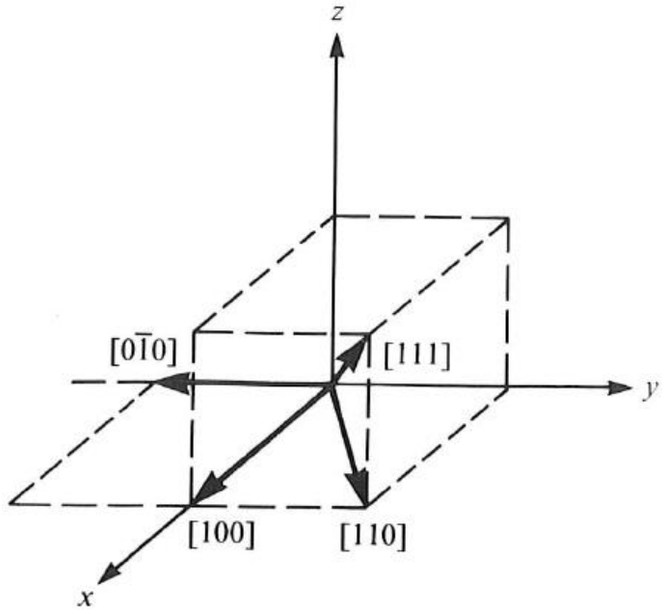
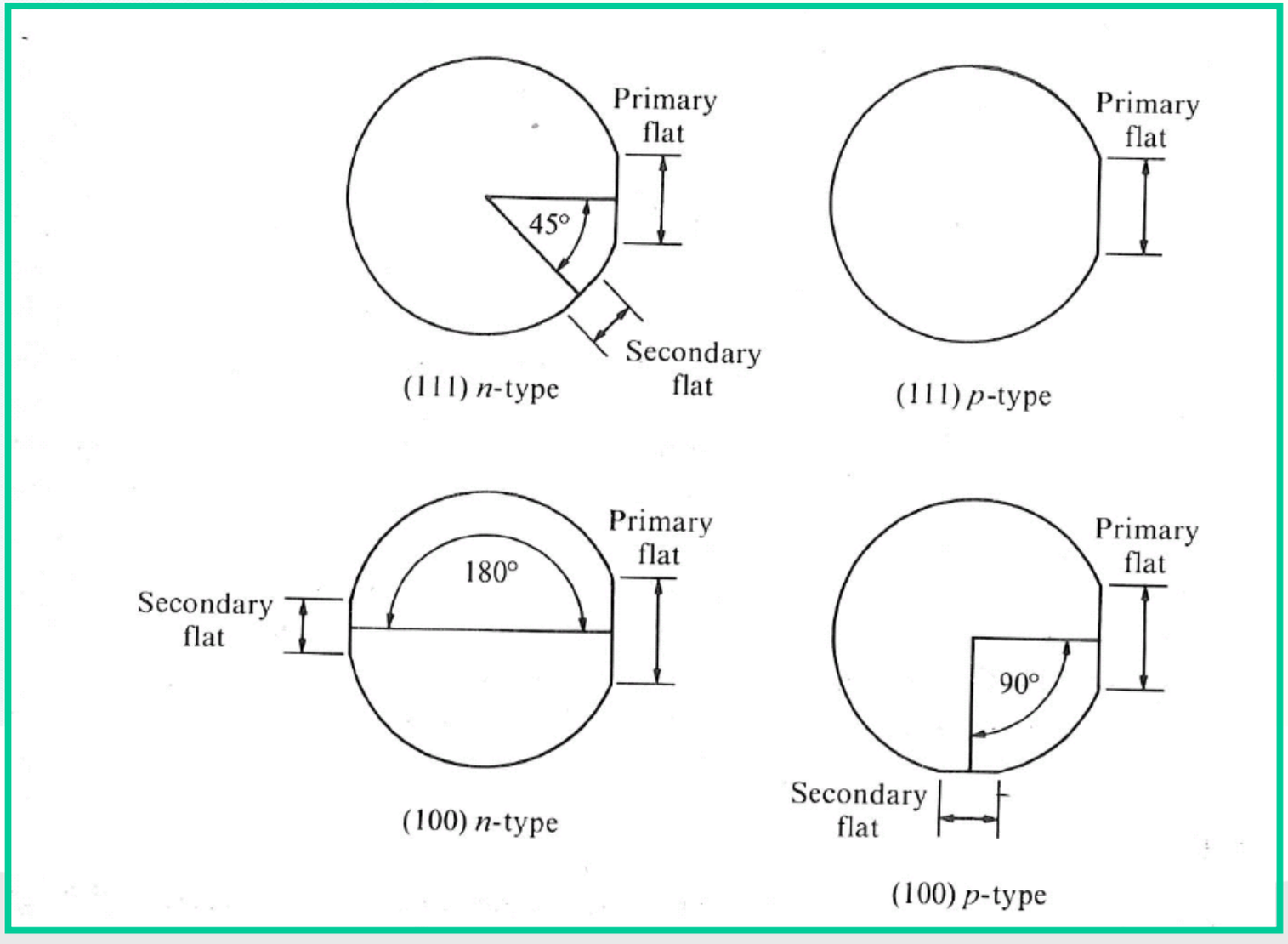


Fig. 1.8 Sample direction vectors and their corresponding Miller indices.

Table 1.6 Miller Notation Summary.

Convention	Interpretation
(hkl)	Crystal plane
$\{hkl\}$	Equivalent planes
$[hkl]$	Crystal direction
$\langle hkl \rangle$	Equivalent directions
$(hkil)$	Plane — Hexagonal system
$[hkil]$	Direction — Hexagonal system

Identification of silicon-wafer orientation

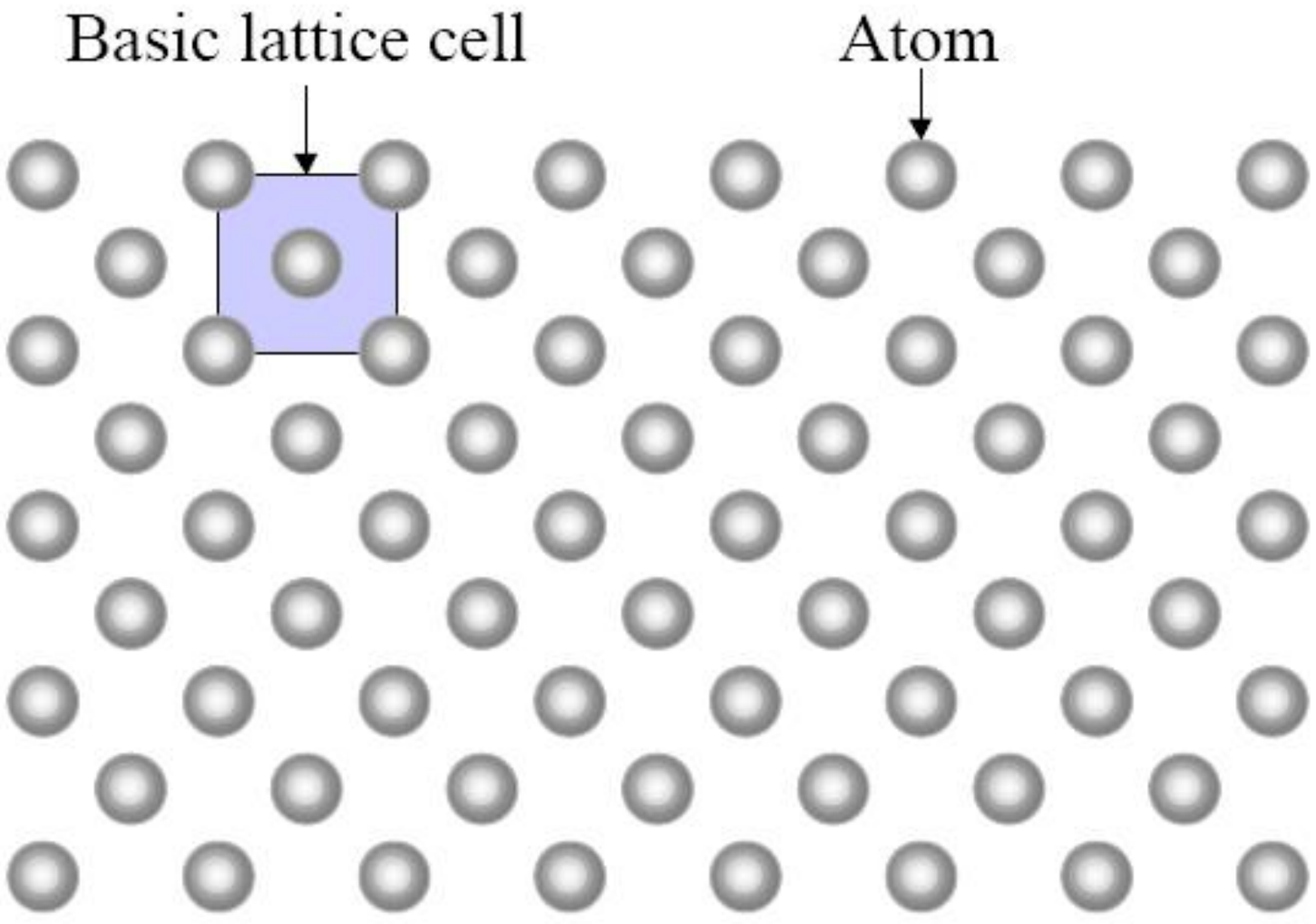


Why Silicon?

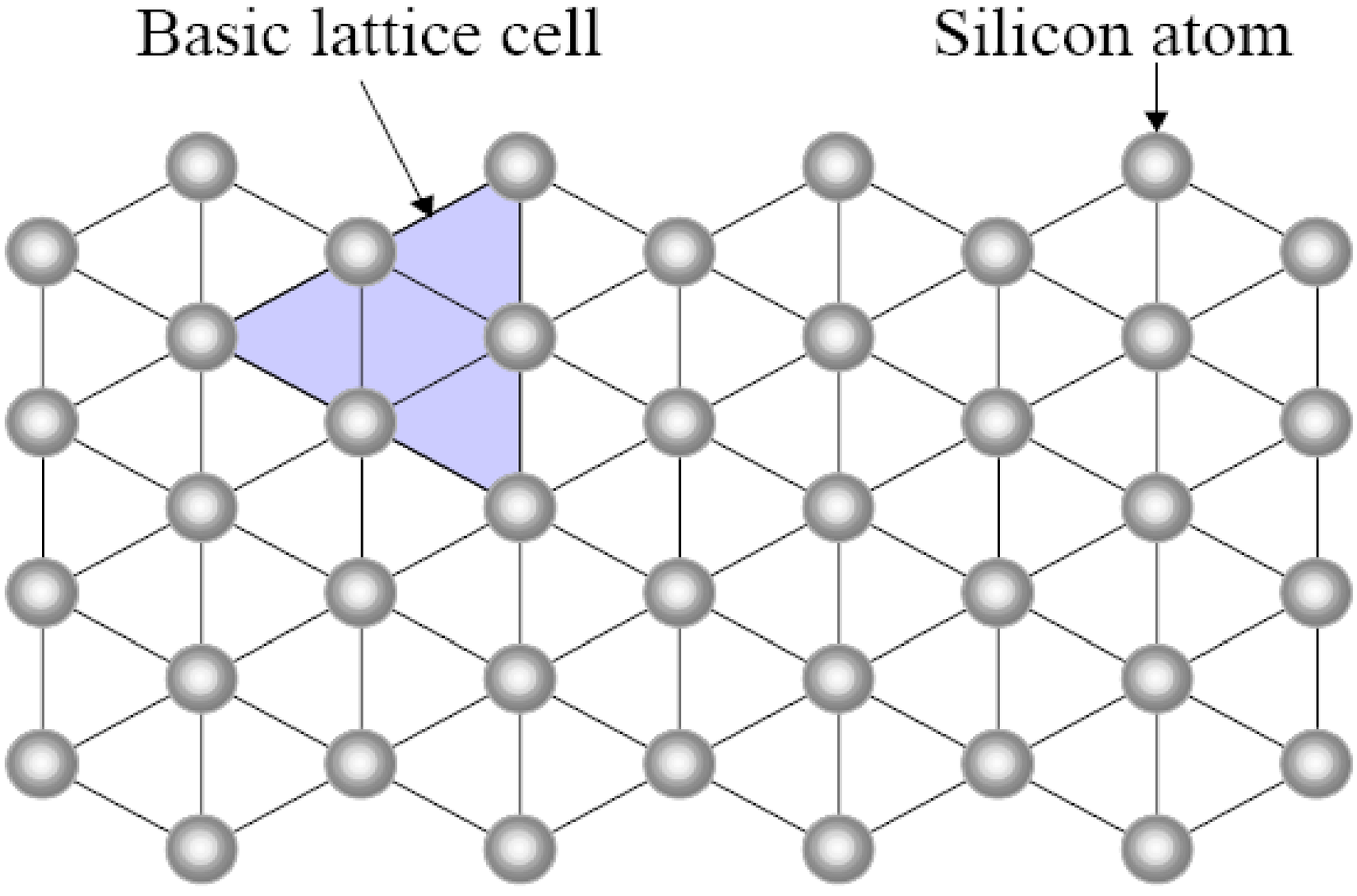
- Abundant, cheap
- Silicon dioxide is very stable, strong dielectric, and it is easy to grow in thermal process.
- Large band gap, wide operation temperature range.

Name	Silicon
Symbal	Si
Atomic number	14
Atomic weight	28.0855
Discoverer	Jöns Jacob Berzelius
Discovered at	Sweden
Discovery date	1824
Origin of name	From the Latin word "silicis" meaning "flint"
Bond length in single crystal Si	2.352 Å
Density of solid	2.33 g/cm^3
Molar volume	12.06 cm^3
Velocity of sound	2200 m/sec
Electrical resistivity	100,000 Ω·cm
Reflectivity	28%
Melting point	1414 °C
Boiling point	2900 °C

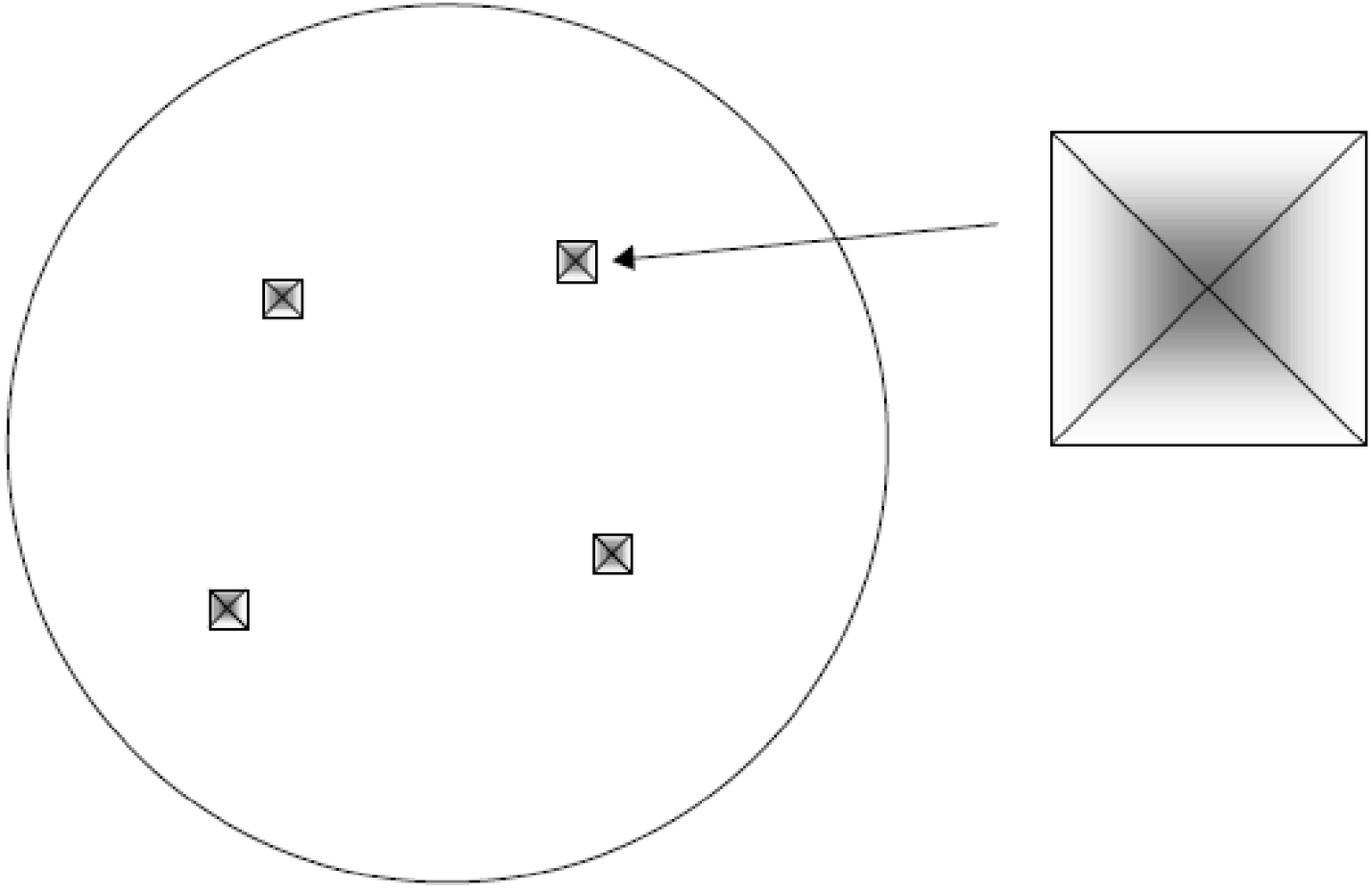
<100> Orientation Plane



<111> Orientation Plane



<100> Wafer Etch Pits



<111> Wafer Etch Pits

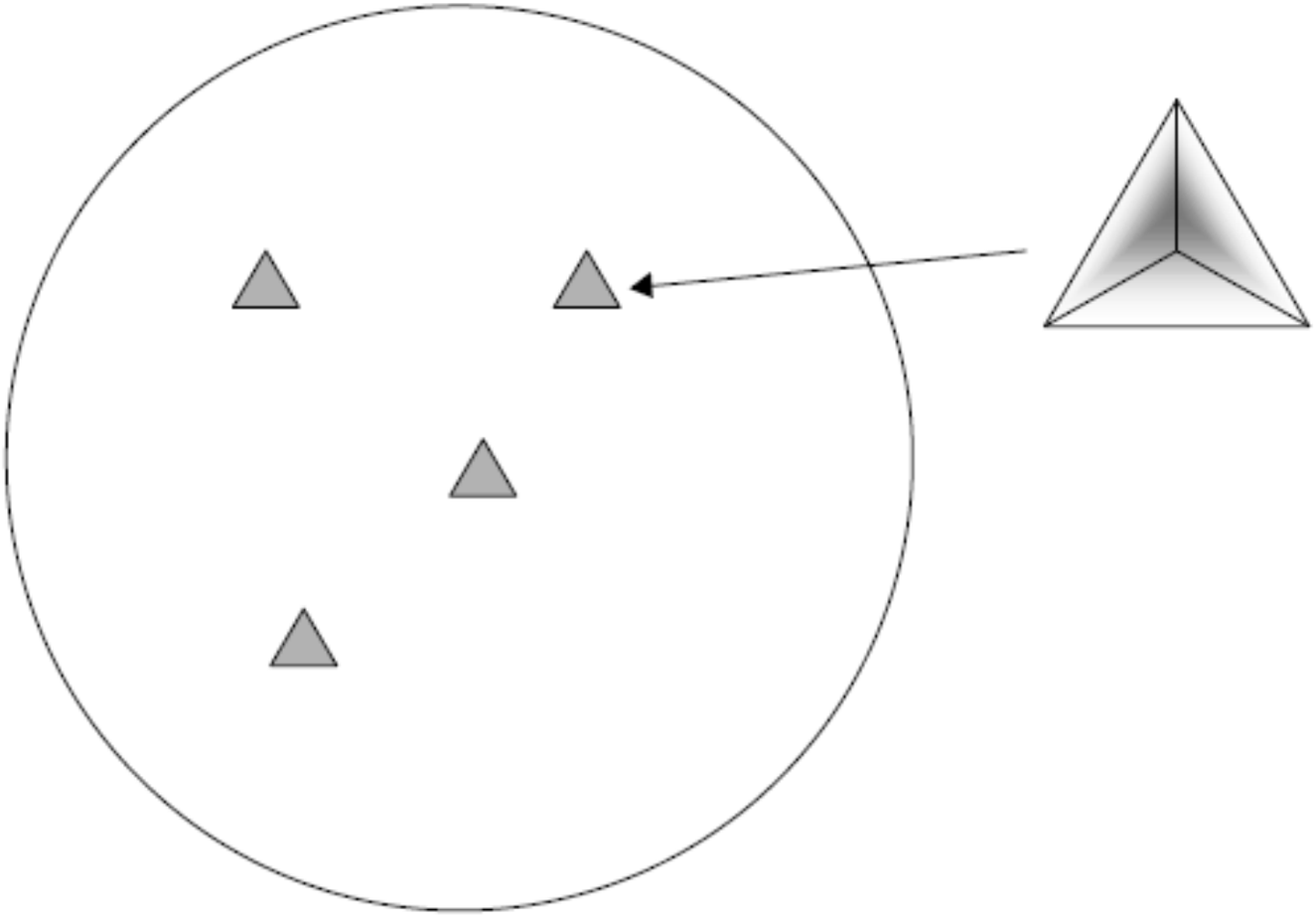
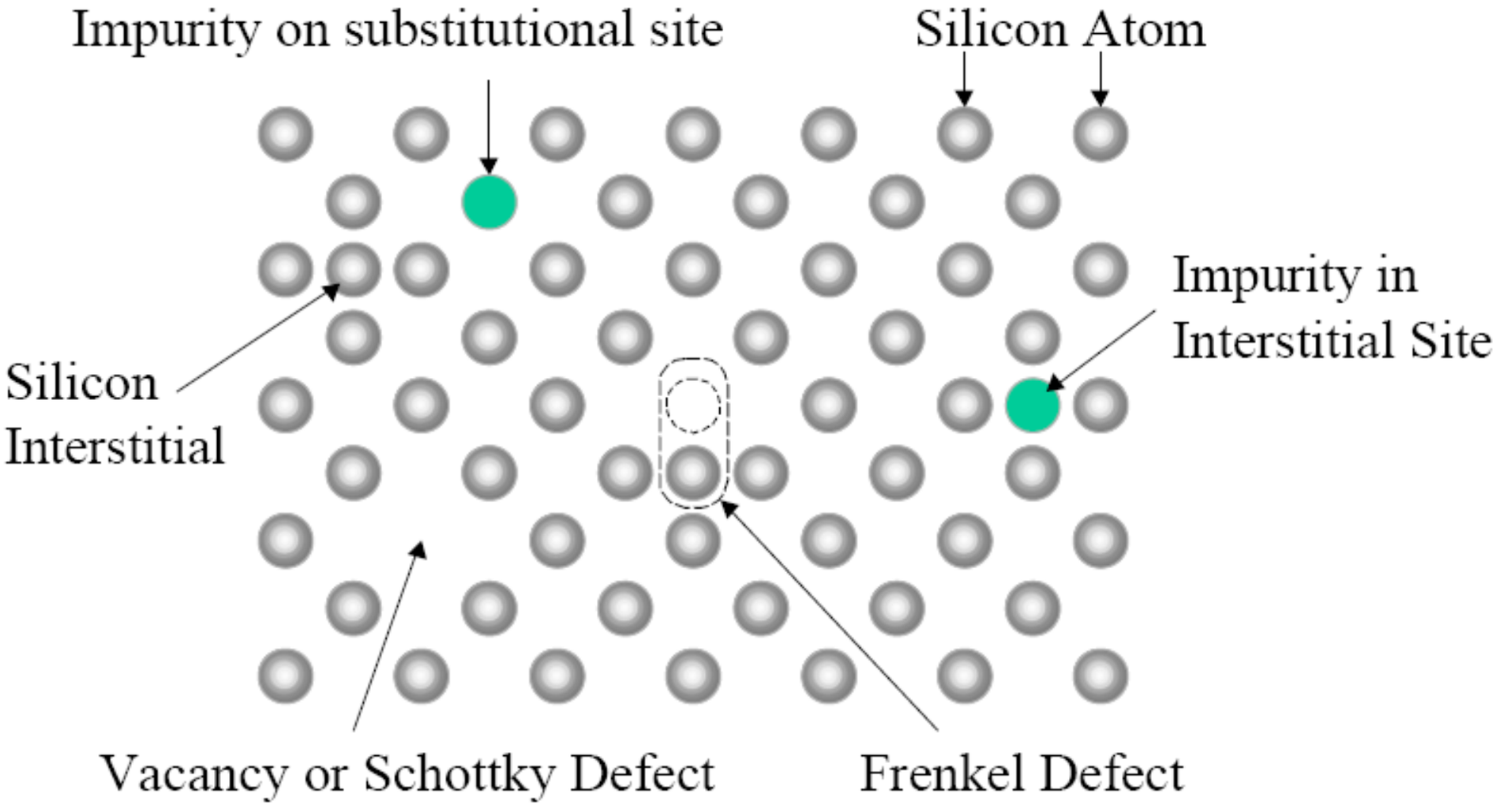
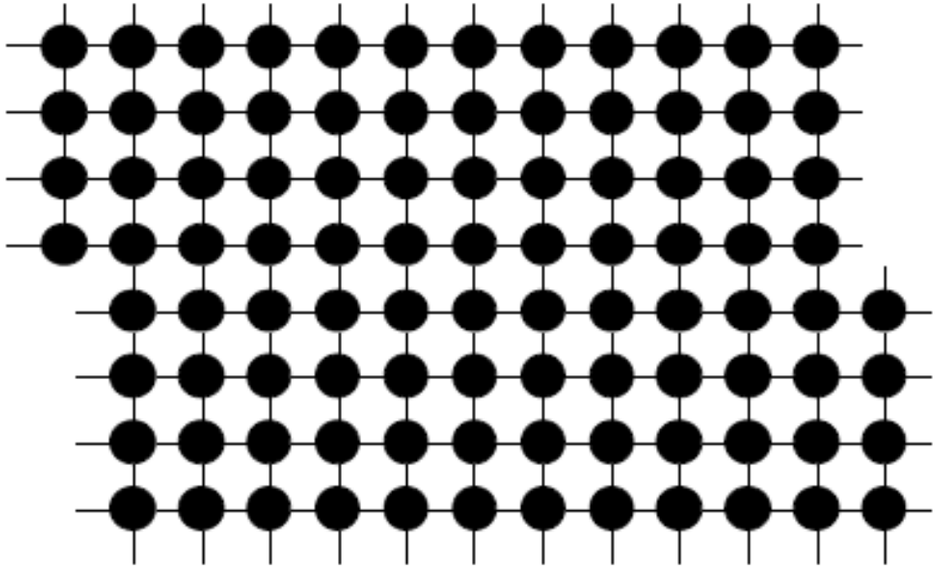
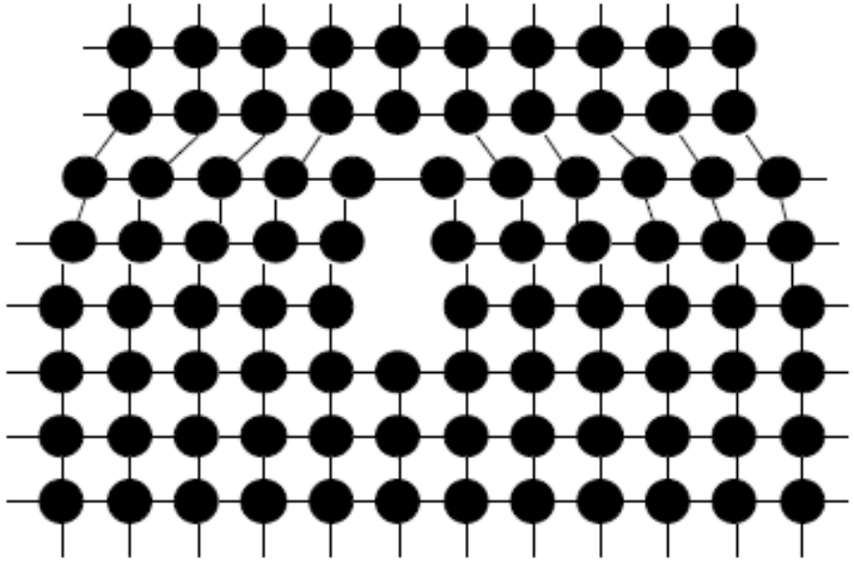


Illustration of the Defects



Dislocation Defects





From Sand to Wafer

- Quartz sand: silicon dioxide
- Sand to metallic grade silicon (MGS)
- React MGS powder with HCl to form TCS
- Purify TCS by vaporization and condensation
- React TCS to H_2 to form polysilicon (EGS)
- Melt EGS and pull single crystal ingot

From Sand to Wafer (cont.)

- Cut end, polish side, and make notch or flat
- Saw ingot into wafers
- Edge rounding, lap, wet etch, and CMP
- Laser scribe

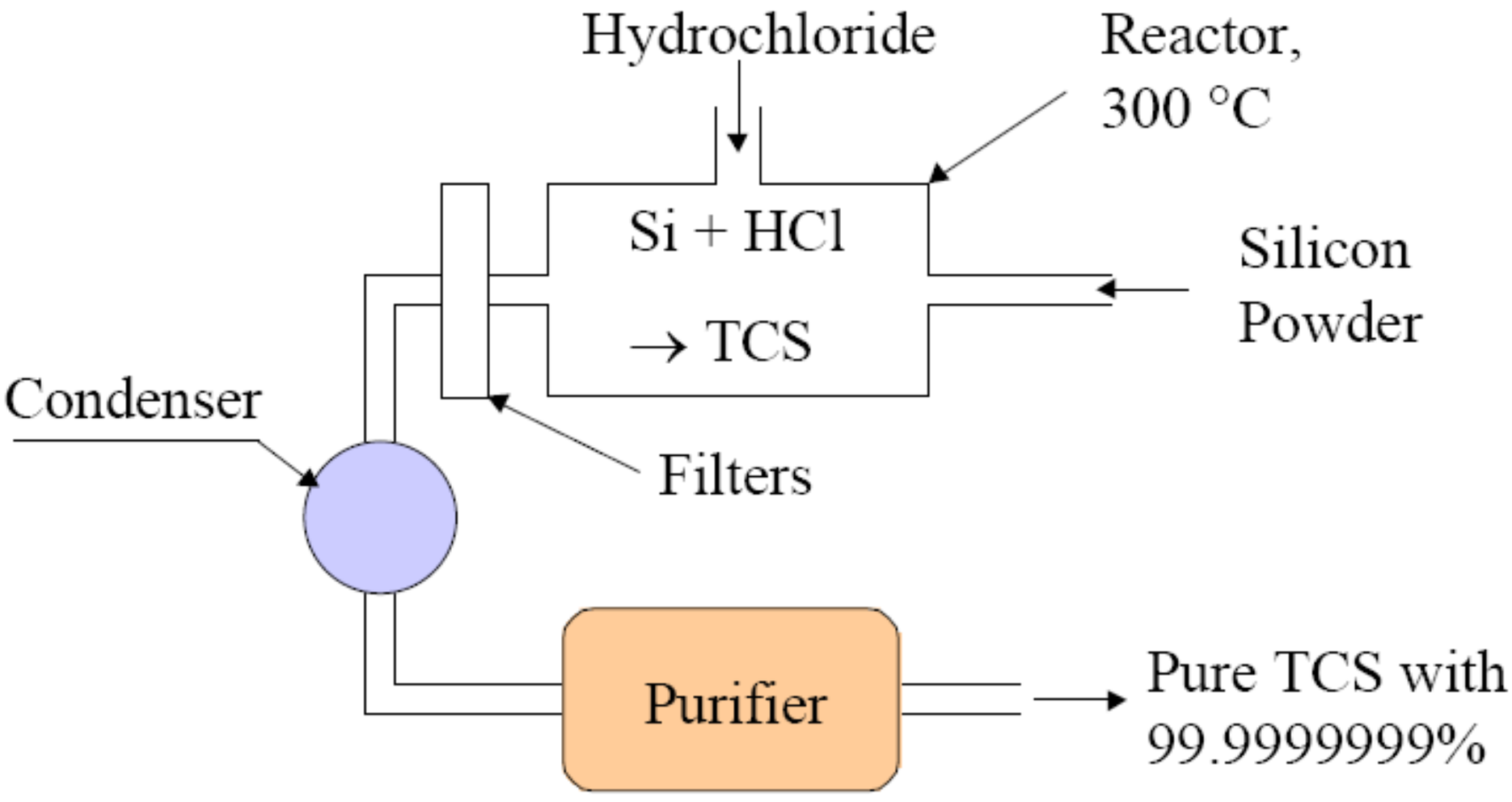
- Epitaxy deposition

From Sand to Silicon

$$SiO_2 + C \xrightarrow{\text{Heat (2000 °C)}} Si + CO_2$$

Sand	Carbon	MGS	Carbon Dioxide

Silicon Purification I

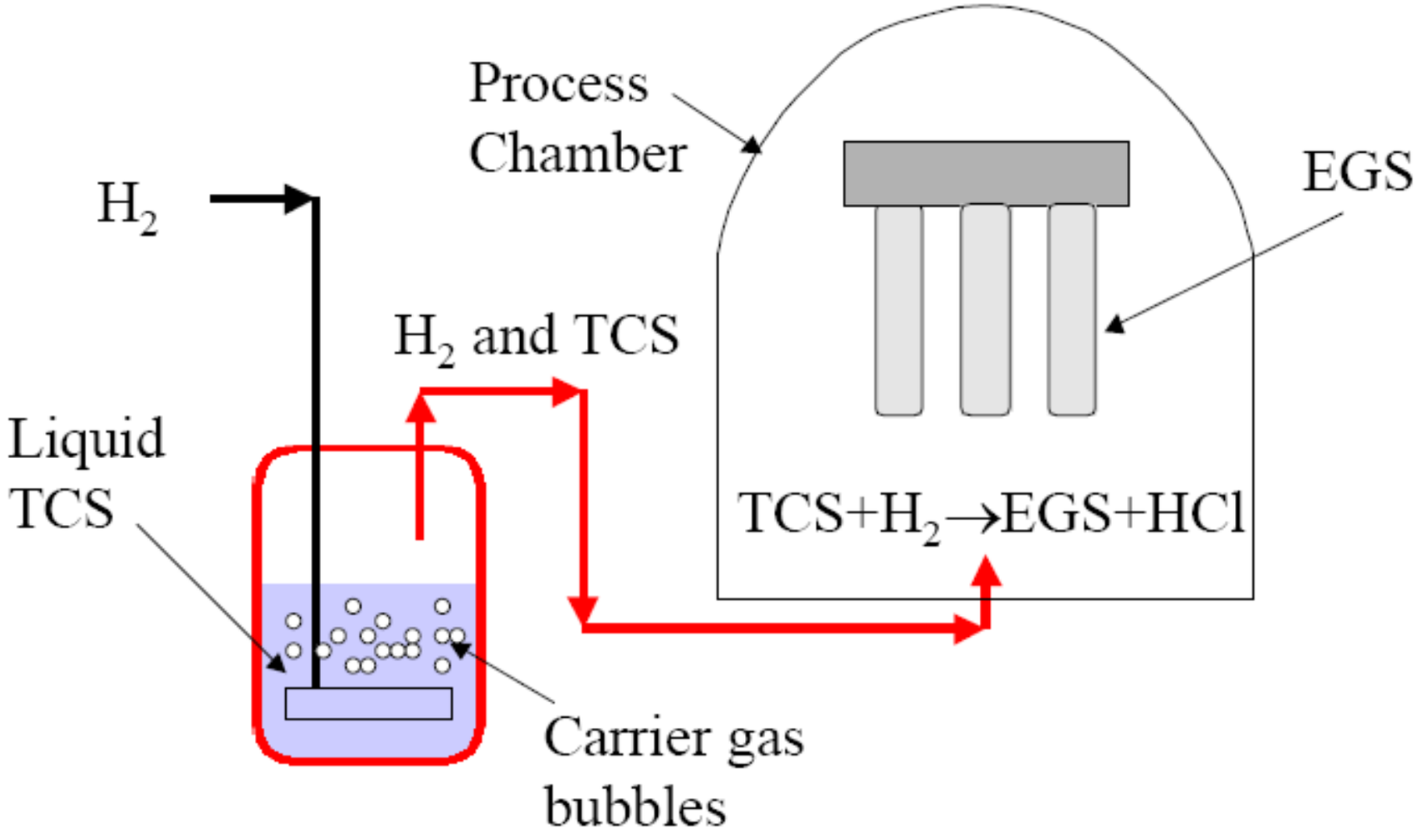


Polysilicon Deposition, EGS

$$SiHCl_3 + H_2 \xrightarrow{\text{Heat (1100 °C)}} Si + 3HCl$$

$SiHCl_3$	+	H_2	→	Si	+	3HCl
TCS		Hydrogen		EGS		Hydrochloride

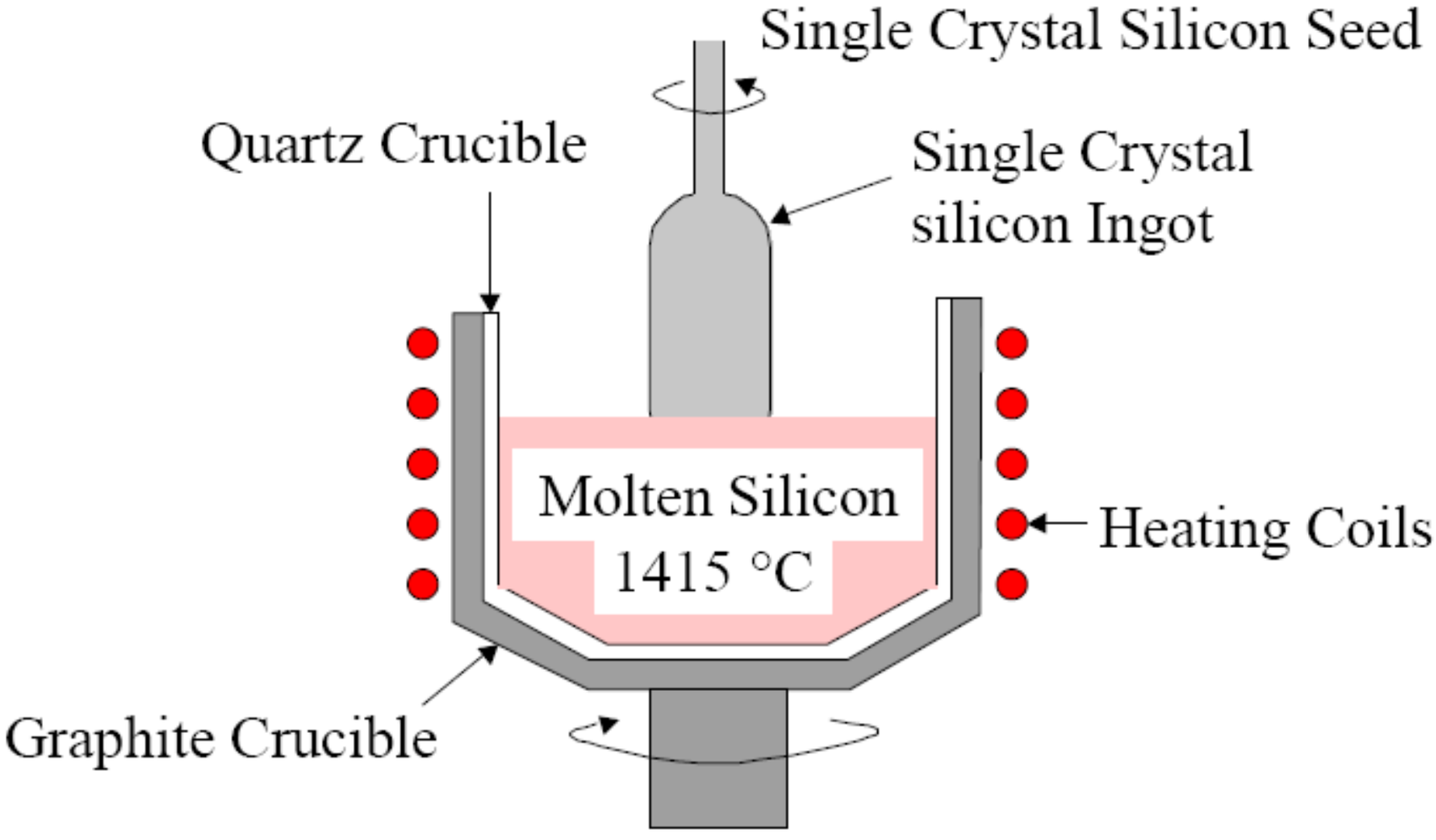
Silicon Purification II



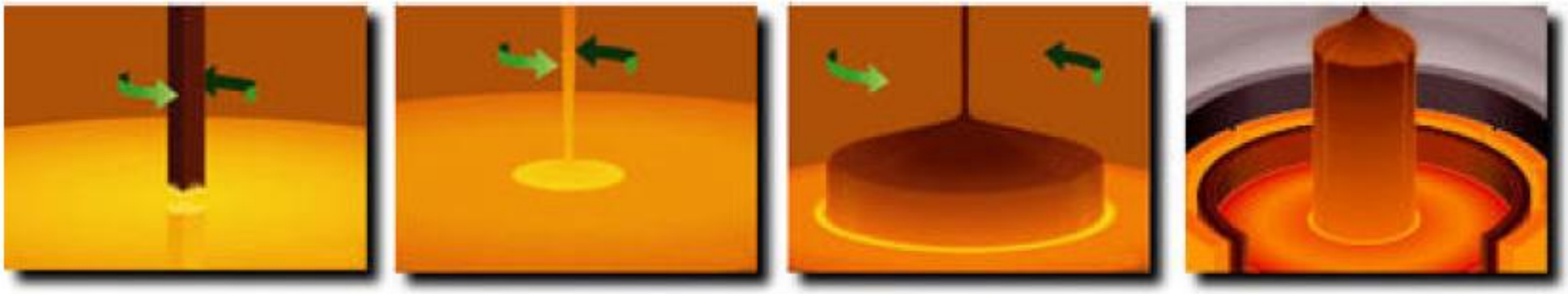
Electronic Grade Silicon

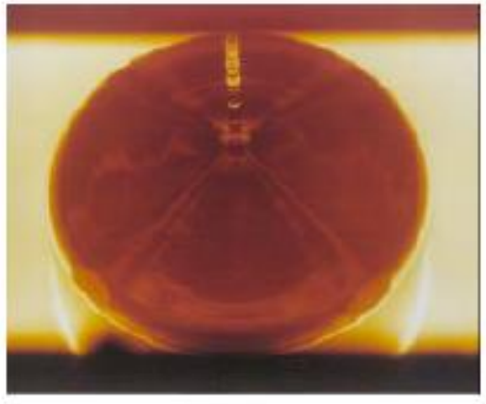
Source: http://www.fullman.com/semiconductors/_polysilicon.html

Crystal Pulling: CZ method



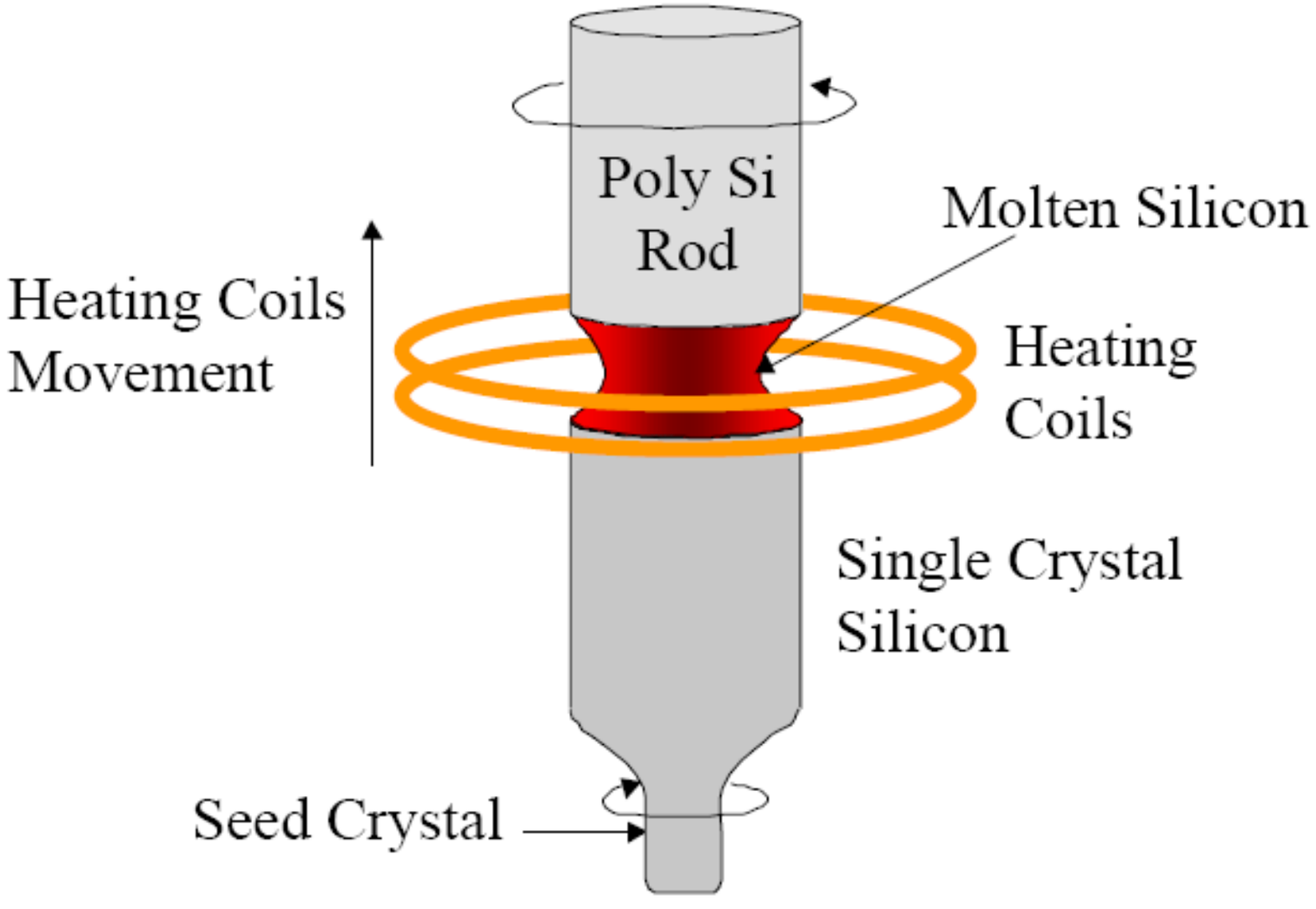
CZ Crystal Pulling





Source: http://www.fullman.com/semiconductors/_crystalgrowing.html

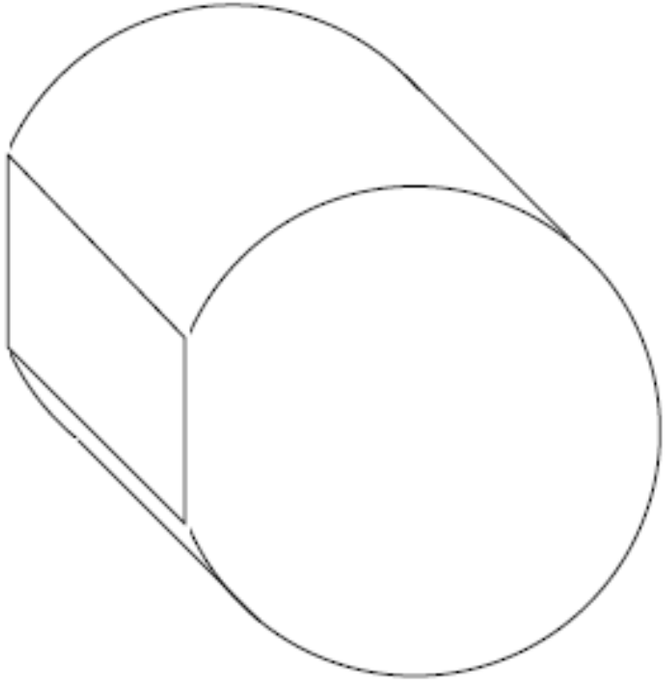
Floating Zone Method



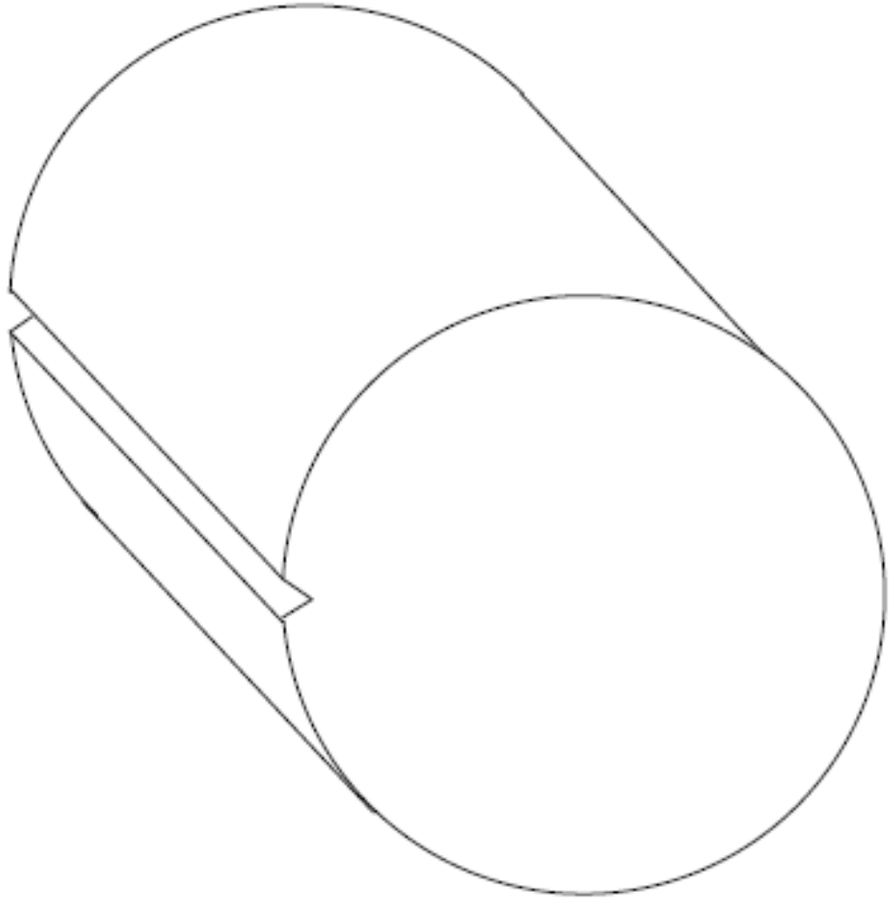
Comparison of the Two Methods

- CZ method is more popular
  - Cheaper
  - Larger wafer size (300 mm in production)
  - Reusable materials
- Floating Zone
  - Pure silicon crystal (no crucible)
  - More expensive, smaller wafer size (150 mm)
  - Mainly for power devices.

Ingot Polishing, Flat, or Notch

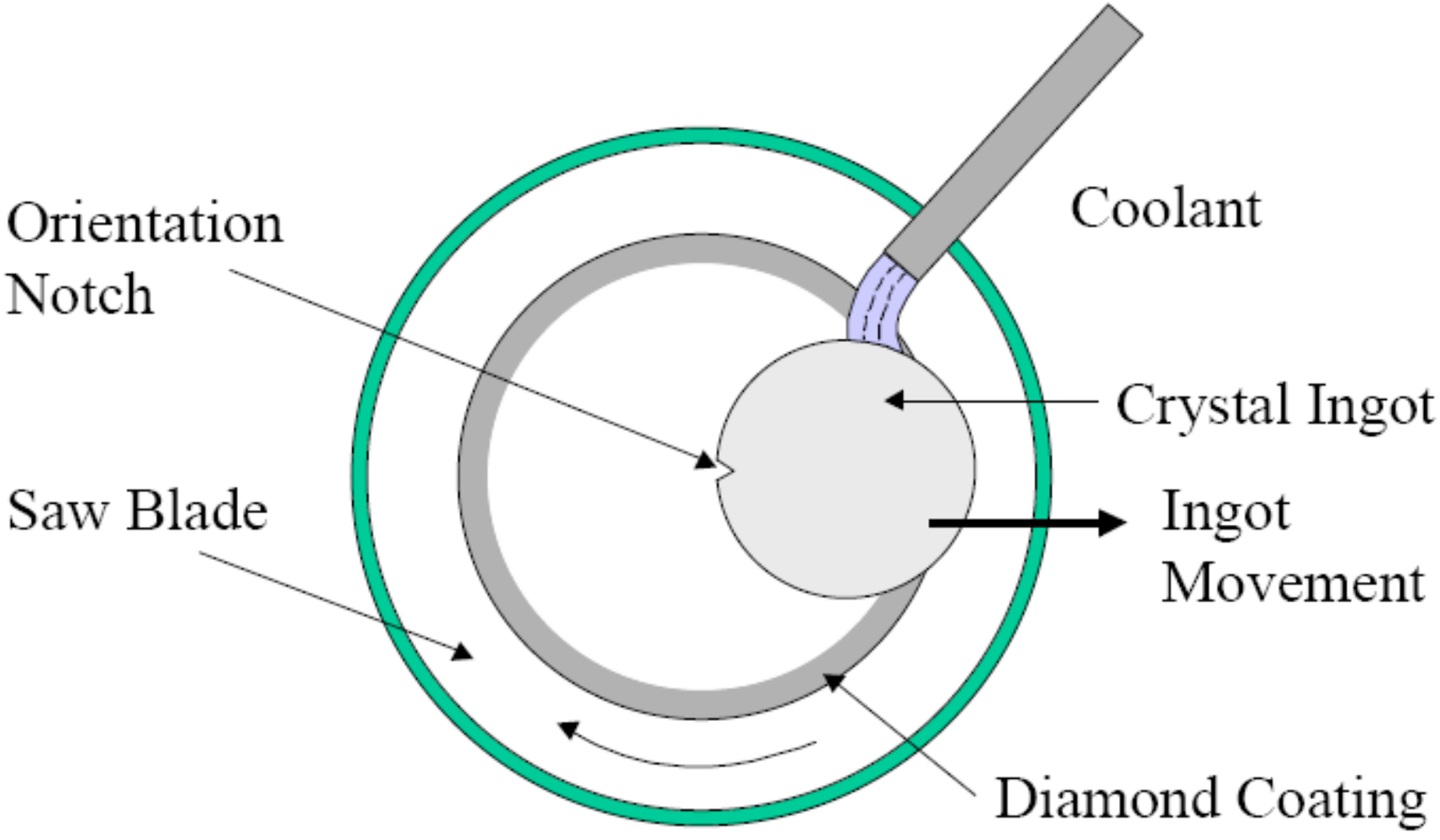


Flat, 150 mm and smaller



Notch, 200 mm and larger

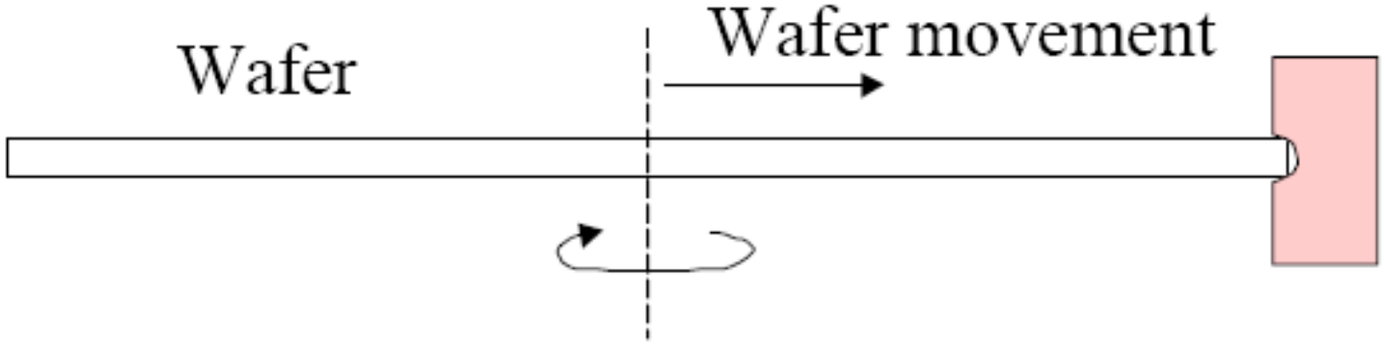
Wafer Sawing

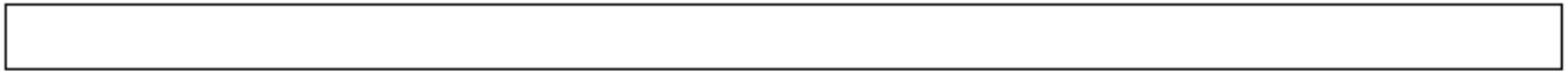


Parameters of Silicon Wafer

Wafer Size (mm)	**Thickness** (μm)	**Area** (cm^2)	**Weight** (grams)
50.8 (2 in)	279	20.26	1.32
76.2 (3in)	381	45.61	4.05
100	525	78.65	9.67
125	625	112.72	17.87
150	675	176.72	27.82
200	725	314.16	52,98
300	775	706.21	127.62

Wafer Edge Rounding





Wafer Before Edge Rounding

Wafer After Edge Rounding

Wafer Lapping

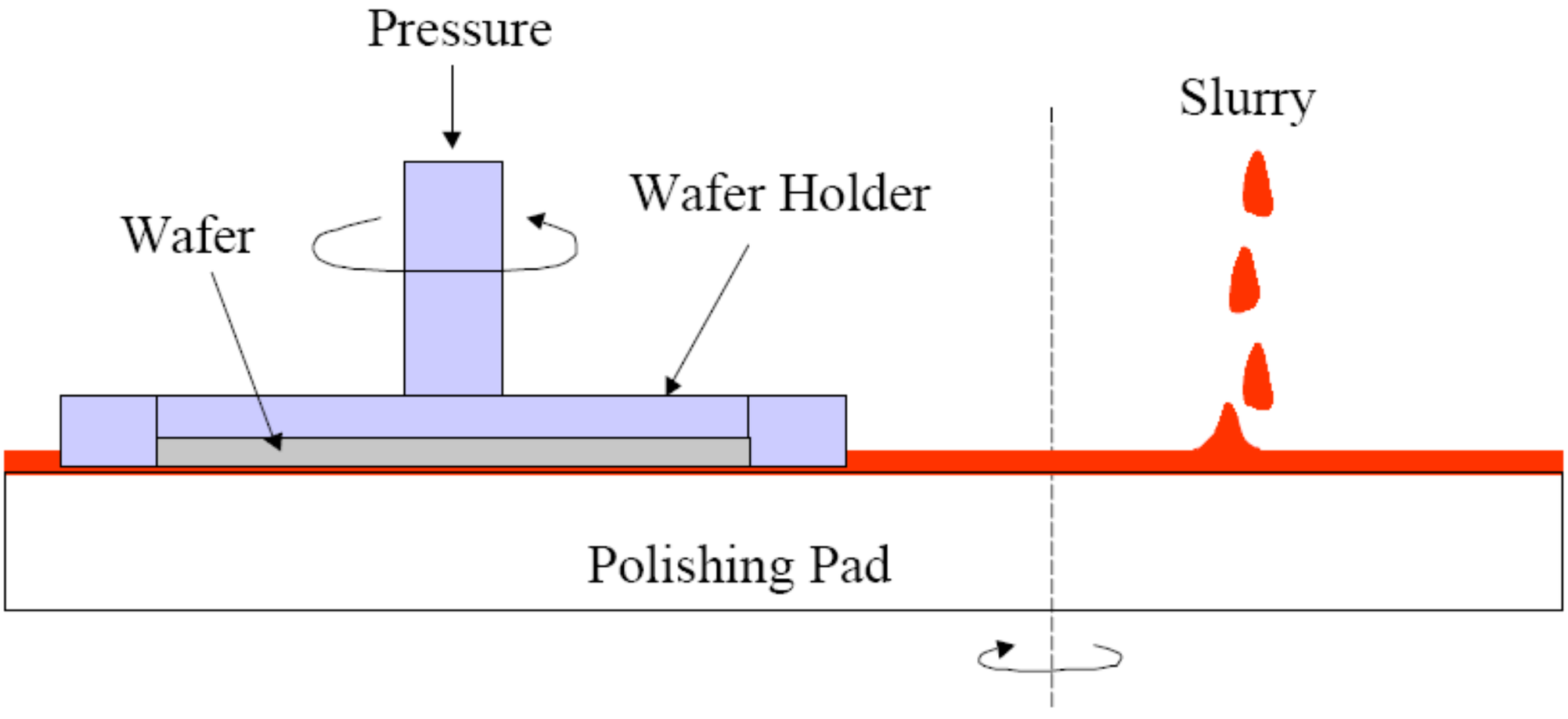
- Rough polished
- conventional, abrasive, slurry-lapping
- To remove majority of surface damage
- To create a flat surface

Wet Etch

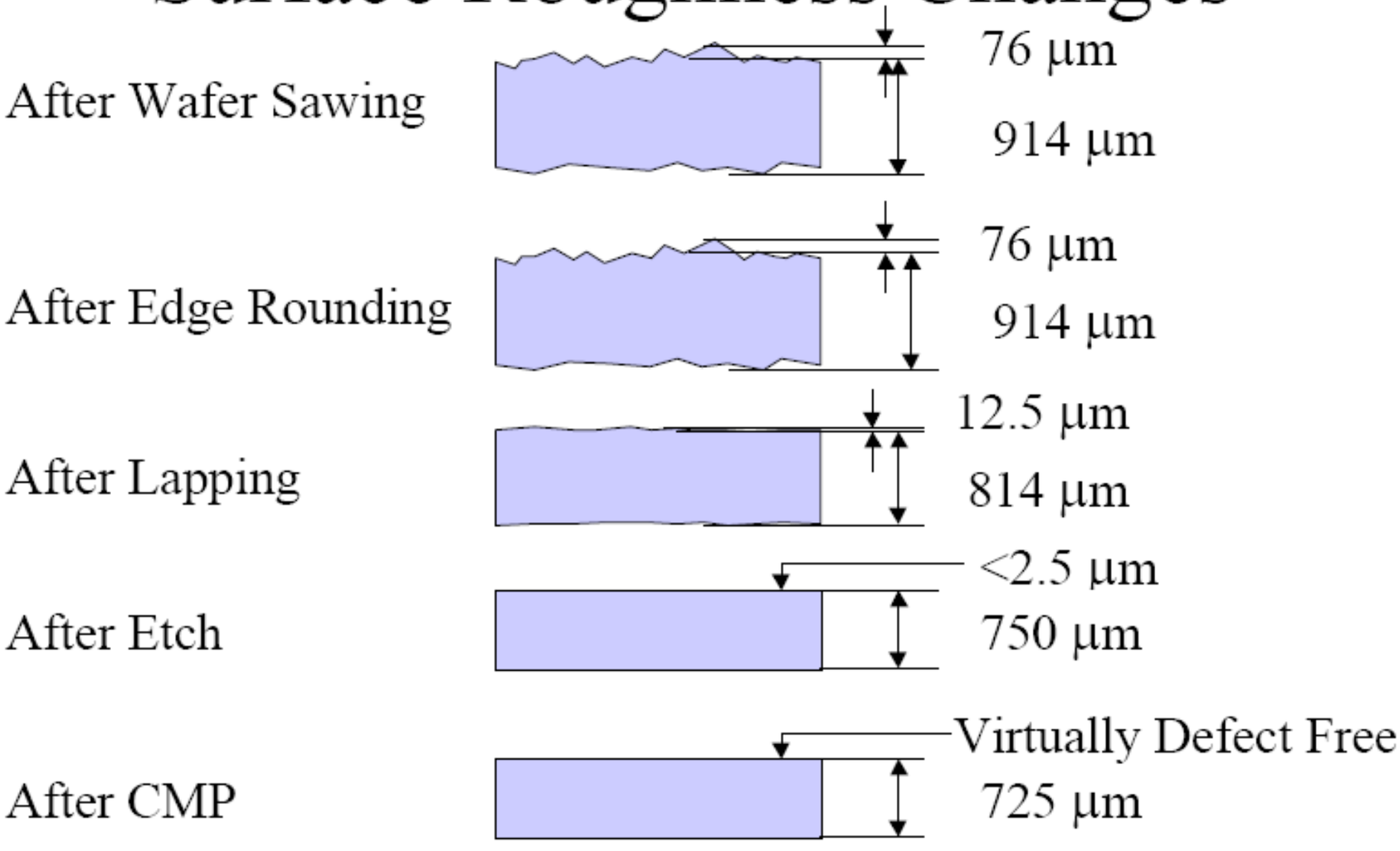
- Remove defects from wafer surface
- 4:1:3 mixture of HNO_3 (79 wt% in H_2O), HF (49 wt% in H_2O), and pure CH_3COOH.
- Chemical reaction:

$$3\ Si + 4\ HNO_3 + 6\ HF \rightarrow\ 3\ H_2SiF_6 + 4\ NO + 8\ H_2O$$

Chemical Mechanical Polishing



200 mm Wafer Thickness and Surface Roughness Changes



Epitaxy Grow

- Definition
- Purposes
- Epitaxy Reactors
- Epitaxy Process

Epitaxy: Definition

- Greek origin
- *epi*: upon
- *taxy*: orderly, arranged

- Epitaxial layer is a single crystal layer on a single crystal substrate.

Epitaxy: Purpose

- Barrier layer for bipolar transistor
  - Reduce collector resistance while keep high breakdown voltage.
  - Only available with epitaxy layer.
- Improve device performance for CMOS and DRAM because much lower oxygen, carbon concentration than the wafer crystal.

Silicon Source Gases

Silane		SiH_4
Dichlorosilane	DCS	SiH_2Cl_2
Trichlorosilane	TCS	$SiHCl_3$
Tetrachlorosilane		$SiCl_4$

Dopant Source Gases

Diborane	B_2H_6
Phosphine	PH_3
Arsine	AsH_3

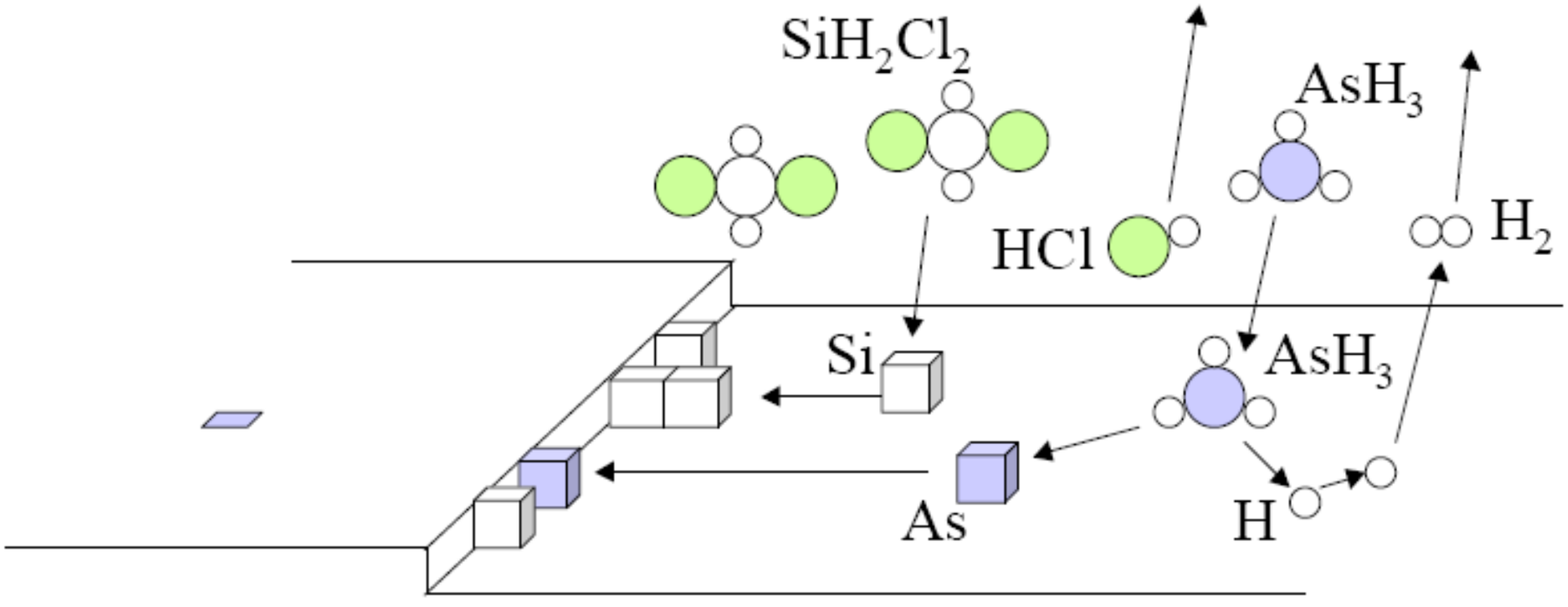
DCS Epitaxy Grow, Arsenic Doping

$$SiH_2Cl_2 \xrightarrow{\text{Heat (1100°C)}} Si + 2HCl$$

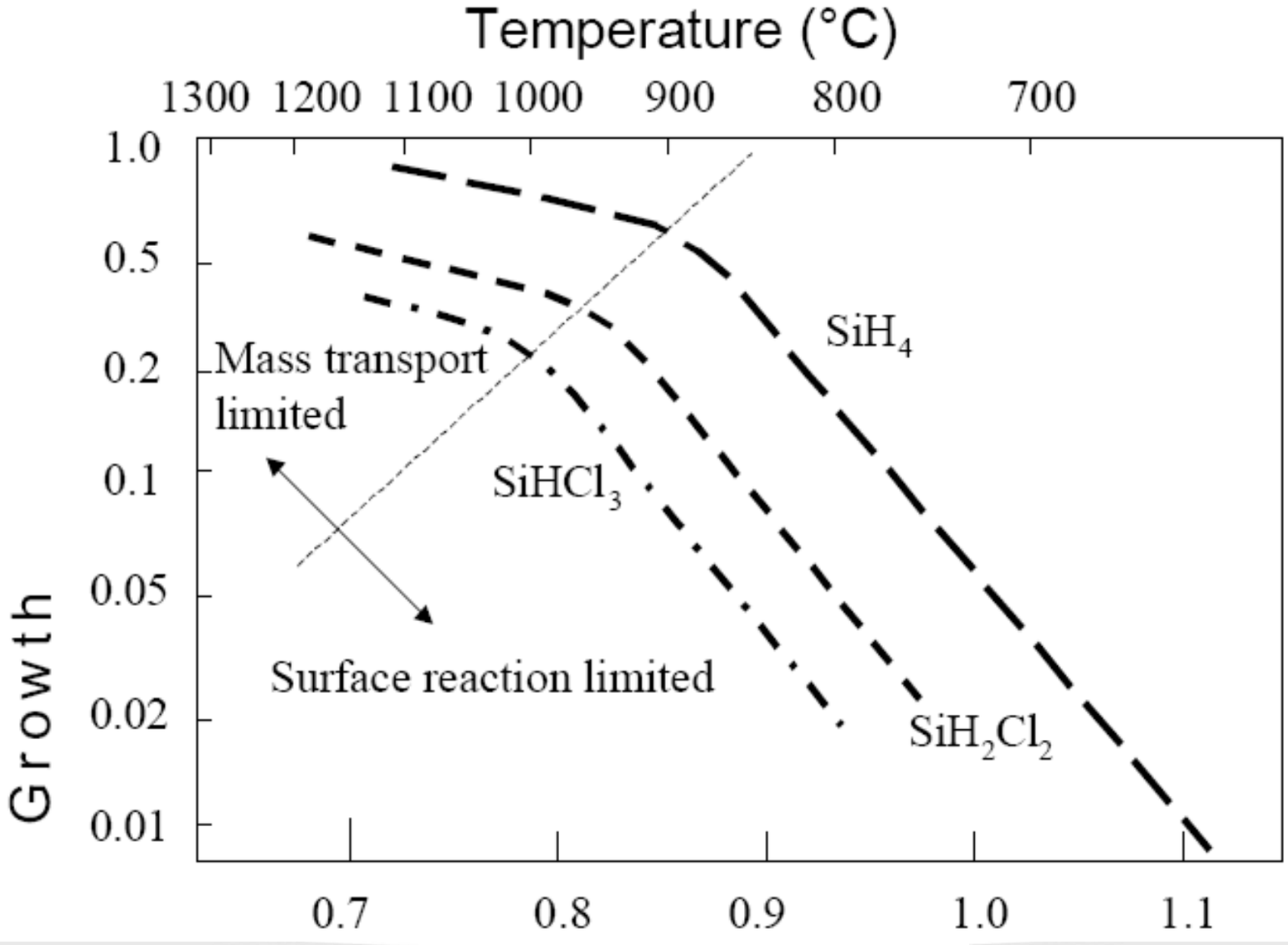
DCS — Epi — Hydrochloride

$$AsH_3 \xrightarrow{\text{Heat (1100°C)}} As + 3/2\ H_2$$

Schematic of DCS Epi Grow and Arsenic Doping Process



Epitaxial Silicon Growth Rate Trends



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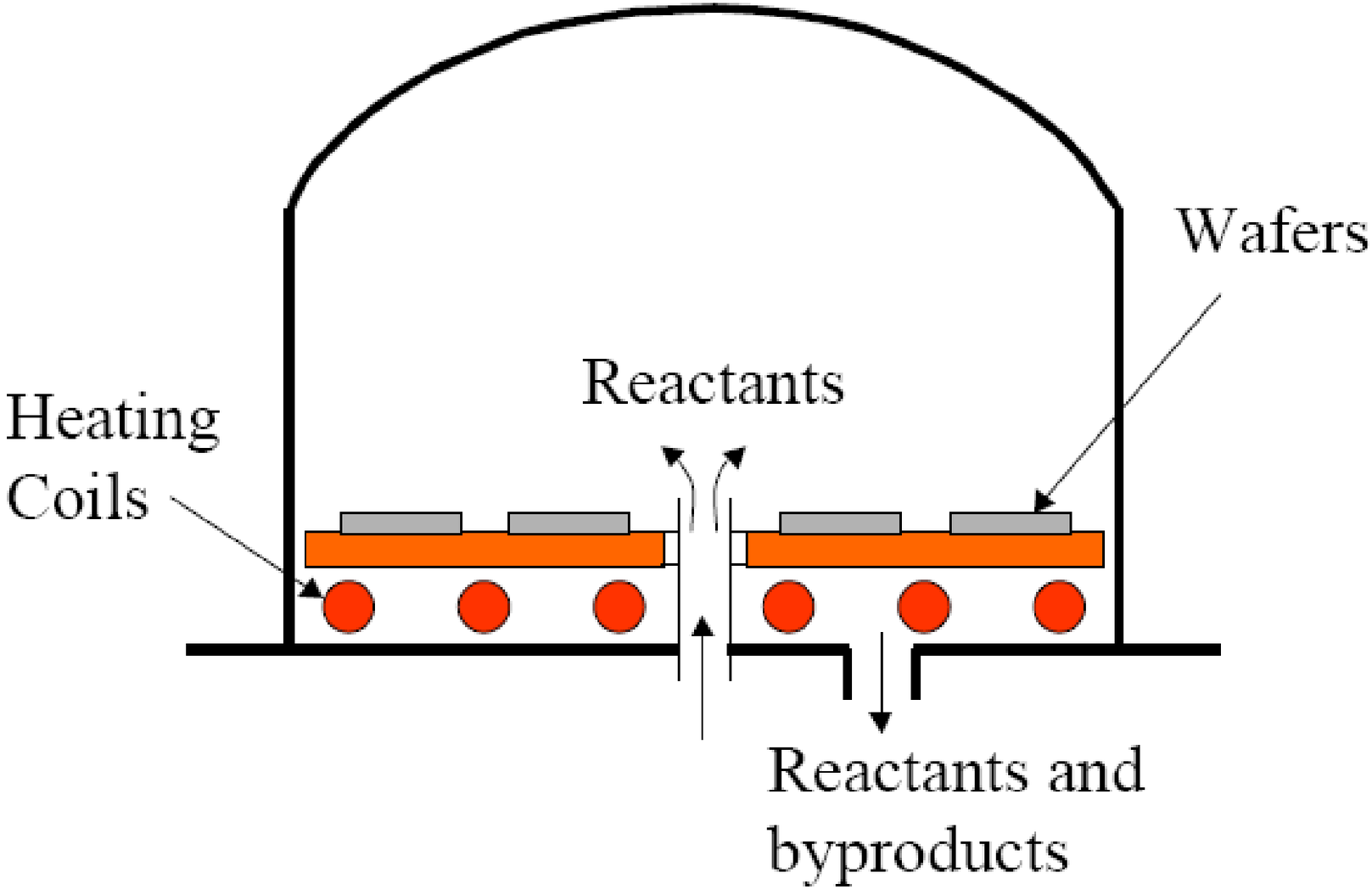
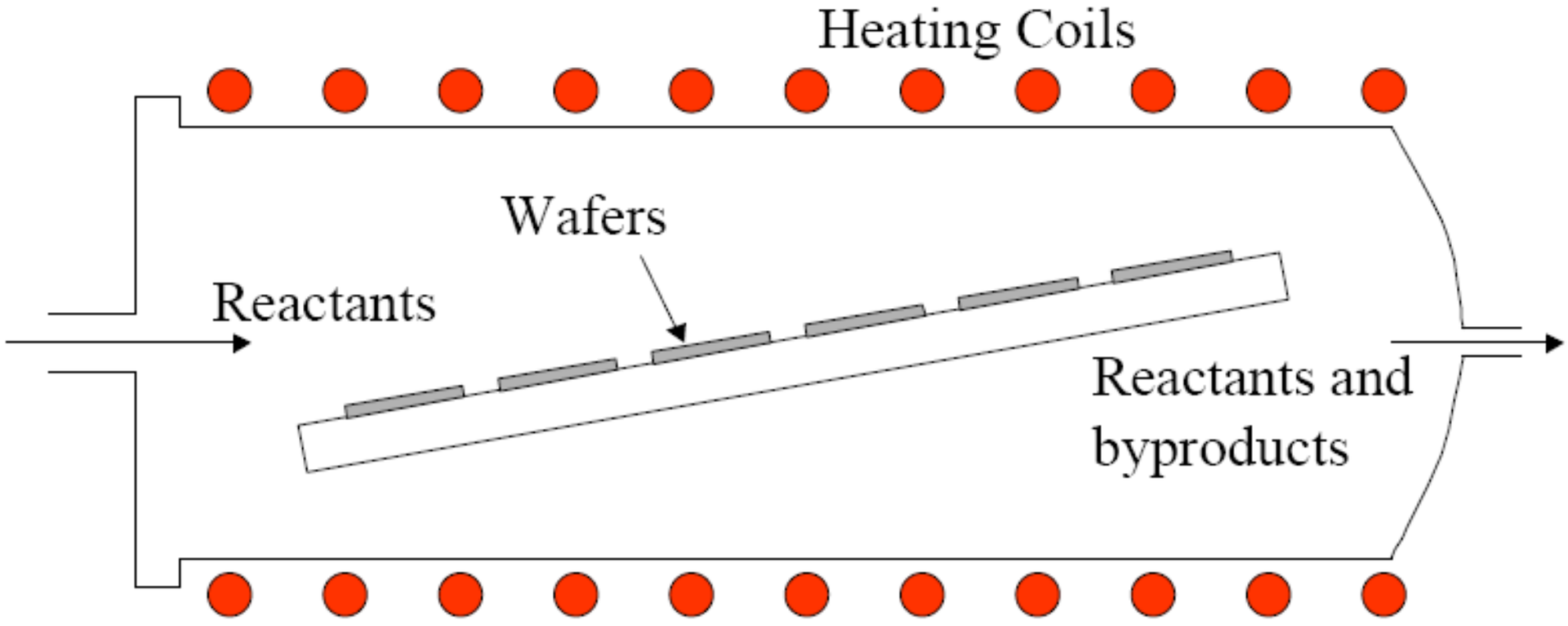
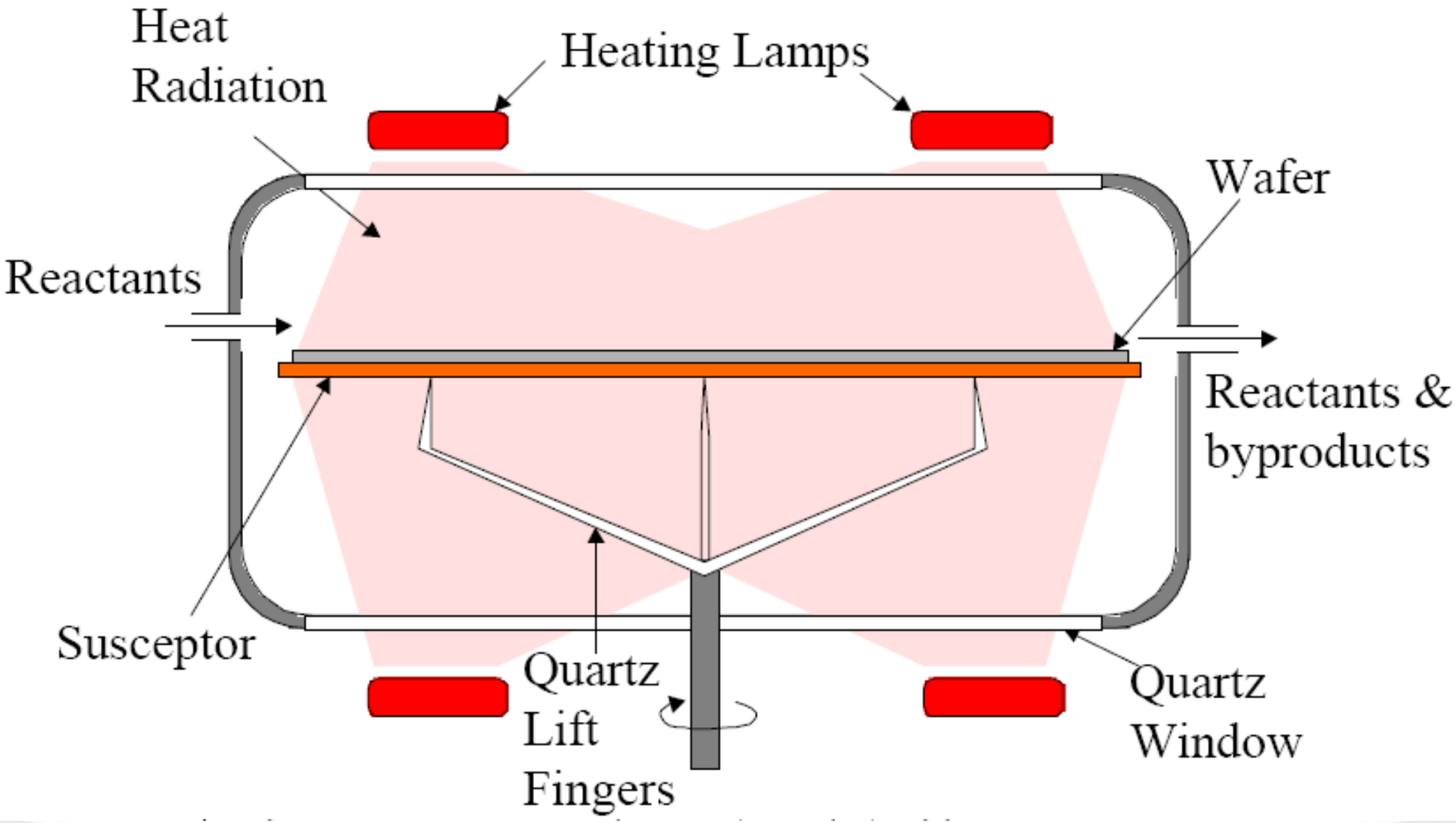
Vertical Reactor



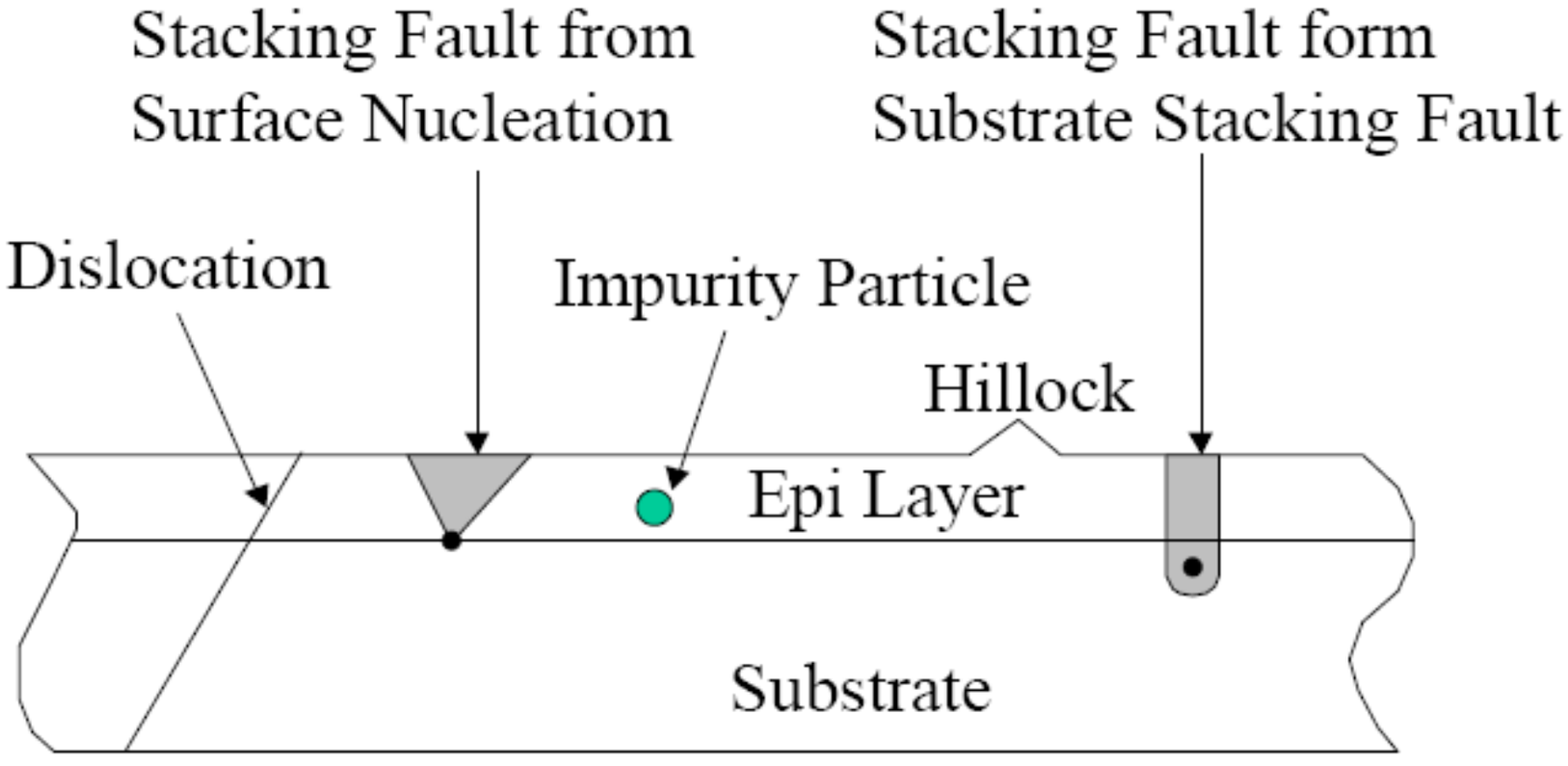
Horizontal Reactor



Single Wafer Reactor



Defects in Epitaxy Layer



After S.M. Zse's *VLSI Technology*

Table 1.3 Representative Impurity Concentrations in as-grown Si and GaAs Single Crystals.[†] [(a) Derived from References [1] and [9]; (b) Data from Hobgood et al.[2]]

(a) Si

Impurity	*Concentration (10^{15} atoms/cm^3)*
C	10–500
O	500–1000
Unintentional dopants (B, P, As, Sb)	≤0.05
Cr, Co, Ta, W, Na	Trace amounts (<0.005)
Cu, Au, Fe, Ni	Below detectable limits

(b) GaAs

Impurity	*Concentration (10^{15} atoms/cm^3)*
C	5
O	20
Si	0.5
S	1
Se	0.4
Te	0.01
Cr	0.4
Mg	0.7
Mn	0.8
B	500(2)[‡]

[†]The concentrations quoted here are for Si crystals formed by the Czochralski-pulled method and GaAs crystals formed by the Liquid Encapsulated Czochralski (LEC) technique. The reader should be cautioned that impurity concentrations considerably above the cited values can be introduced during the subsequent handling and processing of semiconductor crystals.[1]