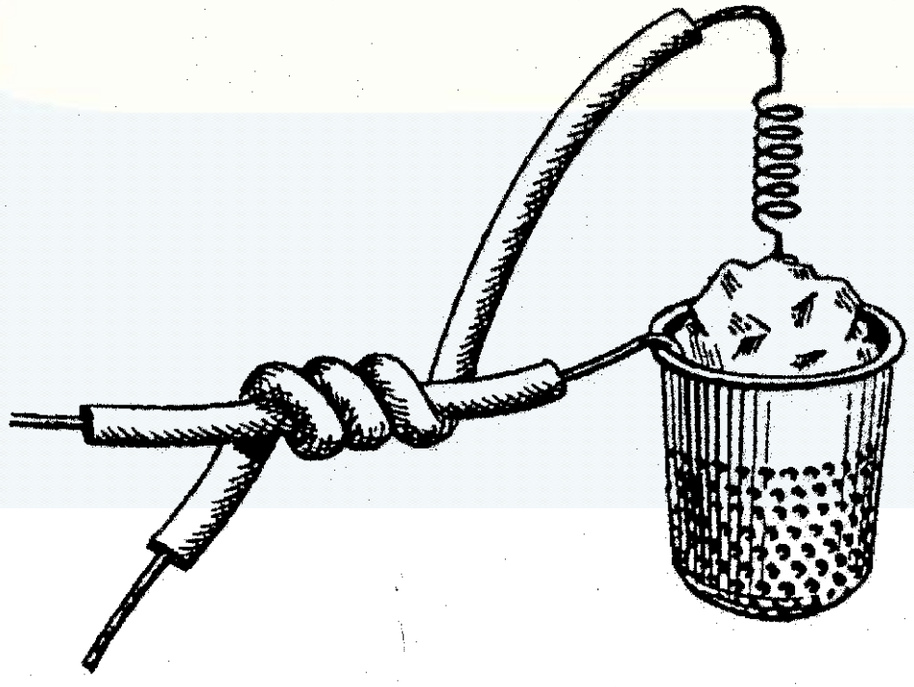
ELECTRONICS
Design Division

Introduction to semiconductor technology



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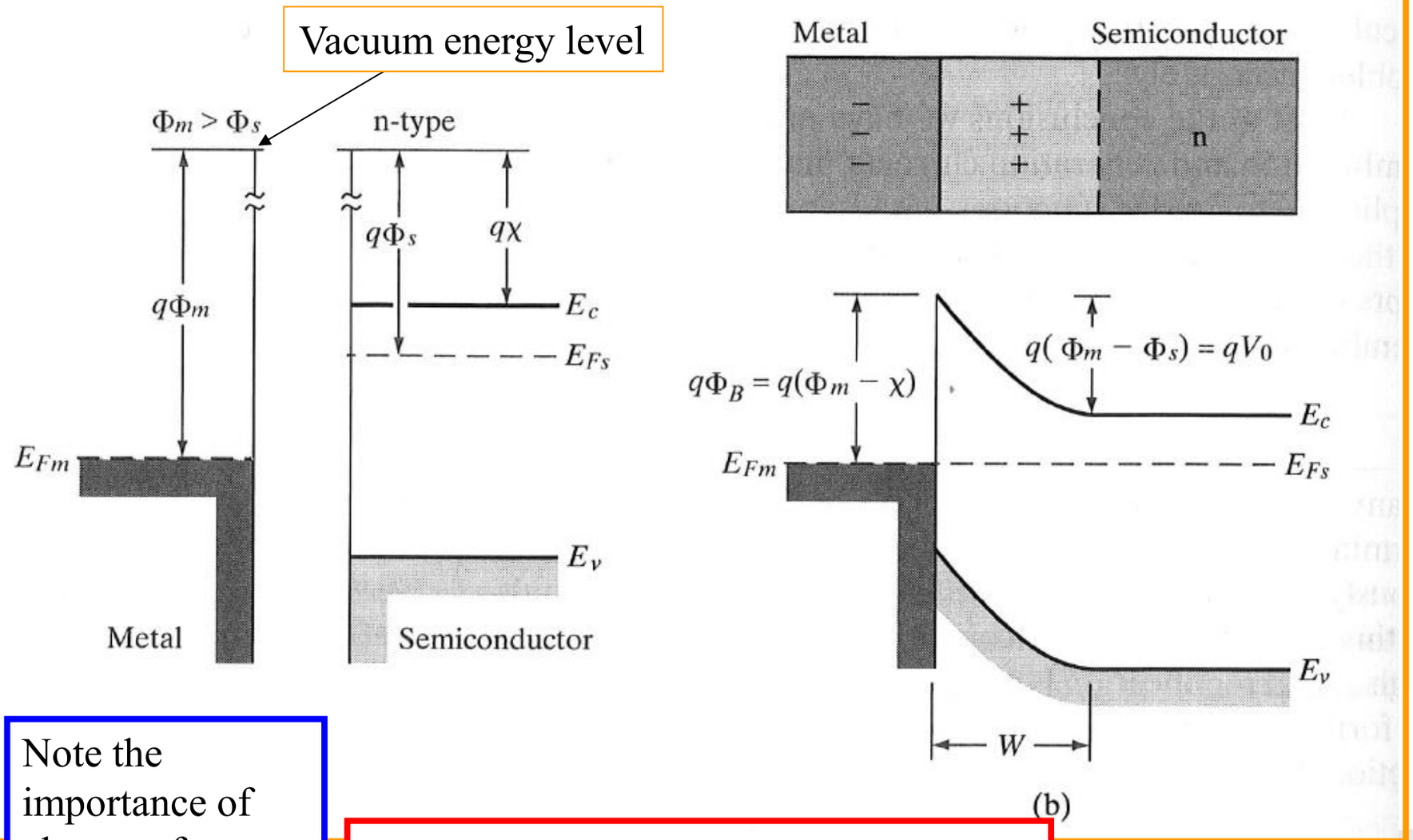
Outline

- **6 Junctions**
  - Metal-semiconductor junctions
- **6 Field effect transistors**
  - JFET and MOS transistors
  - Ideal MOS capacitance
  - Actual MOS capacitance
  - MOS transistor “current equation" (L7)
  - MOS-transitorn "transfer equation" (L7)
  - MOS-transitorn channel mobility (L7)
  - Substrate bias effect (L7)

Metal-semiconductor junctions, rectifying



Note the importance of clean surfaces prior deposition of metal

$$I = ABT^2 e^{-q\Phi_B/kT} e^{qV/\mathbf{n}kT}$$

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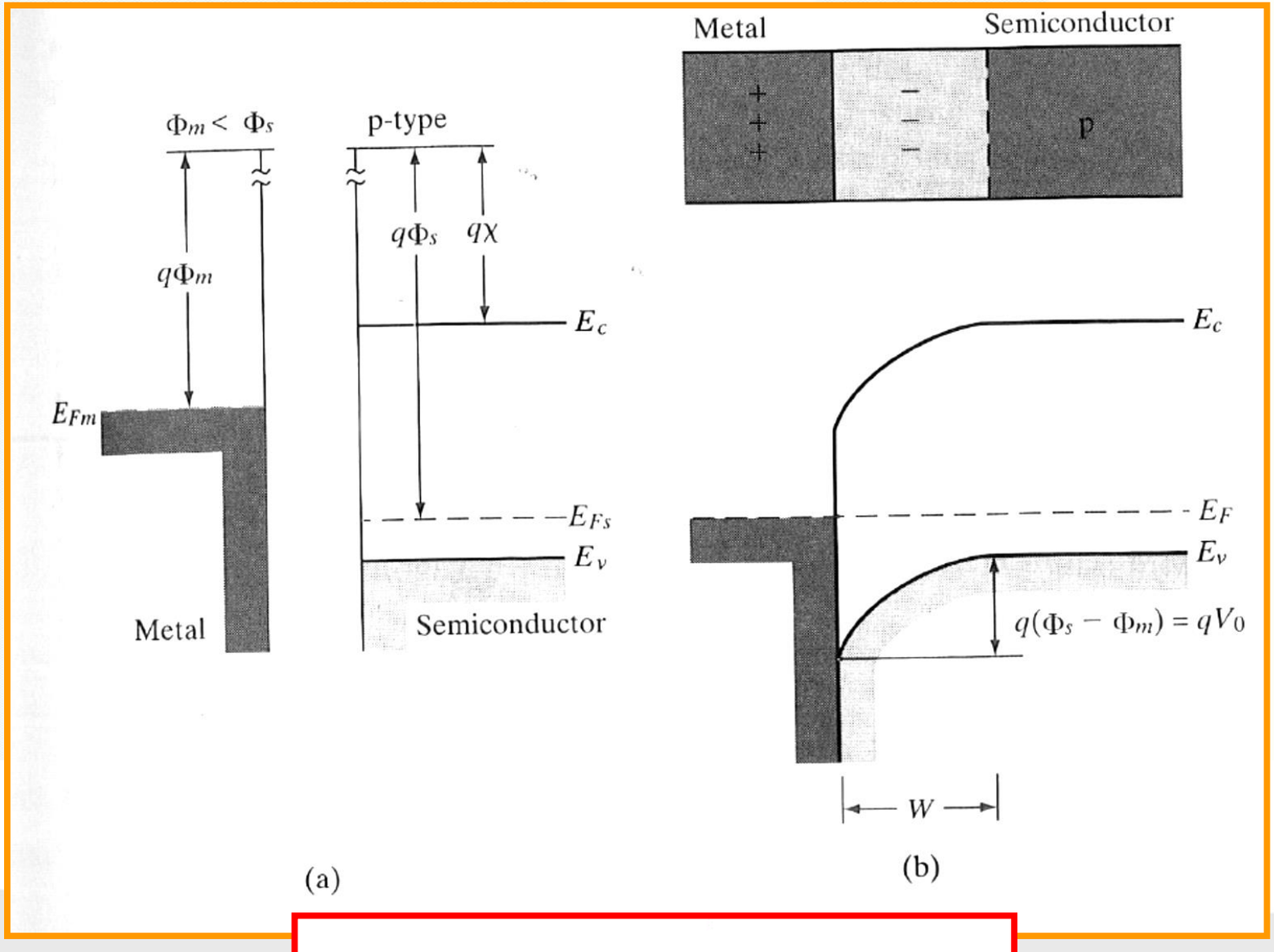
Metal-semiconductor junctions, rectifying



$$I = ABT^2 e^{-q\Phi_B/kT} e^{qV/\mathbf{n}kT}$$

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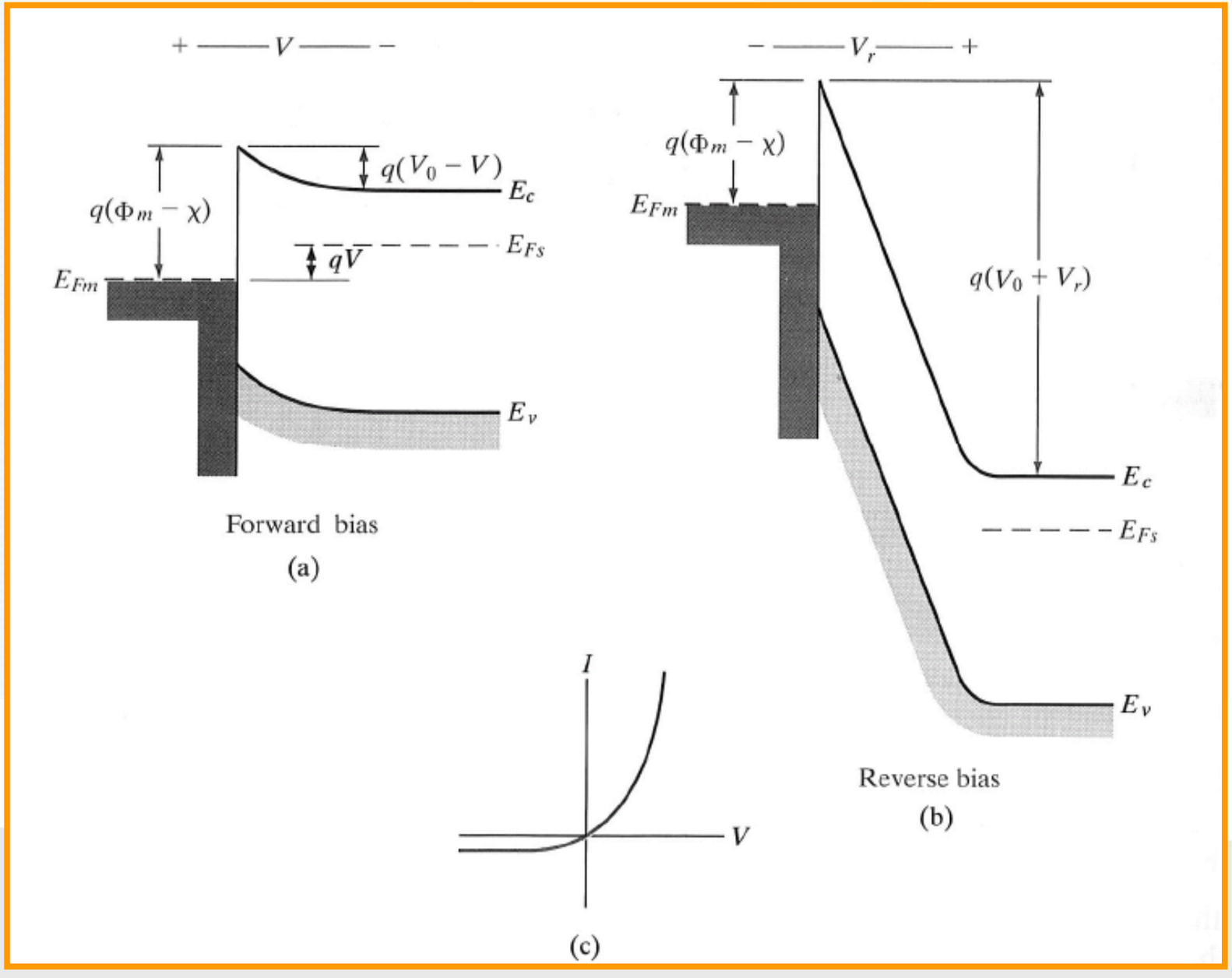
Metal-semiconductor junctions, rectifying, with bias



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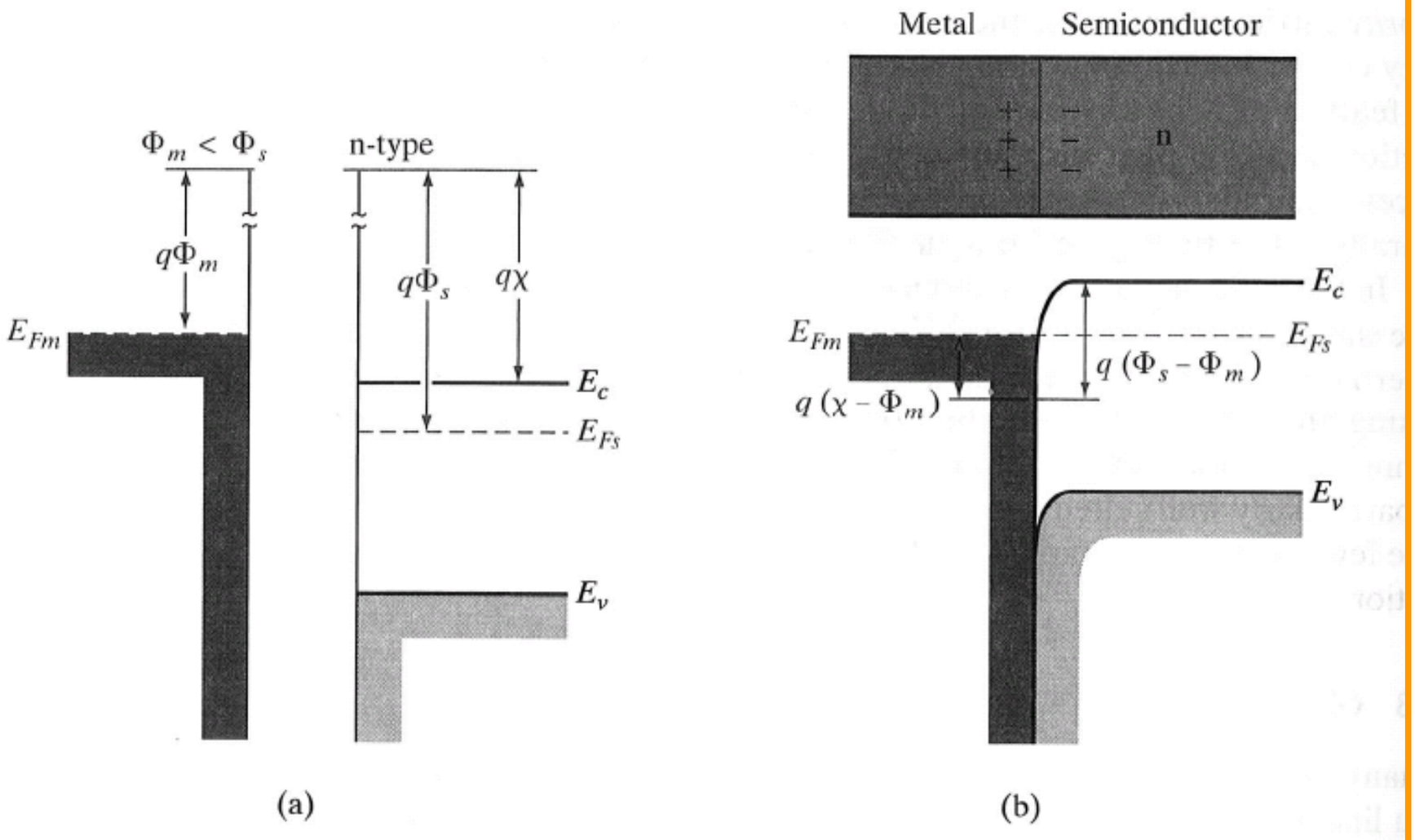
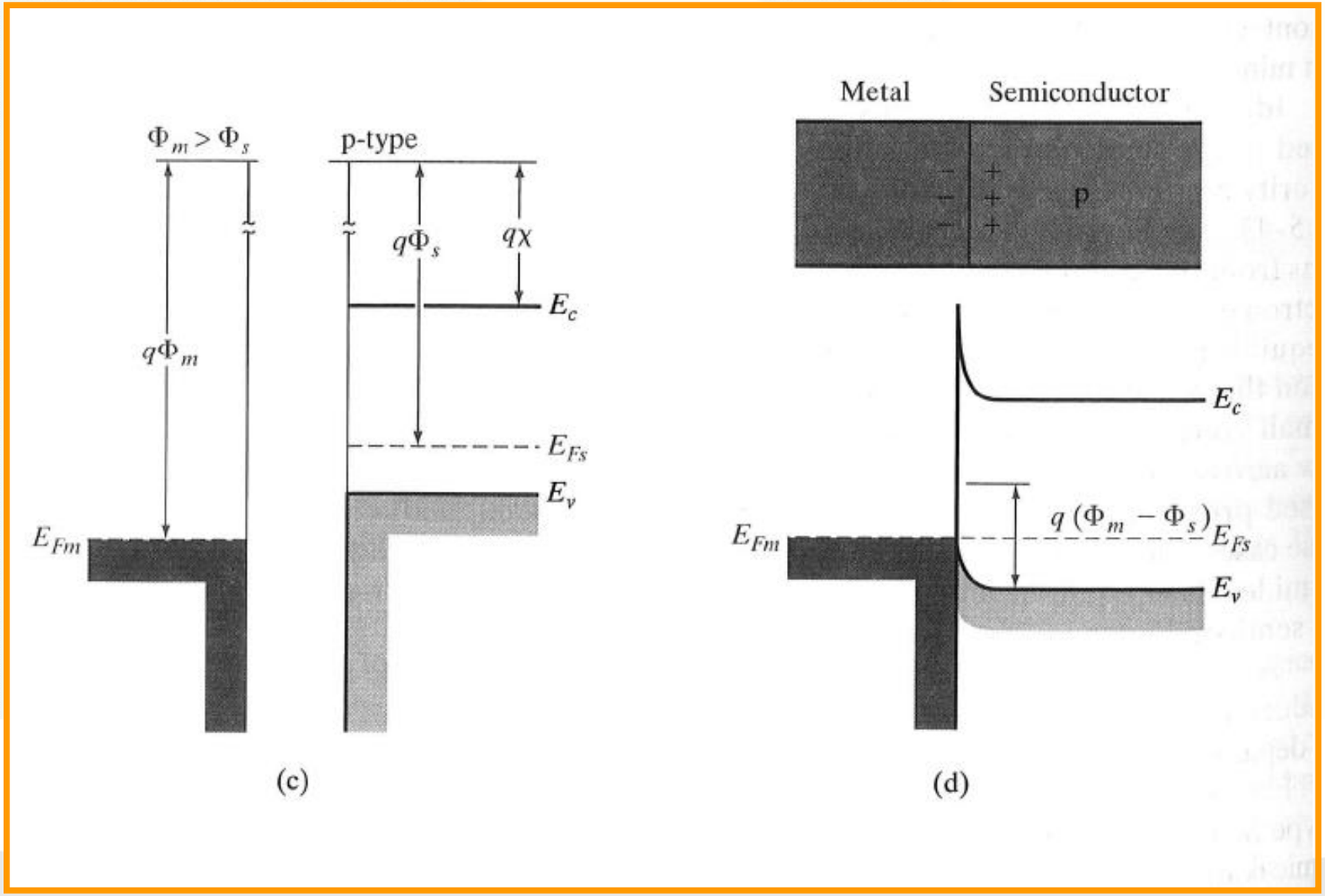
Metal-semiconductor junctions, ohmic, n-substrate



Metal-semiconductor junctions, ohmic, p-substrate



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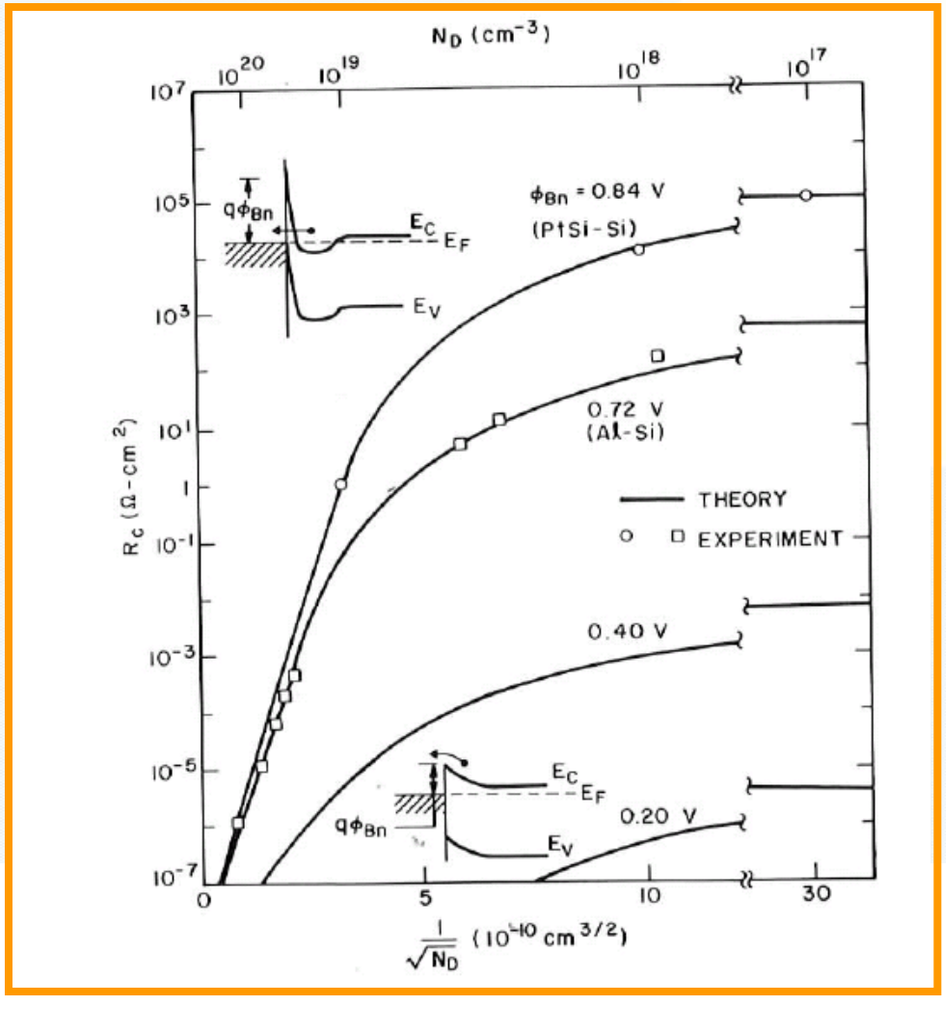
Metal-semiconductor junctions, ohmic, tunneling



Although there is a barrier between the metal and semiconductor, it is possible to make a good ohmic contact, hard doping under the metal so that the tunneling occurs

If the metal has high barrier height to n-type, the most likely low barrier height for p-type. Exceptions exist, so called Fermi-level pinning

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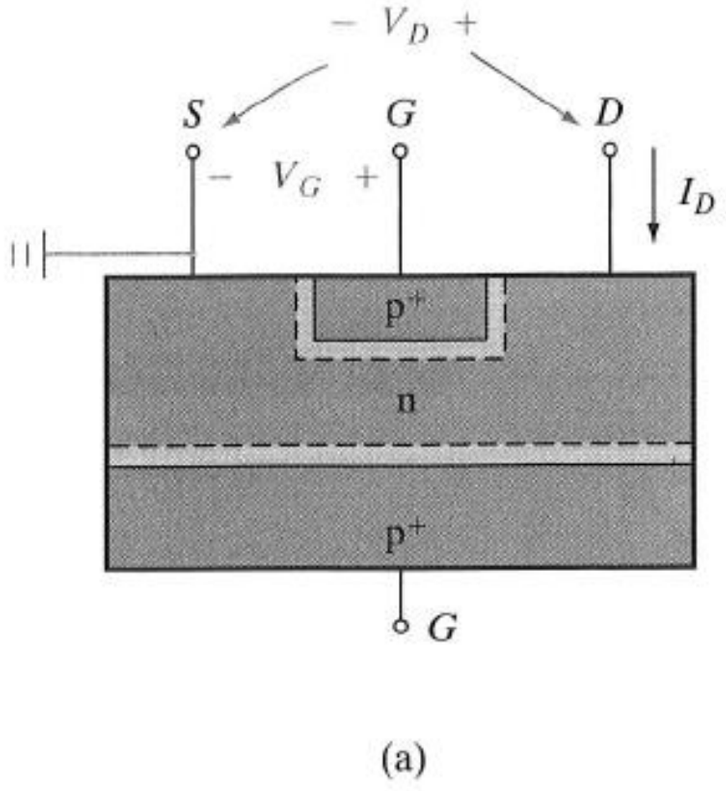
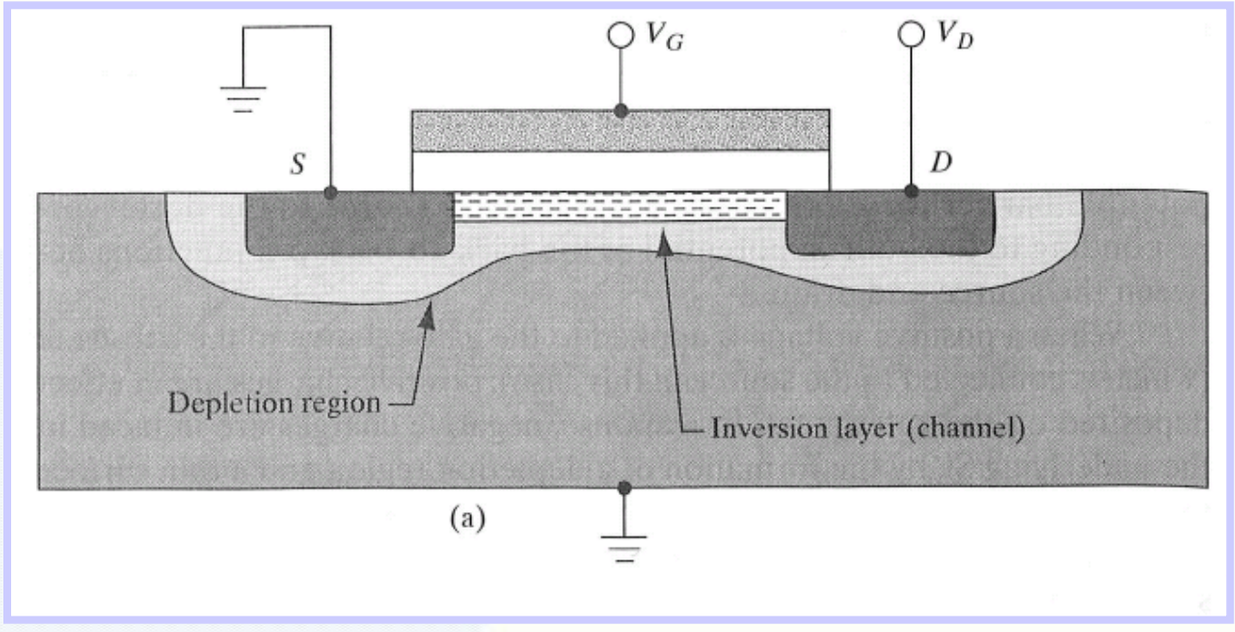
Field effect transistors (FET)

Junction-FET



Metal-oxid-halvledar-FET



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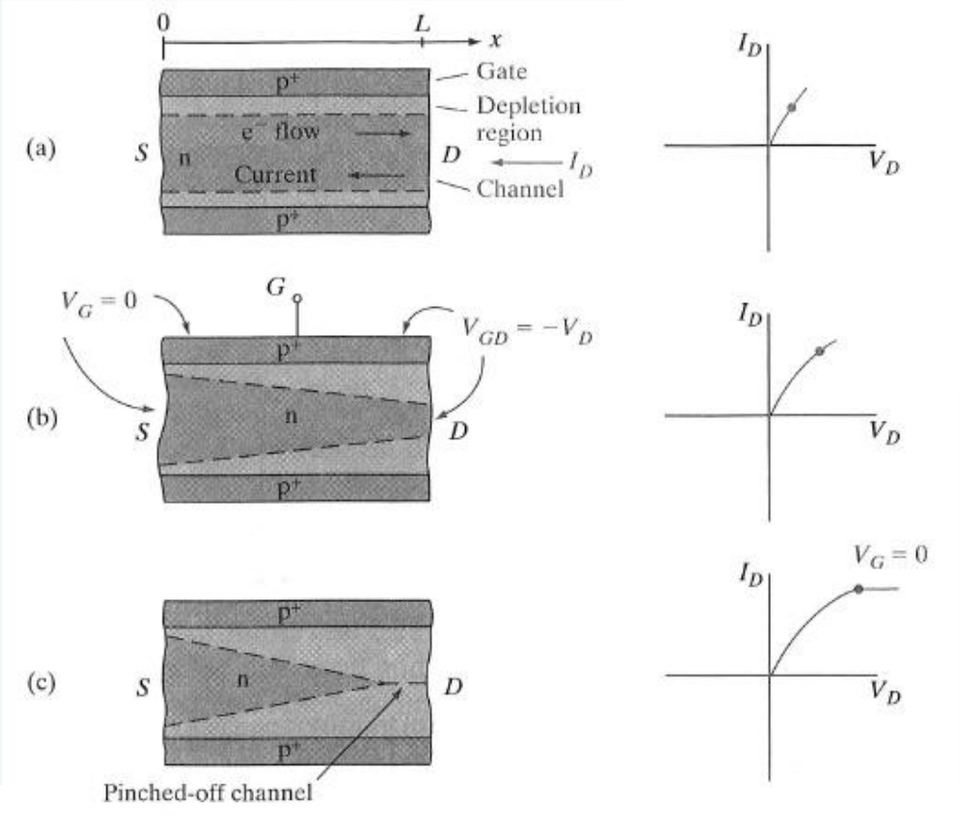
Junction-FET (pinch of the channel and saturation)

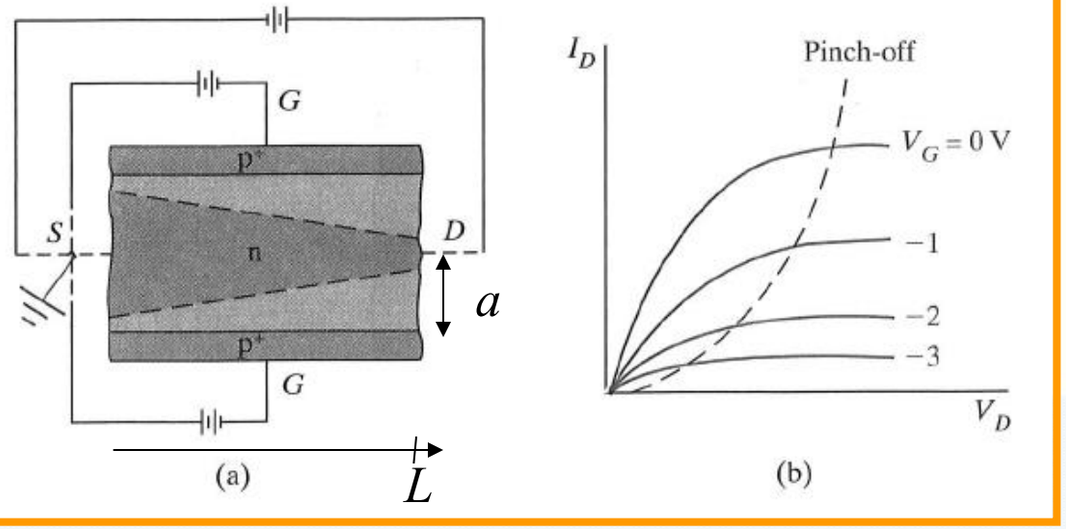


When the drain voltage increases reverse bias the gate/drain.

The depletion region spreads and chokes the channel, Id stop increasing and becomes constant.

Compare with constant current generator

Junction-FET (Gate control)



With modified gate voltage level can the saturation of the current be controlled.

For a p^+n diode applies;

$$W(x = L) = \left[\frac{2\epsilon(-V_{GD})}{qN_d}\right]^{1/2} \quad (V_{GD} \text{ negative})$$

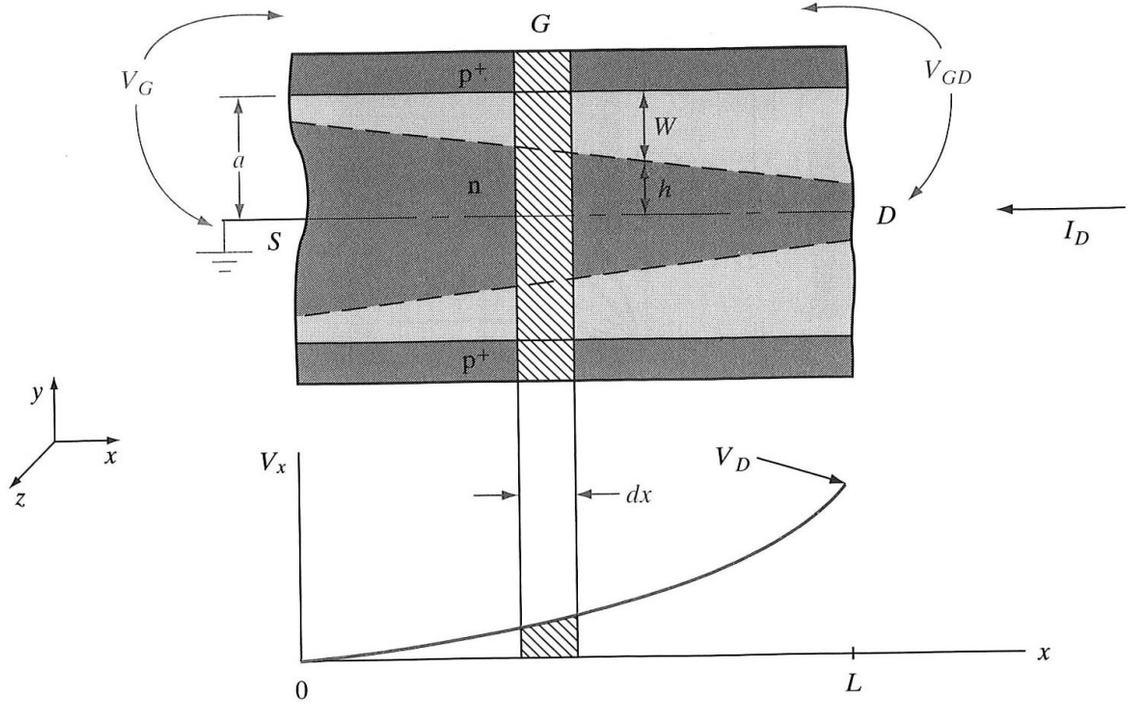
$$\left[\frac{2\epsilon V_P}{qN_d}\right]^{1/2} = a$$

$$V_P = \frac{qa^2N_d}{2\epsilon}$$

When w = a, is precisely depleted, we have reached pinchoff voltage

Note, the junction should not be biased in forward direction

Junction-FET (current-voltage characteristics, long channel)



Current in a cross-section caused by a voltage drop

$$I_D = \frac{Z2h(x)}{\rho}\frac{dV_x}{dx}$$

$$h(x) = a - W(x) = a - \left[\frac{2\epsilon(-V_{Gx})}{qN_d}\right]^{1/2} = a\left[1 - \left(\frac{V_x - V_G}{V_P}\right)^{1/2}\right]$$

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Junction-FET (current-voltage characteristics, long channel)

$$\frac{2Za}{\rho}\left[1-\left(\frac{V_x - V_G}{V_P}\right)^{1/2}\right]dV_x = I_D dx$$

Valid up to V_p

$$I_D = G_0 V_P\left[\frac{V_D}{V_P} + \frac{2}{3}\left(-\frac{V_G}{V_P}\right)^{3/2} - \frac{2}{3}\left(\frac{V_D - V_G}{V_P}\right)^{3/2}\right]$$

$G_0 \equiv 2aZ/\rho L$

$V_D - V_G = V_P$ 

Junction-FET (current-voltage characteristics, long channel)

At saturation applies

$$I_D(\text{sat.}) = G_0 V_P \left[\frac{V_D}{V_P} + \frac{2}{3}\left(-\frac{V_G}{V_P} \right)^{3/2} - \frac{2}{3} \right]$$

$$= G_0 V_P \left[\frac{V_G}{V_P} + \frac{2}{3}\left(-\frac{V_G}{V_P} \right)^{3/2} + \frac{1}{3} \right]$$

V_D-V_G=V_P

$$g_m(\text{sat.}) = \frac{\partial I_D(sat.)}{\partial V_G} = G_0 \left[1 - \left(-\frac{V_G}{V_P} \right)^{1/2} \right]$$

I_{DSS}=I_{dsat} (V_G=0)

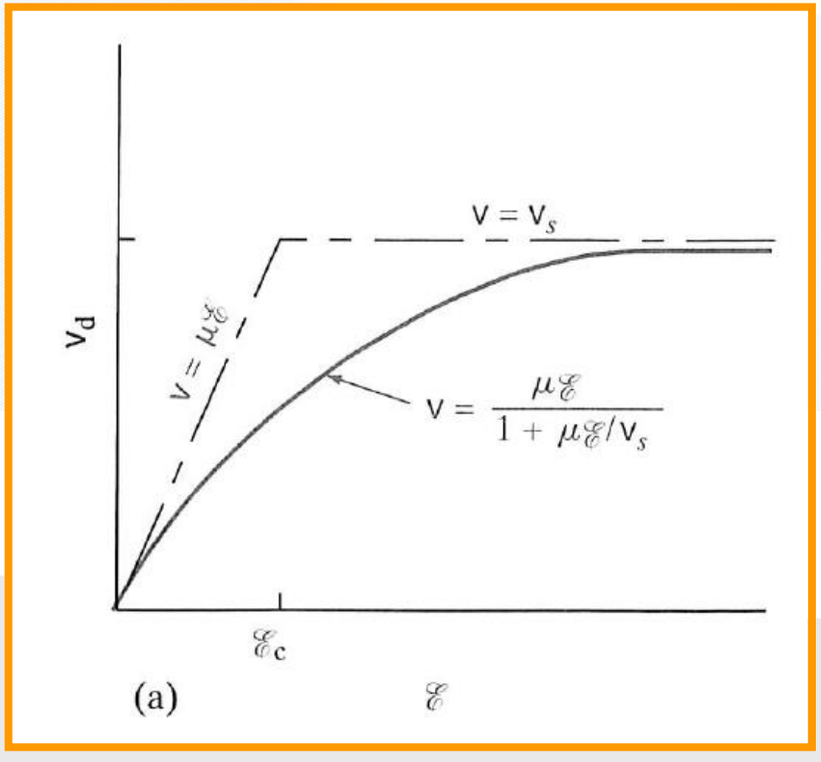
$$I_D(\text{sat.}) \simeq I_{DSS}\left(1 + \frac{V_G}{V_P} \right)^2, \quad (V_G \, negative)$$

Verifierad experimentellt

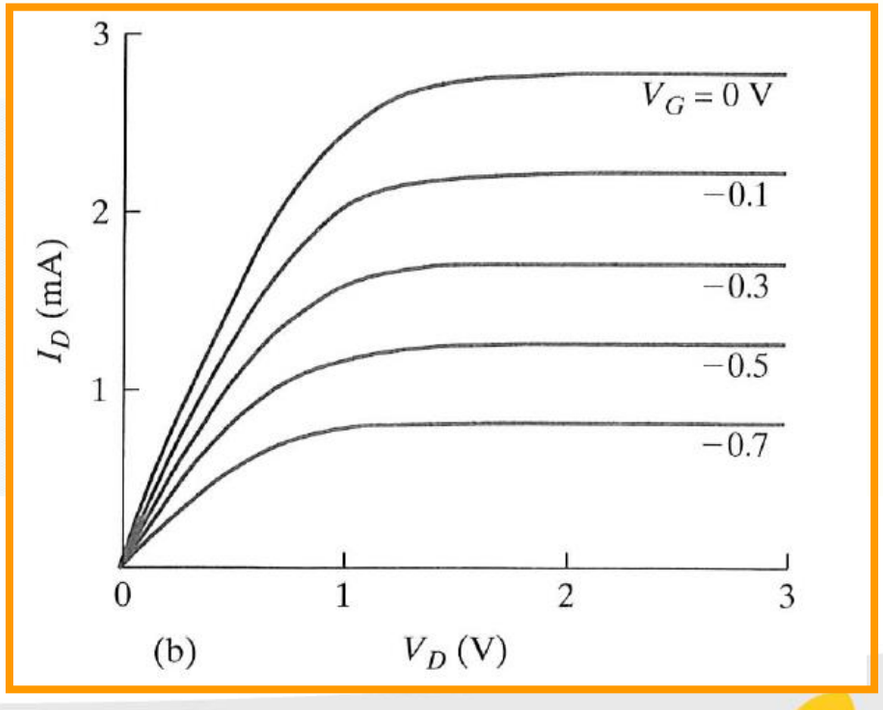
Short channel effects

- With a short channel increases the electric field and the charge carrier reach saturation velocity

$$v_d = \frac{\mu \mathscr{E}}{1 + \mu \mathscr{E}/v_s}$$



$$I_D = qnv_sA = qN_dv_sZh$$



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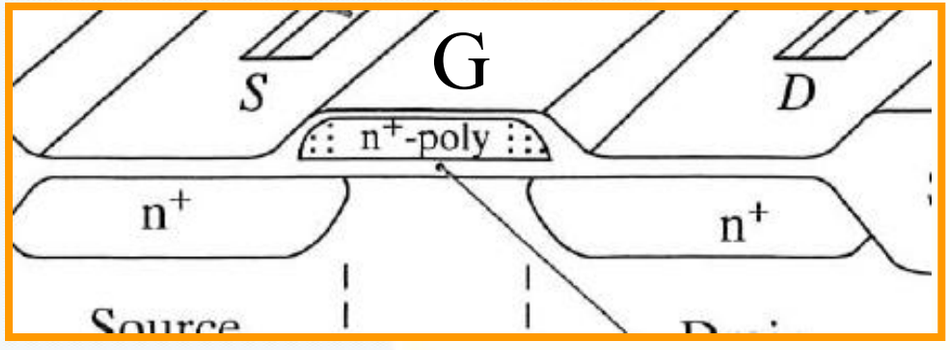
MOS-transistorn

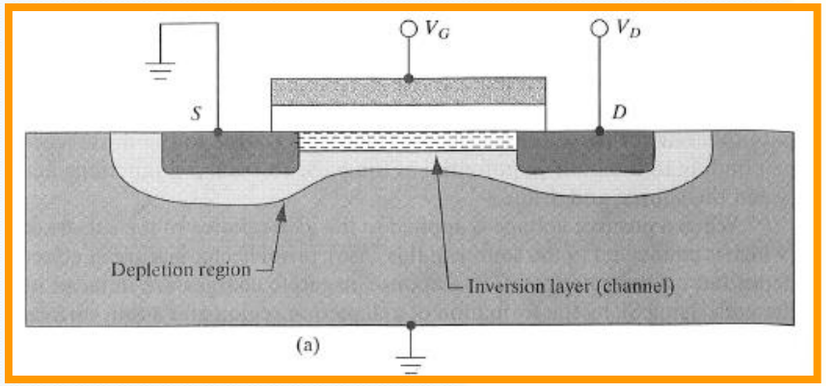


Voltage is applied on the gate and capacitive attracts electrons to form a leading channel

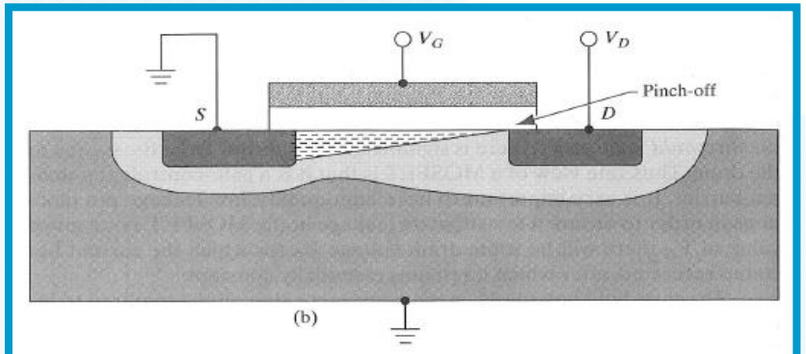
Or

Depleting the channel to block the transistor

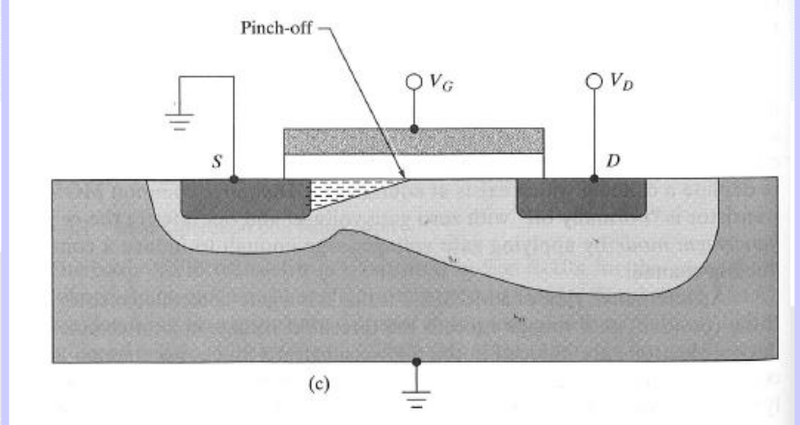
MOS-transistorn



MOS transistor with conducting channel (inversion layer)



Incipient pinch off channel with applied drain voltage



Strong saturation

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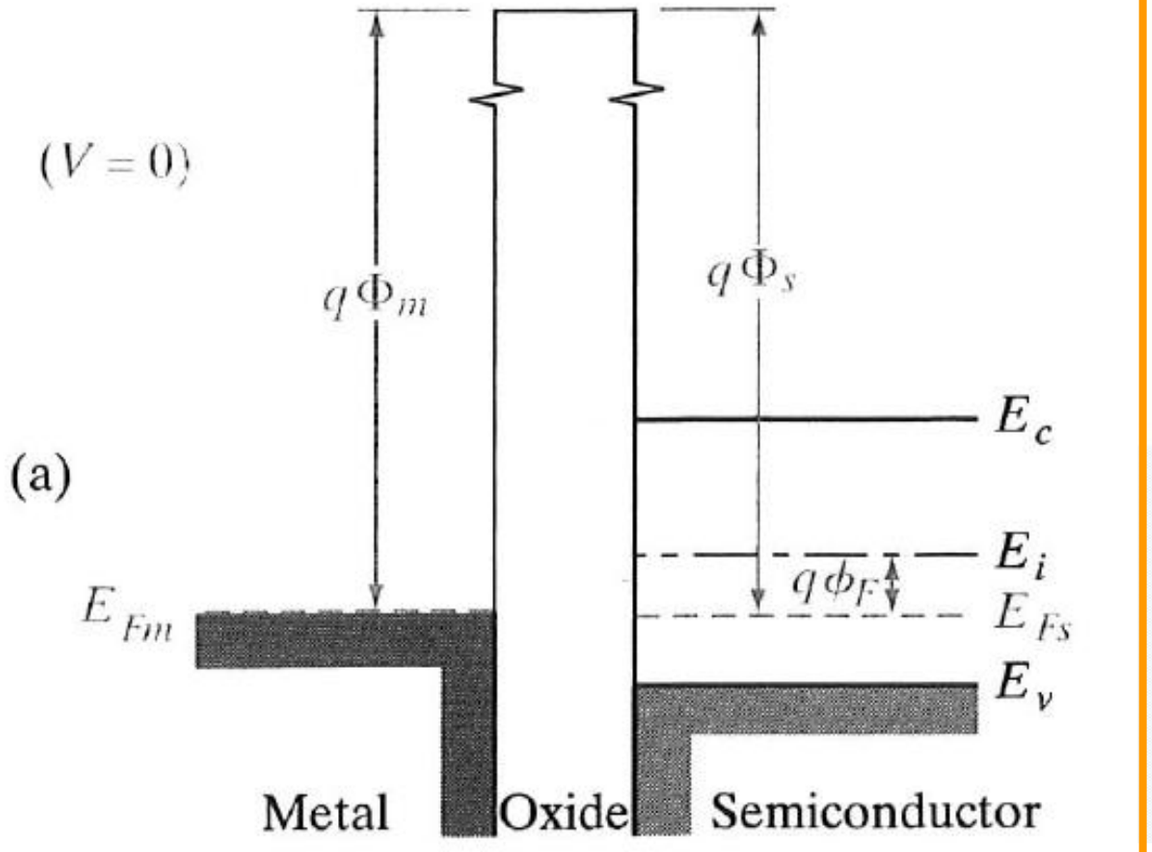
Ideal MOS capacitance



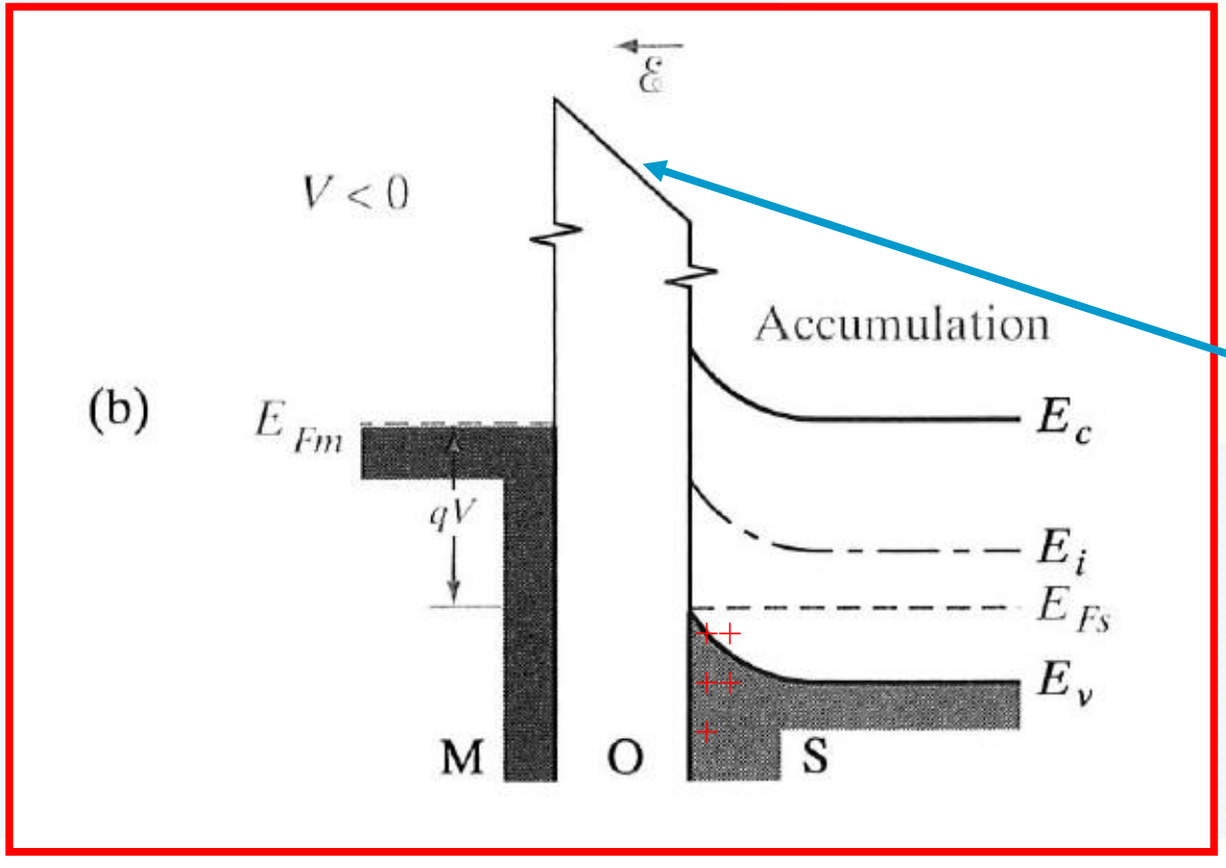
metal

SiO_2

Semiconductor

Work function is measured from the oxides conduction band, “modified"

Ideal MOS capacitance



Accumulated holes is collected by the interface oxide semiconductors

Tilt of the conduction band caused by the electric field

$$\mathscr{E}(x) = \frac{1}{q}\frac{dE_i}{dx}$$

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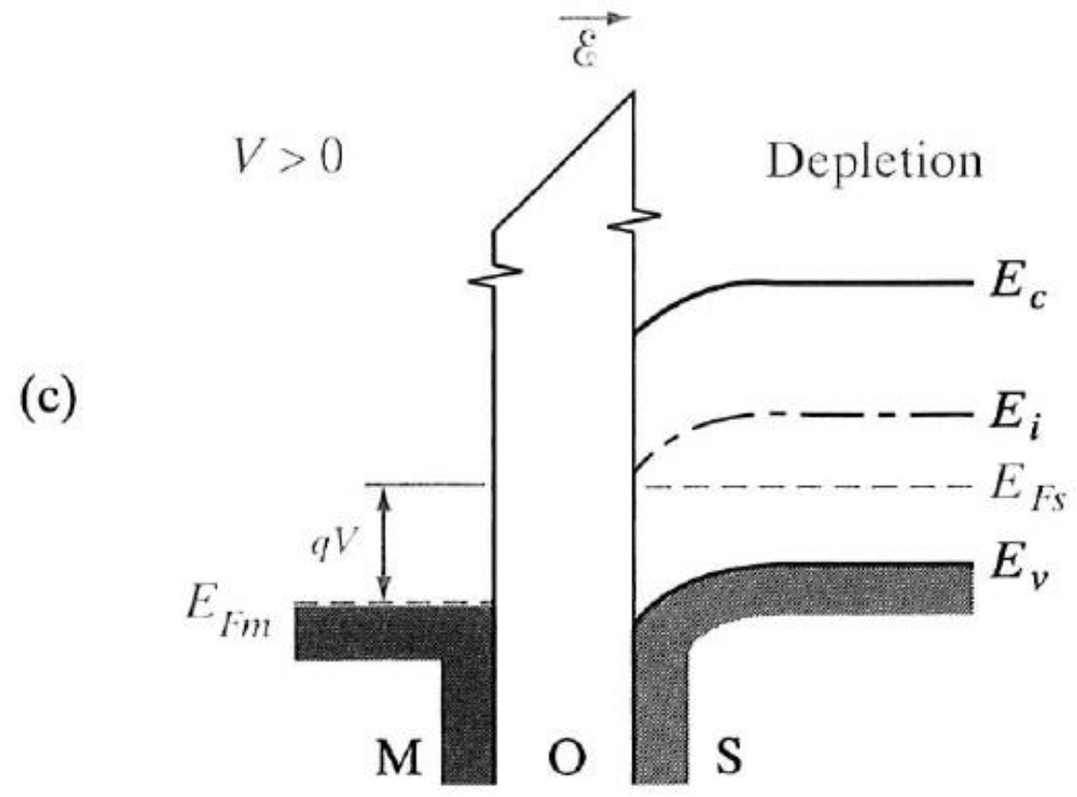
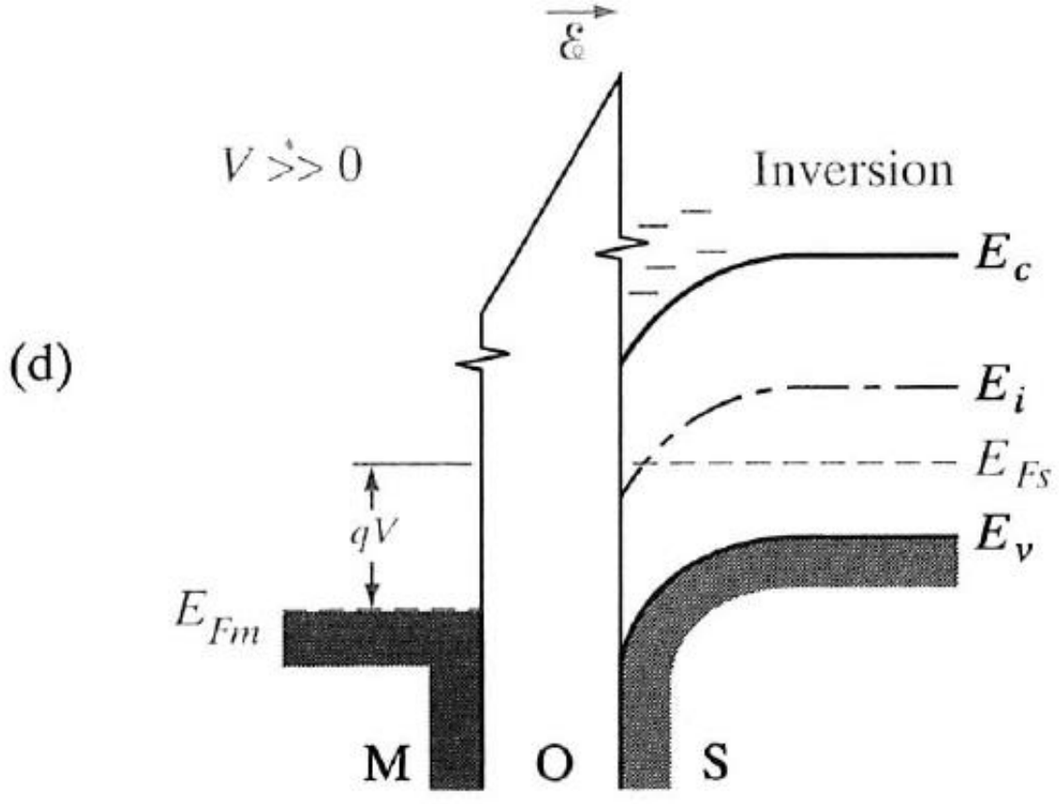
Ideal MOS capacitance



Depletion region is formed nearest the oxide/ semiconductor interface

Ideal MOS capacitance



Inversion, a layer of electrons are formed at oxide/ semiconductor interface

Ideal MOS capacitance, strong inversion

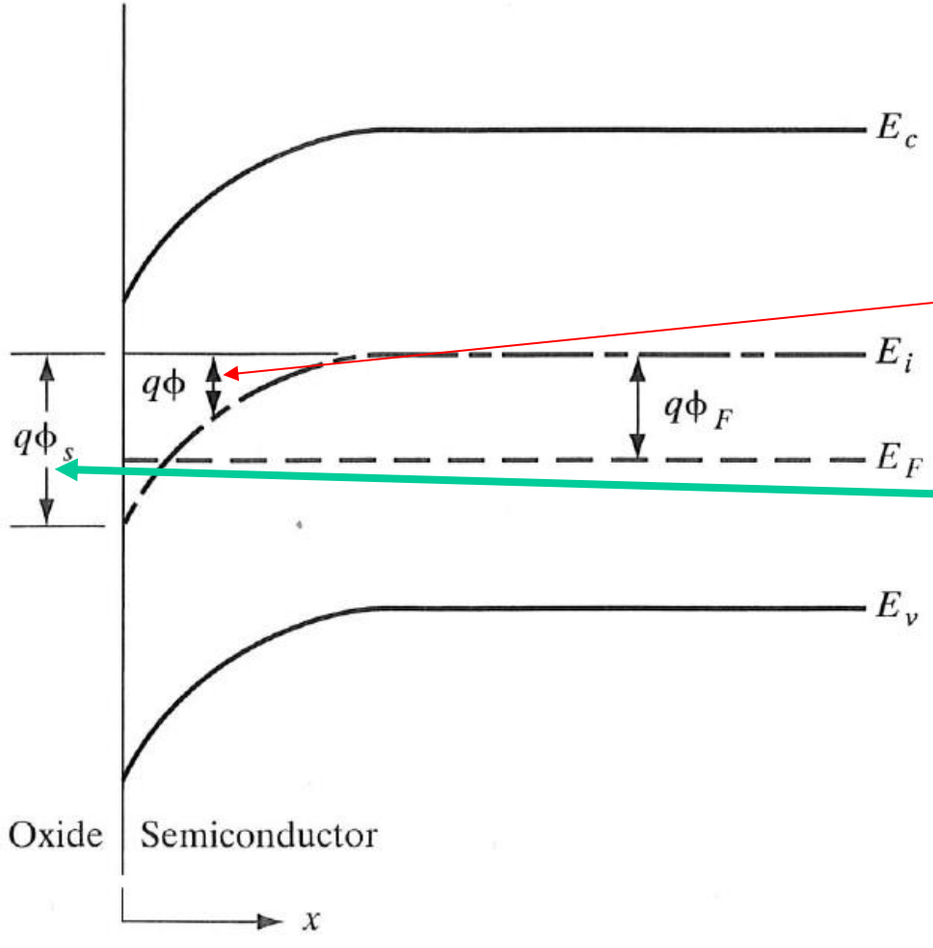
n conc (inversion) = p doping in the substrate

Example 3-5

$$\phi_s(\text{inv.}) = 2\phi_F = 2\frac{kT}{q}\ln\frac{N_a}{n_i}$$

Describes the band bending f(x)

Band bending at the interface, due to surface potential



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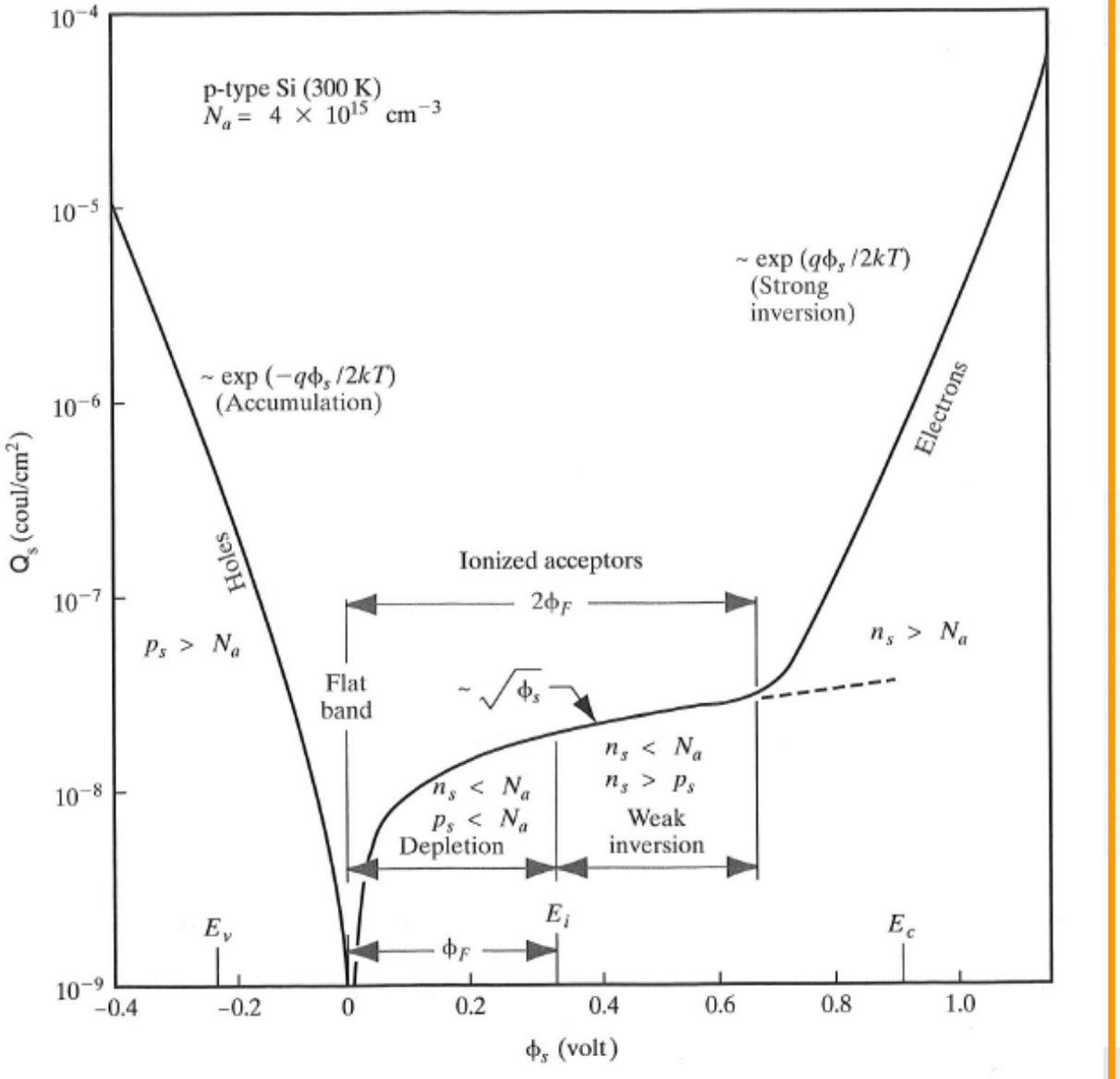
Ideal MOS capacitance



Space charge density as a function of surface potential

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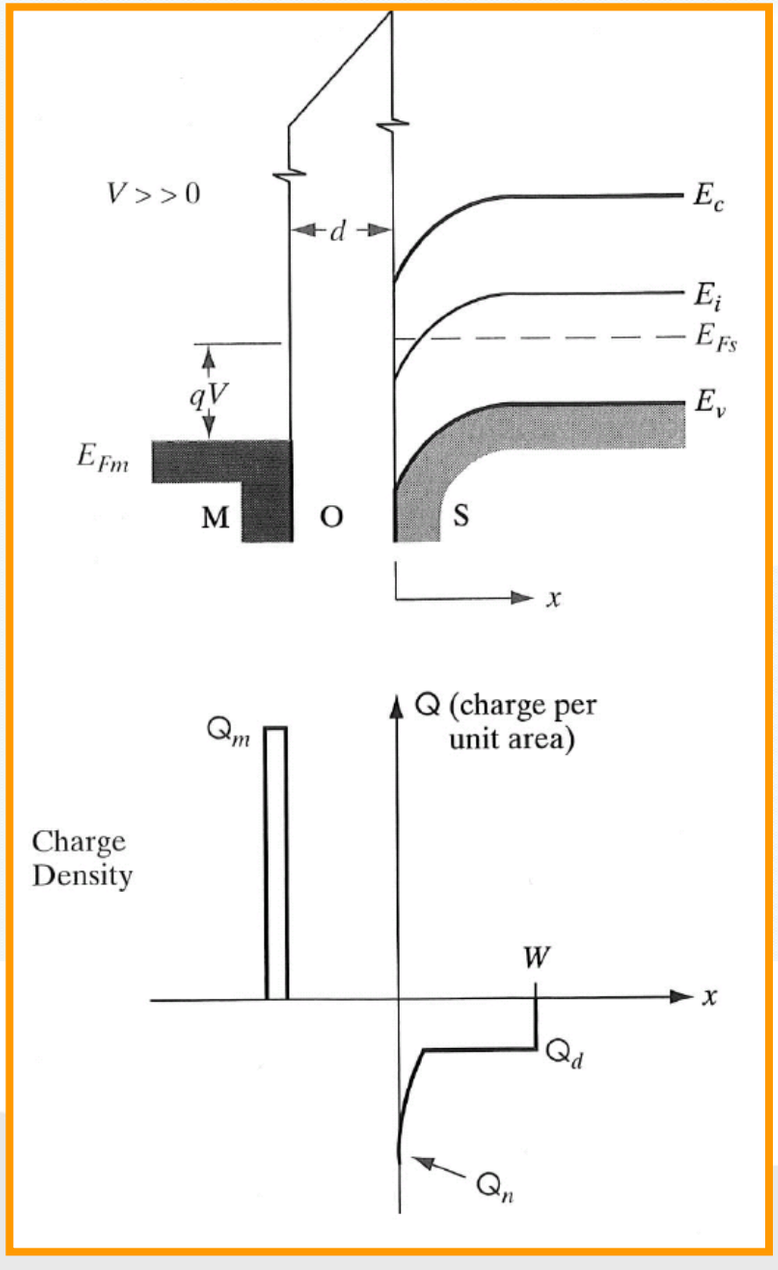
Ideal MOS capacitance, in inversion



$$Q_m = -Q_s = qN_aW - Q_n$$

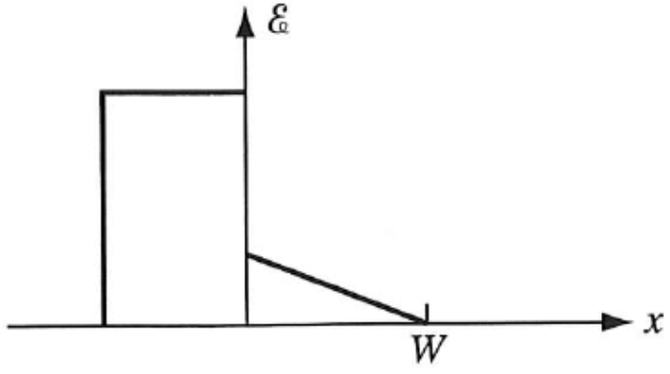
equal number of charges in the metal as in the semiconductor

NOTE no charges in oxide in this case.

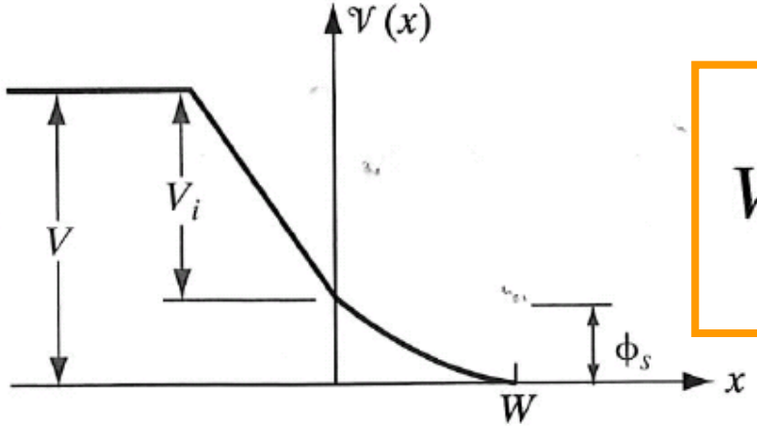
In true MOS structures, are always charges in oxide

Ideal MOS capacitance, in inversion

Electric Field



Electrostatic Potential



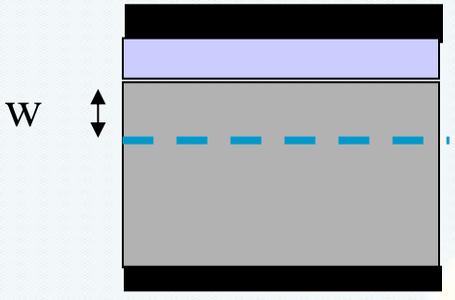
Inversions charge is not included in the drawings for the electric field and potential

$$V = V_i + \phi_s$$

$$V_i = \frac{-Q_s d}{\epsilon_i} = \frac{-Q_s}{C_i}$$

Voltage drop across oxide

Ideal MOS-kapacitans, in inversion



metal
SiO_2

semiconductor

W is calculated as if
it were a **n^+p-diode**

$$W = \left[\frac{2\epsilon_s \phi_s}{qN_a}\right]^{1/2}$$

$$W_m = \left[\frac{2\epsilon_s \phi_s(\text{inv.})}{qN_a}\right]^{1/2} = 2\left[\frac{\epsilon_s kT \ln(N_a/n_i)}{q^2 N_a}\right]^{1/2}$$

Maximum depletion

Ideal MOS capacitance, in inversion

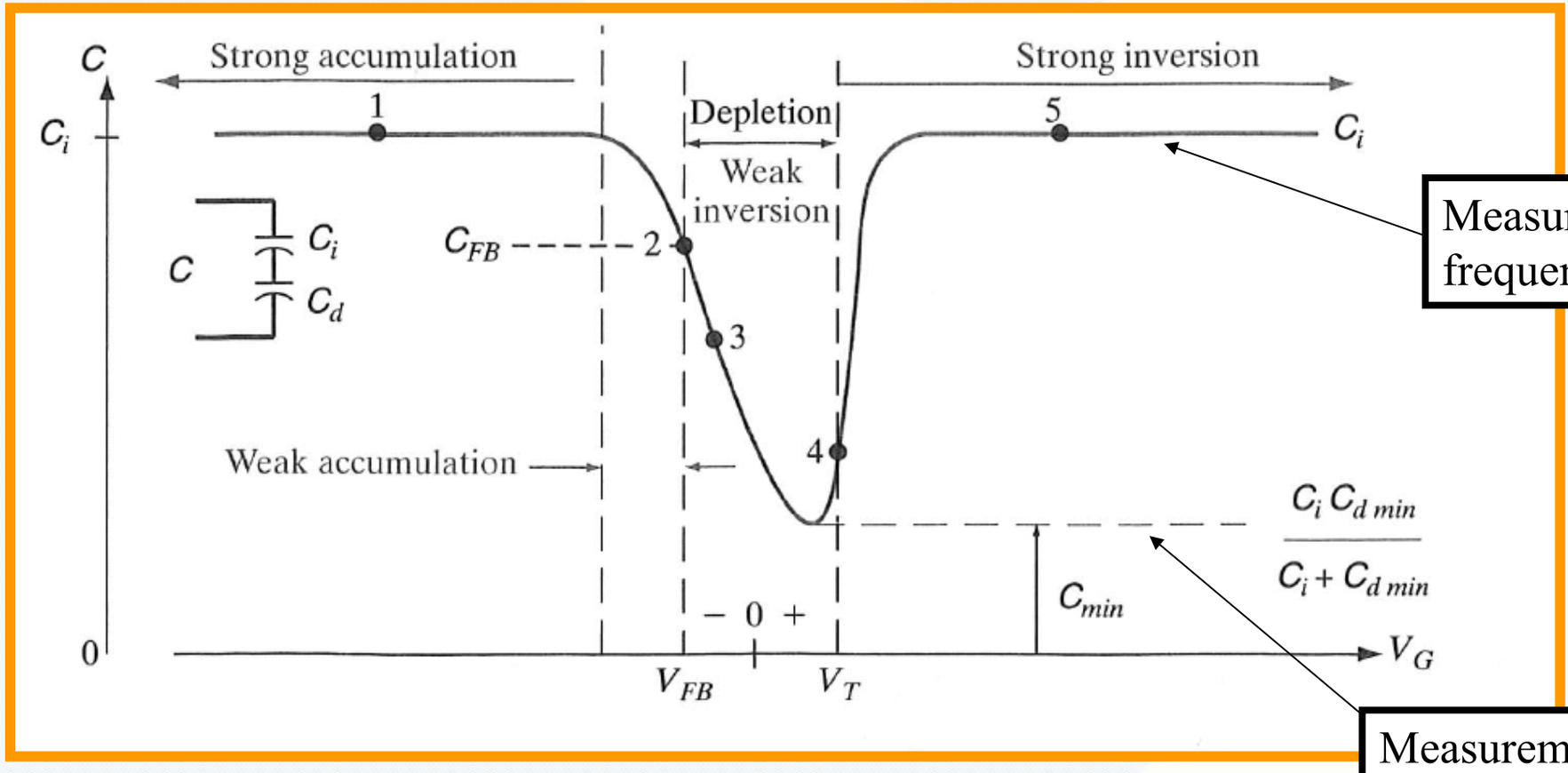
The charge (depending on fixed ionized doping atoms) in the depletion area in strong inversion can then be written:

$$Q_d = -qN_aW_m \longrightarrow W_m = \left[\frac{2\epsilon_s\phi_s(\text{inv.})}{qN_a}\right]^{1/2} \quad \Phi_s(inv) = 2\Phi_F \longrightarrow = -2(\epsilon_s qN_a\phi_F)^{1/2}$$

$$V_T = -\frac{Q_d}{C_i} + 2\phi_F \quad (ideal\ case)$$

Ideal MOS capacitance

”oxide "capacitance in series with depletion capacitances



Measurement at low frequencies (100Hz)

Measurement at high frequencies (1 MHz)

$$C_i = \frac{\varepsilon_i}{d} \qquad C_d = \frac{\varepsilon_s}{w}$$

$$C = \frac{C_i C_d}{C_i + C_d}$$

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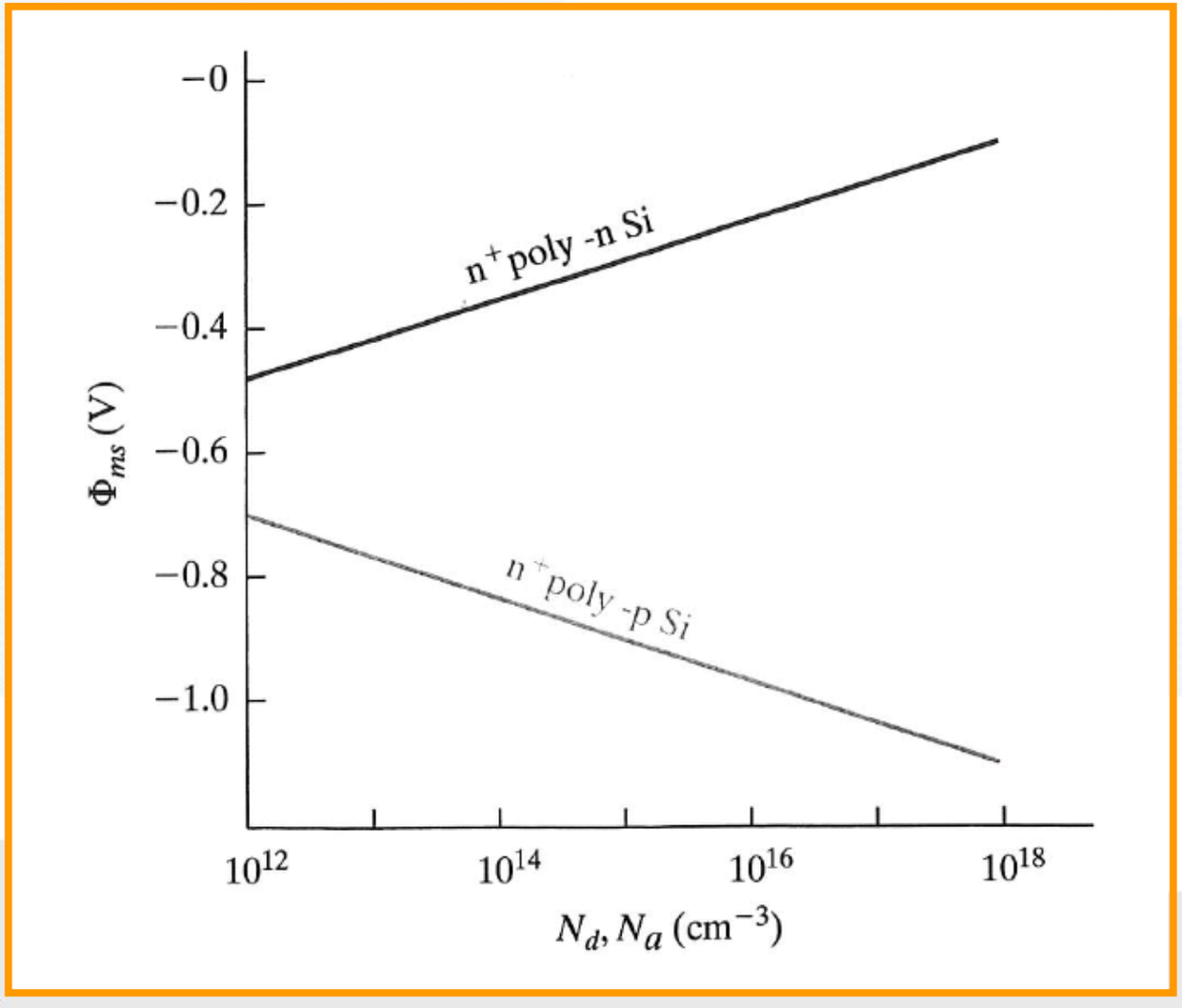
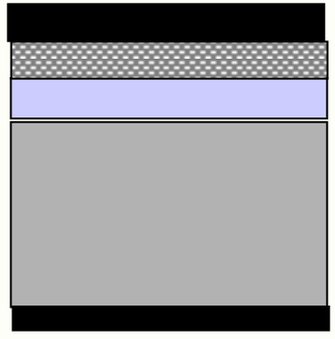
Actual MOS Capacitances

- Change in workfunction



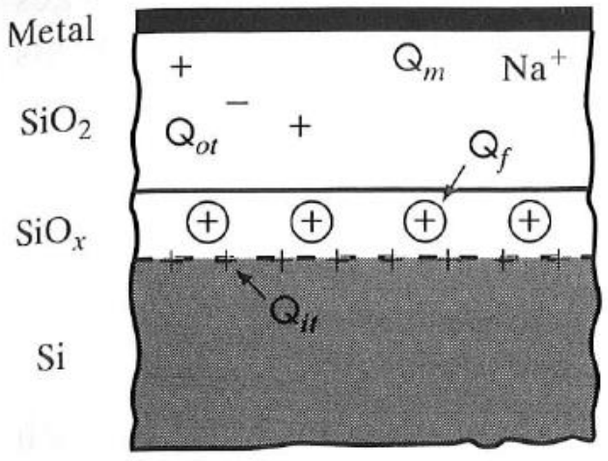


metal
Poly silicon
SiO_2

Semiconductor

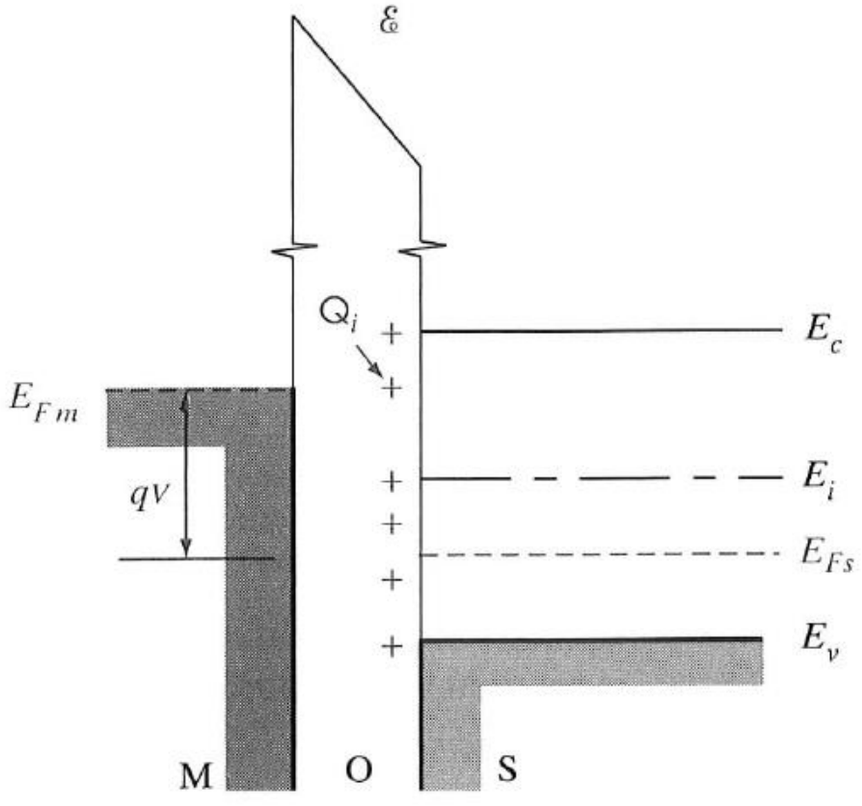
Actual MOS Capacitances

Charges in oxide



Q_m Mobile ionic charge
Q_{ot} Oxide trapped charge
Q_f Oxide fixed charge
Q_{it} Interface trap charge

(a)



(b)

$$V = V_{FB} = -\frac{Q_i}{C_i}$$

Actual MOS Capacitances

Difference in workfunction between the metal (polysilicon) semiconductors influences on the threshold voltage V_T

$$V_T = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F$$

	$V_T =$	Φ_{ms}	$-\frac{Q_i}{C_i}$	$-\frac{Q_d}{C_i}$	$+ 2\phi_F$
(a)		(−)	(−)	(+) n channel (−) p channel	(+) n channel (−) p channel