PHYSICAL CONSTANTS

Symbol	Name	Value
q	Magnitude of electronic charge	1.602×10^{-19}C
m_0	Electron rest mass	9.109×10^{-31}kg
m_p	Proton rest mass	1.673×10^{-27}kg
c	Speed of light in vacuum	2.998×10^{8} m/s
ε_0	Permittivity of vacuum	8.854×10^{-12} F/m
k	Boltzmann's constant	1.381×10^{-23} J/K
		8.617×10^{-5} eV/K
h	Planck's constant	6.625×10^{-34} J-s
		4.135×10^{-15} eV-s
A_0	Avogadro number	6.022×10^{26} molecules/kg-mole
kT	Thermal energy	0.02586 eV ($T = 27°C$) 0.02526 eV ($T = 20°C$)
E_g	Bandgap of silicon at 300K	1.12 eV
K_s	Relative permittivity of silicon	11.7
K_0	Relative permittivity of silicon dioxide	3.9
n_i	Intrinsic carrier density in silicon at 300K	10^{10}/cm^3

CONVERSION FACTORS

1 Å	$= 10^{-8}$ cm	1 mil^2	$= 645.2\ \mu$m^2
	$= 10^{-10}$ m		$= 6.45 \times 10^{-6}$ cm^2
1μm	$= 10^{-4}$ cm	1 eV	$= 1.602 \times 10^{-19}$ J
	$= 10^{-6}$ m	λ	$= 1.24/E\ \mu$m (E in eV)
1 mil	$= 10^{-3}$ in		
	$= 25.4\ \mu$m		

MODULAR SERIES ON SOLID STATE DEVICES

Gerold W. Neudeck and Robert F. Pierret, Editors

Volume V

Introduction to Microelectronic Fabrication

Second Edition

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Upper Saddle River, New Jersey 07458

Contents

Preface

The spectacular advances in the development and application of integrated circuit (IC) technology have led to the emergence of microelectronics process engineering as an independent discipline. Additionally, the pervasive use of integrated circuits requires a broad range of engineers in the electronics and allied industries to have a basic understanding of the behavior and limitations of ICs. One of the goals of this book is to address the educational needs of individuals with a wide range of backgrounds.

This text presents an introduction to the basic processes common to most IC technologies and provides a base for understanding more advanced processing and design courses. In order to contain the scope of the material, we deal only with material related to silicon processing and packaging. The details of many problems specifically related to VLSI/ULSI fabrication are left to texts on advanced processing, although problem areas are mentioned at various points in this text, and goals of the International Technology Roadmap for Semiconductors are discussed as appropriate.

Chapter 1 provides an overview of IC processes, and Chapters 2–6 then focus on the basic steps used in fabrication, including lithography, oxidation, diffusion, ion implantation and thin film deposition, and etching. Interconnection technology, packaging, and yield are covered in Chapters 7 and 8. It is important to understand interactions between process design, device design, and device layout. For this reason, Chapter 9 and 10 on MOS and bipolar process integration have been included. Chapter 11 provides a brief introduction to the exciting area of Microelectromechanical Systems (MEMS).

Major changes in the second edition of this text include new or expanded coverage of lithography and exposure systems, trench isolation, chemical mechanical polishing, shallow junctions, transient-enhanced diffusion, copper Damescene processes, and process simulation. The chapters on MOS and bipolar process integration have been substantially modified, and the chapter on MEMS is entirely new. The problem sets have been expanded, and additional information on measurement techniques has been included.

The text evolved from notes originally developed for a course introducing seniors and beginning graduate students to the fabrication of solid-state devices and integrated circuits. A basic knowledge of the material properties of silicon is needed, and we use Volume I of this Series as a companion text. An introductory knowledge of electronic components such as resistors, diodes, and MOS and bipolar transistors is also useful.

The material in the book is designed to be covered in one semester. In our case, the microelectronics fabrication course is accompanied by a corequisite laboratory. The students design a simple device or circuit based upon their individual capability, and the designs are combined on a multiproject polysilicon gate NMOS chip. Design, fabrication, and testing are completed within the semester. Students from a variety of disciplines, including electrical, mechanical, chemical, and materials engineering; computer science; and physics, are routinely enrolled in the fabrication classes.

Before closing, I must recognize a number of other books that have influenced the preparation of this text. These include *The Theory and Practice of Microelectronics* and *VLSI Fabrication Principles* by S. K. Ghandi, *Basic Integrated Circuit Engineering* by D. J. Hamilton and W. G. Howard, *Integrated Circuit Engineering* by A. H. Glaser and G. E. Subak-Sharpe, *Microelectronic Processing and Device Design* by R. A. Colclaser, *Semiconductor Devices—Physics and Technology* by S. M. Sze, *Semiconductor Integrated Circuit Processing Technology* by W. R. Runyon and K. E. Bean, and *The Science and Engineering of Microelectronic Fabrication* by Stephen A. Campbell.

Thanks also go to the many colleagues who have provided suggestions and encouragement for the new edition and especially to our laboratory manager Charles Ellis who has been instrumental in molding the laboratory sections of our course.

RICHARD C. JAEGER
Auburn, Alabama

CHAPTER 1

An Overview of Microelectronic Fabrication

1.1 A HISTORICAL PERSPECTIVE

In this volume, we will develop an understanding of the basic processes used in monolithic integrated-circuit (IC) fabrication. Silicon is the dominant material used throughout the IC industry today, and in order to conserve space, only silicon processing will be discussed in this book. However, all of the basic processes discussed here are applicable to the fabrication of compound semiconductor integrated circuits (ICs) such as gallium arsenide or indium phosphide, as well as thick- and thin-film hybrid ICs.

Germanium was one of the first materials to receive wide attention for use in semiconductor device fabrication, but it was rapidly replaced by silicon during the early 1960s. Silicon emerged as the dominant material, because it was found to have two major processing advantages. Silicon can easily be oxidized to form a high-quality electrical insulator, and this oxide layer also provides an excellent barrier layer for the selective diffusion steps needed in integrated-circuit fabrication.

Silicon was also shown to have a number of ancillary advantages. It is a very abundant element in nature, providing the possibility of a low-cost starting material. It has a wider bandgap than germanium and can therefore operate at higher temperatures than germanium. In retrospect, it appears that the processing advantages were the dominant reasons for the emergence of silicon over other semiconductor materials.

The first successful fabrication techniques produced single transistors on a rectangular silicon die 1–2 mm on a side. The first integrated circuits, fabricated at Texas Instruments and Fairchild Semiconductor in the early 1960s, included several transistors and resistors to make simple logic gates and amplifier circuits. From this modest beginning, the level of integration has been doubling every one to two years, and we have now reached integration levels of billions of components on a 20-mm × 20-mm die [1–3]. For example, one-gigabit dynamic random-access memory (DRAM) chips have more than 10^9 transistors and more than 10^9 capacitors in the memory array, as

well as millions of additional transistors in the access and decoding circuitry. One-gigabit RAMs are currently being produced with photographic features measuring between 0.13 and 0.18 micron (μm). MOS transistors with dimensions below 0.05 μm have been fabricated successfully in research laboratories, and these devices continue to behave as predicted by macroscopic models. So we still have significant increases in integrated-circuit density yet to come, provided that manufacturable fabrication processes can be developed for deep submicron dimensions.

The larger the diameter of the wafer, the more integrated-circuit dice can be produced at one time. Many wafers are processed at the same time, and the same silicon chip is replicated as many times as possible on a wafer of a given size. The size of silicon wafers has steadily increased from 1-, 2-, 3-, 4-, 5-, and 6-in. diameters to the point where 8-in. (200-mm) wafers are now in production. (See Fig. 1.1(a).) Wafers with 300-mm diameters will be in full production in the near future, and 450 mm wafers are projected to be in used by the end of the decade. Wafer thicknesses range from approximately 350 to 1250 microns. Large-diameter wafers must be thicker in order to maintain structural integrity and planarity during the wide range of processing steps encountered during IC fabrication.

Figure 1.1(c) shows the approximate number of 10-mm × 10-mm dice that fit on a wafer of given diameter. For a given wafer processing cost, the more dice per wafer, the lower the individual die cost becomes. Thus, there are strong economic forces driving the IC industry to continually move to larger and larger wafer sizes.

The dramatic progress of IC miniaturization is depicted graphically in Fig. 1.2 [1–3] on pages 4 and 5. The complexities of memory chips and microprocessors have both grown exponentially with time. In the three decades since 1965, memory density has grown by a factor of more than 10 million from the 64-bit chip to the 1-Gb memory chip, as indicated in Fig. 1.2(a). Similarly, the number of transistors on a microprocessor chip has increased by a factor of more than five thousand since 1970 (Fig 1.2 (b).)

Since the commercial introduction of the integrated circuit, these increases in density have been achieved through a continued reduction in the minimum line width, or minimum feature size, that can be defined on the surface of the integrated circuit, as shown in Fig. 1.3 on page 6. Today, most corporate semiconductor laboratories around the world are actively working on deep submicron processes with feature sizes less than 0.1 μm, less than one one-thousandth the diameter of a human hair!

These trends and future projections are summarized in Table 1.1 on page 6, which is abstracted from the International Technology Road map for Semiconductors (ITRS) generated by the Semiconductor Industry Association [4]. The ITRS is updated every three years; the projections are mind-boggling, even for those of us who have worked in the industry for many years. By the year 2011, MOS transistor gate lengths are projected to reach 30 nm (0.030 μm), multigigabit DRAM chips will be commonplace, and microprocessors will have a billion transistors on die exceeding 25 mm (one inch) on an edge. It remains to be seen whether the industry meets these projections. However, progress will be impressive, even if only a fraction of the projections are achieved.*

Historically there has been a problem with the units of measure used to describe integrated circuits. Horizontal dimensions were originally specified in mils (1 mil = 0.001 in.), whereas specification of the shallower vertical dimensions commonly made

*In the past several years, the IC industry has actually managed to exceed the ITRS goals.

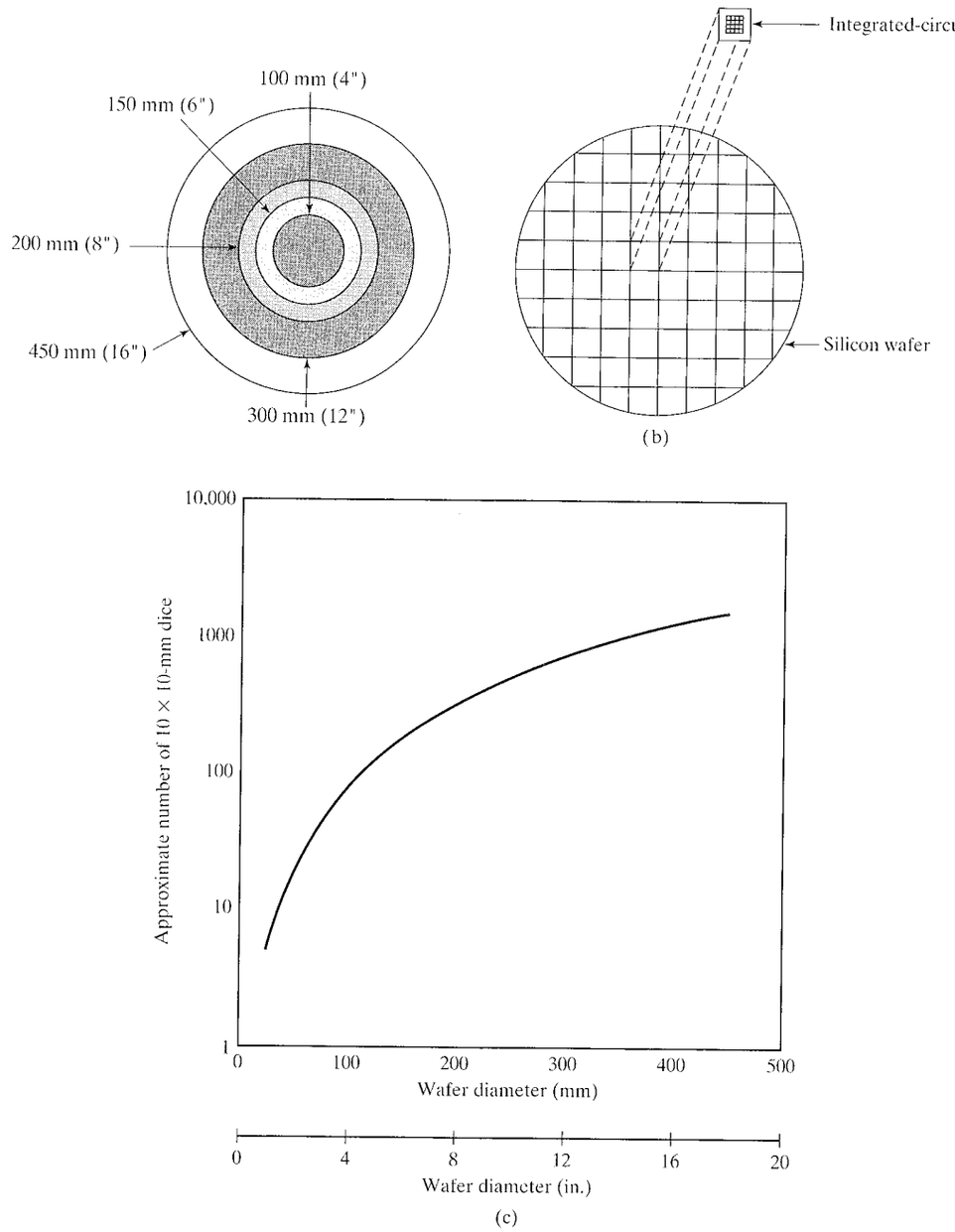

FIGURE 1.1

(a) Relative size of wafers with diameters ranging from 100 to 450 mm; (b) The same integrated circuit die is replicated hundreds of times on a typical silicon wafer; (c) the graph gives the approximate number of 10 x 10 mm dice that can be fabricated on wafers of different diameters.

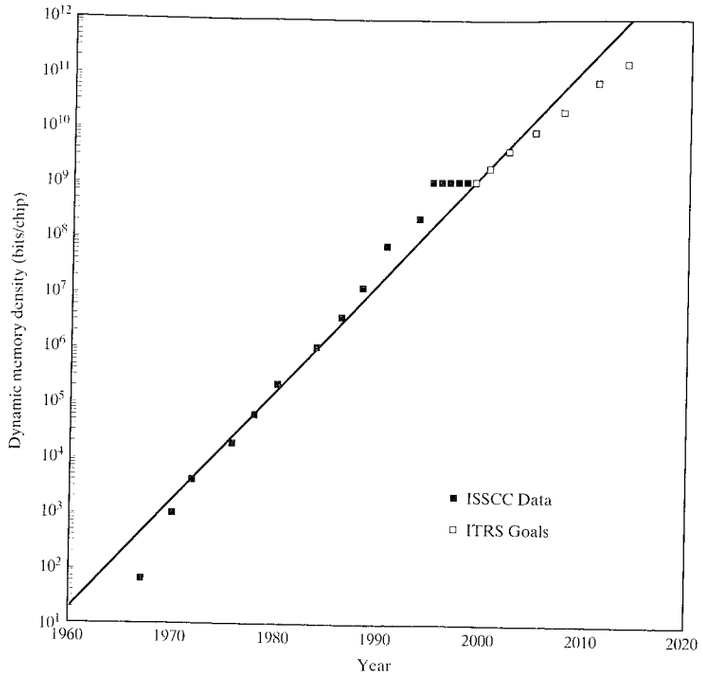

FIGURE 1.2

(a) Dynamic memory density versus year since 1960.

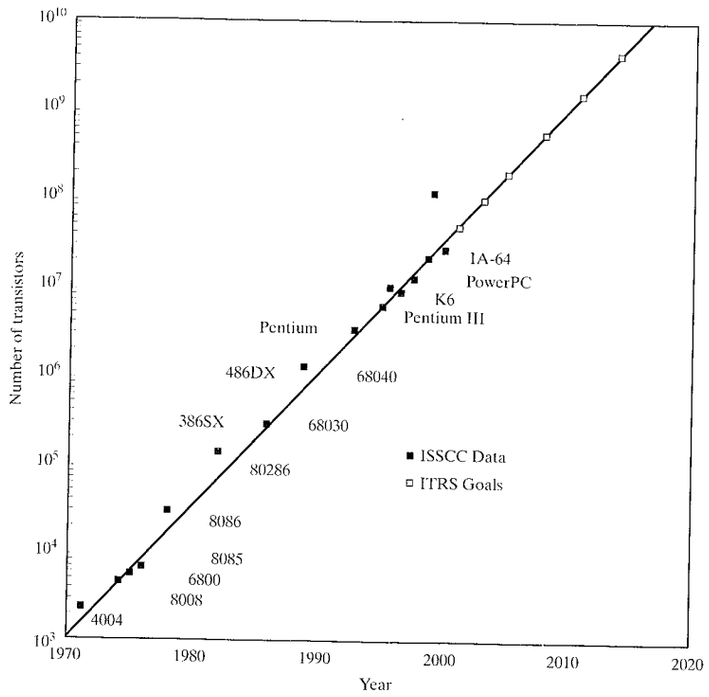

FIGURE 1.2

(b) Number of transistors in a microprocessor versus year.

use of the metric system. Today, most of the dimensions are specified using the metric system, although Imperial units are occasionally still used. Throughout the rest of this book, we will attempt to make consistent use of metric units.

1.2 AN OVERVIEW OF MONOLITHIC FABRICATION PROCESSES AND STRUCTURES

Monolithic IC fabrication can be illustrated by studying the basic cross sections of MOS and bipolar transistors in Figs. 1.4 (on page 7) and 1.5 (on page 8). The *n*-channel MOS transistor is formed in a *p*-type substrate. Source/drain regions are formed by selectively converting shallow regions at the surface to *n*-type material. Thin and thick silicon-dioxide regions on the surface form the gate insulator of the transistor and serve to isolate one device from another. A thin film of polysilicon is used to form the gate of the transistor, and a metal such as aluminum is used to make contact to the source and drain. Interconnections between devices can be made using the diffusions and the layers of polysilicon and metal.

The bipolar transistor in Fig. 1.5 has alternating *n*- and *p*-type regions selectively fabricated on a *p*-type substrate. Silicon dioxide is again used as an insulator, and aluminum is used to make electrical contact to the emitter, base, and collector of the transistor.

Both the MOS and bipolar structures are fabricated through the repeated application of a number of basic processing steps:

- Oxidation
- Photolithography
- Etching
- Diffusion
- Evaporation or sputtering
- Chemical vapor deposition (CVD)
- Ion implantation
- Epitaxy
- Annealing

Silicon dioxide can be formed by heating a silicon wafer to a high temperature (1000 to 1200 °C) in the presence of oxygen. This process is called *oxidation*. Metal films can be deposited through evaporation by heating the metal to its melting point in a vacuum. Thin films of silicon nitride, silicon dioxide, polysilicon, and metals can all be formed through a process known as *chemical vapor deposition* (CVD), in which the material is deposited out of a gaseous mixture onto the surface of the wafer. Metals and insulators may also be deposited by a process called *sputtering*.

Shallow *n*- and *p*-type layers are formed by high-temperature (1000 to 1200 °C) *diffusion* of donor or acceptor impurities into silicon or by *ion implantation*, in which the wafer is bombarded with high-energy donor or acceptor ions generated in a high-voltage particle accelerator.

In order to build devices and circuits, the *n*- and *p*-type regions must be formed selectively in the surface of the wafer. Silicon dioxide, silicon nitride, polysilicon, photo resist, and other materials can all be used to mask areas of the wafer surface to prevent

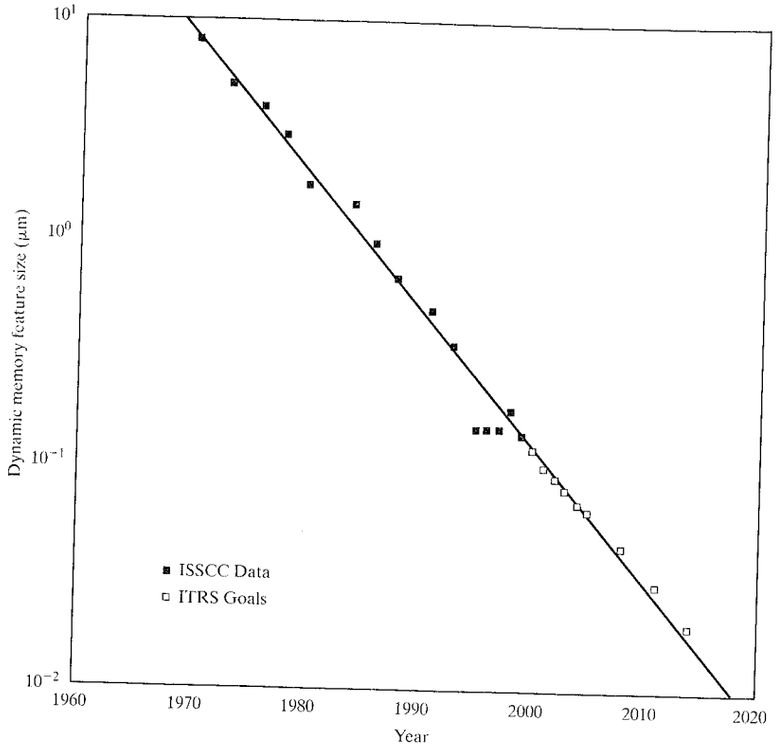

FIGURE 1.3

Feature size used in fabrication of dynamic memory as a function of time.

TABLE 1.1 International Technology Road Map for Semiconductors (ITRS) [4]

	Selected Projections					
Year of First Product Shipment	2001	2003	2005	2008	2011	2014
DRAM Metal Line Half-Pitch (nm)	150	120	100	70	50	35
Microprocessor Gate Widths (nm)	100	80	65	45	30	20
DRAM (G-bits/chip)	2.2	4.3	8.6	24	68	190
Microprocessor (M-transistors/chip)	48	95	190	540	1500	4300
DRAM Chip Area: Year of Introduction (mm^2)	400	480	526	600	690	790
DRAM Chip Area: Production (mm^2)	130	160	170	200	230	260
MPU Chip Size at Introduction (mm^2)	340	370	400	470	540	620
MPU Chip Area: Second "shrink" (mm^2)	180	210	230	270	310	350
Wafer Size (mm)	300	300	300	450	450	450

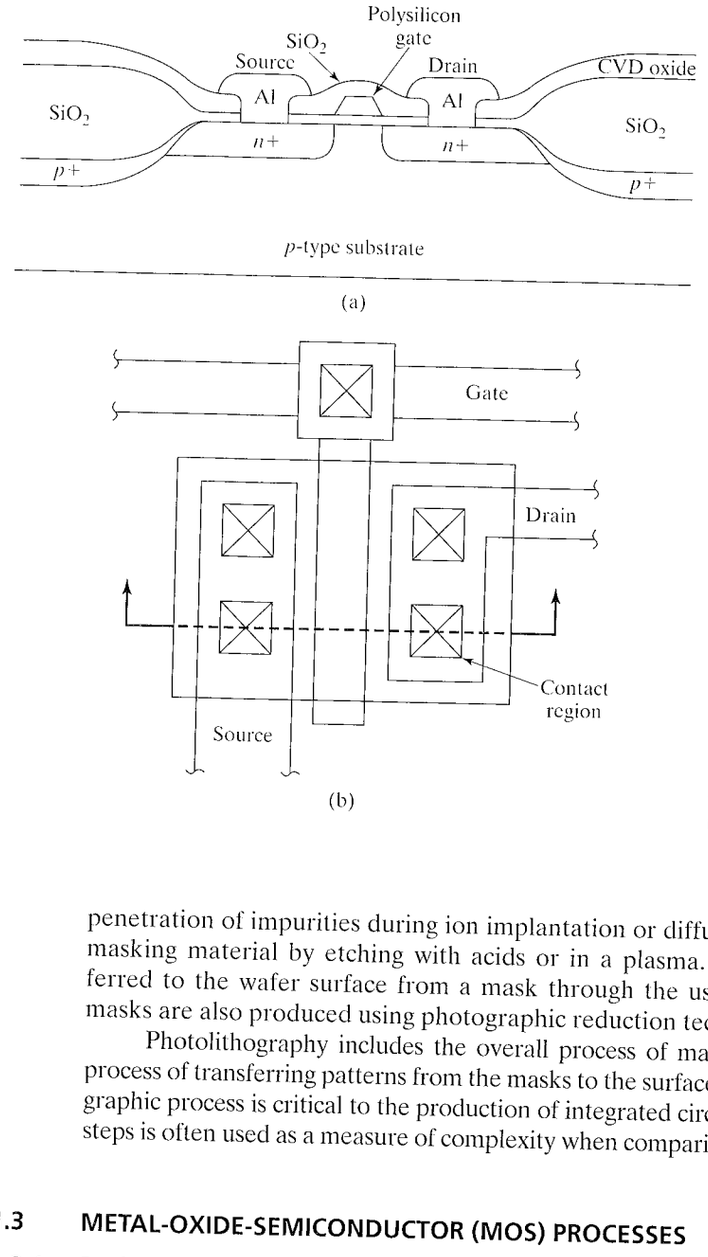

FIGURE 1.4

The basic structure of an n-channel metal-oxide-semiconductor (NMOS) transistor structure. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a). The transistor uses heavily doped polysilicon as the gate "metal."

penetration of impurities during ion implantation or diffusion. Windows are cut in the masking material by etching with acids or in a plasma. Window patterns are transferred to the wafer surface from a mask through the use of optical techniques. The masks are also produced using photographic reduction techniques.

Photolithography includes the overall process of mask fabrication, as well as the process of transferring patterns from the masks to the surface of the wafer. The photolithographic process is critical to the production of integrated circuits, and the number of mask steps is often used as a measure of complexity when comparing fabrication processes.

1.3 METAL-OXIDE-SEMICONDUCTOR (MOS) PROCESSES

1.3.1 Basic NMOS Process

A possible process flow for a basic n-channel MOS process (NMOS) is shown in Fig. 1.6 on page 9 and Fig. 1.7 on page 10. The starting wafer is first oxidized to form a thin-pad oxide layer of silicon dioxide (SiO_2) that protects the silicon surface. Silicon nitride is then deposited by a low-pressure chemical vapor deposition (LPCVD) process. Mask #1 defines the active transistor areas. The nitride/oxide sandwich is etched away

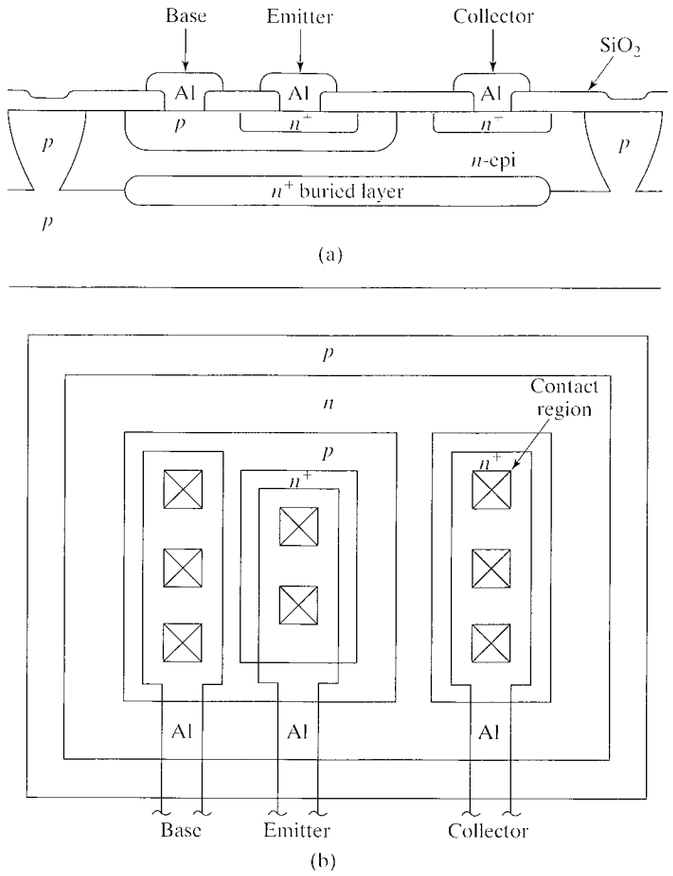

FIGURE 1.5

The basic structure of a junction-isolated bipolar transistor. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a).

everywhere except where transistors are to be formed. A boron implantation is performed and followed by an oxidation step. The nitride serves as both an implantation mask and an oxidation mask. After the nitride and thin oxide padding layers are removed, a new thin layer of oxide is grown to serve as the gate oxide for the MOS transistors. Following gate-oxide growth, a boron implantation is commonly used to adjust the threshold voltage to the desired value.

Polysilicon is deposited over the complete wafer using a CVD process. The second mask defines the polysilicon gate region of the transistor. Polysilicon is etched away everywhere except over the gate regions and the areas used for interconnection. Next, the source/drain regions are implanted through the thin oxide regions. The implanted impurity may be driven in deeper with a high-temperature diffusion step. More oxide is deposited on the surface, and contact openings are defined by the third mask step. Metal is deposited over the wafer surface by evaporation or sputtering. The fourth mask step is used to define the interconnection pattern that will be etched in the metal. A passivation layer of phosphosilicate glass or silicon nitride (not shown in Fig. 1.6) is deposited on the wafer surface, and the final mask (#5) is used to define windows so that bonding wires can be attached to pads on the periphery of the IC die.

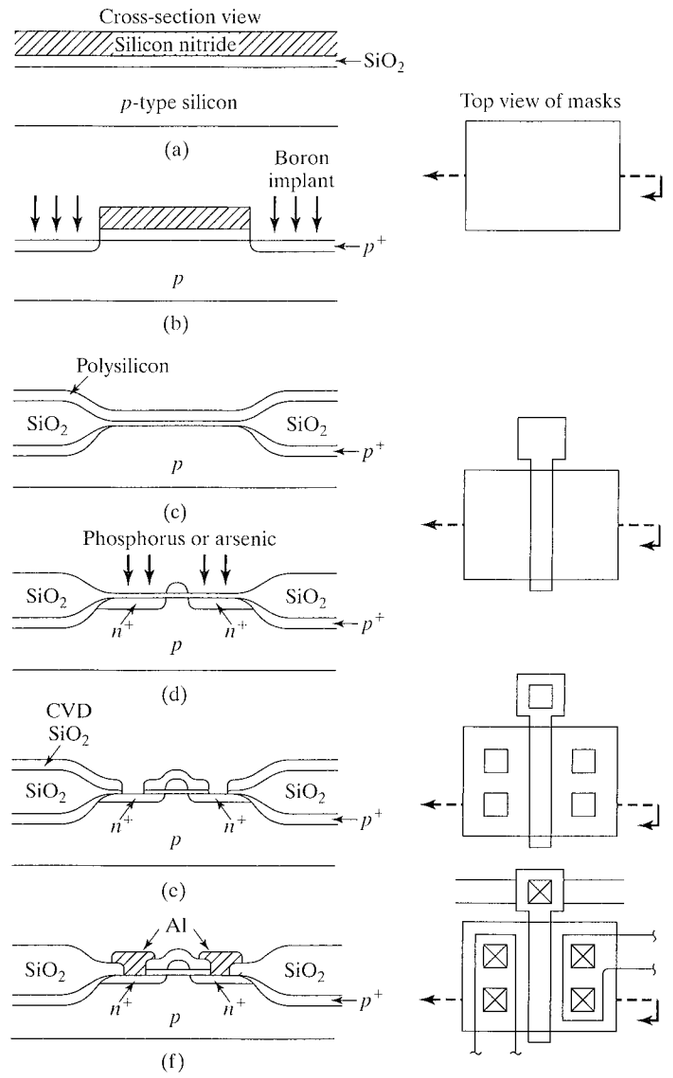

FIGURE 1.6

Process sequence for a semirecessed oxide NMOS process. (a) Silicon wafer covered with silicon nitride over a thin padding layer of silicon dioxide; (b) etched wafer after first mask step. A boron implant is used to help control field oxide threshold; (c) structure following oxidation, nitride removal, and polysilicon deposition; (d) wafer after second mask step and etching of polysilicon; (e) the third mask has been used to open contact windows following silicon dioxide deposition; (f) final structure following metal deposition and patterning with fourth mask.

This simple process requires five mask steps. Note that these mask steps use subtractive processes. The entire surface of the wafer is first coated with a desired material, and then most of the material is removed by wet chemical or dry plasma etching.

1.3.2 Basic Complementary MOS (CMOS) Process

Figure 1.8 shows the mask sequence for a basic complementary MOS (CMOS) process. One new mask, beyond that of the NMOS process, is used to define the "*n*-well," or "*n*-tub," which serves as the substrate for the *p*-channel devices. A second new mask step is used to define the source/drain regions of the *p*-channel transistors.

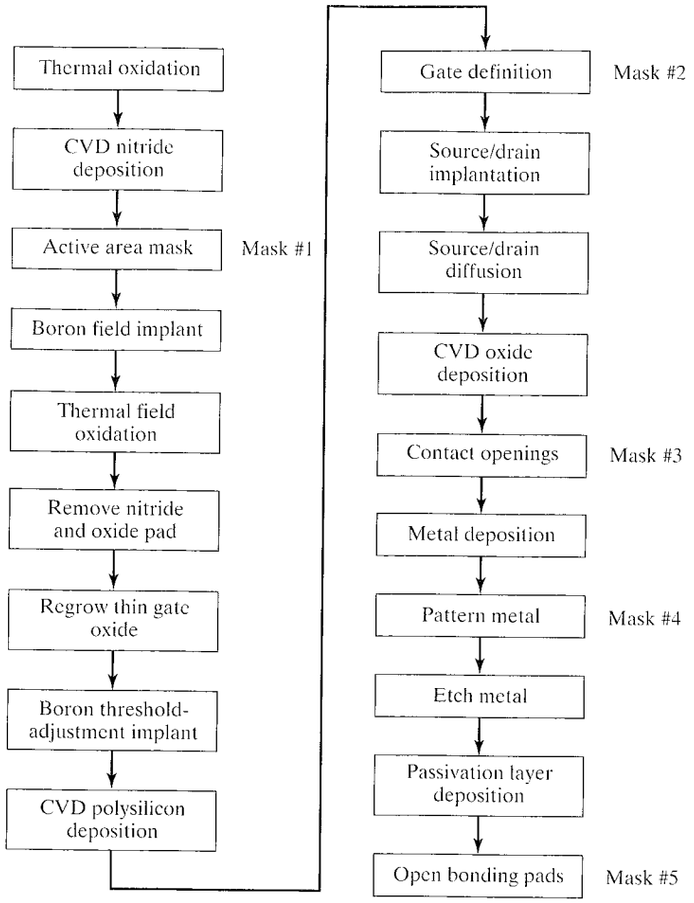

FIGURE 1.7
Basic NMOS process flowchart.

Additional masks may be used to adjust the threshold voltage of the MOS transistors and are very common in state-of-the-art NMOS and CMOS processes.

Older CMOS processes use a *p*-well instead of an *n*-well. Twin-well processes have also been developed recently. Both a *p*-well and an *n*-well are formed in a lightly doped substrate, and the *n*- and *p*-channel devices can each be optimized for highest performance. Twin-well very large-scale integration (VLSI) processes use lightly doped layers grown on heavily doped substrates to suppress a CMOS failure mode called *latchup*.

1.4 BASIC BIPOLAR PROCESSING

Basic bipolar fabrication is somewhat more complex than single-channel MOS processing, as indicated in Figs. 1.9 on page 12 and 1.10 on page 13. A *p*-type silicon wafer is oxidized, and the first mask is used to define a diffused region called the *buried layer*, or *subcollector*. This diffusion is used to reduce the collector resistance of the bipolar transistor. Following the buried-layer diffusion, a process called *epitaxy* is used to grow single-crystal *n*-type silicon on top of the silicon wafer. The epitaxial growth process results in a high-

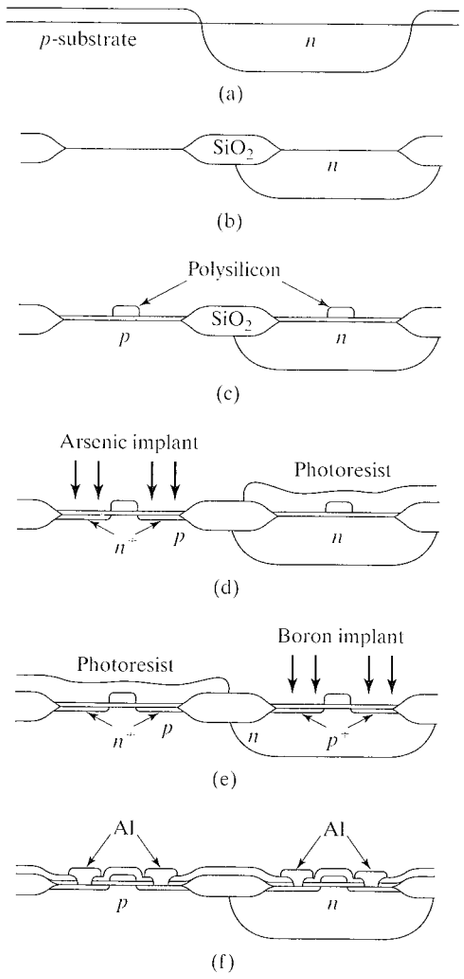

FIGURE 1.8
Cross-sectional views at major steps in a basic CMOS process. (a) Following *n*-well diffusion, (b) following selective oxidation, and (c) following gate oxidation and polysilicon gate definition; (d) NMOS source/drain implantation; (e) PMOS source/drain implantation; (f) structure following contact and metal mask steps.

quality silicon layer with the same crystal structure as the original silicon wafer. An oxide layer is then grown on the wafer. Mask two is used to open windows for a deep *p*-diffusion, which is used to isolate one bipolar transistor from another. Another oxidation follows the isolation diffusion. Mask three opens windows in the oxide for the *p*-type base diffusion. The wafer is usually oxidized during the base diffusion, and mask four is used to open windows for the emitter diffusion. The same diffusion step places an n^+ region under the collector contact to ensure that a good ohmic contact will be formed during subsequent metallization. Masks five, six, and seven are used to open contact windows, pattern the metallization layer, and open windows in the passivation layer just as in the NMOS process described in Section 1.3. Thus, the basic bipolar process requires seven mask levels compared with five for the basic NMOS process.

After the MOS or bipolar process is completed, each die on the wafer is tested, and bad dice are marked with ink. The wafer is then sawed apart. Good dice are mounted in various packages for final testing and subsequent sale or use.

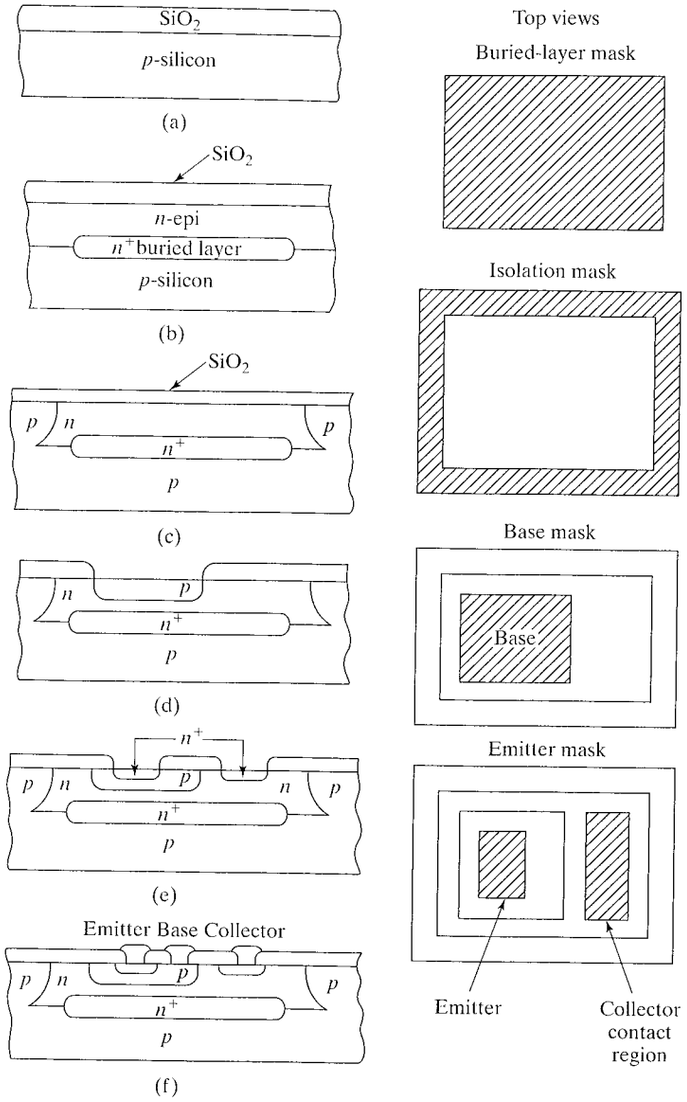

FIGURE 1.9

Cross-sectional view of the major steps in a basic bipolar process. (a) Wafer with silicon dioxide layer; (b) following buried-layer diffusion using first mask, and subsequent epitaxial layer growth and oxidation; (c) following deep-isolation diffusion using second mask; (d) following boron-base diffusion using third mask; (e) fourth mask defines emitter and collector contact regions; (f) final structure following contact and metal mask steps.

1.5 SAFETY

In the course of IC fabrication processes described throughout the rest of this text, we shall encounter a wide variety of acids, highly corrosive bases, organic and inorganic solvents, and materials with carcinogenic properties, as well as extremely toxic gases, and this represents a good opportunity to stress the need to exercise a high degree of caution before proceeding with any semiconductor processing. Because of the dangers, most laboratories require individuals to pass a safety test before they are permitted to work in the laboratory.

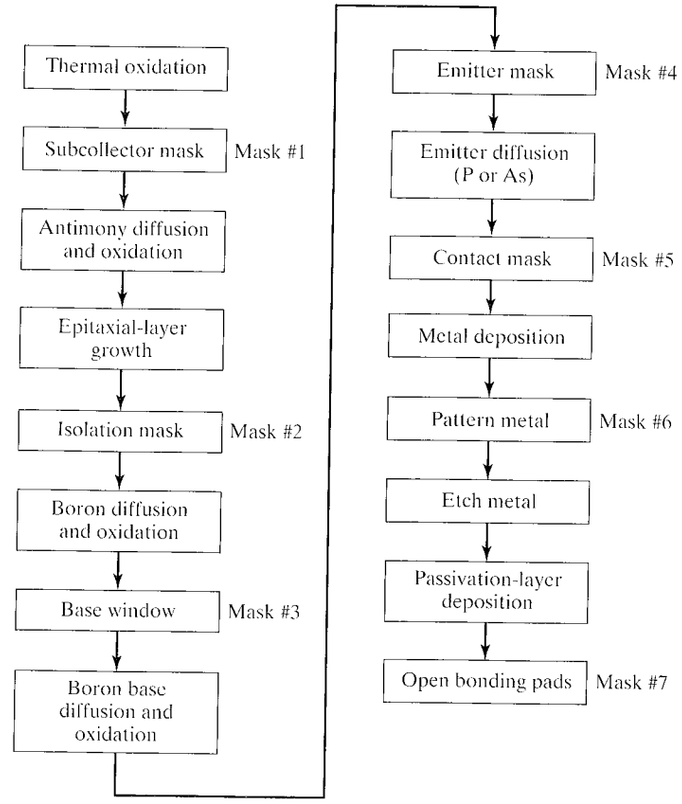

FIGURE 1.10

Basic bipolar process flowchart.

Wet processes, particularly those used for cleaning and etching, involve the use of a wide variety of acids and bases. Both can produce serious burns if they contact the skin, and even the fumes can produce irritation to the skin or serious eye damage. Rubber gloves, an apron, and eye protection should always be worn when handling these materials. However, gloves should not be relied upon to protect one during immersion in liquids, because of pinhole formation in the gloves.

Care must be exercised in handling, mixing, and disposing these liquids. Environmental standards often restrict the methods that can be used for disposal. Acids and bases must not be combined during disposal. When diluting bases or acids, concentrated chemicals should be added to water, not the reverse. Many acids will discolor the skin or give a burning sensation upon contact. However, hydrofluoric acid (HF) is much more insidious. Although a weak acid, HF readily penetrates the skin to produce deep and painful burns that are not detected until after the damage is done. Immediate medical attention is required for such burns.

Ion implantation, low-pressure chemical vapor deposition, and epitaxial growth represent just a few of the processes that may involve extremely toxic or explosive gases. For example, extreme caution must be exercised with the delivery of arsine,

phosphine, germane, silane, and anhydrous ammonia, to name just a few. In addition, many of the systems, such as ion implanters, plasma reactors, and electron-beam evaporation systems, involve lethal voltages.

As a general rule before dealing with any new chemical, one must research and study its overall properties to understand toxicity, safe handling practices, and any unusual reactions that may occur or reaction products that can be produced.

The rest of this book concentrates on the basic processes used in the fabrication of monolithic integrated circuits. Chapters 2 through 8 discuss mask making and pattern definition, oxidation, diffusion, ion implantation, film deposition, interconnections and contacts, and packaging and yield. The last three chapters introduce the integration of process, layout, and device design for MOS, bipolar, and MEMS technologies.

REFERENCES

[1] *Digest of the IEEE International Solid-State Circuits Conference*, held in February of each year. (http://www.sscs.org/isscc)

[2] *Digest of the IEEE International Electron Devices Meeting*, held in December of each year. (http://www.ieee.org/conference/iedm)

[3] *Digests of the International VLSI Technology and Circuits Symposia*, co-sponsored by the IEEE and JSAP, held in June of each year. (http://www.vlsisymposium.org)

[4] *The International Technology Roadmap for Semiconductors*, The Semiconductor Industry Association (SIA), San Jose, CA, 1999. (http://www.semichips.org)

PROBLEMS

1.1 Make a list of two dozen items in your everyday environment that you believe contain IC chips. A PC and its peripherals are considered to be one item. (Do not confuse electromechanical timers, common in clothes dryers or the switch in a simple thermostat or coffee maker, with electronic circuits.)

1.2 **(a)** Make a table comparing the areas of wafers with the following diameters: 25, 50, 75, 100, 125, 150, 200, 300 and 450 mm.

(b) Approximately how many 1-mm × 1-mm dice are on a 450-mm wafer?

(c) How many 25-mm × 25-mm dice?

1.3 **(a)** Calculate an estimate of the number of 20-mm × 20-mm dice on a 300-mm diameter wafer, in terms of the total wafer and die areas.

(b) Calculate the exact number of 20-mm × 20-mm dice that actually fit on the 300-mm wafer. (It may help to draw a picture.)

1.4 The straight line in Fig. 1.2(a) is described by $B = 19.97 \times 10^{0.1977(Y - 1960)}$ bits/chip. If a straight-line projection is made using this equation, what will be the number of memory bits/chip in the year 2020?

1.5 The straight line in Fig. 1.2(b) is described by $N = 1027 \times 10^{0.1505(Y - 1970)}$ transistors. Based upon a straight-line projection of this figure, what will be the number of transistors in a microprocessor in the year 2020?

1.6 **(a)** How many years does it take for memory chip density to increase by a factor of two, based upon the equation in Problem 1.4?

(b) How about by a factor of 10?

1.7 **(a)** How many years does it take for microprocessor circuit density to increase by a factor of two, based upon the equation in Problem 1.5?

(b) How about by a factor of 10?

1.8 If you make a straight-line projection from Fig. 1.3, what will be the minimum feature size in integrated circuits in the year 2020? The curve can be described by $F = 8.214 \times 10^{-0.06079(Y - 1970)}$ μm. Do you think this is possible? Why or why not?

1.9 The filament of a small vacuum tube uses a power of approximately 0.5 W. Suppose that approximately 300 million of these tubes are used to build the equivalent of a 256-Mb memory. How much power is required for this memory? If this power is supplied from a 220-V ac source, what is the current required by this memory?

1.10 An 18-mm × 25-mm die is covered by an array of 0.25-μm metal lines separated by 0.25-μm-wide spaces.

(a) What is the total length of wire on this die?

(b) How about 0.1- μm lines and spaces.

1.11 The curve in Fig. 1.1(b) represents the approximate number of chips on a wafer of a given diameter. Determine the exact number of 10 × 10 mm dice that will fit on a wafer with a diameter of 200 mm. (The number indicated on the curve is 314.)

1.12 The cost of processing a wafer in a particular process is $1,000. Assume that 35% of the fabricated dice are good. Find the number of dice, using Fig. 1.1(b).

(a) Determine the cost per good die for a 150 mm wafer.

(b) Repeat for a 200 mm wafer.

1.13 A certain silicon-gate NMOS transistor occupies an area of 25 λ^2, where λ is the minimum lithographic feature size.

(a) How many MOS transistors can fit on a 5 × 5 mm die if $\lambda = 1$ μm?

(b) 0.25 μm?

(c) 0.10 μm?

1.14 A simple *pn* junction diode is shown in cross section in Fig. P1.14. Make a possible process flowchart for fabrication of this structure, including mask steps.

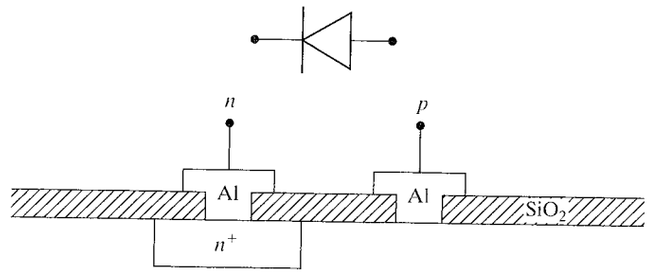

FIGURE P1.14

1.15 Draw a set of contact and metal masks for the bipolar transistor of Fig. 1.9. Use square contact windows with one contact to the emitter and two contacts to the base and collector regions.

CHAPTER 2

Lithography

In order to produce an integrated circuit, thin films of various materials are used as barriers to the diffusion or implantation of impurity atoms or as insulators between conductive materials and the silicon substrate. Holes, or windows, are cut through this barrier material wherever impurity penetration or contact is desired.

Masks contain the patterns of windows that are transferred to the surface of the silicon wafer using a process called *photolithography*. Photolithography makes use of a highly refined version of the photoengraving process. The patterns are first transferred from the mask to a light-sensitive material called *photoresist*. Chemical or plasma etching is then used to transfer the pattern from the photoresist to the barrier material on the surface of the wafer. Each mask step requires successful completion of numerous processing steps, and the complexity of an IC process is often measured by the number of photographic masks used during fabrication. This chapter will explore the lithographic process, including mask fabrication, photoresist processes, and etching.

2.1 THE PHOTOLITHOGRAPHIC PROCESS

Photolithography encompasses all the steps involved in transferring a pattern from a mask to the surface of the silicon wafer. The various steps of the basic photolithographic process given in Figs. 2.1 and 2.2 will each be discussed in detail next.

Ultraclean conditions must be maintained during the lithography process. Any dust particles on the original substrate or that fall on the substrate during processing can result in defects in the final resist coating. Even if defects occur in only 10% of the chip sites at each mask step, fewer than 50% of the chips will be functional after a seven-mask process is completed. Vertical laminar-flow hoods in clean rooms are used to prevent particulate contamination throughout the fabrication process. Clean rooms use filtration to remove particles from the air and are rated by the maximum number of particles per cubic foot or cubic meter of air, as shown in Table 2.1. Clean rooms have evolved from Class 100 to the Class 1 facilities now being used for VLSI/ULSI processing. For comparison, each cubic foot of ordinary room air has several million dust particles exceeding a size of 0.5 μm.