9.23 A number of types of alignment test structures have been developed [12, 13]. Figure P9.23 shows a simple test structure that can be used to measure the misregistration of the contact window mask relative to the diffusion mask [14]. Two linear potentiometers, one in the horizontal direction and one in the vertical direction, are fabricated using diffused resistors. The distance between contacts A and C is the same as that between C and E, and the contact from pad D is nominally one-half the distance between pads C and E. A current is injected between pads B and F, and the voltages between pads C–D and D–E are measured.

(a) Show that the misregistration in the y-direction is given by $\Delta Y = 1/2\ L\ (V_{DE} - V_{CD})/V_{AC}$.

(b) Derive a similar relationship for misregistration in the x-direction.

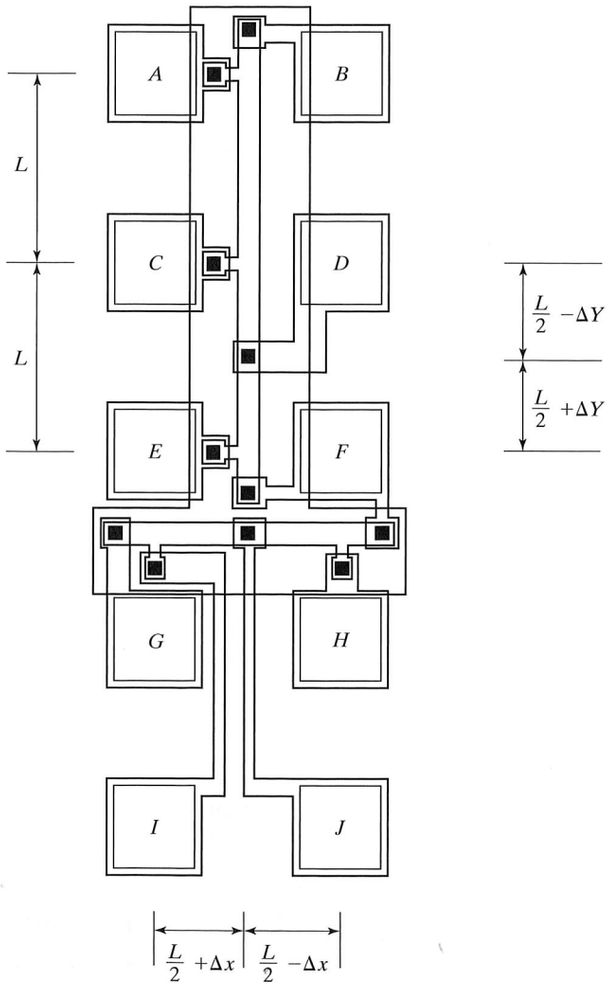


FIGURE P9.23

CHAPTER 10

Bipolar Process Integration

In this chapter, interactions between fabrication processes and bipolar device design and layout will be explored. In particular, we will look closely at relationships between impurity profiles and device parameters such as current gain, transit time, and breakdown voltage. Basic design rules for bipolar structures are introduced. The use of recessed oxidation, deep and shallow trenches, polysilicon electrodes and self-aligned processes in the formation of high-performance bipolar transistors will be presented. Dielectric and collector-diffused isolation processes are discussed, as well as silicon-germanium epitaxial-base transistors and advanced BiCMOS technologies, which provide bipolar and CMOS devices.

10.1 THE JUNCTION-ISOLATED STRUCTURE

The classic SBC process provides a backdrop for understanding the limitations of the basic bipolar transistor, as well as the structure of various other devices that are fabricated in bipolar IC processes. The basic junction-isolated bipolar process of Fig. 10.1 has been used throughout the IC industry for many years and has become known as the *standard buried collector* (SBC) process. In this junction-isolated process, adjoining devices are separated by back-to-back *pn* junction diodes that must be reverse biased to ensure isolation. (See Fig. 10.1(b).) The SBC process remains the primary bipolar process for analog and power circuit applications with power supplies exceeding 15 V. Although the SBC process was also originally used for logic circuits, most digital technologies have evolved to self-aligned, oxide-isolated processes using polysilicon and other technology advances first developed for MOS processes. Wafers with a <111> surface orientation were used specifically for bipolar fabrication for many years. However, in the past few years, it has become common to find bipolar processes also using <100> substrate material, which facilitates transfer of processes from MOS technology. Certainly, all BiCMOS technologies utilize <100> material.

The process flow for the SBC structure of Fig. 10.1(b) was discussed in Section 1.4 and will only be outlined here. An n^+ buried layer is formed by selective diffusion into a <111>-oriented p-type substrate and is followed by growth of an n-type epitaxial

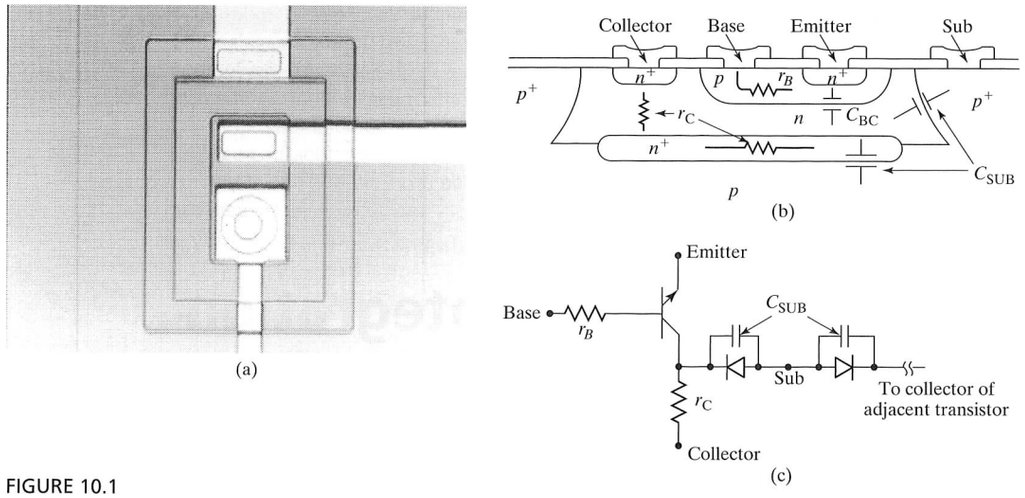


FIGURE 10.1

(a) Photo of an SBC transistor; (b) Cross section of a transistor fabricated with the SBC process showing the collector-base capacitances and the base and collector series resistances; (c) lumped circuit model for the transistor showing back-to-back diodes, which provide isolation between adjacent transistors.

layer. Isolated n-type collector islands are formed using a deep boron diffusion that surrounds the collector island. The base and emitter are formed by successive p- and n-type diffusions into the epitaxial layer. The structure is completed with contact window formation and metallization.

A cross section of the SBC impurity profile through the center of the device is shown in Fig. 10.2. In the next several sections, we will consider how the design of this profile is related to several important measures of device performance. An understanding of the basic profile design for the SBC process will help us see the advantages and disadvantages of other types of processes.

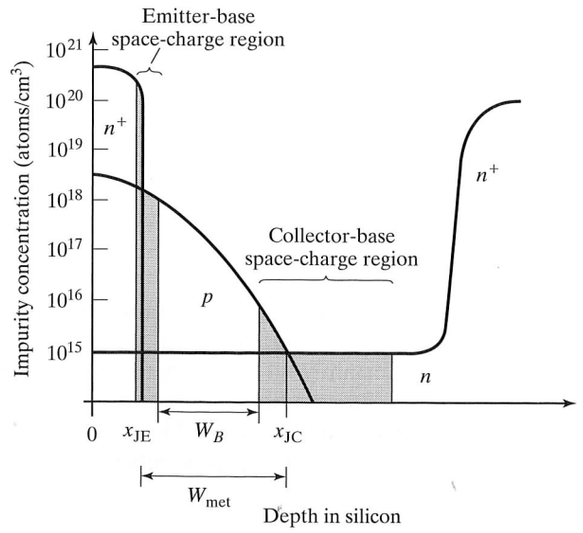


FIGURE 10.2

Vertical impurity profile in typical bipolar junction transistor. The shaded regions represent the emitter-base and collector-base space-charge regions. The metallurgical basewidth and electrical basewidth are indicated by W_{met} and W_B, respectively.

10.2 CURRENT GAIN

To be useful in circuits, the bipolar transistor must have a current gain of at least 10 to 20 for digital applications and an order of magnitude greater for analog applications. An expression for the current gain of the bipolar transistor is

$$\beta^{-1} = \frac{G_B}{G_E} + \frac{W_B^2}{\eta L_B^2} \tag{10.1}$$

The basewidth, W_B, is the width of the electrically neutral base region of the transistor. The constant η is determined by the shape of the impurity profile in the base and ranges from 2 to 20. L_B is the diffusion length for minority carriers in the base, and G_B and G_E are called the *Gummel numbers* in the base and emitter, respectively.

The *Gummel numbers* are defined by

$$G_B = \int_{\text{base}} \frac{N(x)}{D_B(x)} dx \quad \text{and} \quad G_E = \int_{\text{emitter}} \frac{N(x)}{D_E(x)} dx \tag{10.2}$$

where D_E and D_B are the minority-carrier diffusion constants in the emitter and base. Heavy doping effects in the emitter typically limit the value of G_E to 10^{13} to 10^{14} sec/cm^4. The basewidth is defined by the distance between the edges of the two space-charge regions in the base. For wide-base transistors, this is approximately equal to the distance between the metallurgical junctions, as shown in Fig. 10.2. For narrow-base transistors, the space-charge regions must be subtracted from the metallurgical basewidth, as discussed further in Section 10.4.

For large current gain, Eq. (10.1) should be as small as possible. The ratio of the Gummel numbers in the base and emitter should be low, the width of the base region should be small, and L_B should be large. Figure 10.3 shows the dependence of the diffusion length on impurity concentration. As the doping level increases, L_B decreases, but is greater than 10 μm for typical base-doping concentrations. In modern high-frequency transistors, the basewidth W_B is typically far less than the diffusion length L_B, and the first term in Eq. (10.1) determines the current gain.

From Eqs. (10.1) and (10.2), the emitter must be heavily doped relative to the base in order to obtain high gain. In fabricating a bipolar transistor, each successive diffusion is heavier than the last, and the final n^+ diffusion naturally performs best as the emitter. Thus, the n^+ layer nearest the surface is used as the emitter.

Example 10.1

Estimate the current gain for a transistor with the following parameters: $N_E/D_E = 5 \times 10^{13}$ sec/cm^4, $N_B/D_B = 10^{12}$ sec/cm^4, $W_B = 1$ μm, $L_B = 20$ μm, and $\eta = 10$.

Solution: Plugging these parameters into Eq. (10.1) yields $\beta^{-1} = 0.02 + 0.00025$ and $\beta = 50$. In this transistor, the current gain is dominated by the ratio of the Gummel number terms.

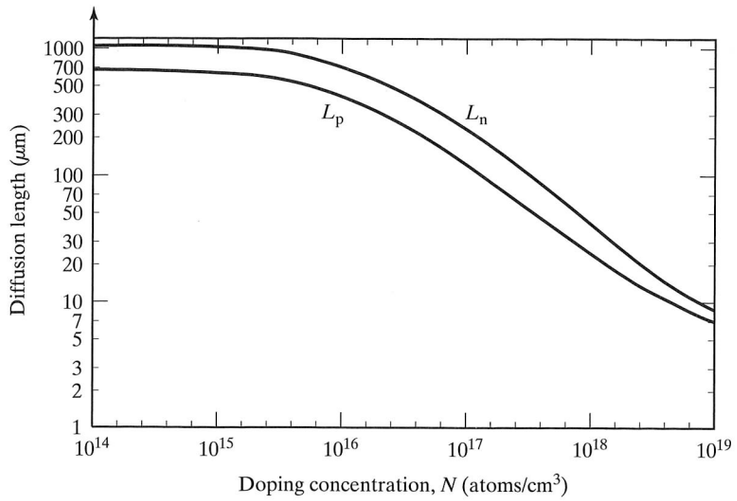


FIGURE 10.3

Calculated minority-carrier diffusion lengths as a function of doping concentration for bulk silicon using lifetime equations from Ref. [1].

10.3 TRANSIT TIME

Another important bipolar device parameter is the delay incurred during carrier propagation between the emitter and collector terminals of the transistor. Both logic switching speed and amplifier frequency response are limited by the *transit time*, which is defined by

$$\tau = r_E C_{BE} + W_B^2/\eta D_B + (C_{jC} + C_{sub})r_C + X_C/2V_s \tag{10.3}$$

The unity-gain frequency of the transistor, f_T, is given approximately by

$$f_T = \frac{1}{2\pi\tau} \tag{10.4}$$

The first term is the product of the small-signal resistance of the emitter region r_E and the emitter-base capacitance C_{BE}. The second term in Eq. (10.3), called the *base transit time*, represents the time required for a carrier to move across the neutral base region W_B. The third term is the delay associated with charging the capacitances connected to the collector node through the collector series resistance r_C. The capacitances C_{JC} and C_{sub} are determined by the collector-base and collector-substrate junction areas and by the doping concentrations of the base, collector, and substrate regions. The last term is the delay time associated with a carrier crossing the depletion region of the collector-base junction. X_C is the width of the depletion layer and V_S is the saturation velocity of the carriers.

In order to minimize τ, the basewidth is made as narrow as possible, the buried layer is added to minimize the value of r_C, and light doping is used to minimize the capacitances. Estimates of the capacitance of the junctions can be made using the one-sided step-junction expression (Eq. (9.3)) in which the capacitance is determined by the concentration on the lightly-doped side of the junction.

Example 10.2

Calculate the transit time for a bipolar transistor with the following parameters: r_E=25 Ω, C_{BE}=10pF, $W_B = 1$ μm, $\eta = 10$, $D_B = 20$ cm^2/sec, $C_{JC} + C_{sub} = 2$ pF, $r_C = 250$ ohms, $X_C = 10$ μm, and $V_s = 10^7$ cm/sec.

Solution: Substituting these values into Eq. (10.3) gives the following values for the four terms: 0.25×10^{-9} sec; 0.05×10^{-9} sec; 0.5×10^{-9} sec; 0.05×10^{-9} sec. The resulting value of transit time is 0.85×10^{-9} sec. The unity-gain frequency f_T is equal to 188 MHz.

Another important measure of the high-frequency performance of bipolar transistors is the product of the base resistance and collector-base capacitance, $r_B \bullet C_{BC}$. This product can be shown to limit the gain-bandwidth product of single-stage amplifiers [6]. A narrow basewidth increases the value of r_B. Employing heavier base doping counteracts the increase in base resistance, but increases the values of C_{BC} and C_{BE}. Choosing the base profile for optimum $r_B C_{BC}$ product is a delicate design issue.

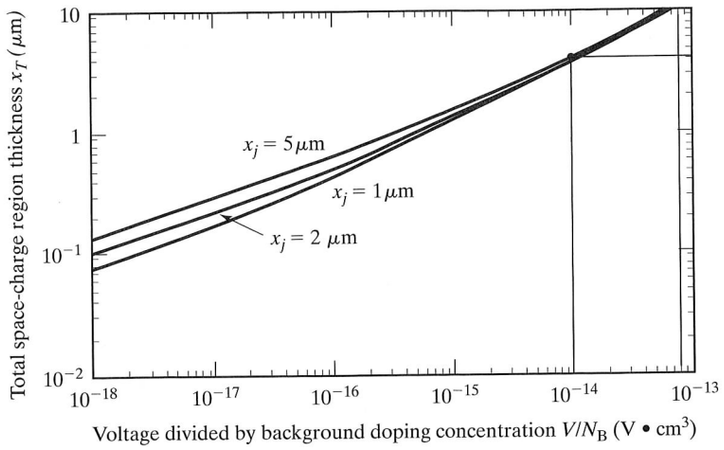
10.4 BASEWIDTH

Equations (10.1) through (10.3) indicate that device performance is improved by making the basewidth as narrow as possible. The primary restrictions on reducing the basewidth are set by breakdown-voltage requirements and by tolerances on the basewidth, due to variations in process control. For low-voltage logic devices, the metallurgical basewidth may be less than 1 μm. For higher voltage devices used in analog circuit or power applications, the basewidth must be wide enough to support the collector-base depletion-layer width under large reverse bias.

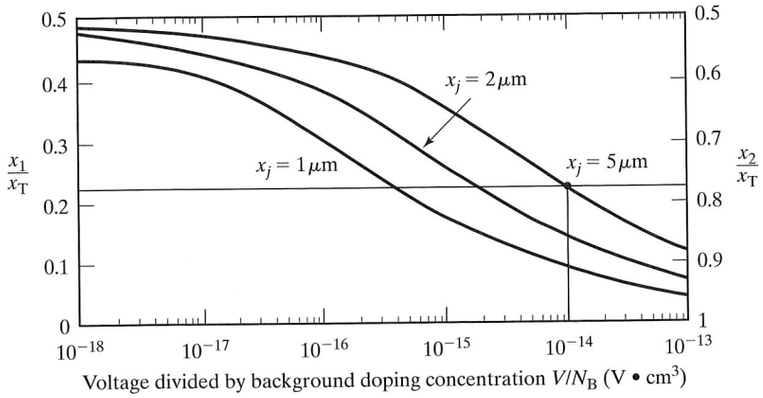
The actual basewidth of the transistor is determined by reducing the metallurgical basewidth by the portions of the emitter-base and collector-base space-charge regions, which protrude into the base as shown in Fig. 10.2. The emitter and base are both heavily doped near the base-emitter junction, and although the space-charge-region width of the emitter-base junction is usually quite small, it does extend almost entirely into the base. Its width can be estimated from Fig. 9.4.

The collector-base space-charge-region width is dependent on the voltage across the junction and extends into both the base and collector regions. Figure 10.4 shows the depletion-layer width on either side of a *pn* junction formed by a Gaussian diffusion into a uniformly doped substrate, the normal situation for a bipolar transistor fabricated using the SBC process.

Total space-charge region width X_T as a function of the ratio of applied voltage to background concentration (V/N_B) appears in Fig. 10.4(a), whereas the division of the total between the heavily doped side (x_1) and the lightly doped side (x_2) appears in the second half of the same figure.



(a)



(b)

FIGURE 10.4

The space-charge region width as a function of voltage and doping for a *pn* junction formed by a Gaussian diffusion into a uniformly doped substrate. (a) Total space-charge region width x_T; (b) fraction of total space-charge region width extending on the heavily doped side, x_1, and on the lightly doped side, x_2, respectively. After Ref. [4]. Reprinted with permission from the *AT&T Technical Journal*. Copyright 1960 AT&T.

Example 10.3

Estimate the space-charge region widths on each side of the collector-base junction of a bipolar transistor fabricated on a 1-ohm-cm *n*-type epitaxial layer. The reverse-bias voltage across the junction is 40 V, and the collector-base junction depth is 5 μm.

Solution: The doping of the epitaxial layer is 4×10^{15} /cm^3, giving a value of $V/N_B = 1 \times 10^{-14}$ V-cm^3. From Fig. 10.4(a), the total depletion-layer width is approximately 4 μm. From Fig. 10.4(b), 77%, or 3.1 μm, extends into the collector region, and 23%, or 0.9 μm, extends into the base region.

Increased base doping reduces the size of the space-charge regions in the base, permitting a narrow-base design. However, heavy base doping tends to increase the Gummel number in the base, which reduces the current gain of the transistor. Heavy doping also increases the collector-junction capacitance, thus increasing the transit time in Eq. (10.3). This is another situation in which conflicts arise when trying to optimize several different device parameters simultaneously.

10.5 BREAKDOWN VOLTAGES

The process designer must understand the magnitude of the voltages that will be applied to the transistors in circuit applications. The device in Ex. 10.3 had to withstand 40 V and was probably designed for analog-circuit applications. On the other hand, transistors designed for logic applications must support only relatively low voltages. For example, the devices used in TTL circuits are designed to withstand only 7 V. The multi-gigahertz oxide-isolated devices described subsequently in Section 10.8 often have breakdown voltages of 2.5 V or less.

10.5.1 Emitter-Base Breakdown Voltage

The emitter-base breakdown voltage is determined by the doping concentration and radius of curvature of the junction, as was discussed previously in Section 9.1.2. Breakdown occurs first in the region of the junction where the electric field is the largest, usually corresponding to the portion of the junction where the doping levels and curvature are the highest. The actual breakdown voltage is then determined by the doping on the more lightly doped side of the junction.

To achieve high current gain, the emitter region is doped heavily, and the breakdown voltage of this junction will be determined by the impurity concentration of the more lightly doped base region. The base impurity concentration is highest at the surface, so the emitter-base junction will tend to break down first at the surface. The curvature of the junction enhances the electric field and reduces the breakdown voltage. Figure 10.5 gives the breakdown voltage of the emitter-base junction as a function of

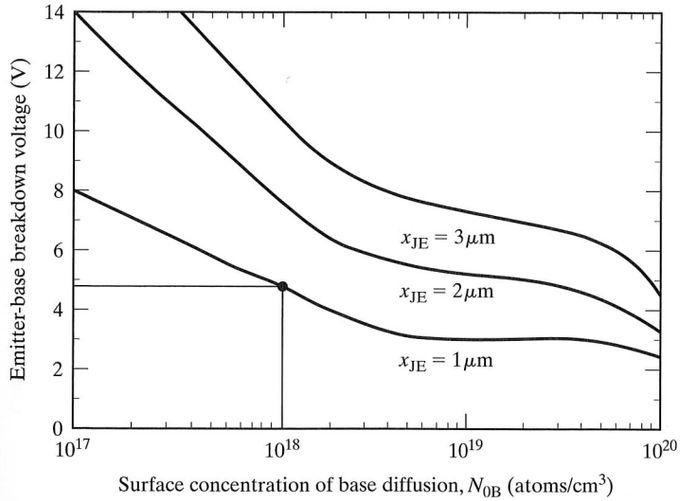


FIGURE 10.5

Emitter-base junction breakdown voltage as a function of base surface concentration with emitter-base junction depth as a parameter. After Ref. [4]. Reprinted with permission from *Solid-State Electronics*, Vol. 17, P. R. Wilson, "The Emitter-Base Breakdown Voltage of Planar Transistors." Copyright 1974, Pergamon Press, Ltd.[3]

the final surface concentration of the base region, with junction radius as a parameter. Emitter-base breakdown voltages are low because of the relatively large impurity concentrations on both sides of the junction.

Example 10.4

An *npn* transistor has a 1-μm-deep emitter-base junction and the base diffusion given in Example 4.2. What is the expected breakdown voltage of this junction?

Solution: The base-region surface concentration in Fig. 4.9 is $1.1 \times 10^{18}/\text{cm}^3$. Figure 10.5 predicts the breakdown voltage of a 1-μm-deep junction with this surface concentration to be approximately 4.8 V. (The emitter-base junctions of most common bipolar transistors will break down well below 10 V.)

10.5.2 Circular Emitters

Although the structures shown thus far have been drawn with square or rectangular emitter regions, circular emitters (see Fig. 10.6) commonly appear in technologies used for analog applications. Matching tends to be better with circular emitters, and the use of circular emitters increases the radius of curvature of the junction and therefore the breakdown voltage of the emitter-base junction. (See Figs. 9.3 and 10.5.) Figure 10.6 shows a quad of cross-connected *npn* transistors that are often used to improve matching in differential amplifiers.

10.5.3 Collector-Base Breakdown Voltage

The bipolar transistor can begin to conduct excessive collector current by two mechanisms. The first is Zener or avalanche breakdown of the collector-base junction. As previously discussed, breakdown is localized to the region where the doping concentrations

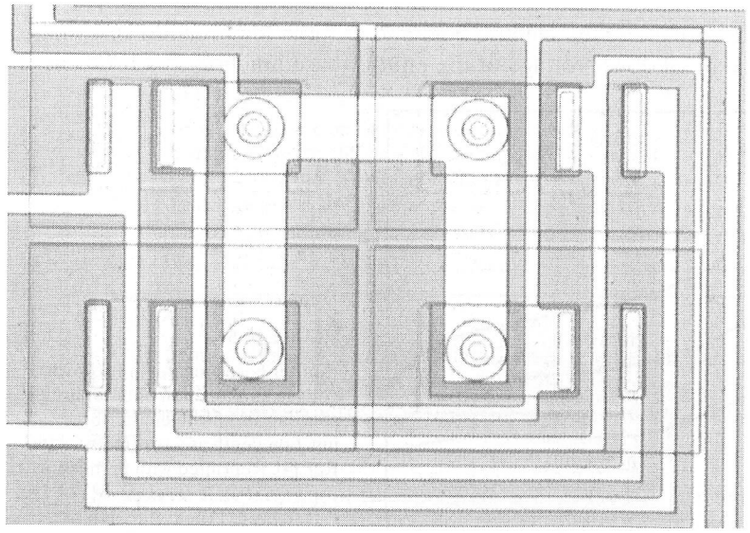


FIGURE 10.6
Cross-connected quad of transistors with circular emitters.

are the largest, but it is determined primarily by the doping concentration on the more lightly-doped side of the junction. The collector is formed in the uniformly doped epitaxial layer. The base region is diffused into the epitaxial layer and is the more heavily doped side of the junction. Since the collector is uniform, junction breakdown will occur first where the electric field is enhanced by junction curvature. The breakdown voltage for the collector-base junction as a function of epitaxial-layer impurity concentration and junction radius is given in Fig. 10.7.

The second breakdown mechanism is punch-through of the base region and is illustrated in Fig. 10.8. The epitaxial layer is more lightly doped than the base region, and the collector-base junction depletion layer extends predominantly into the epitaxial layer. As the collector-base voltage increases, the depletion layer expands further into the epitaxial layer and will eventually hit the n^+ buried layer. At this point, further depletion-layer expansion will occur in the base, and any increase in collector-base voltage will quickly punch through the remaining base region.

The second set of curves in Fig. 10.7 shows collector-base junction breakdown limitations set by punch-through. As already described, the primary parameters determining the punch-through voltage are the epitaxial-layer doping and the width, $X_{BL} - X_{BC}$, of the region between the collector-base junction and the n^+ buried layer.

Example 10.5

What is the collector-base breakdown voltage of a transistor with a 10-μm-thick epitaxial layer doped at a level of $10^{15}/\text{cm}^3$ if the collector-base junction depth is 5 μm? Assume that the buried layer has diffused upward 2 μm.

Solution: First, determine the avalanche breakdown voltage of an isolated *pn* junction. Figure 10.7 gives a breakdown voltage of approximately 130 V for a doping of $10^{15}/\text{cm}^3$. Next, we must also check the punch-through limitations for $X_{BL} - X_{BC} = 3$ μm. From Fig. 10.7 the transistor will punch through at approximately 30 V. So the collector-base breakdown voltage is limited to 30 V by punch-through in this transistor.

As usual, different device requirements produce conflicting design constraints. High Zener breakdown voltage requires low epitaxial-layer doping. Low epitaxial-

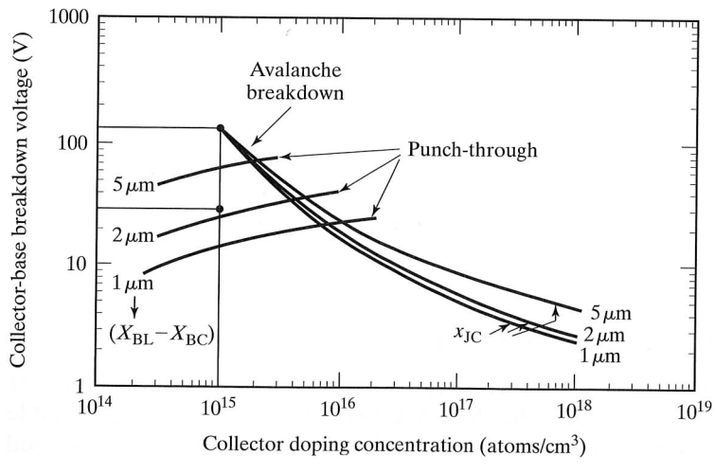


FIGURE 10.7
Collector-base junction breakdown voltage as a function of collector-doping concentration with collector-base junction depth and punch-through limits as parameters. After Ref. [4]. Reprinted from the *Journal of the Electrochemical Society*, Volume 113 (1966), pages 508–510, by permission of the publisher, The Electrochemical Society, Inc.,[19] and Pergamon Press, Ltd.[20]

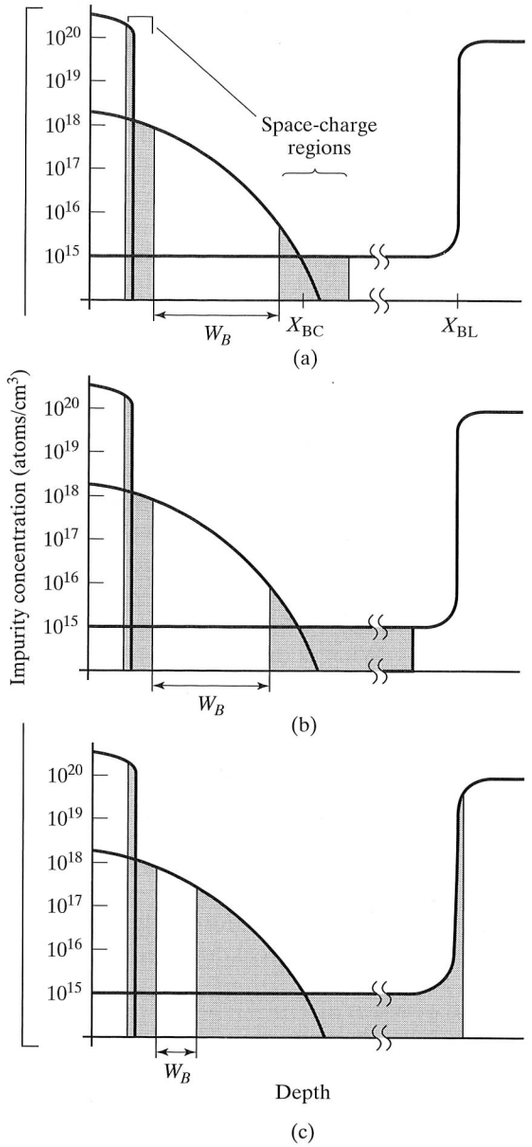


FIGURE 10.8

Collector-base space-charge region growth as the collector-base voltage is increased. (a) Zero bias; (b) intermediate collector-base voltage; (c) large collector-base voltage just below the punch-through voltage.

layer doping requires a relatively wide epitaxial-layer thickness in order to prevent punch-through. However, a wide depletion-layer width in the epitaxial layer increases the transit time and reduces the frequency response of the device.

10.6 OTHER ELEMENTS IN THE SBC TECHNOLOGY

Obviously, other electronic elements, such as resistors, diodes, and *pnp* transistors, are required to build circuits in bipolar technology. Several resistor structures are available with widely divergent values of sheet resistance. The SBC technology is optimized

TABLE 10.1 Resistors in the SBC Technology.

Resistor Layer	Sheet Resistance (Ω/□)	Absolute Tolerance (%)	Matching (%)
Emitter Diffusion	5–20	20	2
Base Diffusion	100–200	20	0.2–2
Epitaxial Layer	1000–5000	30	5
Pinched Base	2000–10,000	50	10
Ion Implanted	100–1000	3	0.1–1

around the *npn* transistor whose characteristics are dominated by high-mobility electron transport across the base region. High-quality *pnp* transistors are more difficult to form in this technology. However, there are two types of useful *pnp* transistors that can readily be fabricated. The first is a *substrate pnp*, which has its collector permanently tied to the substrate potential. The second is the *lateral pnp*, which does provide uncommitted collector, base, and emitter terminals, but has much poorer current gain and frequency response compared with the vertical *npn* transistor.

10.6.1 Emitter Resistor

A resistor may be formed from the emitter diffusion, as depicted in Fig. 10.9. The emitter layer is a low-sheet-resistance region and is therefore useful only for relatively small-value resistors. A meandering resistor pattern is often used to achieve the

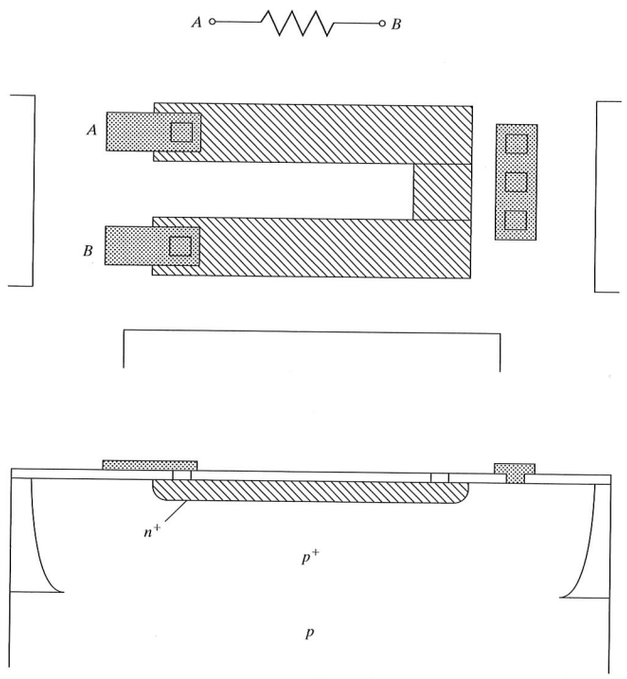


FIGURE 10.9

Resistor using the n^+ emitter diffusion into the isolation region.

required number of squares in the resistor. (See Prob. 4.10.) In Fig. 10.9, the emitter layer is placed directly in the relatively heavily doped p-type isolation region, which is normally connected directly to the most negative power supply. Resistor-substrate isolation will be maintained by a reverse bias across the pn junction. The resistor body represents an n^+–p^+ junction, which leads to a relatively large junction capacitance per unit area and low breakdown voltage. (See Fig. 7.8.)

10.6.2 Base Resistor

The most common resistor utilizes the base diffusion within an isolated n-type epitaxial region, as in Fig. 10.10. Here, again, a meandering resistor pattern can be used to achieve the desired resistance value. The resistor body must be kept reverse biased

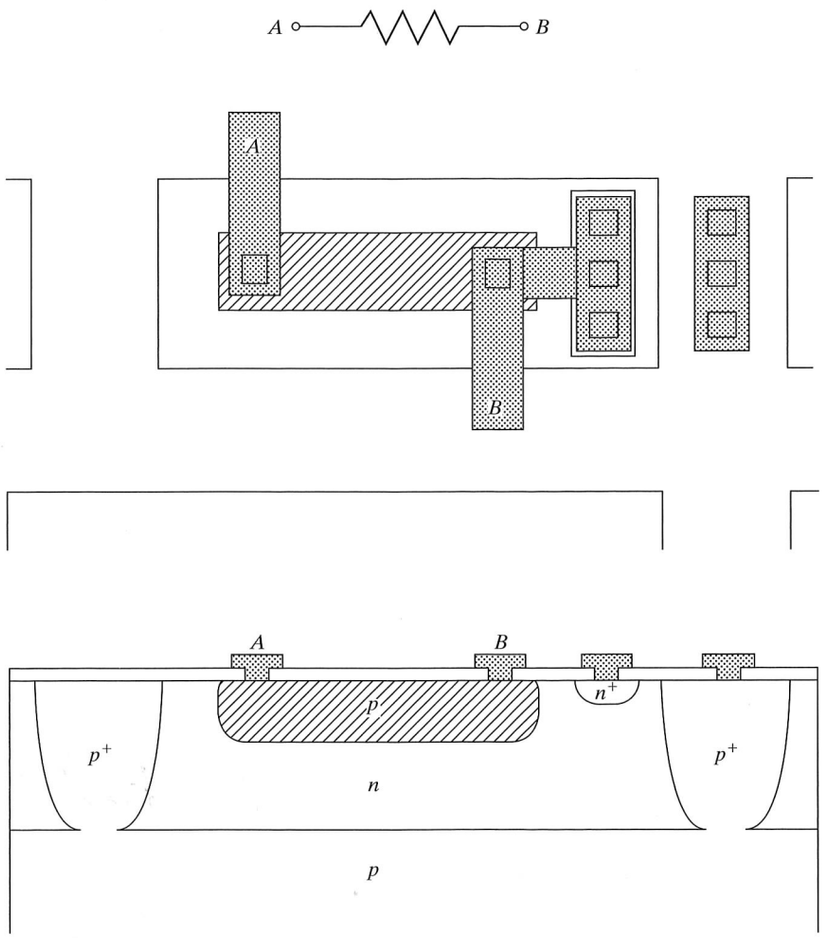


FIGURE 10.10
Resistor formed from the standard p-type base diffusion.

along its length, so the n-region contact is tied to either the most positive end of the resistor or directly to the most positive power supply in the circuit. An n^+ region is placed below the aluminum contact to ensure the formation of an ohmic contact and not a Schottky barrier diode.

10.6.3 Epitaxial Layer Resistor

The epitaxial layer itself provides a high-sheet-resistance layer, and high-value resistors can be formed with a small number of squares, but the absolute value is often poorly controlled. The epitaxial-layer resistor is formed by making two ohmic contacts to an isolated epitaxial region, as in Fig. 10.11.

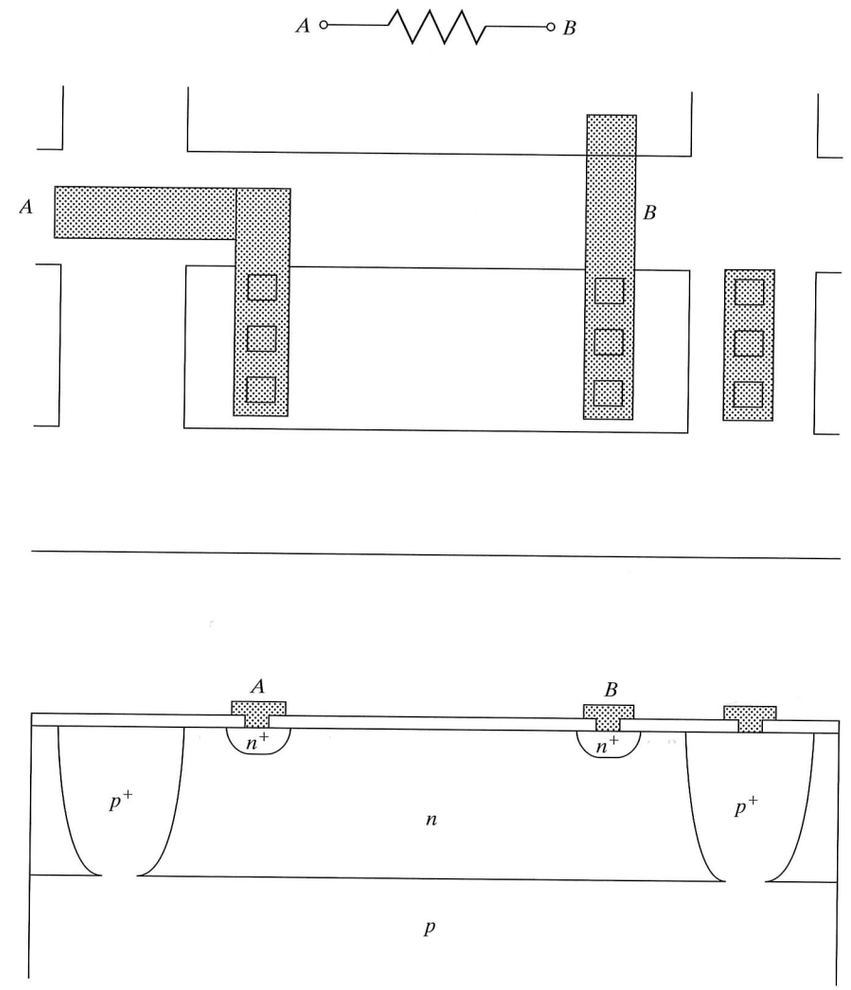


FIGURE 10.11
Resistor formed from the n-type epitaxial layer.

10.6.4 Pinch Resistor

An alternative technique used to obtain higher sheet resistance is to narrow the thickness of the base diffusion by crossing it with an emitter diffusion, as drawn in Fig. 10.12. The structure is very similar to the *npn* transistor, except that the emitter diffusion merges with the epitaxial-layer island beyond the edges of the *p*-type region. The high-sheet-resistance region that is obtained corresponds to the active base region of the *npn* transistor. The resistance value is highly dependent upon the thickness of the pinched base region, and the absolute tolerance is relatively poor. The pinched base resistor may also be used as a JFET with terminals *A* and *B* acting as source and drain and the *n* serving as the gate.

10.6.5 Substrate *pnp* Transistor

The so-called *substrate pnp* transistor is formed from the *p*-type diffusion (emitter), isolated epitaxial tub (base) and *p*-type substrate (collector), as shown in Fig. 10.13.

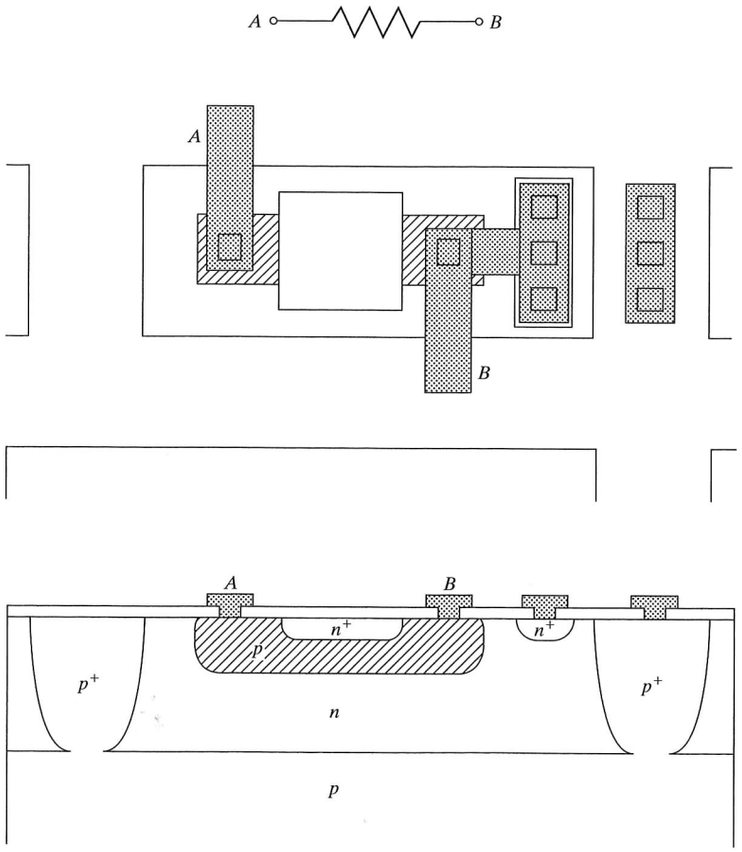


FIGURE 10.12
Pinched base resistor.

The basewidth W_B, set by the distance between the bottom of the *p*-type diffusion and the bottom of the *n*-type epitaxial layer, is typically much wider than that of the *npn* device. Thus, the current gain and frequency response are correspondingly less than those associated with the *npn* transistor. Also, the collector, formed from the *p*-type substrate, is inherently tied to the most negative power supply level in the circuit. Thus, only the base and emitter terminals are free for connection. Even so, the substrate *pnp* is often found as an emitter follower in the output stages of op-amps. The substrate *pnp* structure also appears in the *n*-well CMOS technology, where it is formed from the *p*-type source–drain region, the *n*-well, and the *p*-type substrate. In *p*-well CMOS technology, a substrate *npn* transistor can be formed.

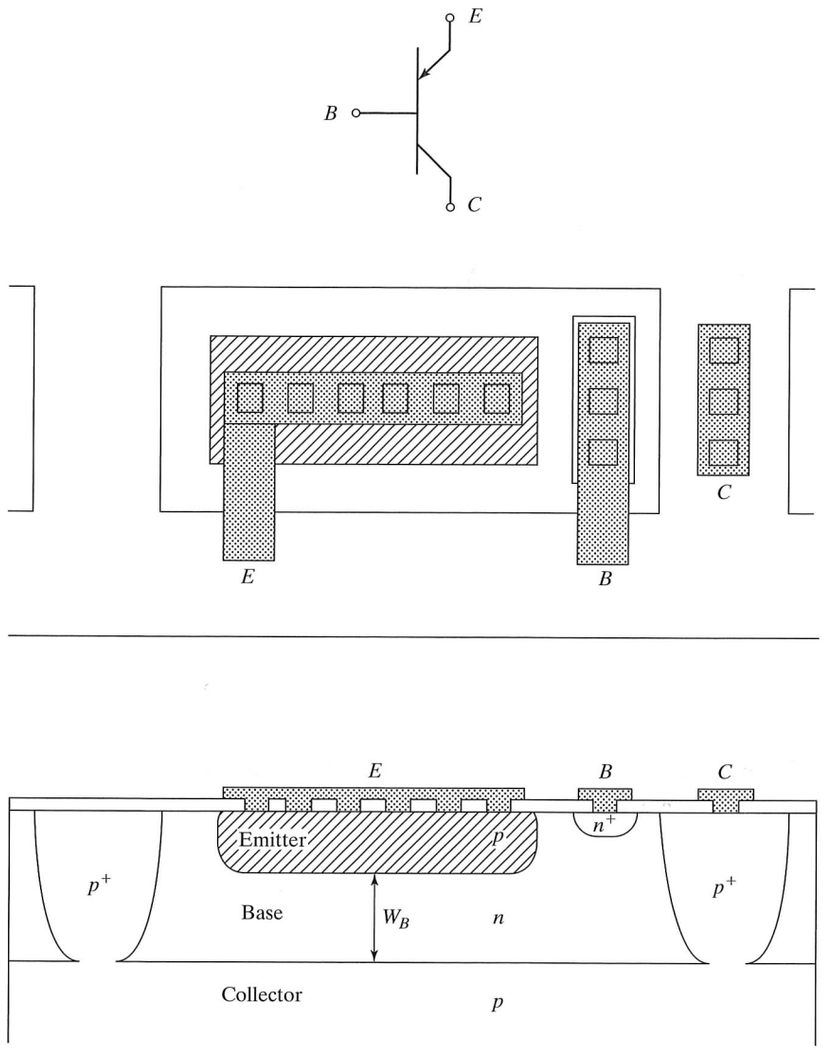


FIGURE 10.13
Substrate *pnp* transistor.

10.6.6 Lateral *pnp* Transistors

The lateral *pnp* structure in Fig. 10.14 provides a transistor with uncommitted collector, base, and emitter contacts. The emitter and collector are formed from the *p*-type region that is used for the base of the *npn* transistor. The basewidth is determined by the lithographic spacing between the two diffusions plus the degree of lateral diffusion

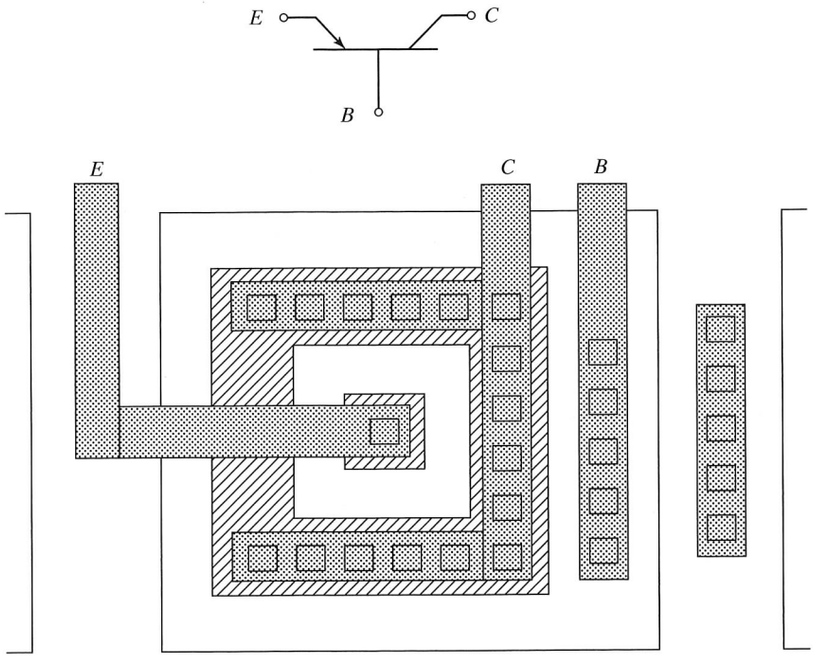


FIGURE 10.14
Enclosed lateral *pnp* transistor structure.

and is therefore much wider than that of the *npn* transistor. This leads to low current gain and poor f_T. It is difficult to achieve a high current gain, because the emitter tends to inject carriers equally in all directions, but the collector only collects those carriers that cross the base region between the sides of the two *p*-type regions. Thus, *pnp* transistors are often enclosed structures with the emitter surrounded by the collector, as in Fig. 10.14. (See Prob. 10.9.)

10.6.7 Schottky Diodes

Bipolar logic circuits, for example, classic Schottky TTL, have used Schottky diodes to prevent the saturation of *npn* transistors. A simple Schottky diode can be formed from an aluminum contact to the lightly doped *n*-type layer as shown in Fig. 10.15(a). A *p*-type ring is often used to minimize problems with high fields at the edges of the metal contact, as are circular diode layouts. Although the resulting structure places a Schottky diode in parallel with a *pn* junction diode, forward conduction is dominated by the low forward voltage drop of the Schottky diode.

Schottky diodes tend to have both higher leakage current and lower breakdown voltage in the reverse direction than a *pn* junction diode. A clever solution to this problem appears in Fig. 10.15(b), in which multiple *p*-type diffusions have been added to the interior of the Schottky diode region [7]. In the forward direction, multiple Schottky and *pn* junction diodes are in parallel, but the low voltage drop of the Schottky diode again dominates the forward region of the diode. However, under reverse bias, the depletion regions of the *pn* diodes merge, and the reverse breakdown appears as that of the *pn* junction, rather than the Schottky barrier diode. This structure shows the use of a detailed understanding of the behavior of the *pn* junction to achieve a novel result.

10.7 LAYOUT CONSIDERATIONS

This section will explore mask layout for a classic SBC transistor. The analysis will expand our understanding of the interaction of process design and layout. In particular, the top view of the mask set for a bipolar transistor often differs greatly from the final device structure, due to large lateral diffusions, although this is much less true of the high-performance digital technologies discussed in Section 10.8.

10.7.1 Buried-Layer and Isolation Diffusions

The spacing between adjacent buried layers and the width of the intervening isolation diffusion determines how closely two transistors can be spaced. To maintain electrical isolation, the substrate is tied to the most negative voltage present in the circuit. The collector of a transistor, on the other hand, is often connected to the most positive voltage in the same circuit. Thus, the collector-substrate junction must be designed to support a voltage equal to the sum of the positive and negative voltages supplying the circuit. For analog circuits, this may be more than 40 V. A typical design value of 60 V would provide an adequate safety margin.

Figure 10.16 shows the depletion layer in the *p* and *n* material near the isolation region of the transistor. The doping of the isolation diffusion is heavy at the surface and

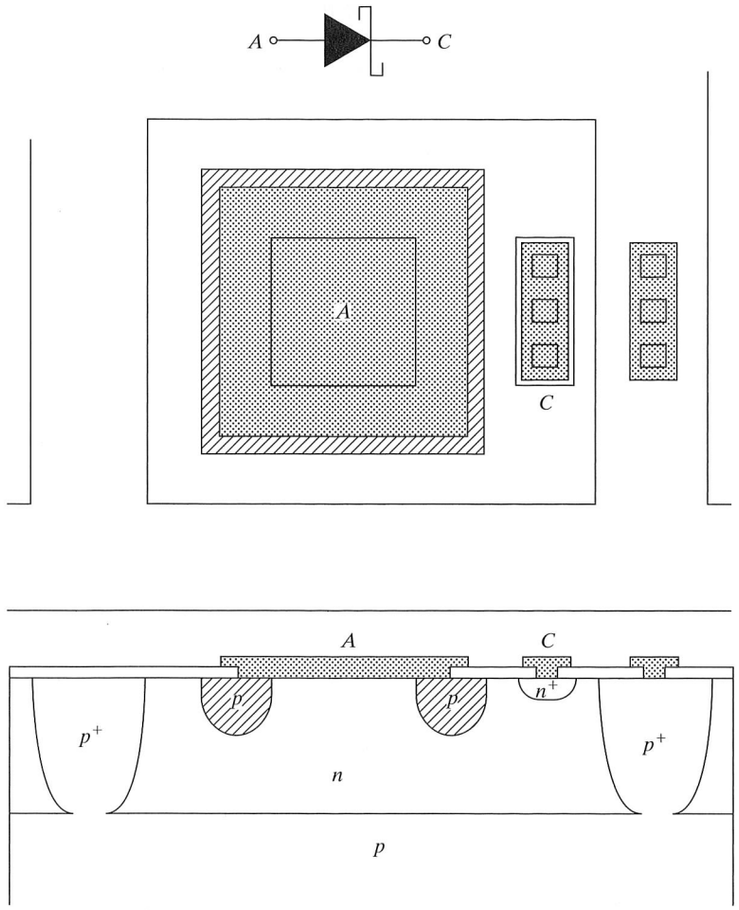


FIGURE 10.15

(a) Schottky barrier diode with p-type breakdown protection ring; (b) high reverse breakdown Schottky barrier diode.

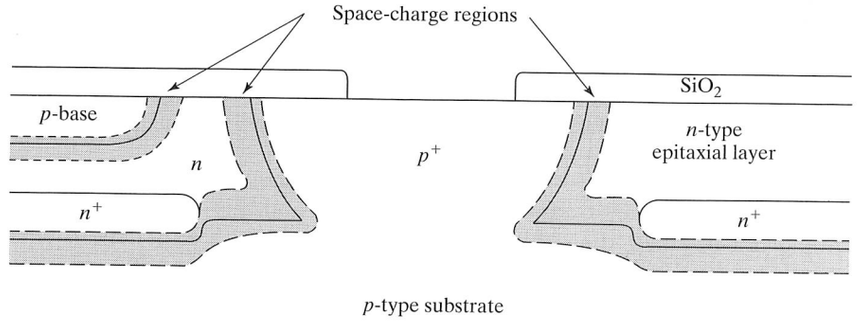


FIGURE 10.16

Isolation region between two bipolar transistors. The spacing must be large enough to ensure that the two space-charge regions do not merge together.

intersects the original substrate to produce isolation. At the surface, the window defining the isolation diffusion may be a minimum feature size, but the total width of the isolation region at the surface will be determined by lateral diffusion. For example, if the epitaxial layer is 15 μm thick and the minimum feature size is 10 μm, the isolation region will approach 40 μm in width, assuming that lateral diffusion equals vertical diffusion. Obviously, this form of isolation is not acceptable for VLSI/ULSI logic circuits.

The n^+ buried-layer diffusion is not usually permitted to intersect the p^+ isolation diffusion. If the two diffusions meet, the breakdown voltage of the junction will decrease, and the capacitance of the junction will increase. Thus, there will be a layout design rule associated with the minimum spacing between the n^+ region and the isolation diffusion.

10.7.2 Base Diffusion to Isolation Diffusion Spacing

At the surface, the collector-base and collector-substrate depletion regions of Fig. 10.16 must not merge. The minimum spacing can be determined from a knowledge of the applied voltages and the epitaxial-layer impurity concentration. Additional spacing must be added to account for the alignment sequence and accumulated alignment tolerances.

Example 10.6

What is the minimum spacing between the edge of the base diffusion and the edge of the isolation diffusion at the surface of a bipolar transistor if the alignment tolerance is 1 μm and the epitaxial-layer resistivity is 10 ohm-cm? Assume that the two junctions must each support 40 V. Use a collector-base junction depth of 5 μm.

Solution: A 10-ohm-cm epitaxial layer has an impurity concentration of $5 \times 10^{14}/\text{cm}^3$, giving a value of $V/N_B = 8 \times 10^{-14}$ V-cm^3. From Fig. 10.7, the total depletion-layer width is approximately 10 μm, with 8.7 μm in the epitaxial layer. The conditions at the isolation-collector junction are essentially the same, so the minimum spacing will be two times the depletion-layer width of 8.7 μm plus the alignment tolerance of 1 μm for a total of 18.4 μm.

10.7.3 Emitter-Diffusion Design Rules

The minimum spacing between the edges of the emitter and base diffusions must be greater than the sum of the emitter and collector depletion-layer widths in the base, the accumulated alignment tolerance between the emitter and base masks, and the active base-region width.

In the basic SBC process, the n^+ emitter diffusion is also used to ensure the formation of a good ohmic contact to the collector, and this collector contact diffusion should not intersect the depletion layers associated with either the p-type base or isolation diffusions. If this occurs, the breakdown voltage of the junctions will be reduced and the junction capacitances increased. (See Prob. 10.7.)

10.7.4 A Layout Example

A set of design rules for a hypothetical bipolar transistor is given in Table 10.2, and Fig. 10.17 shows the layout of a minimum-size transistor based on these rules and making maximum use of lateral diffusion. It is important to note that the active area of the transistor—the region directly under the emitter—is a small fraction of the total device area of approximately 4536 μm^2. The final emitter area is 11×11 μm, or 121 μm^2, which represents only 2.67% of the total area of the transistor. (Remember, a similar area utilization problem occurred with the layout of the metal gate MOS transistor.)

The rest of the area is needed to make contacts, to support depletion layers, and to provide isolation between adjacent devices. In this layout, the isolation area is 2800 μm^2, or more than 60% of the total area! Minimization of the isolation region represents an important issue in high-performance devices, not only for density improvement, but also for junction-capacitance reduction.

The solid lines in the top view of the transistor layout represent the edges of the masks used to fabricate the transistor. The various dotted lines represent the final positions of the emitter, base, and isolation diffusions. For the design rules of Table 10.2, the window for the emitter diffusion happens to coincide exactly with the emitter contact window. The lateral diffusion of 3 μm provides more than the required 2-μm alignment tolerance for the emitter contact window.

TABLE 10.2 Bipolar Transistor Design Rules for Fig. 10.17.

Minimum feature size	5 μm
Worst-case alignment tolerance between levels	2 μm
Epitaxial-layer thickness	10 μm
Collector-base junction depth	5 μm
Emitter-base junction depth	3 μm
Minimum emitter-to-collector spacing at surface	5 μm
Minimum base-to-isolation spacing at surface	5 μm
Minimum collector contact n^+ diffusion to isolation spacing	5 μm
Minimum collector contact n^+ diffusion to base spacing	5 μm
Buried-layer diffusion (both up and down)	2 μm
Buried layer to isolation spacing	5 μm
Buried layer pattern slift	10 μm
Lateral diffusion = vertical diffusion	

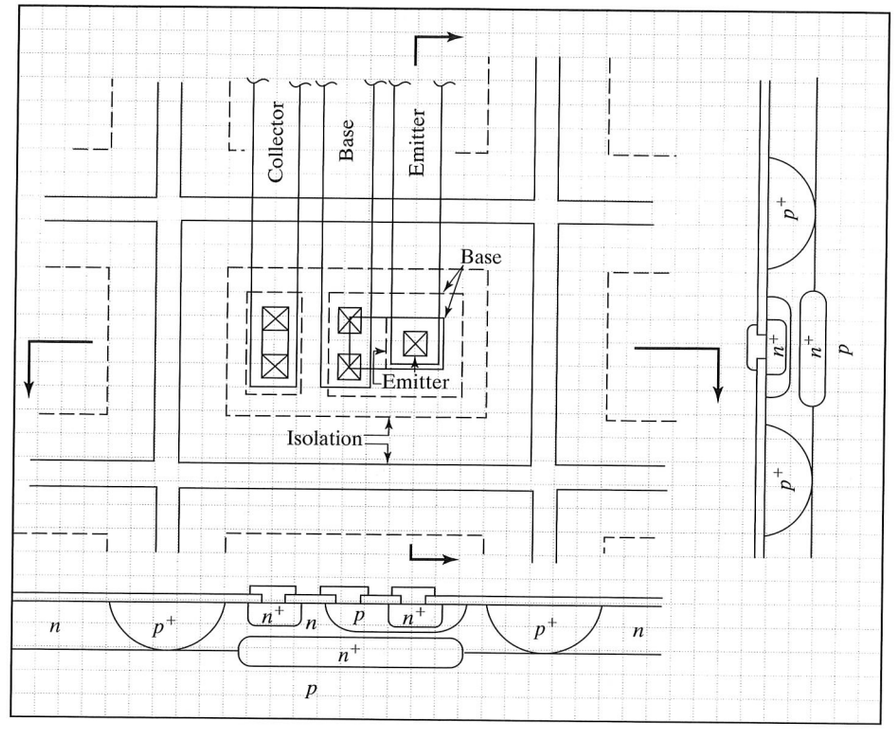


FIGURE 10.17

Minimum-size bipolar transistor layout based on the design rules of Table 10.2. The buried layer is not shown in the top view for reasons of clarity. Each square is 5 μm × 5 μm.

The base diffusion is 5 μm deep and is assumed to diffuse laterally 5 μm. In the layout, the base contact windows actually extend outside the base region at the mask level, but are more than one alignment tolerance within the base region following diffusion. This is an excellent example of the interaction between processing and layout. However, only a most aggressive designer would consider a layout ground rule such as this.

The width of the base-contact metallization has been widened to more than a minimum feature size to help clarify the figure. This did not affect the size of the device, as space was available, because of other design rule limitations. Two base and two collector contact windows fit within the minimum base and n^+ collector contact regions. The collector contact windows align with the edges of the n^+ diffusion window, as was the case for the emitter.

The buried-layer mask has also been omitted from the figure for clarity. In this particular structure, the design rules relating to the buried layer are not limiting factors in the size of this layout.

10.8 ADVANCED BIPOLAR STRUCTURES

For digital logic circuits, structures are optimized to provide as short a transit time as possible. This requires minimizing the basewidth, eliminating as much capacitance as possi-

ble by minimizing total junction area, minimizing the width of the collector space-charge region, and reducing the collector and base series resistances. A reduced current gain is traded for a shorter transit time. As mentioned earlier, although <111> wafers were originally used for bipolar processing, silicon with a <100> surface orientation is now commonly used in most advanced bipolar processes.

10.8.1 Locos-Isolated Self-Aligned Contact Structure

Figure 10.18 shows a high-performance bipolar structure that attempts to achieve the a forementioned goals by using a very thin epitaxial layer and shallow ion-implanted base and emitter regions. As much *pn* junction area as possible is eliminated through the use of oxide isolation. The sides of the emitter and base regions are actually walled by the oxide isolation regions. The n^+ buried layer is relatively large to minimize r_C, and the total base region is minimized to reduce the base resistance. Self-aligned contacts are made to the base, emitter, and collector regions.

The formation of the transistor of Fig. 10.18 begins with the implantation and diffusion of the buried layer with a typical sheet resistance of 10 to 50 ohms per square. The masking oxide is removed, and a thin epitaxial layer is grown on the surface. A recessed oxide isolation process is used to form the isolation regions between devices and to eliminate the unnecessary junction area between the collector and emitter contacts. Prior to oxidation, part of the epitaxial layer is etched away so that the subsequent oxidation will extend completely through the epitaxial layer. An implantation is used to overcome boron depletion in the substrate during oxidation.

Next, the silicon nitride–oxide sandwich is removed, and an oxide is regrown on the surface. A boron implantation creates the shallow active base region. A mask is used to create windows for the emitter, and contacts to the base, emitter, and collector are all defined at the same time. Note that a single oxide strip defines both the emitter and base contact regions, eliminating alignment tolerances that would be needed if the regions were formed separately. The width of this strip is set by the metal-to-metal spacing plus accumulated alignment tolerances.

Photoresist is used as a barrier material during implantation of the base contact region. This p^+ implantation further reduces the base resistance of the device. Photoresist is also used as a barrier material during implantation of the emitter and collector contact regions. Note that these two mask steps use noncritical *blockout* masks similar to those used for threshold adjustment in a CMOS process.

Contacts are made through the same openings used for the base and emitter implantations. These contact areas are all cleared by a short wet or dry etch prior to metallization. Because of the very shallow junction depths involved in this structure, the metallization will be a multilayer sandwich structure including a barrier metal in the contact region. Interconnection of devices to form circuits will typically involve a multilevel metal process.

10.8.2 Dual Polysilicon Self-Aligned Processes

Figure 10.19 outlines an early dual-polysilicon self-aligned process whose steps remain representative of those used to form many of today's high-performance bipolar devices [8]. A nonselective n^+ buried layer and *n*-epitaxial layer are fabricated on the *p*-type substrate. Deep trenches are used to provide isolation between devices. After etching, the

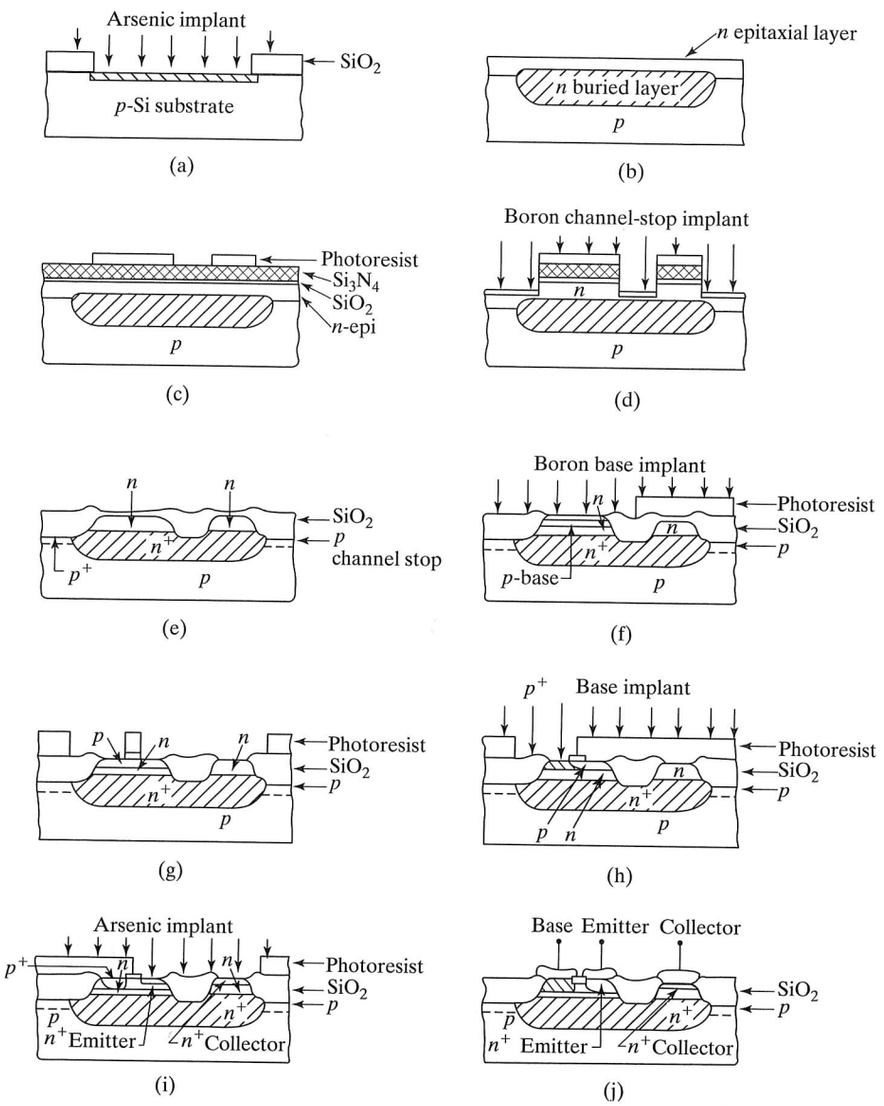


FIGURE 10.18

Process sequence for a high-performace oxide-isolated bipolar transistor. (a) Buried-layer formation; (b) epitaxial layer growth; (c) mask for selective oxidation; (d) boron implant prior to recessed oxide growth; (e) selective oxidation; (f) base mask and boron base implantation; (g) emitter, base contact, and collector contact mask; (h) p^+ base contact implantation; (i) arsenic implantation for emitter and collector contact; (j) structure completed with multilayer metallization. Copyright 1985, John Wiley & Sons, Inc. Reprinted with permission from Ref. [5].

trench walls are oxidized and then refilled with polysilicon. (CVD oxide is also used in some processes.) A p^+ implant is used to minimize the impact of boron depletion in the trench. Next, shallow trench regions are formed, yielding a planarized surface. An n^+ "sinker" diffusion is used to contact the n^+ buried collector layer.

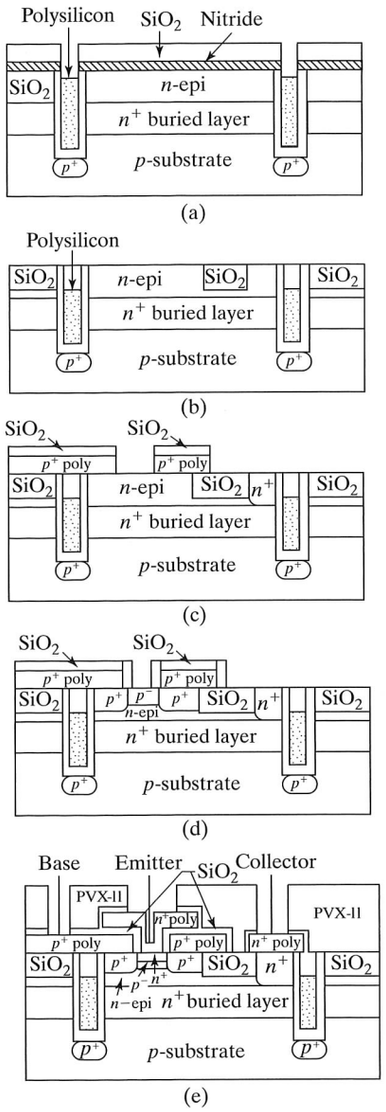


FIGURE 10.19

A high-performance bipolar transistor structure with an f_T of 10 GHz. (a) Isolation is achieved using deep-trench isolation with polysilicon and silicon dioxide refill; (b) structure following selective oxidation; (c) p^+ polysilicon deposited and patterned; (d) diffusion from doped polysilicon forms the extrinsic base region and base contacts; a self-aligned implantation forms the intrinsic base; (e) diffusion from n^+ polysilicon forms the emitter and the emitter and collector contacts of the transistor. Copyright 1997, IEEE. Reprinted with permission from Ref. [8].

Polysilicon is deposited and heavily doped with p-type impurities, commonly by ion implantation. The base opening is delineated, the intrinsic base region is implanted through the base window, and the polysilicon is oxidized. During subsequent annealing and processing steps, the extrinsic base region outdiffuses from the polysilicon forming p^+ side contacts to the more lightly doped intrinsic base region. The heavy poly doping minimizes the extrinsic base region's contribution to the base resistance. The oxide on the polysilicon provides an insulating layer that will separate the emitter contacts from the base contacts. Note the added formation of oxide on the sides of the polysilicon layer similar to that used for LDD processing in MOS devices.

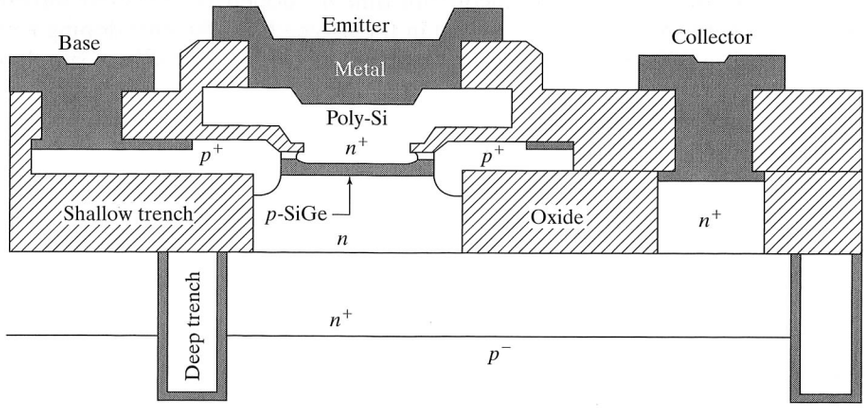
The second layer of polysilicon, this time n^+ doped, is deposited and annealed, forming a very shallow emitter region in the p-type base. Arsenic doping is typically used, because of its smaller diffusion coefficient. The n^+ polysilicon simultaneously provides contacts to both the emitter and the n^+ collector sinker. Note that the intrinsic base, base contacts, and emitter are defined and formed as a result of a single lithographic step and are referred to as being self-aligned. The elimination of alignment tolerances between emitter, base, and base contact layers results in significant reduction in overall size of the transistor and attendant minimization of device capacitances.

In these processes, the devices have extremely shallow emitters and narrow base-widths in order to achieve high f_T. To constrain and control the depletion-layer extents and value of the base resistance, the doping of the base region must be increased, and both the narrow base and increased doping levels lead to relatively low breakdown voltage in the transistor. Many of these devices are designed to operate with supply voltages of 2.5 V and below. In addition, the overall "thermal budget" (Dt product) is very small.

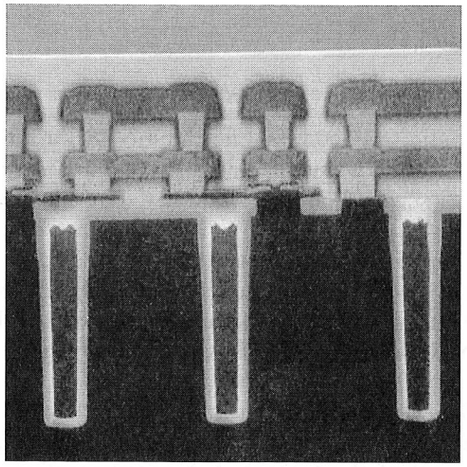
10.8.3 The Silicon–Germanium Epitaxial Base Transistor

By adding germanium to silicon [9], one can modify the silicon bandgap and perform "bandgap engineering" in a manner similar to that achieved in III–V compound semiconductor materials such as GaAs, InP, and InAs. Germanium is a Column IV element, as is silicon, so it does not act as a dopant impurity in silicon. However, when germanium replaces silicon in the lattice, it modifies the bandgap of the composite material. The bandgap change enhances the current gain and can result in a built-in base field that increases the unity-gain frequency of the transistor. At the time of this writing, cutoff frequencies in excess of 200 GHz have been reported in such SiGe heterojunction bipolar transistors (SiGe HBTs).

In SiGe HBTs, germanium is introduced into the base region of the device, with peak concentrations of less than 15%, during an epitaxial growth step that is used to form the base region of the transistor. A representative cross section of the SiGe device structure appears in Fig. 10.20(a), with a microphotograph of the structure in Fig. 10.20(b). The structure uses a combination of deep and shallow trenches for isolation. (The deep trenches in the photograph are approximately 5 μm deep.) The base region is formed by a carefully controlled epitaxial growth under ultrahigh-vacuum (UHV) conditions, which produces a single crystal intrinsic base region in the silicon window, but results in the formation of polycrystalline silicon over the oxide. During the epitaxial growth, various germanium profiles can be introduced into the intrinsic base region to produce the SiGe base device. A sacrificial gate structure is used to protect the emitter region during a p^+ implant that heavily dopes the polysilicon and provides the side wall contacts to the intrinsic base region. (This implant is actually the *S/D* implant for a PMOS transistor in a BICMOS process; see Section 10.10.) The emitter is formed by outdiffusion following deposition of the heavily doped polysilicon emitter contact. Transient enhanced diffusion (TED, discussed in Section 5.6.3) of base impurity implants can result in loss of control of the base profile, and the use of an epitaxial base results in a more abrupt transition and narrower basewidth.



(a)



(b)

FIGURE 10.20

(a) Cross section of an epitaxial base silicon–germanium heterojunction bipolar transistor (SiGe HBT) (b) Photomicrograph of actual structure with 5-μm-deep trench isolation. Copyright 1995, IEEE. Reprinted with permission from Ref. [9].

A typical profile for an SiGe HBT is shown in Fig. 10.21 [10]. Without the addition of germanium, this profile is also characteristic of the oxide-isolated double-polysilicon structures, as depicted in Fig. 10.19, although TED may increase the basewidth in implanted base devices. In the profile in Fig. 10.21, the metallurgical basewidth is less than 100 nm, and the emitter-base junction is only 150 nm below the surface of the polysilicon. The desired germanium-doping profile is achieved during the base epitaxy. For film stability, the peak concentration is typically maintained below 15%. Also evident in the profile are the phosphorus collector and heavily doped arsenic subcollector regions.

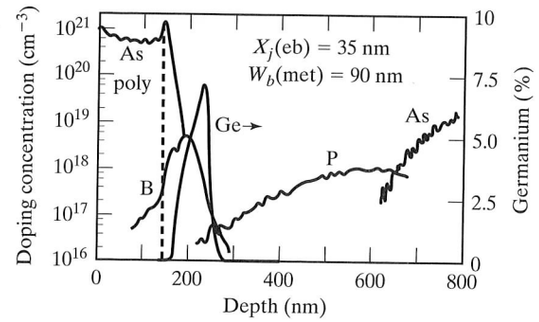


FIGURE 10.21

SiGe HBT impurity profile. The same profile applies to high-performance silicon BJTs if the Ge is eliminated. Copyright 1985, IEEE. Reprinted with permission from Ref. [9].

10.9 OTHER BIPOLAR ISOLATION TECHNIQUES

Several other interesting approaches to device isolation have been developed over the years, and two are surveyed here. Dielectric isolation processes are in use in high-performance analog circuits; the CDI process is replaced by oxide-isolated structures.

10.9.1 Collector-Diffusion Isolation (CDI)

The collector-diffusion-isolation (CDI) [8] structure, shown in Fig. 10.22, was developed primarily for digital applications. The process eliminates the *p*-type isolation diffusion, achieving reduced device area and process complexity.

The process starts with diffusion of a low-sheet-resistance buried layer, which will serve as the collector of the transistor. A thin *p*-type epitaxial layer forms the base region and is grown in the next step. Device isolation is achieved via an n^+ diffusion that completely encloses the transistor and also provides the collector contact area. Next, a shallow emitter is implanted or diffused into the device, followed by contacts and metallization. Typical parameters for the CDI process include a buried-layer sheet resistance of 15 to 30 ohms per square, a 2-μm-thick, 0.25-ohm-cm epitaxial layer, and an emitter depth of less than 1 μm.

This process produces high-performance, narrow-base transistors with minimum r_C, but with relatively large collector-base and collector-substrate capacitances. It has for the most part been replaced with advanced oxide-isolated structures that also minimize these capacitances, although at a cost of considerable process complexity.

10.9.2 Dielectric Isolation

One of the "holy grails" of bipolar processes has been to find a process that can provide *npn* and *pnp* devices with similar levels of performance. Such processes are referred to as complementary bipolar processes. However, parasitic coupling between

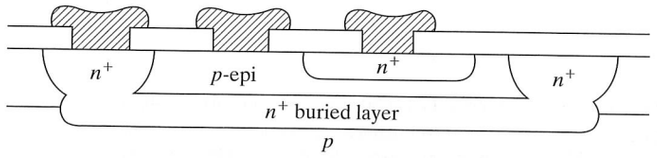
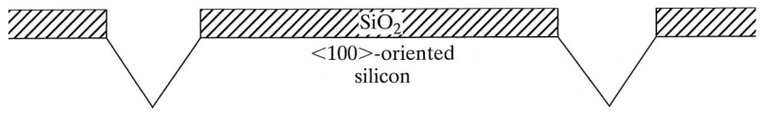


FIGURE 10.22

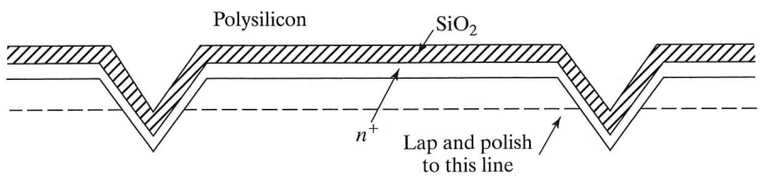
Cross section of a transistor fabricated in the CDI process.[18]

devices and susceptibility to latchup prevent the simple addition of diffusions to the *npn* process to produce vertical *pnp* transistors. Instead, some form of dielectric isolation has been used to isolate the two types of transistors.

The first successful dielectric-isolated process was developed by Harris Semiconductor [11–12], and the basic process flow is depicted in Fig. 10.23. Deep *V*-grooves are first etched in the surface of <100> oriented silicon wafers. (This etching process will be discussed in more detail in Chapter 11.) A nonselective n^+ diffusion is performed, and a silicon dioxide layer is grown on the surface. A thick layer of polycrystalline silicon is then deposited on the surface of the wafer. Silicon is removed from the back surface of the wafer by lapping until the silicon dioxide in the *V*-grooves is exposed, as indicated by the dotted line in Fig. 10.23(b). The surface is then mechanically and chemically polished. The wafer is turned over, yielding islands of silicon completely isolated from each other by the silicon dioxide dielectric layer. Standard processing is then used to form *npn* transistors. This process is expensive, but an important variation permits formation of complementary, vertical *npn* and *pnp* transistors. It is used in the fabrication of high-performance analog circuits. In addition, the structures are highly tolerant to radiation and are used in military applications.



(a)



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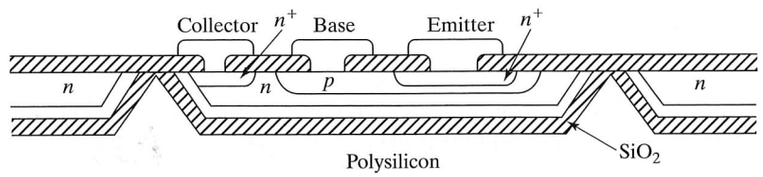
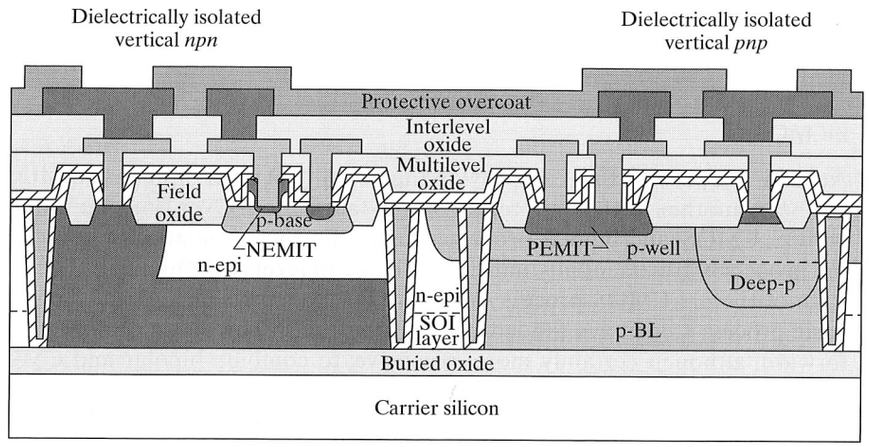


(c)

FIGURE 10.23

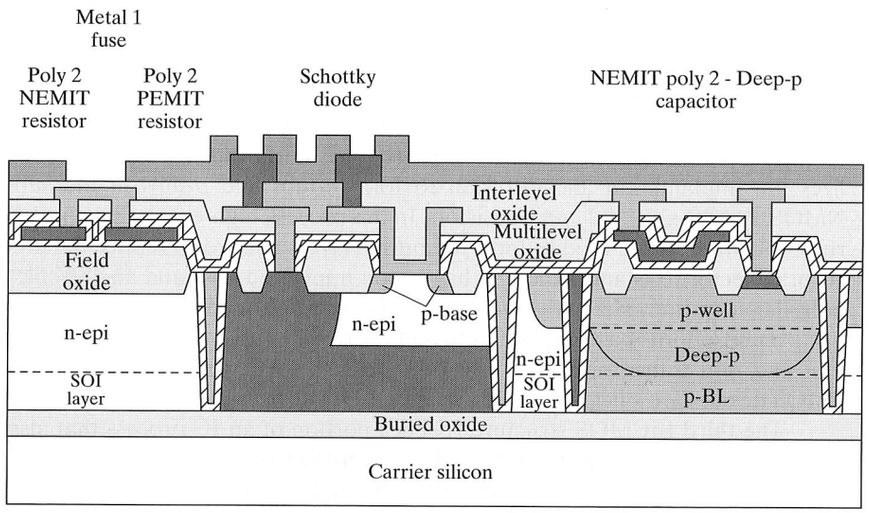
Several steps in the dielectric isolation process.[11,12] (a) V-grooves anisotropically etched in the silicon substrate; (b) the structure following n^+ diffusion and oxidation; the wafer is turned over, lapped back and polished to the dotted line; (c) bipolar transistors are then fabricated in the isolated islands of silicon.

A myriad of recent processing developments, including buried-oxide and bonded-wafer SOI, deep-trench RIE with oxide and polysilicon refill, etc., have come together to permit the development of more straightforward processes for producing dielectrically isolated BJTs. Figure 10.24(a) depicts the cross sections resulting from one such process [13]. In this particular process, the starting substrates are bonded SOI wafers. However, SIMOX wafers could also be utilized. Heavily doped *p*- and *n*- type buried collectors are implanted and followed by the growth of an *n*-type epitaxial layer for the



npn and *pnp* transistors

(a)



Passive components

(b)

FIGURE 10.24

(a) High-performance bipolar transistors and (b) passive components fabricated on a SIMOX wafer using shallow trench isolation. Copyright 1997, IEEE. Reprinted with permission from Ref. [13].

npn collector. A *p*-well forms the *pnp* collector region, and deep *n*- and *p*-type sinker diffusions are added to contact the buried collectors of both transistors. Isolation between devices is achieved by etching deep trenches down to the buried-oxide layer. The trenches are then refilled with oxide and polysilicon. LOCOS isolation at the surface is followed by separate base region implants for the *npn* and *pnp* transistors. An undoped polysilicon layer is deposited and then selectively implanted with *n*- and *p*-type impurities. Outdiffusion from the implanted polysilicon layer forms the emitters of the two types of transistors. This process results in complementary transistors with f_T's of 2.5 GHz. Figure 10.24(b) shows the realization of resistors, capacitors, and Schottky diodes in the same process.

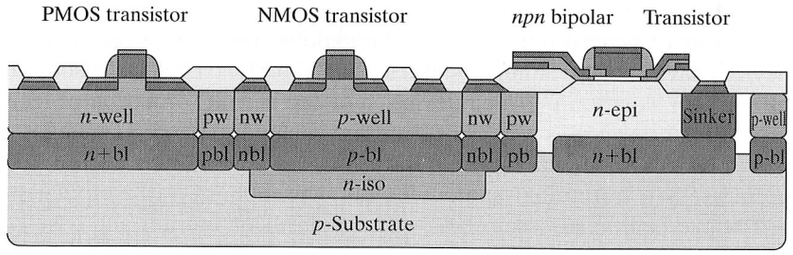
10.10 BICMOS

Achieving a process that can provide the benefits of both bipolar and MOS devices has been another of the long-term goals in fabrication. Over time, the complexity of NMOS, CMOS, and bipolar processes have all grown dramatically to the point that the processes are essentially indistinguishable in terms of complexity. For example, a state-of-the-art CMOS process may have 20–25 mask steps. At the same time, the basic process steps have tended to converge, and it has become relatively straightforward, although certainly more expensive, to combine bipolar and CMOS structures into a technology most often termed BiCMOS. (The inclusion of JFETs in the bipolar process is often called a BiFET process.) A good review can be found in [14].

Three approaches to realizing a BiCMOS technology are presented in Fig. 10.25. Because of the presence of CMOS devices, <100> silicon is the substrate of choice for BiCMOS processing. The first case [15] forms heavily doped *n*-type and *p*-type buried layers in the *p*-type substrate. Following epitaxial layer growth, *n*-well and *p*-well regions are formed by implantation and diffusion, and then NMOS and PMOS devices are formed in the two wells. The *npn* transistor, actually a SiGe HBT, has an epitaxial base with polysilicon side-wall contacts and a polysilicon emitter. Standard lateral *pnp* transistors can be formed in *n* regions similar to those used for the *npn* devices.

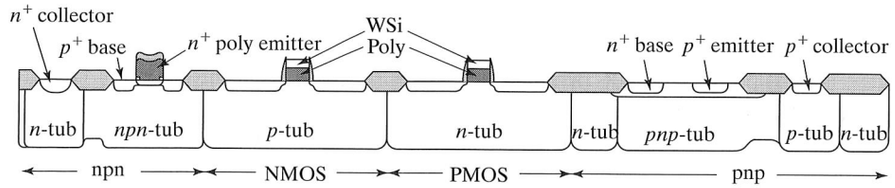
The process illustrated in Fig. 10.25(b) [16] starts with LOCOS isolation and utilizes ion implantation and diffusion to form *n*-tubs and *p*-tubs in the substrate for NMOS, PMOS, *npn*, and *pnp* transistors. In this process, high-energy boron and phosphorus implantations are used to form the buried layers needed to reduce the bipolar transistor collector resistance. The *npn* has an ion-implanted base and an aresenic-doped n^+ polysilicon emitter. Here, a *vertical pnp* transistor is formed in one of the *p*-tub regions using a phosphorus base implantation and the p^+ *S/D* implant as its emitter. The f_T of the *npn* and *pnp* transistors exceed 40 GHz and 10 GHz, respectively. The NMOS and PMOS devices are silicided polysilicon gate LDD devices with 5-nm gate oxides.

The third BiCMOS structure [17] is a portion of an IC process that also includes vertical power devices. Here, n^+ buried layers are formed below all the CMOS and bipolar devices. Following epitaxial layer growth, *n*-tub formation, and p^+ isolation, straightforward processing is used to form the vertical *npn*, lateral *pnp*, and PMOS transistors. A *p*-well is added to the *n*-tubs to act as the substrate for the NMOS device. Note the common connection of the source, *p*-well and *n*-tub by the source contact of the NMOS transistor. The *n*-epitaxial layer with n^+ backside contact is required by vertical power device structures, which are also included in the process.



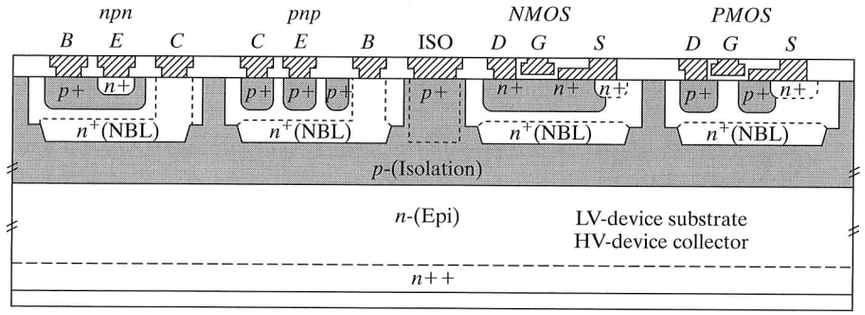
Schematic cross section of the BiCMOS6G technology

(a)



Schematic cross-sectional view of HECIBiC technology.

(b)



(c)

FIGURE 10.25

BiCMOS technology cross sections. (a) A dual-well CMOS + *npn* process. Well formation is preceded by *n*- and *p*-type buried-layer diffusion; (b) A twin-well process, which utilizes high-energy implantation to reduce collector resistance of the BJTs. Vertical *npn* and *pnp* transistors are available in this process; (c) BiCMOS devices in a process designed for power semiconductor applications. Copyright 1999, 1998, 1997, IEEE. Reprinted with permission from Refs. [15, 16, 17].

SUMMARY

The *standard buried collector* (SBC) process is widely used throughout the IC industry for analog and power circuit applications. More recently developed digital bipolar technologies have benefited greatly from process advances originally developed for use in MOS dynamic RAMs. These include locos-isolation, deep- and shallow-trench formation, the use of polysilicon, and the introduction of ion implantation.

Bipolar technologies for analog applications are typically designed to yield current gains of several hundred, with breakdown voltages of up to 50 V. The resulting devices have cutoff frequencies of less than 500 MHz. Dielectric isolation provides the ultimate in isolation between devices and can permit formation of truly complementary bipolar devices, as well as devices that can operate at high voltages.

Devices for digital applications can operate with lower current gains and supply voltages than traditional analog circuits. The modern VLSI bipolar process utilizes self-aligned epitaxial base region with a polysilicon emitter and base contact regions. Shallow- and deep-trench isolation are combined to minimize the area and capacitance of the bipolar transistor. Very narrow base transistors can also be formed by ion implantation. These factors permit device designs with cutoff frequencies exceeding 40 GHz. Germanium can be introduced into the base region of the epitaxial base transistor to produce an SiGe heterojunction transistor (HBT). These devices have already exibited cutoff frequencies in excess of 200 GHz.

Bipolar and MOS processes and complexity have largely converged to the point that it is possible to fabricate both types of transistors in a single composite technology. Although there are widely varying approaches, these processes are termed BiCMOS technology.

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PROBLEMS

10.1 Evaluate the Gummel number expressions for a uniformly doped transistor with impurity concentrations of N_E and N_B in the emitter and base, respectively. The effective width of the emitter is L_E, and W_B is the basewidth. What is the current gain for a device with $N_E = 10^{20}/\text{cm}^3$, $N_B = 10^{18}/\text{cm}^3$, $W_B = 4\ \mu\text{m}$, $L_E = 20\ \mu\text{m}$, $L_B = 50\ \mu\text{m}$, $D_B = 20\ \text{cm}^2/\text{sec}$, and $D_E = 5\ \text{cm}^2/\text{sec}$? Assume that $\eta = 1$.

10.2 Using Eq. (10.1), estimate the current gain of the transistor with the impurity profiles given in Fig. 10.2. Assume that $W_B \ll L_B$, and $D_B = 20\ \text{cm}^2/\text{sec}$. Use $G_E = 5 \times 10^{13}\ \text{sec/cm}^4$, $x_{JE} = 1.5\ \mu\text{m}$, $x_{JC} = 4\ \mu\text{m}$.

10.3 What is the maximum collector-base breakdown voltage of a transistor with $X_{BL} - X_{BC} = 5\ \mu\text{m}$? What epitaxial layer doping may be used to achieve this breakdown voltage?

10.4 A Zener reference diode is often formed using breakdown of the emitter-base junction.

(a) What base surface concentration is required to produce a breakdown voltage of 6 V for a 1-μm-deep junction?

(b) If the base surface concentration is too small by a factor of two, what is the actual breakdown voltage of the diode?

10.5 Calculate the collector-base depletion-layer width for the transistor of Example 10.3 using the expression for a one-sided step junction given in Eq. (9.3). How does this compare with the width derived from Fig. 10.4?

10.6 The effective Gummel number in the emitter is substantially reduced from that calculated from the profile by bandgap narrowing in the emitter. Calculate G_E using the expressions in Chapter 4 for an As emitter with a sheet resistance of 10 ohms per square. Compare G_E to the values stated in the text.

10.7 In Section 10.7.3, the importance of correct positioning of the n^+ collector contact diffusion was discussed. To illustrate this point, three simple *npn* transistors are fabricated in an *n*-type substrate using the structure drawn in Fig. P10.7. An n^+ collector ring is used to reduce the collector series resistance R_c. Three different spacings—0 μm, 3 μm, and 5 μm—are used between the edge of the n^+ ring and the edge of the base diffusion. Explain why the breakdown voltage will be different for these three cases, and estimate the collector-base breakdown voltage for the three devices. Assume a base surface concentration of $10^{18}/\text{cm}^3$ and a junction depth of 5 μm.

10.8 Surface conditions can degrade the breakdown voltage of Zener diodes. Subsurface breakdown can be achieved using an ion-implanted process with the profile shown in Fig. P10.8. Estimate the breakdown voltage of this diode.

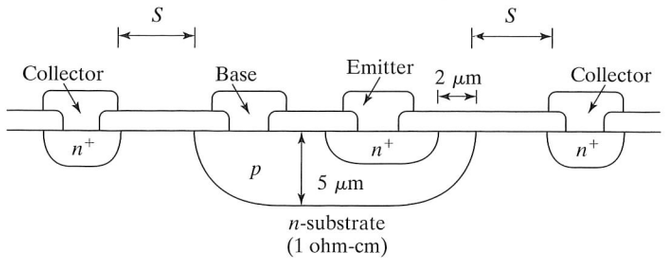
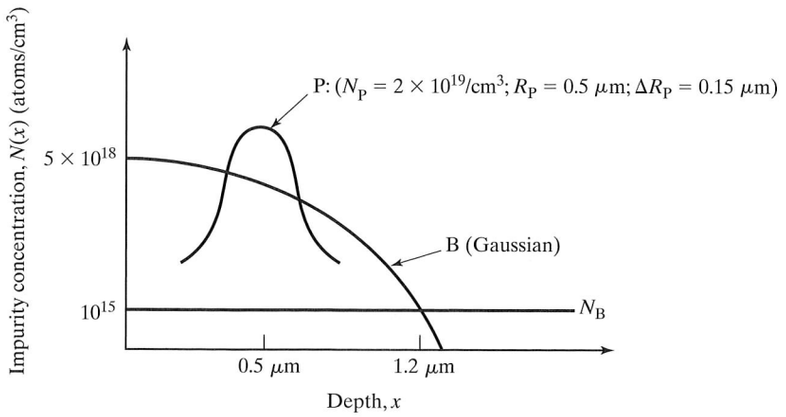


FIGURE P10.7



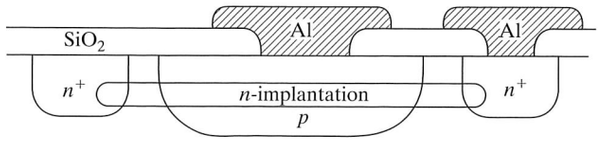


FIGURE P10.8

10.9 A simple lateral *pnp* structure is shown in Fig. P10.9(a). The current gain of this transistor is collection limited and does not obey Eq. (10.1). Assume that the emitter injects current uniformly in all directions and that the collector collects all the current coming its way.

- **(a)** Under these assumptions, what is the value of the common base current gain = I_C/I_E? What is the common emitter current gain β?
- **(b)** Derive an expression for β as a function of the length and width of the device. For a given area, what relationship between the length and width maximizes the gain?
- **(c)** What geometry would be used to optimize the current gain?
- **(d)** Repeat Prob. 10.9(a) for the circular device structure in Fig. 10.9(b).

10.10 Determine a reasonable diffusion schedule for the isolation diffusion of a junction-isolated structure with a 15-μm-thick epitaxial layer with the geometry of Fig. P10.10.

- **(a)** Assume that the width of the isolation at the bottom is to be 10 μm, that there is no up-diffusion from substrate, and that lateral diffusion equals vertical diffusion.
- **(b)** Modify your diffusion time in part (a) to account for up-diffusion of boron from the substrate. Assume that the substrate represents an infinite supply of boron impurities with a constant concentration of 10^{18}/cm^3.

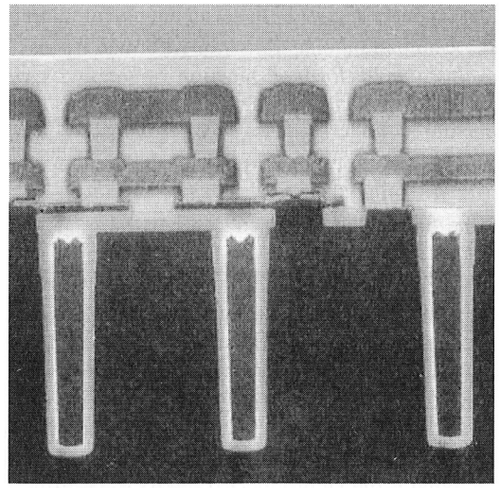


FIGURE P10.9

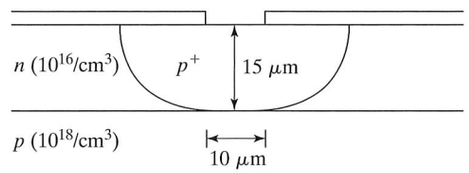


FIGURE P10.10

10.11 The distance $X_{BL} - X_{BC} = 5$ μm in a certain bipolar SBC process with an epitaxial layer doping of 10^{15}/cm^3. Use the one-sided step-junction formula [Eq. (9.3)] to estimate the punch-through voltage for this transistor. Compare with Fig. 10.7.

10.12 What epitaxial-layer doping would give approximately the same value for the Zener and punch-through voltage limits in Example 10.5.

10.13 Suppose the resistor in Fig. P4.10 is formed as an epilayer resistor. What is its resistance, based upon the values in Table 10.1 if lateral diffusion is ignored? (b) How about if the resistor is formed from the base layer? (c)How about for an emitter layer resistor?

10.14 Draw the cross section of (a) a substrate *npn* transistor in a *p*-well CMOS process, and (b) a substrate *pnp* transistor in an *n*-well CMOS process.

10.15 Redraw the layout in Fig. 10.17 using an alignment tolerance of 1 μm.

10.16 A Schottky clamped bipolar transistor is formed by placing a Schottky barrier diode in parallel with the collector-base junction by simply overlapping the base contact metal over the collector region. Draw a cross section of this structure, and include a guard ring on the edge of the diode.

10.17 List the mask steps required for the oxide-isolated bipolar transistor of Fig. 10.19. Which are noncritical alignment steps?

10.18 Estimate the emitter-base and collector-base breakdown voltages and punch-through voltage, for the impurity profiles in Fig. 10.21. Ignore the presence of germanium in the base region.

10.19 Estimate the space-charge region extents in the base for the impurity profiles in Fig. 10.21. Ignore the presence of germanium in the base region. The metallurgical base-width was estimated to be 100 nm in the text. What is the actual base region?

10.20 Estimate the permissible Dt products associated with the arsenic and boron profiles in Fig. 10.21. (a) Assume that the arsenic follows an erfc profile with a concentration of $10^{21}/cm^3$ at the surface ($x' = 0$) and intersects the boron profile at a level of $5 \times 10^{18}/cm^3$ at $x' = 50$ nm. What is the Dt product? If the As were diffused at 1000°C, what would be the diffusion time? (b) Assume that the boron follows an Guassian profile with a concentration of $5 \times 10^{18}/cm^3$ at the surface ($x' = 0$) and intersects the phosphorus profile at a level of $5 \times 10^{16}/cm^3$ at $x' = 100$ nm. What is the Dt product? If the boron were diffused at 1000°C, what would be the diffusion time?

10.21 Draw the cross section of a complementary bipolar process that simply adds an additional p diffusion to an npn process. Show the required biasing of the various diffusions, and indicate any problems you encounter.

10.22 A silicon bipolar transistor is to be designed to have an f_T of 50 GHz. What is its transit time? Suppose the transistor has $r_C = 40\ \Omega$. What is the largest possible value for $(C_{jC} + C_{sub})$? What is a lower bound on the width of the collector depletion layer? What is an lower bound on the basewidth? If $r_E = 25\ \Omega$, what is an lower bound on the emitter-base capacitance? (Assume that $V_s = 10^7$ cm/sec, $\eta = 10$, and $D_B = 20\ cm^2/sec$.)

10.23 Identify potential latchup paths in the BiCMOS structures in Figs. 10.25(a)–(c).

10.24 A high energy (5 MeV) is used to implant oxygen well below the silicon surface to form a buried SiO_2 layer. Assume that the SiO_2 layer is desired to be 0.50 μm wide. (a) What is the oxygen dose required in silicon? (b) What beam current is required to be able to implant at least four 200-mm wafers per hour? (c) How much power is being supplied to the ion beam?

10.25 It was noted that the CDI process is used mainly for digital applications. What characteristics of the structure make this true?

10.26 **(a)** How many masks are required for the CDI process?

(b) Design a good mask-alignment sequence for this process.

10.27 A CDI process uses a 0.25-ohm-cm epitaxial base layer and a 5-ohm-cm substrate. Estimate the breakdown voltages of the emitter-base and collector-base junctions. The emitter junction depth is 1 μm, and the expitaxial layer thickness is 2 μm.

CHAPTER 11

Processes for MicroElectroMechanical Systems: MEMS

MEMS represent one of today's most exciting areas of microelectronics activity. MEMS technology has brought together innovations from many areas of microelectronics only to develop rapidly into a discipline of its own. Today's micromachined systems combine the signal processing and computational capability of analog and digital integrated circuits with a wide variety of nonelectrical elements, including pressure, temperature and chemical sensors, mechanical gears, and actuators, 3D mirror structures, etc., and we have only begun to scratch the surface of biomedical applications. As a brief introduction, this chapter attempts to provide a flavor of the creativity and wide variety of devices and structures that are being conceived as you read this text. A wealth of greater detail on the subject can be found in the books by Madou [1] and Kovacs [2], the paper compendia edited by Muller [3] and Trimmer [4], and many other publications [5–8]. The latest research in the field is presented at the bienniel International Conference on Solid-State Sensors and Actuators, the Solid-Sate Sensors and Actuator Workshop held on intervening years, and the yearly IEEE International Electron Devices Meeting.

MEMS structures are based upon our ability to sculpt or machine silicon on a microelectronic scale. These micromachining technologies can be broken into three groups: (i) Bulk micromachining, (ii) Surface micromachining, and (iii) High-aspect-ratio electroplated structures. The first, bulk micromachining dates back to the 1960s, when techniques for wet anisotropic etching of various forms of trenches, grooves, and membranes in silicon wafers were first developed. Advances in bulk micromachining continued rapidly through the 1970s with development of impurity-dependent etch stops, wafer-dissolution processes, and wafer fusion bonding. During the next two decades, surface micromachining, which makes use of the full lithography capability of IC processing, emerged to form a wide range of new beam, comb, microactuator, and rotary structures. The application of circuits to improve the sensor characteristics