1.15 Draw a set of contact and metal masks for the bipolar transistor of Fig. 1.9. Use square contact windows with one contact to the emitter and two contacts to the base and collector regions.

CHAPTER 2

Lithography

In order to produce an integrated circuit, thin films of various materials are used as barriers to the diffusion or implantation of impurity atoms or as insulators between conductive materials and the silicon substrate. Holes, or windows, are cut through this barrier material wherever impurity penetration or contact is desired.

Masks contain the patterns of windows that are transferred to the surface of the silicon wafer using a process called *photolithography*. Photolithography makes use of a highly refined version of the photoengraving process. The patterns are first transferred from the mask to a light-sensitive material called *photoresist*. Chemical or plasma etching is then used to transfer the pattern from the photoresist to the barrier material on the surface of the wafer. Each mask step requires successful completion of numerous processing steps, and the complexity of an IC process is often measured by the number of photographic masks used during fabrication. This chapter will explore the lithographic process, including mask fabrication, photoresist processes, and etching.

2.1 THE PHOTOLITHOGRAPHIC PROCESS

Photolithography encompasses all the steps involved in transferring a pattern from a mask to the surface of the silicon wafer. The various steps of the basic photolithographic process given in Figs. 2.1 and 2.2 will each be discussed in detail next.

Ultraclean conditions must be maintained during the lithography process. Any dust particles on the original substrate or that fall on the substrate during processing can result in defects in the final resist coating. Even if defects occur in only 10% of the chip sites at each mask step, fewer than 50% of the chips will be functional after a seven-mask process is completed. Vertical laminar-flow hoods in clean rooms are used to prevent particulate contamination throughout the fabrication process. Clean rooms use filtration to remove particles from the air and are rated by the maximum number of particles per cubic foot or cubic meter of air, as shown in Table 2.1. Clean rooms have evolved from Class 100 to the Class 1 facilities now being used for VLSI/ULSI processing. For comparison, each cubic foot of ordinary room air has several million dust particles exceeding a size of 0.5 μm.

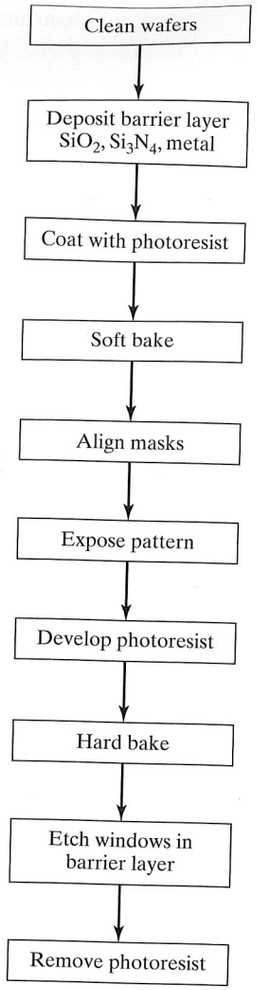


FIGURE 2.1

Steps of the photolithographic process.

TABLE 2.1 Ratings by Class of Effectiveness of Filtration in Clean Rooms

Class	Number of 0.5-μm particles per ft^3 (m^3)	Number of 5-μm particles per ft^3 (m^3)
10,000	10,000 (350,000)	65 (23,000)
1,000	1,000 (35,000)	6.5 (2,300)*
100	100 (3,500)	0.65 (230)*
10	10 (350)	0.065 (23)*
1	1 (35)*	0.0065 (2.3)*

*It is very difficult to measure particulate counts below 10 per ft^3.

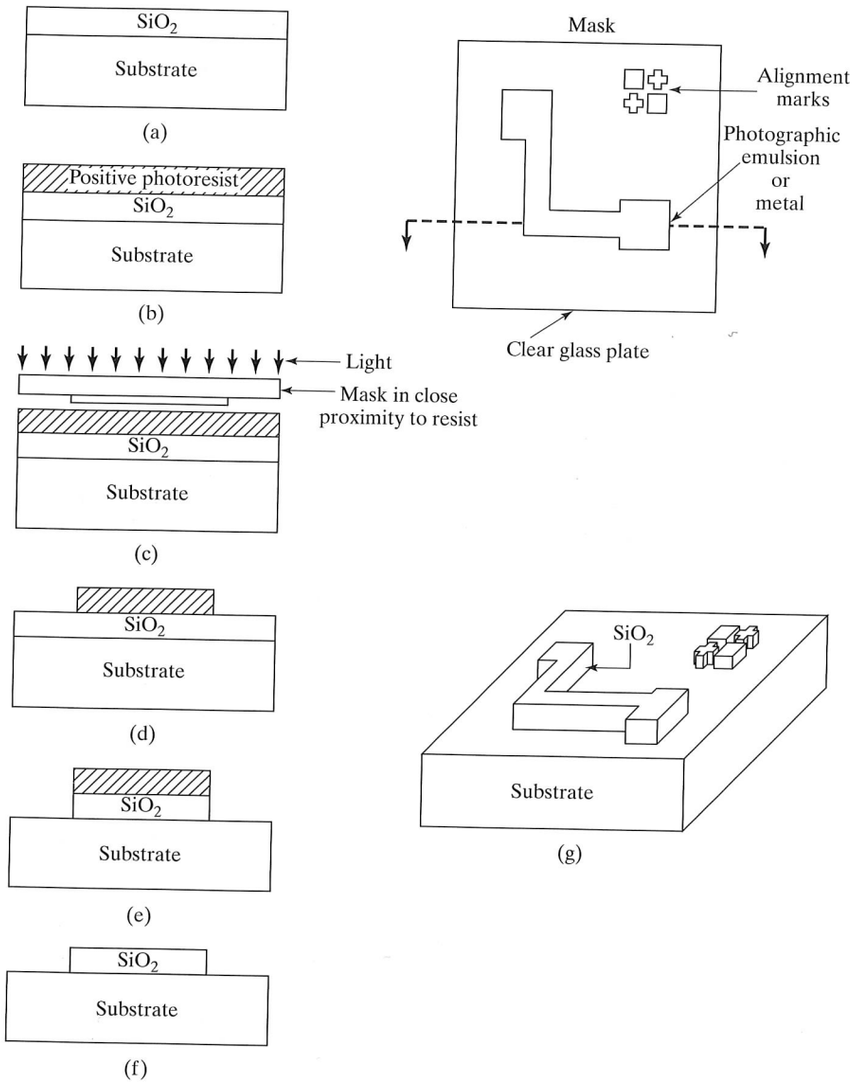


FIGURE 2.2

Drawings of a wafer through the various steps of the photolithographic process. (a) Substrate covered with silicon dioxide barrier layer; (b) positive photoresist applied to the surface of the wafer; (c) mask in close proximity to the surface of the resist-covered wafer; (d) substrate following resist exposure and development; (e) substrate following etching of the silicon dioxide layer; (f) oxide barrier on wafer surface after resist removal; (g) view of substrate with silicon dioxide pattern on the surface.

2.1.1 Wafer and Wafer Cleaning

IC fabrication starts with *n*- or *p*-type silicon wafers supplied with a specified resistivity. The wafers range in thickness from 250 to 500 μm. Two-hundred-mm (eight-inch)

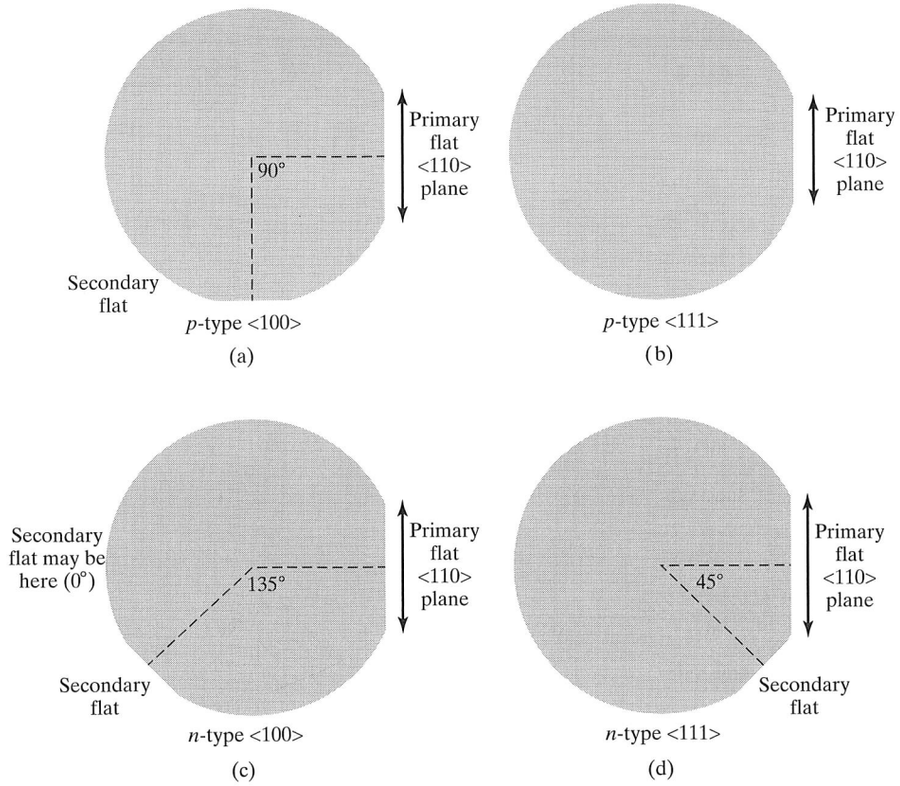


FIGURE 2.3

Illustration of wafer flat standard used to identify 100 mm wafers.

diameter wafers are widely used at the time of this writing, and processing equipment for 300-mm (12-inch) wafers is already becoming available. Wafers with diameters of 1, 1.5, 2, 3, 4, 5, and 6 in. have all been used at various stages in history, and Table 1.1 indicates that 450-mm wafers will be in use by the end of the decade.

The silicon wafers are identified by a standard system[1] of straight edges or wafer *flats*. These flats are ground into the silicon ingot before it is sliced into wafers and are used to indicate the wafer type (*n*-type or *p*-type) and the surface orientation (<100> or <111>) as indicated in Fig. 2.3. The primary wafer flat identifies the <110> crystal plane. (It is important to note, however, that this identification system is not always utilized, particularly with wafer sizes of 150 mm and above.)

Prior to use, wafers are chemically cleaned to remove particulate matter on the surface, as well as any trace of organic, ionic, and metallic impurities. A cleaning step utilizing a solution of hydrofluoric acid removes any oxide that may have formed on the wafer surface. A typical cleaning process is presented in Table 2.2.

One very important chemical used in wafer cleaning and throughout microelectronic fabrication processes is deionized (DI) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. The

[1]A SEMI (Semiconductor Equipment and Materials International) standard.

TABLE 2.2 Silicon Wafer Cleaning Procedure[7, 8]

A. Solvent Removal
1. Immerse in boiling trichloroethylene (TCE) for 3 min.
2. Immerse in boiling acetone for 3 min.
3. Immerse in boiling methyl alcohol for 3 min.
4. Wash in DI water for 3 min.

B. Removal of Residual Organic/Ionic Contamination
1. Immerse in a (5:1:1) solution of H_2O–NH_4OH–H_2O_2; heat solution to 75–80 °C and hold for 10 min.
2. Quench the solution under running DI water for 1 min.
3. Wash in DI water for 5 min.

C. Hydrous Oxide Removal
1. Immerse in a (1:50) solution of HF–H_2O for 15 sec.
2. Wash in running DI water with agitation for 30 sec.

D. Heavy Metal Clean
1. Immerse in a (6:1:1) solution of H_2O–HCl–H_2O_2 for 10 min at a temperature of 75–80 °C.
2. Quench the solution under running DI water for 1 min.
3. Wash in running DI water for 20 min.

theoretical resistivity of pure water at 25 °C is 18.3 Mohm-cm. Basic DI water systems achieve resistivities of 18 Mohm-cm with fewer than 1.2 colonies of bacteria per milliliter and with no particles larger than 0.25 μm.

Cleanliness and contamination control is such an overarching concern in VLSI/ULSI fabrication that an NSF Industry University Cooperative Research Center in Micro Contamination Control was established at the University of Arizona.

2.1.2 Barrier Layer Formation

After cleaning, the silicon wafer is covered with the material that will serve as a barrier layer. The most common material is silicon dioxide (SiO_2), so we will use it as an example here. Silicon nitride (Si_3N_4), polysilicon, photoresist, and metals are also routinely used as barrier materials at different points in a given process flow. In subsequent chapters, we will discuss thermal oxidation, chemical vapor deposition, sputtering, and vacuum evaporation processes, all of which are used to produce thin layers of these materials.

The original silicon wafer has a metallic gray appearance. Once an SiO_2 layer is formed on the silicon wafer, the surface will have a color that depends on the SiO_2 thickness. The finished wafer will have regions with many different thicknesses. Each region will produce a different color, resulting in beautiful, multicolored IC images, photographs of which appear in many books and magazines.

2.1.3 Photoresist Application

After the SiO_2 layer is formed, the surface of the wafer is coated with a light-sensitive material called *photoresist*. The surface must be clean and dry to ensure good photoresist adhesion. Freshly oxidized wafers may be directly coated, but if the wafers have been stored, they should be carefully cleaned and dried prior to application of the resist.

Lack of adhesion of photoresist to many film surfaces is a commonly encountered problem in silicon processing. In order to promote adhesion, the wafer surface is

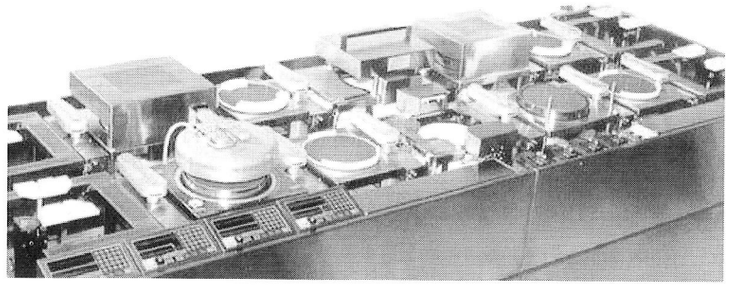


FIGURE 2.4

Rite Track 88e wafer processing system. (Courtesy of Rite Track Equipment Services, Inc.)

treated with an adhesion promoter such as hexamethyldisilazane (HMDS) prior to photoresist application. This treatment provides good photoresist adhesion to a variety of films, including silicon dioxide (SiO_2), silicon dioxide containing phosphorous, polycrystalline silicon, silicon nitride (Si_3N_4), and aluminum.

Photoresist is typically applied in liquid form. The wafer is held on a vacuum chuck and then spun at high speed for 30 to 60 sec to produce a thin uniform layer. Speeds of 1,000 to 5,000 rpm result in layers ranging from 2.5 to 0.5 μm, respectively. The actual thickness of the resist depends on its viscosity and is inversely proportional to the square root of the spinning speed.

Figure 2.4 shows an automated cassette-to-cassette wafer track system that automatically dispenses a tightly controlled amount of photoresist onto each wafer and controls the spinning profile to achieve highly reproducible resist film thicknesses. Each cassette typically contains 25 wafers.

2.1.4 Soft Baking or Prebaking

A drying step called *soft baking*, or *prebaking*, is used to improve adhesion and remove solvent from the photoresist. Times range from 5 to 30 min in an oven at 60 to 100°C in an air or nitrogen atmosphere. The soft-baking process is specified on the resist manufacturer's data sheet and should be followed closely. After soft baking, the photoresist is ready for mask alignment and exposure.

2.1.5 Mask Alignment

The complex pattern from a photo mask (or just mask), a square glass plate with a patterned emulsion or metal film on one side, must be transferred to the surface of the wafer. Each mask following the first[2] must be carefully aligned to the previous pattern

[2]In many MEMS (see Chapter 11 for an introduction) and sensor applications, the first mask must also be carefully aligned to the crystallographic axes. Double-sided alignment is also used with infrared systems that can "see" through the wafer or with specialized optics systems that permit simultaneous viewing of both sides of the wafer.

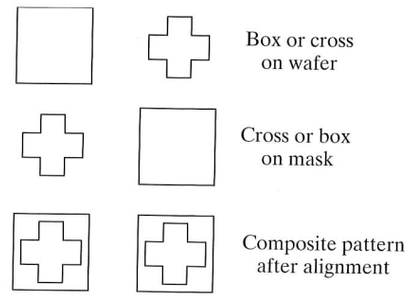


FIGURE 2.5

A simple set of alignment marks. At some steps a cross may be aligned within a box. At others, a box may be placed around the cross. The choice depends on the type of resist being used at a given mask step.

on the wafer. Manual operation of alignment and exposure equipment was used in early fabrication systems. However, VLSI/ULSI designs require extremely small geometrical features (minimum line width or space) and tight alignment tolerances. For example, 100 nm (0.1 μm) lithography will require a worst-case alignment error of 35 nm (mean + 3σ), and computer-controlled alignment systems are required to achieve these required levels of alignment precision.

With basic manual alignment equipment, the wafer is held on a vacuum chuck and carefully moved into position below the mask using an adjustable x–y stage. The mask is spaced 25 to 125 μm above the surface of the wafer during alignment. If contact printing is being used, the mask is brought into contact with the wafer after alignment.

Alignment marks are introduced on each mask and transferred to the wafer as part of the IC pattern. The marks are used to align each new mask level to one of the previous levels. A sample set of alignment marks is shown in Fig. 2.5. For certain mask levels, the cross on the mask is placed in a box on the wafer. For other mask levels, the box on the mask is placed over a cross on the wafer. The choice depends on the type of resist used during a given photolithographic step. Split-field optics are used to simultaneously align two well-separated areas of the wafer.

2.1.6 Photoresist Exposure and Development

Following alignment, the photoresist is exposed through the mask with high-intensity ultraviolet light. Resist is exposed wherever silicon dioxide is to be removed. The photoresist is developed with a process very similar to that used for developing ordinary photographic film, using a developer supplied by the photoresist manufacturer. Any resist that has been exposed to ultraviolet light is washed away, leaving bare silicon dioxide in the exposed areas of Fig. 2.6(d). A photoresist acting in the manner just described is called a *positive resist*, and the mask contains a copy of the pattern that will remain on the surface of the wafer. Windows are opened wherever the exposing light passes through the mask.

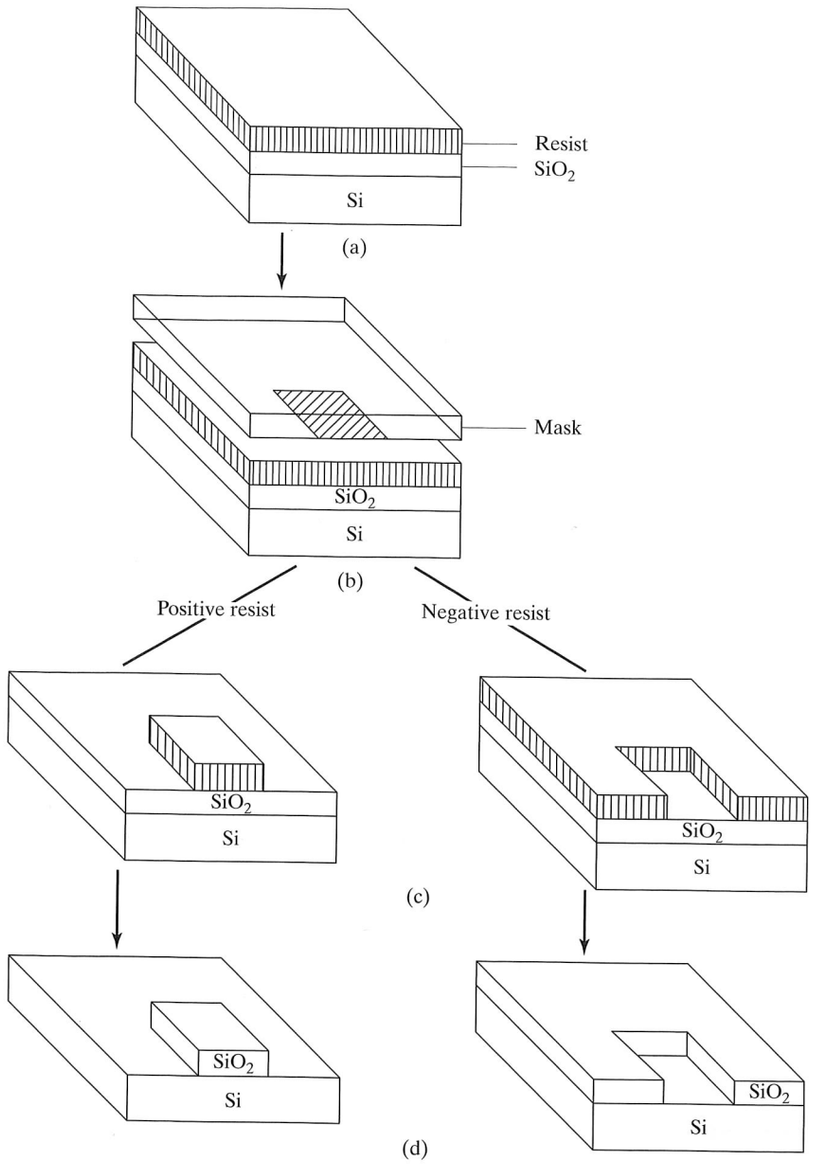


FIGURE 2.6

Resist and silicon dioxide patterns following photolithography with positive and negative resists.

Negative photoresists can also be used. A negative resist remains on the surface wherever it is exposed. Figure 2.6 shows simple examples of the patterns transferred to a silicon dioxide barrier layer using positive and negative photoresists with the same mask. Negative resists were widely used in early IC processing. However, positive resist yields better process control in small-geometry structures and is now the main type of resist used in VLSI processes.

2.1.7 Hard Baking

Following exposure and development, a baking step is used to harden the photoresist and improve adhesion to the substrate. A typical process involves baking in an oven for 20 to 30 min at 120 to 180°C. Details of this step are again specified on the manufacturer's photoresist data sheets.

2.2 ETCHING TECHNIQUES

Chemical etching in liquid or gaseous form is used to remove any barrier material not protected by hardened photoresist. The choice of chemicals depends on the material to be etched. A high degree of selectivity is required so that the etchant will remove the unprotected barrier layer much more rapidly than it attacks the photoresist layer.

2.2.1 Wet Chemical Etching

A buffered oxide etch (BOE, or BHF) is commonly used to etch windows in silicon dioxide layers. BOE is a solution containing hydrofluoric acid (HF), and etching is performed by immersing the wafers in the solution. At room temperature, HF etches silicon dioxide much more rapidly than it etches photoresist or silicon. The etch rate in BOE ranges from 10 to 100 nm/min at 25 °C, depending on the density of the silicon dioxide film. Etch rate is temperature dependent, and temperature is carefully monitored during the etch process. In addition, etch rates depend on the type of oxide present. Oxides grown in dry oxygen etch more slowly than those grown in the presence of water vapor. A high concentration of phosphorus in the oxide enhances the etch rate, whereas a reduced etch rate occurs when a high concentration of boron is present. High concentrations of these elements convert the SiO_2 layer to a phosphosilicate or borosilicate glass.

HF and water both wet silicon dioxide, but do not wet silicon. The length of the etch process may be controlled by visually monitoring test wafers that are etched along with the actual IC wafers. Occurrence of a hydrophobic condition on the control wafer signals completion of the etch step.

Wet chemical etching tends to be an isotropic process, etching equally in all directions. Figure 2.7(a) shows the result of isotropic etching of a narrow line in silicon dioxide. The etching process has etched under the resist by a distance equal to the thickness of the film. This "etch bias" becomes a serious problem in processes requiring line widths with dimensions similar to the thickness of the film.

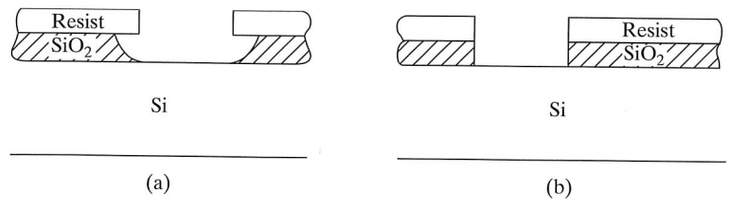


FIGURE 2.7

Etching profiles obtained with (a) isotropic wet chemical etching and (b) dry anisotropic etching in a plasma or reactive-ion etching system.

2.2.2 Dry Etching Plasma Systems

Dry plasma etching processes are widely used in VLSI fabrication. Highly anisotropic etching profiles can be obtained as shown in Fig 2.7(b), avoiding the undercutting problem of Fig. 2.7(a) characteristic of wet processes. Dry processes require only small amounts of reactant gases, whereas wet etching requires disposal of relatively large amounts of liquid chemical wastes.

Plasma systems use RF excitation to ionize a variety of source gases in a vacuum system. The RF power source typically operates at a frequency of 13.56 MHz, which is set aside by the Federal Communcations Commission (FCC) for industrial and scientific purposes. However, plasma systems can also operate at frequencies as low as a few hundred kilohertz, and microwave excitation is in use in certain systems.

The mode of operation of the plasma system depends upon the operating pressure, as shown in Table 2.3, as well as the structure of the reaction chamber. Standard plasma etching corresponds to the highest of the three pressure regimes, and a conceptual drawing for a parallel-plate plasma-etching system in shown in Fig. 2.8(a). In this case, the electrode structure is symmetric, and the wafer to be etched is placed upon the grounded electrode. Free radicals such as fluorine or chlorine are created in the plasma and react at the wafer surface to etch silicon, silicon dioxide, silicon nitride, organic materials, and metals. A sample of possible source gases used to etch these materials appears in Table 2.4, but a much broader range of choices is available [3]. The basic plasma-etching process is isotropic, and additional atomic species such as argon, hydrogen, and oxygen are often introduced to improve etch rate or selectivity.

Ion milling uses energetic noble gas ions such as Ar^+ to bombard the wafer surface. Etching occurs by physically knocking atoms off the surface of the wafer. Highly anisotropic etching can be obtained, but selectivity is often poor. Metals can be used as barrier materials to protect the wafer from etching. Ion milling operates in the lowest of the three pressure ranges given in Table 2.3. In this case, ions are accelerated toward the surface by a strong electric field that can be introduced by adding a variable external dc-bias voltage between the electrodes.

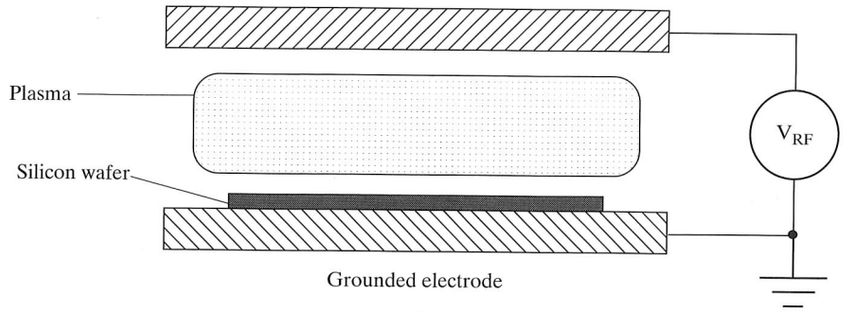
Reactive-ion etching (RIE) combines the plasma and sputter etching processes. Plasma systems are used to ionize reactive gases, and the ions are accelerated to bombard the surface. Etching occurs through a combination of the chemical reaction and momentum transfer from the etching species and is highly anisotropic. The voltage required to accelerate ions from the plasma toward the wafer surface can be developed by introducing an asymmetry into the structure of the plasma chamber as indicated in Fig. 2.8(b). In this drawing, the surface area of the upper electrode is made larger than that of the lower electrode, the upper electrode is now grounded, and the wafer is placed on the electrode driven by the RF source. The physical asymmetry of the system produces a self-bias between the electrodes that provides the acceleration potential required to direct the ions toward the wafer surface.

2.2.3 Photoresist Removal

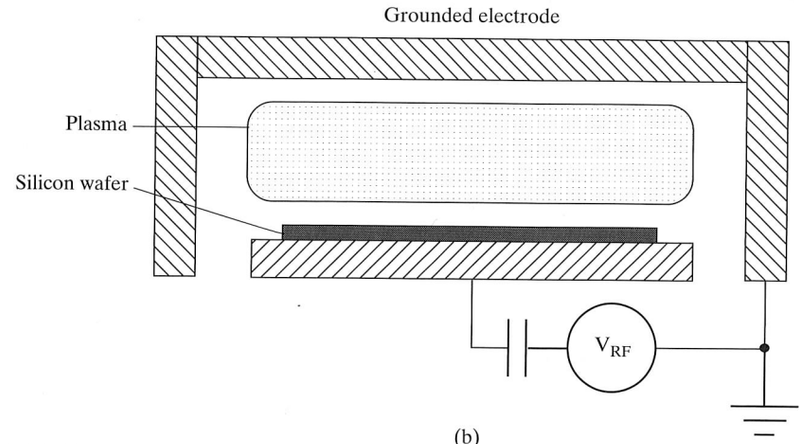
After windows are etched through the SiO_2 layer, the photoresist is stripped from the surface, leaving a window in the silicon dioxide. Photoresist removal typically uses proprietary-liquid resist strippers, which cause the resist to swell and lose adhesion to the substrate. Dry processing may also be used to remove resist by oxidizing (burning) it in an oxygen plasma system, a process often called *resist ashing*.

TABLE 2.3 Etching Pressure Ranges

Etching Mode	Pressure (Torr)
Ion Milling	10^{-4}–10^{-3}
Reactive Ion Etching/Ion Milling	10^{-3}–10^{-1}
Plasma Etching	10^{-1}–5



(a)



(b)

FIGURE 2.8

(a) Concept of a parallel plate plasma etcher (b) Asymmetrical reactive ion etching (RIE) system

TABLE 2.4 Plasma-Etching Sources

Material	Source Gases
Organic Materials	O_2, SF_6, CF_4
Polysilicon	CCl_4, CF_4, NF_3, SF_6
Silicon Dioxide	CF_4, C_2F_6, C_3F_8, CHF_3
Silicon Nitride	CF_4, C_2F_6, CHF_3, SF_6
Aluminum	CCl_4, Cl_2, BCl_3
Titanium	$C_2Cl_2F_4$, CF_4
Tungsten	Cl_2

2.2.4 Metrology and Critical Dimension Control

It is extremely important to be able to maintain accurate control of critical dimensions (CDs) through photolithography and etching processes, as well as subsequent process steps. The ITRS contains projections of the required levels of CD control. The ability to reliably measure the fabricated features with the required accuracy and repeatability is itself a major problem, and semiconductor process metrology has emerged as a separate discipline of its own that concentrates on the development of the test structures and instrumentation required to support high-yield manufacturing.

2.3 PHOTOMASK FABRICATION

Photomask fabrication involves a series of photographic processes outlined in Fig. 2.9. An IC mask begins with a large-scale drawing of each mask. Early photomasks were cut by hand in a material called *rubylith*, a sandwich of a clear backing layer and a thin red layer of Mylar. The red layer was cut with a stylus and peeled off, leaving the desired pattern in red. The original rubylith copy of the mask was 100 to 1,000 times larger than the final integrated circuit and was photographically reduced to form a reticle for use in a step-and-repeat camera, as described later.

Today, computer graphics systems and optical or electron beam pattern generators have supplanted the use of rubylith. An image of the desired mask is created on a computer graphics system. Once the image is complete, files containing the commands needed to drive a pattern generator are created. An optical pattern generator uses a flash lamp to expose the series of rectangles composing the mask image directly onto a photographic plate called the *reticle*. An electron beam system draws the pattern directly in an electron-sensitive material.

Reticle images range from 1 to 10 times final size. A step-and-repeat camera is used to reduce the reticle image to its final size and to expose a two-dimensional array of images on a master copy of the final mask. On a 200-mm wafer, it is possible to get approximately 1,200 copies of a 5-mm × 5-mm IC chip! Figure 2.10 shows examples of a computer graphics plot, a reticle, and a final mask for a simple integrated circuit.

A final master copy of the mask is usually made in a thin film of metal, such as chrome, on a glass plate. The mask image is transferred to photoresist, which is used as an etch mask for the chrome. Working emulsion masks are then produced from the chrome master. Each time a mask is brought into contact with the surface of the silicon wafer, the pattern can be damaged. Therefore, emulsion masks can only be used for a few exposures before they are thrown away.

2.4 EXPOSURE SYSTEMS

Because contact printing can damage the surfaces of both the mask and the wafer, manufacturing lines utilize proximity and projection printing systems, as illustrated in Fig. 2.11. However, contact printing is still used in research and prototyping situations, because it can economically achieve high-resolution pattern transfer. In proximity printing, the mask is brought in very close proximity to the wafer, but does not come in contact with the wafer during exposure, thus preventing damage to the mask. Projection printing uses a dual-lens system to project a portion of the mask image onto the wafer surface. The wafer and masks may be scanned, or the system may operate in a step-and-repeat mode. The actual mask and lenses are mounted many centimeters from the wafer surface.

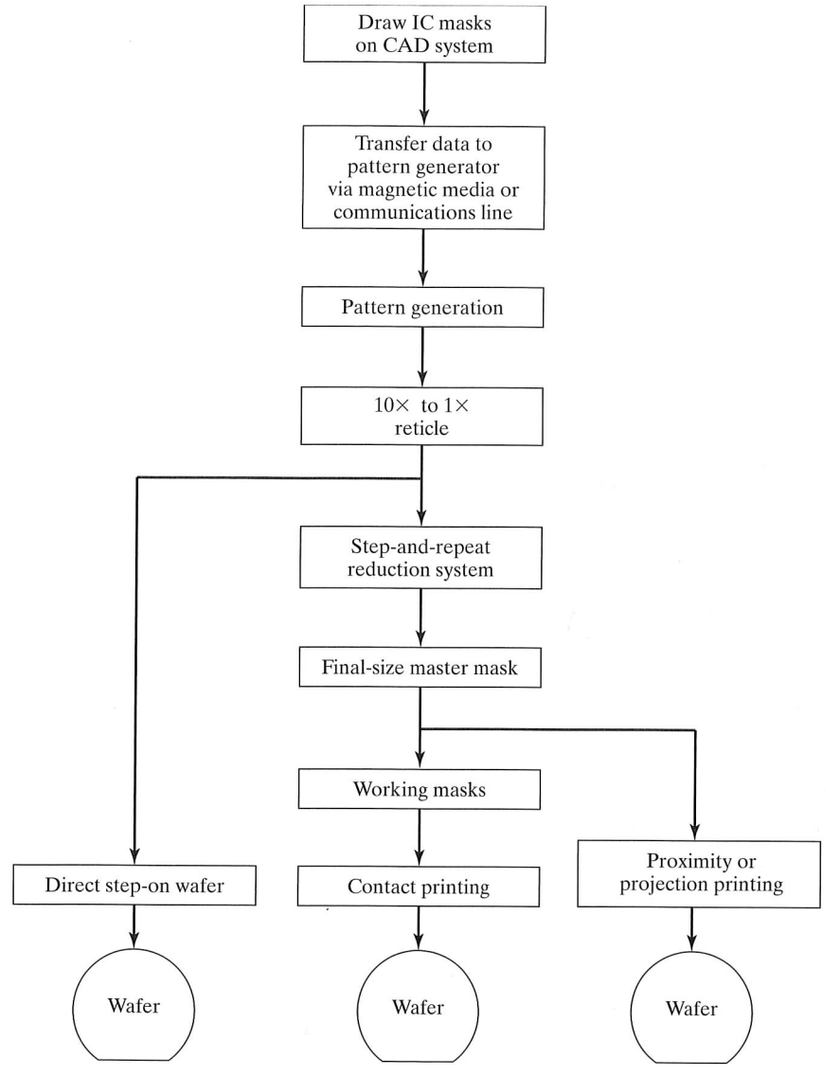


FIGURE 2.9

Outline of steps in the mask fabrication process.

For large-diameter wafers, it is impossible to achieve uniform exposure and to maintain alignment between mask levels across the complete wafer, particularly for submicron feature sizes. High-resolution VLSI lithography systems now use some form of exposure of the individual die pattern directly onto the wafer. A projection system is used with a reticle to expose the IC die pattern directly on the wafer. No step-and-repeat masks of the circuit are produced. The pattern is aligned and exposed separately at each die site.

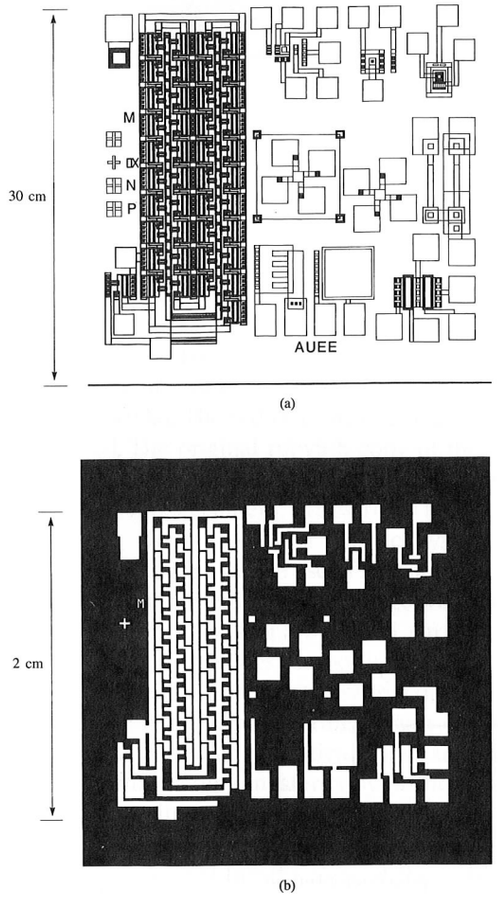


FIGURE 2.10

Mask fabrication. (a) Composite computer graphics plot of all masks for a simple integrated circuit; (b) 10X reticle of metal-level mask; (c) final-size emulsion mask with 400 copies of the metal level of the integrated circuit in (a).

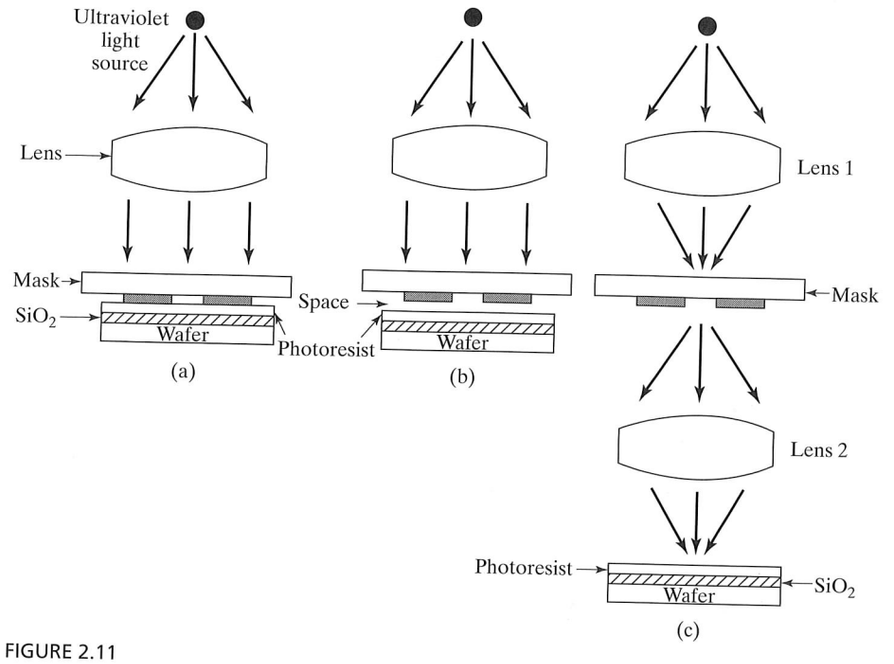


FIGURE 2.11

Artist's conception of various printing techniques. (a) Contact printing, in which wafer is in intimate contact with mask; (b) proximity printing, in which wafer and mask are in close proximity; (c) projection printing, in which light source is scanned across the mask and focused on the wafer. Copyright, 1983, Bell Telephone Laboratories, Incorporated. Reprinted by permission from Ref. [5].

Figure 2.12 on page 32 shows an artist's diagram of a direct step-on-wafer system (usually termed a "stepper"). A single die image is projected directly onto the surface of the wafer. The reticle pattern may range from 1 to 10 times the final die size. The wafer is moved (stepped) from die site to die site on the wafer, and the pattern is aligned and exposed at each individual site. The drawing in Fig. 2.12 actually hides the complexity of these systems, as can be seen from the drawing of a complete stepper system shown in Fig. 2.13 on page 33. These systems are often housed in their own environmentally controlled sections of clean rooms.

Another variation can be used when the individual die pattern becomes too large. The step-and-scan method projects only a narrow rectangular stripe of the reticle image onto the wafer. The wafer and the reticle are scanned in tandem until the complete reticle pattern is transferred to the wafer. The wafer is then indexed to the next site, and the process of alignment and scanning proceeds again. Large die images or multiple dice can be patterned using this technique.

The minimum feature size that can be reproduced using optical lithography is intimately tied to the wavelength of light used for exposure, and experts have repeatedly predicted the demise of optical lithography for many years.[3] However, the technology continues to be pushed further and further into the submicron regime. A

[3]The author remembers attending a number of lithography panel sessions where it was predicted that optical lithography could not be used below 1–2 μm.

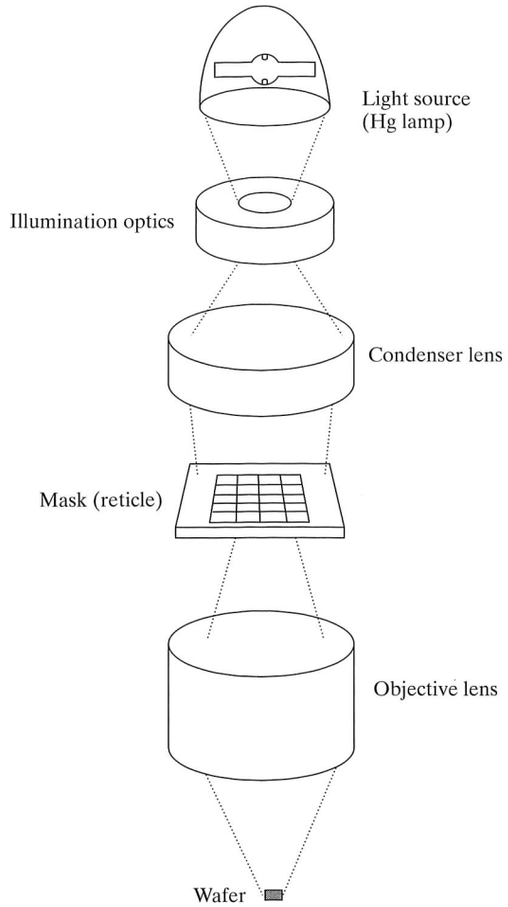


FIGURE 2.12
Concept of lens system for a wafer stepper.

rough estimate of the minimum feature size F (line or space) that can be transferred to the wafer surface is given by

$$F = 0.5\frac{\lambda}{NA} \tag{2.1}$$

where λ is the wavelength of the illumination, and NA is the numerical aperture of the lens defined in terms of the convergence angle θ in Fig. 2.14 on page 33:

$$NA = \sin\theta. \tag{2.2}$$

For $NA = 0.5$, Eq. (2.1) predicts the minimum feature size to be approximately the same as the wavelength of the optical illumination. A second concern is the depth of field DF over which focus is maintained; an estimate for DF is

$$DF = 0.6\frac{\lambda}{(NA)^2} \tag{2.3}$$

FIGURE 2.13
The true complexity of a wafer stepper is apparent in this system drawing. (Courtesy of ASM Lithography, Inc.)

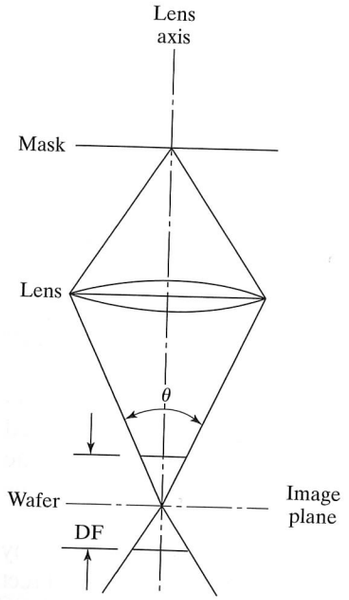


FIGURE 2.14
Optical focal plane and depth of focus

Based upon Eqs. (2.1) and (2.3) with $NA = 0.5$, one-tenth-micron technology ($F = 0.10$ μm) would require a 100-nm illumination source and have only a 240 nm (0.24 μm) depth of field. Thus, wafer planarity at each exposure step represents a critical issue, since focus will be maintained over a distance of only ±0.12 μm from the primary focal plane.

2.5 EXPOSURE SOURCES

For many years, the source of illumination for photolithography has been high-pressure mercury (Hg) or Hg–rare gas discharge lamps. A typical emission spectra from a Hg–Xe lamp is given in Fig. 2.15. Output is relatively low in the deep ultraviolet (DUV) region (200–300 nm), but exhibits several strong peaks in the UV region between 300 and 450 nm. To minimize problems in the lens optics, the lamp output must be filtered to select one of the spectral components. The most common monochromatic selections are the 436-nm, or "g-line," and 365-nm, or "i-line," spectral components.

It can be observed in the NTRS lithography projections in Table 2.3, however, that DUV sources are required for lithography for 0.25-μm technology and below. Excimer lasers are the choice at these wavelengths with the KrF laser used as the 248-nm source and ArF for 193 nm. It is not clear what the lithography source will be for technology generations of below 130 nm.

Phase-shifting mask technology is representative of the inventions that have been found in the drive to squeeze the most out of optical lithography. The conceptual diagram in Fig. 2.16 compares the imaged light intensity profile of two closely spaced lines. In Fig. 2.16(a), resolution is lost, because diffraction has caused overlap of the individual line images. In Fig. 2.16(b), a 180° phase-shifting layer is applied over one of the openings on the mask, and the two individual lines appear well defined in the intensity profile at the image plane. A minimum feature size approaching one-half of the wavelength of the illumination source can be achieved using a phase-shifting mask and $NA \geq 0.5$. For highly complex IC patterns, however, designing the phase-shifting masks represents a significant challenge.

Various alternatives to optical lithography have been explored since the mid 1960s. Electron beams can be focused to spots of the order of 0.10 μm and can be used to directly write IC patterns in electron-sensitive resists. However, this process is relatively slow, since the pattern must be rewritten at each die site, and the throughput of electron-beam systems has never been sufficient for IC manufacturing. On the other hand, it is an excellent technology for producing the 1-X to 10-X reticles used in stepper systems, and "e-beam" lithography has become an extremely important technology for mask fabrication.

X-rays with energies in the 0.1–5-keV range have wavelengths that range from 10 to 0.3 nm. Thus, even the finest feature sizes in Table 2.3 would represent many wavelengths if x-rays were used for illumination. Mask generation is one of several barriers to the use of x-ray lithography in IC production. Heavy metals such as gold can be used as mask materials for x-ray lithography, but limit practical x-ray wavelengths to the 0.4–2-nm range. In addition to mask fabrication, x-ray lithography also requires a new set of illumination, resist, and alignment technologies.

Research efforts continue to expand the capabilities of electron-beam and x-ray lithography as outlined in Table 2.5 on page 36. Extreme ultraviolet [10], e-beam direct write, e-beam projection, x-ray proximity, and ion-beam projection all offer potential for future lithography systems. However, significant innovation will be required along the way to achieve the ITRS goals.

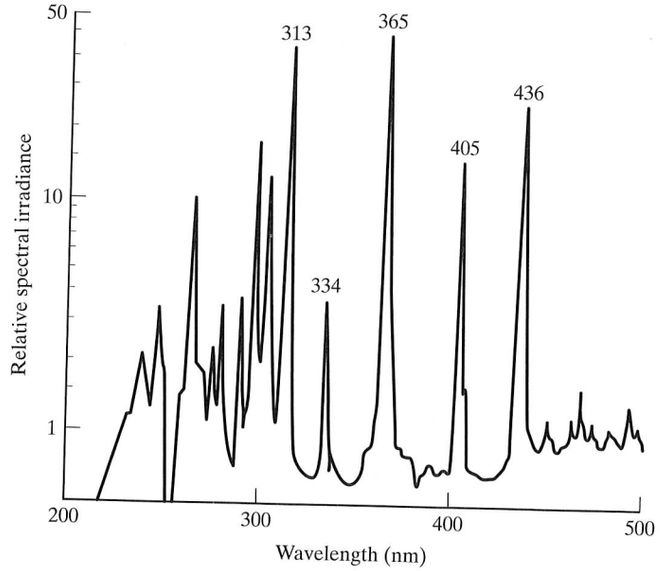


FIGURE 2.15

Spectal content of an Xe-Hg lamp (Courtesy of SVG)

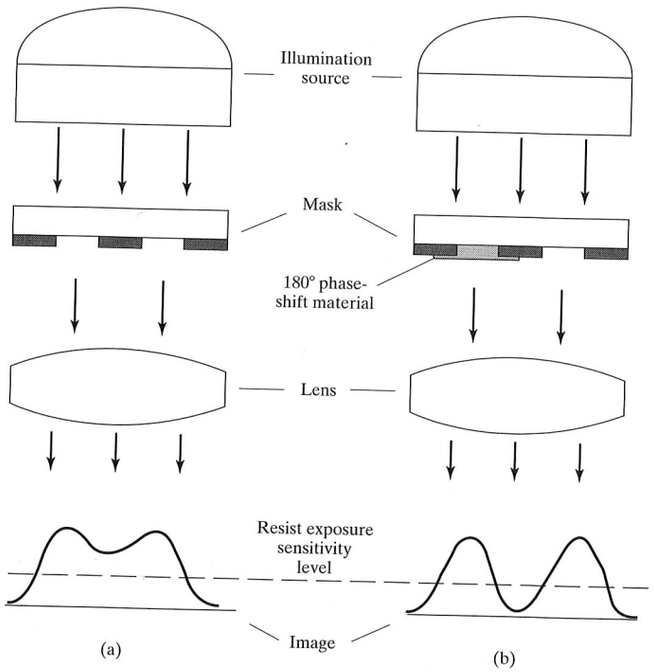


FIGURE 2.16

Pattern transfer of two closely spaced lines (a) using conventional mask technology (b) using a phase-shifting mask

TABLE 2.5 ITRS Lithography Projections

Year	2001	2003	2005	2008	2011	2014
Dense Line Half-Pitch (nm)	150	120	100	70	50	35
Worst-Case Alignment Tolerance Mean + 3 σ (nm)	52	42	35	25	20	15
Minimum Feature Size F (nm) Microprocessor Gate Width	100	80	65	45	30	20
Critical Dimension Control (nm) Mean + 3 σ -Post Etching	9	8	6	4	3	2
Equivalent Oxide Thickness (nm)	1.5–1.9	1.5–1.9	1.0–1.5	0.8–1.2	0.6–0.8	0.5–0.6
Lithography Technology Options	248 nm DUV	248 nm + PSM 193 nm DUV	193 nm + PSM 157 nm E-beam projection Proximity x-ray Ion Projection	157 nm + PSM E-beam projection E-beam direct write EUV Ion Projection Proximity x-ray	EUV E-beam projection E-beam direct write Ion Projection	EUV E-beam projection E-beam direct write Ion Projection Innovation

DUV: deep ultraviolet; EUV: extreme ultraviolet; PSM: phase-shift mask.

2.6 OPTICAL AND ELECTRON MICROSCOPY

Most of us believe the old adage "a picture is worth a thousand words," and visual inspection of masks and subsequent determination of the physical structure (morphology) of the patterns transferred to the wafer surface is extremely important in VLSI fabrication. Three methods—optical microscopy, Scanning Electron Microscopy (SEM), and Transmission Electron Microscopy (TEM)—find wide application in the visualization of VLSI morphologies and provide increasingly higher levels of magnification.

2.6.1 Optical Microscopy

Optical microscopes are a common laboratory tool familiar to most of us, and they are used to inspect and monitor the wafers throughout the fabrication process. The resolution of an optical microscope corresponds to the minimum feature size introduced in Section 2.4. Using white light for illumination with wavelengths centered on 0.5 μm, and with a numerical aperture of 0.95, the resolution is approximately 0.25 μm. On the other hand, the resolution of the human eye itself is approximately 0.25 μm. Hence, optical microscopes typically have a maximum magnification of 1,000X. The lower end of the magnification range is usually 1X–5X.

Analytical microscopes usually can operate in either the bright-field or dark-field mode. Bright-field operation is the mode that we most often encounter. The sample is illuminated by light perpendicular to the plane of the sample directly through the optics of the microscope. Light is reflected from the sample back up into same optical path in the microscope. For dark-field mode, the sample is illuminated from an oblique angle, and light that is reflected or refracted from features on the surface of the sample enters by the microscope lens system. The surface of the sample appears mostly dark with the surface features standing out in bright contrast against the dark background. In this manner, surface features that are "washed out" in bright-field mode can be clearly observed.

2.6.2 Scanning Electron Microscopy

In the Scanning Electron Microscope (SEM), the surface of the sample is bombarded with a low-energy (0.5–40 KeV) beam of electrons. The incident electron beam causes low-energy (0–50 eV) secondary electrons to be ejected from the inner shells of the atoms making up the surface of the sample under analysis. An image is formed by scanning the surface of the sample and recording the intensity of the secondary electron current. The magnitude of the secondary electron current depends upon the materials present and on the curvature of the surface, and significant contrast can be achieved due to varying surface morphology and materials. The SEM extends the minimum resolution limit to 20–30Å, with magnifications up to 300,000. At a magnification of 10,000, the SEM provides a depth of field of 2–4 μm, which makes it an extremely useful tool for investigating VLSI structures. As an example, the SEM image of a MEMS structure is shown in Fig. 2.17 on page 38. The image is a micro-mirror that has been raised out of the surface plane by a gear-driven linear actuator.

Some types of SEMs can suffer from electrical charge-up of the sample by the electron beam, particularly on insulating surfaces. This can be eliminated by coating the surface with a thin conducting layer of gold. However, this requires special processing of samples prior to their imaging by the SEM.

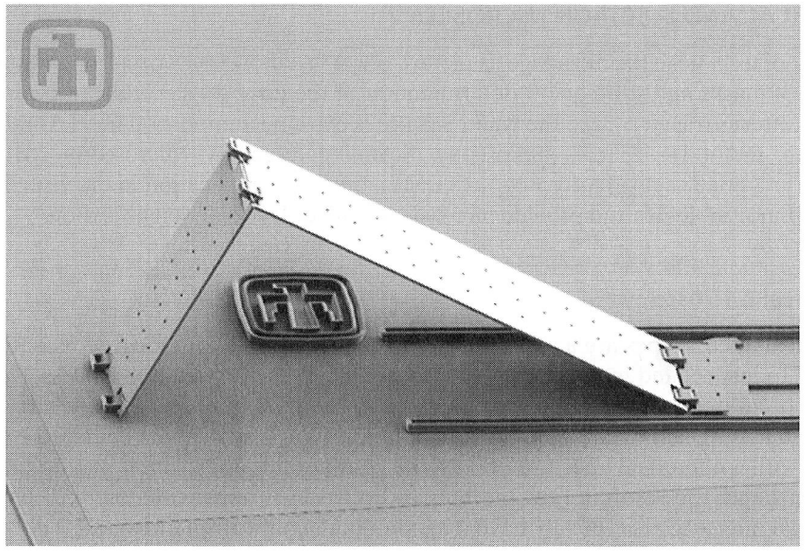


FIGURE 2.17

SEM image of a three-dimensional micromechanical system (MEMS) structure (Courtesy Sandia National Laboratories)

2.6.3 Transmission Electron Microscopy

The Transmission Electron Microscope (TEM) extends the resolution of microscopy another order of magnitude down to the 2Å range, which corresponds to a distance below the radius of most atoms. In this instrument, a 60–400-KeV beam of electrons is used to illuminate a thin sample only 0.5–2 μm thick. The amplitude of the electron current that passes through the sample is detected, and an image is created as the beam scans the sample. In a MOS structure, for example, the TEM can display an image of the transition from the regular array of atoms in the silicon lattice to the irregular amorphous layer of the silicon dioxide gate insulator as depicted in Fig. 2.18. Although the TEM provides very high resolution, its application requires special preparation of the extremely thin samples.

SUMMARY

Photolithography is used to transfer patterns from masks to photoresist on the surface of silicon wafers. The resist protects portions of the surface while windows are etched in barrier layers such as silicon dioxide, silicon nitride, or metal. The windows may be etched using either wet- or dry-processing techniques. Wet chemical etching tends to etch under the edge of the mask, causing a loss of linewidth control at small

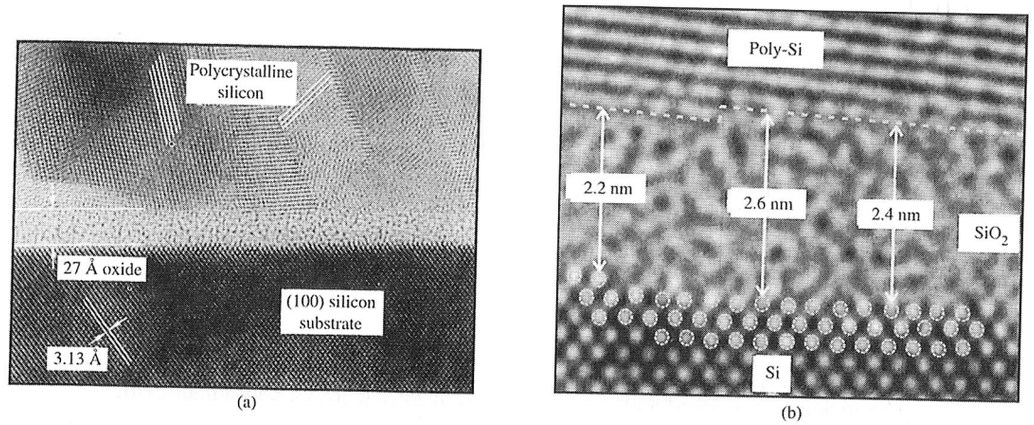


FIGURE 2.18

Cross-sectional high-resolution transmission electron microscope images for MOS structures with (a) 27-Å and (b) 24-Å image. The polysilicon grains are easily noticeable in (a); the Si/SiO_2 and poly-Si/SiO_2 interfaces are shown in part (b). On a local, atomic scale, thickness variations of 2-3 Å are found which are a direct result of atomic silicon steps at both interfaces. Copyright 1969 by International Business Machines Corporation; reprinted with permission from Ref. [9].

dimensions. Dry etching can yield highly anisotropic etching profiles and is required in most VLSI processing.

After etching, impurities can be introduced into the wafer through the windows using ion implantation or high-temperature diffusion, or metal can be deposited on the surface making contact with the silicon through the etched windows. Masking operations are performed over and over during IC processing, and the number of mask steps required is used as a basic measure of process complexity.

Mask fabrication uses computer graphics systems to draw the chip image at 100 to 2,000 times final size. Reticles 1 to 10 times final size are made from this computer image, using optical pattern generators or electron-beam systems. Step-and-repeat cameras are used to fabricate final masks from the reticles, or direct step-on-wafer systems may be used to transfer the patterns directly to the wafer.

Today, we are reaching the limits of optical lithography. Present equipment can define windows that are approximately 0.15 μm wide. (Just a few years ago, experts were predicting that 1–2 μm would be the limit!) The wavelength of light is too long to produce much smaller geometrical features, because of fringing and interference effects. Electron-beam and X-ray lithography are now being used to fabricate devices with geometrical features smaller than 0.10 μm, and lithography test structures have reproduced shapes with minimum feature sizes below 0.05 μm.

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PROBLEMS

2.1 A complex CMOS fabrication process requires 25 masks. (a) What fraction of the dice must be good (i.e., what yield must be obtained) during each mask step if we require 30% of the final dice to be good? (b) How about if we require 70% to be good?

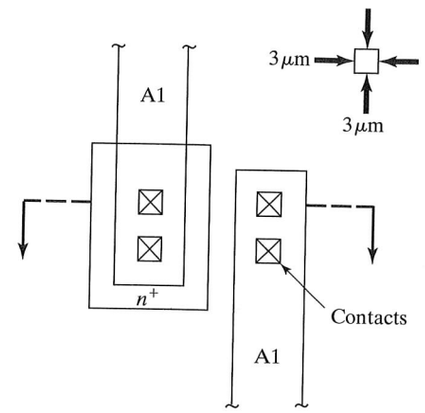
2.2 The mask set for a simple rectangular *pn* junction diode is shown in Fig. P2.2. The diode is formed in a *p*-type substrate. Draw a picture of the horizontal layout for the diode that

results when a worst-case misalignment of 3 μm occurs in both the *x*- and *y*-directions on each mask level.

(a) Assume that both the contact and metal levels are aligned to the diffusion level.

(b) Assume that the contact level is aligned to the diffusion level and the metal level is aligned to the contact level.

2.3 Figure P2.3 shows a resist pattern on top of a silicon dioxide film 1 μm thick. Draw the silicon–silicon dioxide structure after etching and removal of the photoresist for:



Composite top view of masks

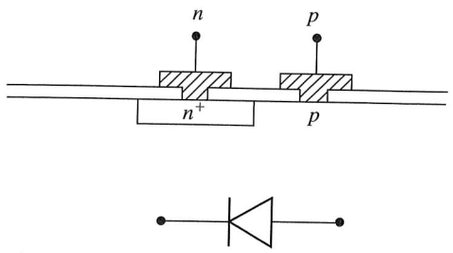


FIGURE P2.2

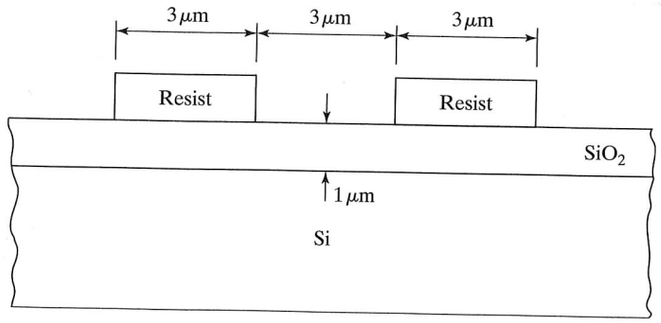


FIGURE P2.3

(a) Isotropic wet chemical etching.

(b) Anisotropic dry etching with no undercutting.

2.4 **(a)** What type of photoresist must be used with each of the three mask levels (*n*-diffusion window, contact windows, and metal etch) used to fabricate the diode of Problem 2.2? Assume that the areas shown are dark on the mask (a "light-field mask").

(b) Draw a set of alignment marks suitable for use with the alignment sequence of Problem 2.2(b).

2.5 In Table 2.5, 193-nm DUV lithography is shown as an alternative for 120-nm technology generation. (a) What value of NA would be required based upon Eq. 2.1? (b) What is the depth of field for this system?

2.6 **(a)** What wavelength illumination is required to achieve $F = 0.25$ μm with $NA = 1$ and without the use of phase-shifting masks? What is the value of DF corresponding to your value of NA?

(b) Repeat for $NA = 0.5$.

2.7 Based upon the discussion in Section 2.4, what is the smallest feature size F that can be reproduced with a 193-nm optical source?

2.8 An extreme ultra violet (EUV) lithography source uses a 13-nm exposure wavelength. Based upon the discussion in Section 2.4, what is the smallest feature size F that can be reproduced with this source?

CHAPTER 3

Thermal Oxidation of Silicon

Upon exposure to oxygen, the surface of a silicon wafer oxidizes to form silicon dioxide. This native silicon dioxide film is a high-quality electrical insulator and can be used as a barrier material during impurity deposition. These two properties of silicon dioxide were the primary process factors leading to silicon becoming the dominant material in use today for the fabrication of integrated circuits. This chapter discusses the theory of oxide growth, the oxide growth processes, factors affecting oxide growth rate, impurity redistribution during oxidation, and techniques for selective oxidation of silicon. Methods for determining the thickness of the oxide film are also presented, and the SUPREM process simulation software is introduced.

3.1 THE OXIDATION PROCESS

Thermal oxidation of silicon is easily achieved by heating the wafer to a high temperature, typically 900 to 1200 °C, in an atmosphere containing either pure oxygen or water vapor. Both water vapor and oxygen move (diffuse) easily through silicon dioxide at these high temperatures. (See Fig. 3.1.) Oxygen arriving at the silicon surface can then combine with silicon to form silicon dioxide. The chemical reaction occurring at the silicon surface is

$$Si + O_2 \rightarrow SiO_2 \tag{3.1}$$

for dry oxygen and

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \tag{3.2}$$

for water vapor. Silicon is consumed as the oxide grows, and the resulting oxide expands during growth, as shown in Fig. 3.2. The final oxide layer is approximately 54% above the original surface of the silicon and 46% below the original surface.