4.23 A gas cylinder contains 100 ft^3 of a mixture of diborane and argon. The diborane represents 0.1% by volume. An accident occurs and the complete cylinder is released into a room measuring $10 \times 12 \times 8$ ft.

(a) What will be the equilibrium concentration of diborane in the room in ppm?

(b) Compare this level with the toxic level based on Table 4.3.

(c) Would your answer to part (b) change if the gas cylinder contained arsine?

4.24 **(a)** Numerically calculate the sheet resistance of the diffusion in Problem 4.15 if the electron mobility can be described by

$$\mu_n = \left[92 + \frac{1270}{1 + \left(\frac{N}{1.3 \times 10^{17}} \right)^{.091}} \right] \frac{cm^2}{V-sec}$$

(b) Repeat for a similar p-type Gaussian layer in an n-type substrate if the hole moblility is given by

$$\mu_p = \left[48 + \frac{447}{1 + \left(\frac{N}{6.3 \times 10^{16}} \right)^{.076}} \right] \frac{cm^2}{V-sec}$$

CHAPTER 5

Ion Implantation

Ion implantation offers many advantages over diffusion for the introduction of impurity atoms into the silicon wafer and has become a workhorse technology in modern IC fabrication. In this chapter, we will first discuss ion implantation technology and mathematical modeling of the impurity distributions obtained with ion implantation. We will subsequently explore deviations from the model caused by nonideal behavior and will discuss annealing techniques used to remove crystal damage caused by the implantation process.

5.1 IMPLANTATION TECHNOLOGY

An ion implanter is a high-voltage particle accelerator producing a high-velocity beam of impurity ions that can penetrate the surface of silicon target wafers. The following list shows the basic parts of the system, shown schematically in Fig. 5.1, beginning with the impurity-source end of the system.

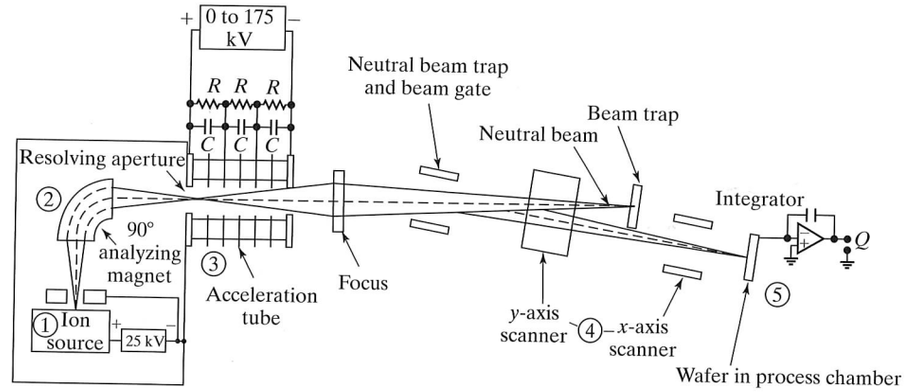


FIGURE 5.1

Schematic drawing of a typical ion implanter showing (1) ion source, (2) mass spectrometer, (3) high-voltage accelerator column, (4) *x*- and *y*-axis deflection system, and (5) target chamber.

1. **Ion Source**. The ion source operates at a high voltage (25 kV) and produces a plasma containing the desired impurity, as well as other undesired species. Arsine, phosphine, and diborane, as well as other gases, can be used in the source. Solids can be sputtered in special ion sources, and this technique offers a wide degree of flexibility in the choice of impurity.

2. **Mass Spectrometer**. An analyzer magnet bends the ion beam through a right angle to select the desired impurity ion. The selected ion passes through an aperture slit into the main accelerator column.

3. **High-Voltage Accelerator**. The accelerator column adds energy to the beam (up to 5 MeV) and accelerates the ions to their final velocity. Both the accelerator column and the ion source are operated at a high voltage relative to the target. For protection from high voltage and possible X-ray emission, the ion source and accelerator are mounted within a protective shield.

4. **Scanning System**. x- and y-axis deflection plates are used to scan the beam across the wafer to produce uniform implantation and to build up the desired dose. The beam is bent slightly to prevent neutral particles from hitting the target.

5. **Target Chamber**. Silicon wafers serve as targets for the ion beam. For safety, the target area is maintained near ground potential. The complete implanter system is operated under vacuum conditions.

The analyzer magnet is used to select the desired impurity ions from the output of the source. A charged particle moving with velocity $\boldsymbol{v}$ through a magnetic field $\boldsymbol{B}$ will experience a force $\boldsymbol{F}$, given by

$$\mathbf{F} = q(\mathbf{v} \times \mathbf{B}) \tag{5.1}$$

The force will tend to move the particle in a circle and the centrifugal force will balance $\boldsymbol{F}$. For the case where $\boldsymbol{B}$ is perpendicular to v, $q\mathbf{v}\,\mathbf{B} = m|\mathbf{v}|^2/r$, where $m|\mathbf{v}|^2/2 = qV$ and V is the accelerator voltage. Thus, the magnitude of the magnetic field $\boldsymbol{B}$ may be adjusted to select an ion species with a given mass:

$$|\mathbf{B}| = \sqrt{(2mV/qr^2)} \tag{5.2}$$

The ion source in the figure operates at a constant potential (25 keV) so that the voltage V is known, and an ion species is selected by changing the dc current supplying the analyzer magnet. The selected impurity is then accelerated to its final velocity in the high-voltage column.

The silicon wafer is maintained in good electrical contact with the target holder, so electrons can readily flow to or from the wafer to neutralize the implanted ions. This electron current is integrated over time to measure the total dose Q from the implanter given by

$$Q = \frac{1}{mqA}\int_0^T I\,dt \tag{5.3}$$

where I is the beam current in amperes, A is the wafer area, $n = 1$ for singly ionized ions and 2 for doubly ionized species, and T is the implantation time. The use of a doubly ionized species increases the energy capability of the machine by a factor of 2, since $E = nqV$.

The target wafers can be maintained at relatively low temperatures during the implantation. Low-temperature processing prevents undesired spreading of impurities by diffusion, which is very important in VLSI fabrication. Another advantage of ion implantation is the ability to use a much wider range of impurity species than possible with diffusion. In principle, any element that can be ionized can be introduced into the wafer using implantation.

A production-level ion implanter costs millions of dollars, and this high cost is its greatest disadvantage. However, the advantages of flexibility and tight process control have far outweighed the disadvantage of cost, and ion implantation is now used routinely throughout bipolar and MOS integrated-circuit fabrication.

5.2 MATHEMATICAL MODEL FOR ION IMPLANTATION

As an ion enters the surface of the wafer, it collides with atoms in the lattice and interacts with electrons in the crystal. Each nuclear or electronic interaction reduces the energy of the ion until it finally comes to rest within the target. Interaction with the crystal is a statistical process, and the implanted impurity profile can be approximated by the Gaussian distribution function illustrated in Fig. 5.2. The distribution is described mathematically by

$$N(x) = N_p \exp\left[-\frac{(x - R_p)^2}{2\Delta R_p^2}\right] \tag{5.4}$$

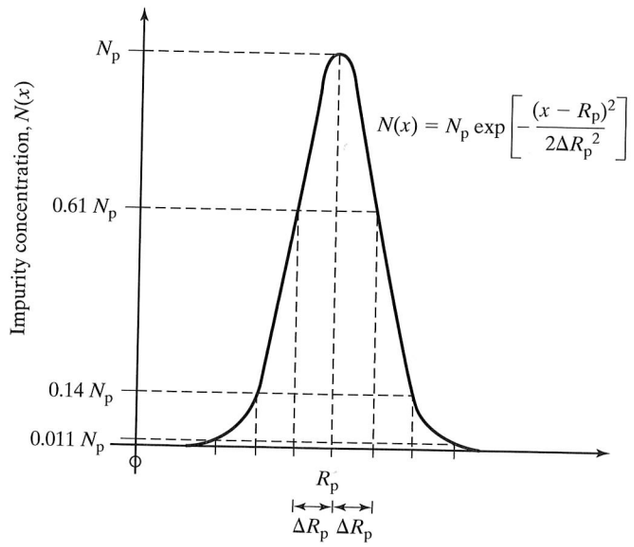


FIGURE 5.2

Gaussian distribution resulting from ion implantation. The impurity is shown implanted completely below the wafer surface ($x = 0$).

R_p is called the *projected range* and is equal to the average distance an ion travels before it stops. The peak concentration N_p occurs at $x = R_p$. Because of the statistical nature of the process, some ions will be "lucky" and will penetrate beyond the projected range R_p, and some will be "unlucky" and will not make it as far as R_p. The spread of the distribution is characterized by the standard deviation, ΔR_p, called the *straggle*.

The area under the impurity distribution curve is the implanted dose Q, defined by

$$Q = \int_0^\infty N(x)dx \tag{5.5}$$

For an implant completely contained within the silicon, the dose is equal to

$$Q = \sqrt{2\pi} N_p \Delta R_p \tag{5.6}$$

Implanted doses typically range from $10^{10}/cm^3$ to $10^{18}/cm^3$. For example, ion implantation is often used to replace the predeposition step in a two-step diffusion process. Doses in the range of 10^{10} to $10^{13}/cm^2$ are required for threshold adjustment in MOS technologies and are almost impossible to achieve using diffusion. CMOS well formation is another example where the dose control of the ion implanter is a distinct advantage. However, doses exceeding $10^{15}/cm^2$ are quite large and can be time-consuming to produce using ion implantation. As a reference for comparison, the silicon lattice atomic sheet density is approximately 7×10^{14} silicon atoms/cm^2 on the <100> surface.

The implanted dose can be controlled within a few percent, and this tight control represents a major advantage of ion implantation. For example, resistors can be fabricated with absolute tolerances of a few percent in carefully controlled processes using ion implantation, whereas the same resistors would have an absolute tolerance exceeding 20% if they were formed using only diffusion.

The projected range of a given ion is a function of the energy of the ion, and of the mass and atomic number of both the ion and the target material. A theory for range and straggle was developed by Lindhard, Scharff, and Schiott and is called the *LSS theory* [1]. This theory assumes that the implantation goes into an amorphous material in which the atoms of the target material are randomly positioned. Figure 5.3 displays the results of LSS calculations for the projected range and straggle for antimony, boron, phosphorus, and arsenic in amorphous silicon and silicon dioxide. For the moment, we will assume that these results are also valid for crystalline silicon. Deviations from the LSS theory will be discussed in Section 5.5.

Range and straggle are roughly proportional to ion energy over a wide range, although nonlinear behavior is clearly evident in the figure. For a given energy, the lighter elements strike the silicon wafer with a higher velocity and penetrate more deeply into the wafer. The results indicate that the projected ranges in Si and SiO_2 are essentially the same, and we will assume that the stopping power of silicon dioxide is equal to that of silicon. Figure 5.3 also gives values for the transverse straggle $\Delta R_\perp$, which will be discussed in the next section.

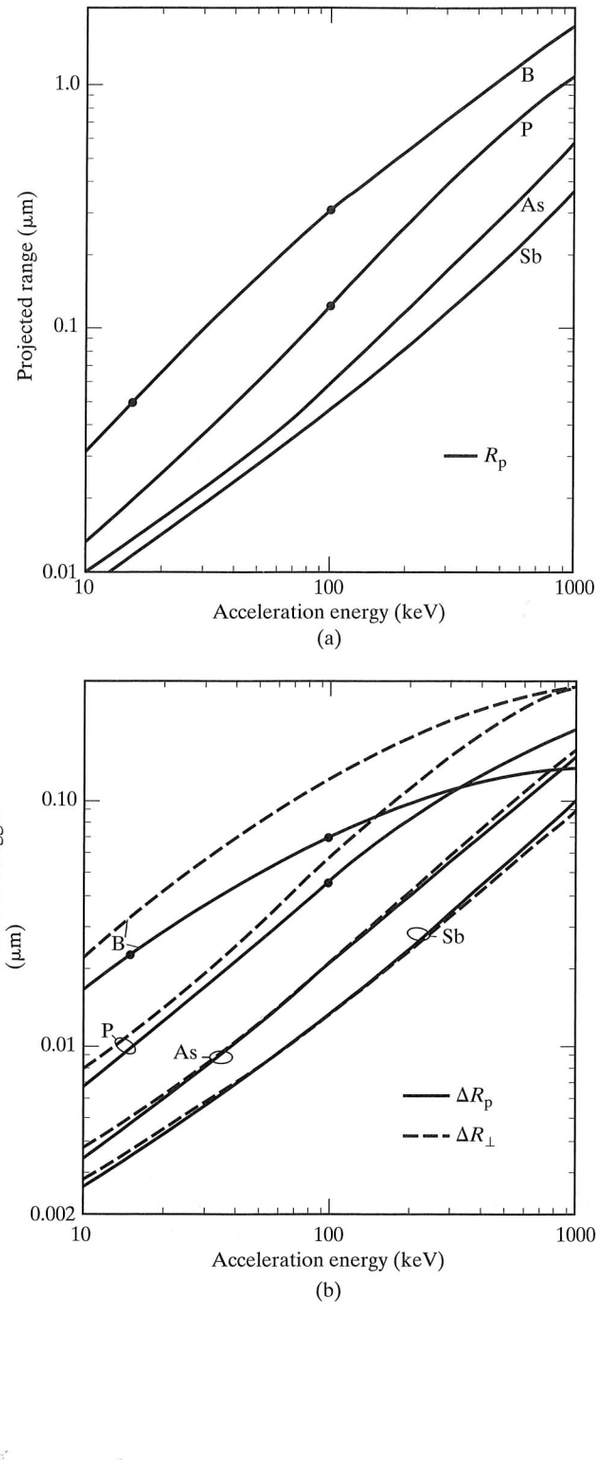


FIGURE 5.3

Projected range and straggle calculations based on LSS theory. (a) Projected range R_p for boron, phosphorus, arsenic, and antimony in amorphous silicon. Results for SiO_2 and for silicon are virtually identical. (b) Vertical ΔR_p and transverse $\Delta R_\perp$ straggle for boron, phosphorus, arsenic, and antimony. Reprinted with permission from Ref. [2]. (Copyright van Nostrand Reinhold Company, Inc.)

Example 5.1

Phosphorus with an energy of 100 keV is implanted into a silicon wafer. (**a**) What are the range and straggle associated with this implantation? (**b**) What should the implanted dose be if a peak concentration of $1 \times 10^{17}/\text{cm}^3$ is desired? (**c**) What length of time is required to implant this dose into a 200-mm wafer using a 2 μA beam current with singly ionized phosphorus?

Solution: Using Fig. 5.3, we find that the range and straggle are 0.12 μm and 0.045 μm, respectively. The dose and peak concentration are related by Eq. (5.6). Note that this is an approximation, since the peak is only a little over $2\Delta R_p$ below the silicon surface.

$$Q = \sqrt{2\pi} N_p \Delta R_p = \sqrt{2\pi}(1 \times 10^{17}/\text{cm}^3)(4.5 \times 10^{-6}\text{cm}) = 1.13 \times 10^{12}/\text{cm}^2$$

Rearranging Eq. (5.3) assuming a constant beam current gives:

$$T = \frac{nqAQ}{I} = \frac{(1)(1.6 \times 10^{-19}\text{coul})(\pi)(10\text{cm})^2(1.13 \times 10^{-12}/\text{cm}^2)}{2 \times 10^{-6}\text{coul/sec}} = 28.4 \text{ sec}$$

5.3 SELECTIVE IMPLANTATION

In most cases, we desire to implant impurities only in selected areas of the wafer. Windows are opened in a barrier material wherever impurity penetration is desired. In the center of the window, the impurity distribution is described by Eq. (5.4), but near the edges the distribution decreases and actually extends under the edge of the window, as shown in Fig. 5.4. The overall distribution can be modeled by[3]

$$N(x,y) = N(x)F(y)$$

$$F(y) = 0.5[\text{erfc}\{(y - a)/\sqrt{2}\Delta R_\perp\} - \text{erfc}\{(y + a)/\sqrt{2}\Delta R_\perp\}] \quad (5.7)$$

where $N(x)$ is given by Eq. (5.4) and $2a$ is the width of the window. The parameter $\Delta R_\perp$ is called the *transverse straggle* and characterizes the behavior of the distribution near the edge of the window. Figure 5.4 shows normalized impurity distributions near the barrier edge calculated with Eq. (5.7). Figure 5.3(b) gives values of both normal straggle ΔR_p and transverse straggle $\Delta R_\perp$.

In order to mask the ion implantation, it is necessary to prevent the implanted impurity from changing the doping level in the silicon beneath the barrier layer. Figure 5.5 shows a silicon wafer with a layer of silicon dioxide on the surface. An impurity has been implanted into the wafer with the peak of the distribution in the silicon dioxide. To prevent significantly altering the doping in the silicon, we require that the implanted concentration be less than 1/10th the background concentration at the interface between the silicon and silicon dioxide:

$$N(X_0) < N_B/10 \quad (5.8)$$

or

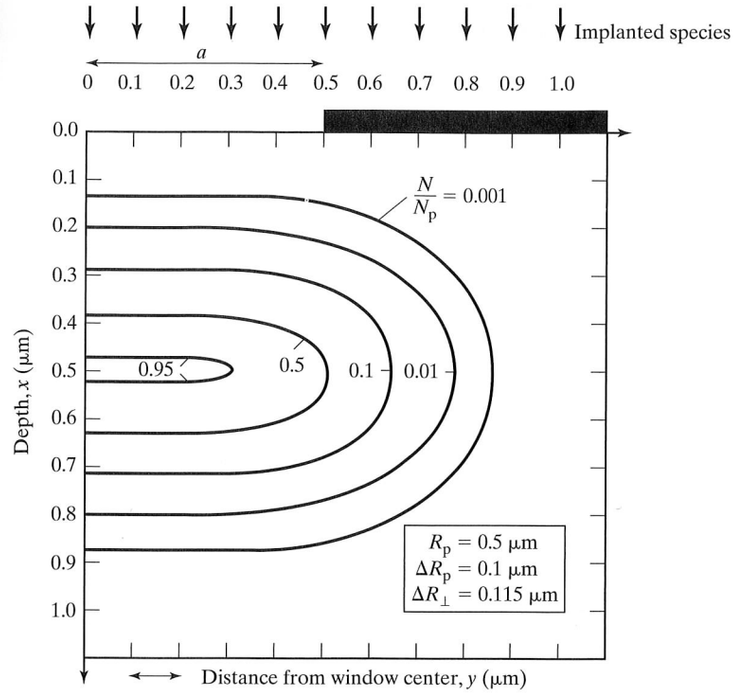


FIGURE 5.4

Contours of equal ion concentration for an implantation into silicon through a 1 μm window. The profiles are symmetrical about the x-axis and were calculated using Eq. (5.7), which is taken from Ref. [3].

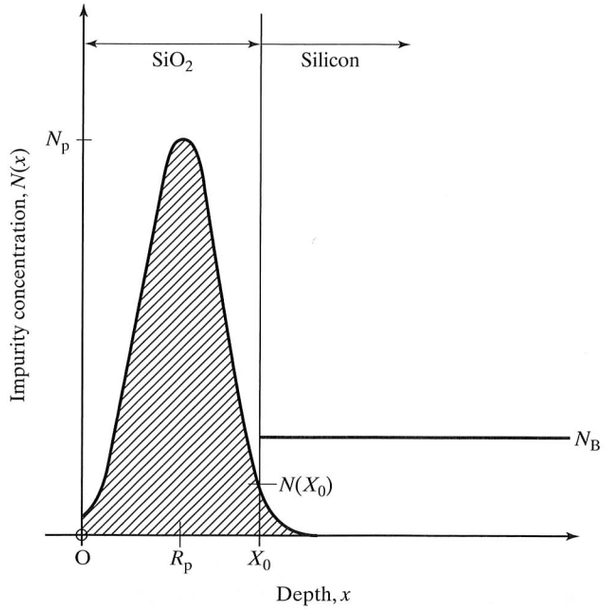


FIGURE 5.5

Implanted impurity profile with implant peak in the oxide. The barrier material must be thick enough to ensure that the concentration in the tail of the distribution is much less than N_B.

TABLE 5.1 Values of m for Various Values of N_p/N_B.

N_p/N_B	m
10^1	3.0
10^2	3.7
10^3	4.3
10^4	4.8
10^5	5.3
10^6	5.7

$$N_p \exp[-\frac{(X_0 - R_p)^2}{2\Delta R_p^2}] < N_B/10 \tag{5.9}$$

Solving Eq. (5.9) for X_0 yields a minimum oxide thickness of

$$X_0 = R_p + \Delta R_p\sqrt{2\ln(10N_p/N_B)} = R_p + m\,\Delta R_p \tag{5.10}$$

The oxide thickness must be at least equal to the projected range plus some multiple m times the straggle. Table 5.1 gives values of m for various ratios of peak concentration to background concentration. An oxide thickness equal to the projected range plus six times the straggle should mask most ion implantations.

Silicon dioxide and silicon nitride are routinely used as barrier materials during implantation. Since implantation is a low-temperature process, additional materials such as photoresist and aluminum, which cannot withstand high-temperature diffusion, may be used as barrier materials during the implantation.

Silicon nitride is more effective than silicon dioxide in stopping ions, and a silicon nitride barrier layer need only be 85% of the thickness of an SiO_2 barrier layer. On the other hand, photoresist is less effective in stopping ions, and a photoresist barrier layer must be 1.8 times the thickness of an SiO_2 layer under the same implantation conditions. Metals are of such a high density that even a very thin layer will mask most implantations.

Example 5.2

A boron implantation is to be performed through a 50-nm gate oxide so that the peak of the distribution is at the Si–SiO_2 interface. The dose of the implant in silicon is to be $1 \times 10^{13}/cm^2$. **(a)** What are the energy of the implant and the peak concentration at the interface? **(b)** How thick should the SiO_2 layer be in areas that are not to be implanted, if the background concentration is $1 \times 10^{16}/cm^3$? **(c)** Suppose the oxide is 50 nm thick everywhere. How much photoresist is required on top of the oxide to completely mask the ion implantation?

Solution: The projected range needs to be 0.05 μm in order to place the peak of the distribution at the Si–SiO_2 interface. Using Fig. 5.3(a), we find that the R_p of 0.05 μm requires an energy of 15 keV. Since the peak of the implant is at the interface, the total dose will be twice the dose needed in silicon. The peak concentration is

$$N_p = Q/\Delta R_p\sqrt{2\pi} = 2 \times 10^{13}/(2.3 \times 10^{-6}\sqrt{2\pi}) = 3.5 \times 10^{18}/cm^3$$

where the straggle was found using Fig. 5.3(b). To completely mask the implantation, the tail of the distribution must be less than the background concentration at the interface. The minimum oxide thickness is found using Eq. (5.9):

$$X_0 = 0.05 + 0.023\sqrt{2\ln(10 \times 3.5 \times 10^{18}/10^{16})}\ \mu m = 0.14\ \mu m$$

Since the oxide is 0.05 μm thick, the photoresist must provide a thickness equivalent to 0.09 μm. The resist thickness must be 1.8 times the needed thickness of SiO_2 to provide an equivalent barrier layer, so the photoresist should be at least 0.16 μm thick. This thickness requirement is easily met with most photoresist layers.

5.4 JUNCTION DEPTH AND SHEET RESISTANCE

Ion implantation is often used to form shallow *pn* junctions for various device applications. The implanted profile approximates a Gaussian distribution, and the junction depth may be found by equating the implanted distribution to the background concentration, as explained in Chapter 4:

$$N_p \exp\left[\frac{(X_j - R_p)^2}{2\Delta R_p^2}\right] = N_B$$

$$x_j = R_p \pm \Delta R_p\sqrt{2\ln(N_p/N_B)} \tag{5.11}$$

Both roots may be meaningful, as indicated in Fig. 5.6, in which a deep subsurface implant has junctions occurring at two different depths, x_{j1} and x_{j2}.

Example 5.3

Boron is implanted into an n-type silicon wafer to a depth of 0.3 μm. Find the location of the junction if the peak concentration is $1 \times 10^{18}/cm^3$ and the doping of the wafer is $3 \times 10^{16}/cm^3$.

Solution: From Fig. 5.3(a), the implant energy is 100 keV. From Fig. 5.3(b), the straggle is 0.07 μm. Equating the Gaussian distribution to the background concentration yields

$$3 \times 10^{16} = 10^{18} \exp -\left[\frac{(X_j - R_p)^2}{2\Delta R_p^2}\right]$$

or

$$x_j = R_p \pm 2.65\Delta R_p$$

This yields junction depths of 0.12 μm and 0.49 μm.

The peak of an implantation is often positioned at the silicon surface. For this special case, we may use Irvin's curves for Gaussian distributions to find the sheet resistance of the implanted layer, as discussed in Chapter 4. These curves may also be

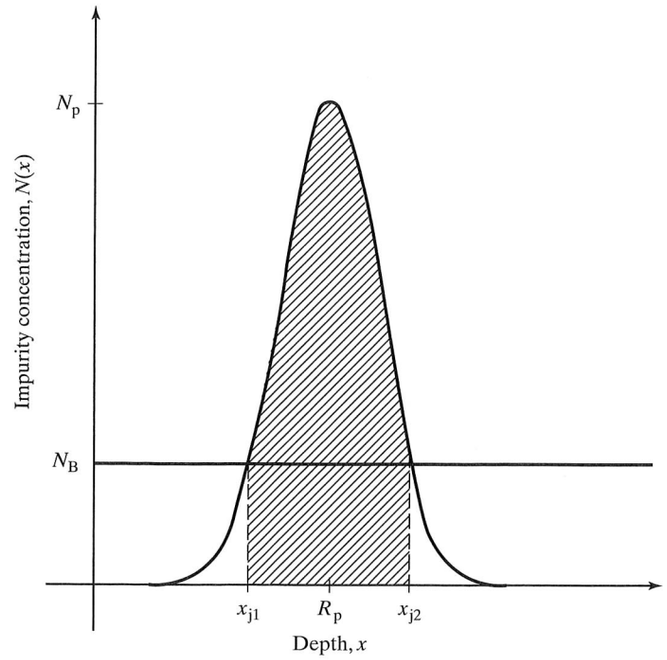


FIGURE 5.6

Junction formation by impurity implantation in silicon. Two *pn* junctions are formed at x_{j1} and x_{j2}.

used to find the sheet resistance of a layer which is completely below the surface. (See Problem 5.4.) Note that an implanted Gaussian impurity distribution will remain Gaussian through any subsequent high-temperature processing steps.

Diffused profiles generally have the maximum impurity concentration at the silicon surface. Ion-implantation techniques can be used to produce profiles with subsurface peaks or "retrograde" profiles that decrease toward the wafer surface. Multiple implant steps at different energies can also be used to build up more complicated impurity profiles.

5.5 CHANNELING, LATTICE DAMAGE, AND ANNEALING

5.5.1 Channeling

The LSS results of Section 5.2 are based on the assumption that the target material is amorphous, having a completely random order. This assumption is true of thermal SiO_2, deposited Si_3N_4 and SiO_2, and many thin metal films, but it is not valid for a crystalline substrate. The regular arrangement of atoms in the crystal lattice leaves a large amount of open space in the crystal. For example, Fig. 5.7 shows a view through the silicon lattice in the <110> direction. If the incoming ion flux is improperly oriented with respect to the crystal planes, the ions will tend to miss the silicon atoms in the lattice and will "channel" much more deeply into the material than the LSS theory predicts. However, electronic interactions will eventually stop the ions.

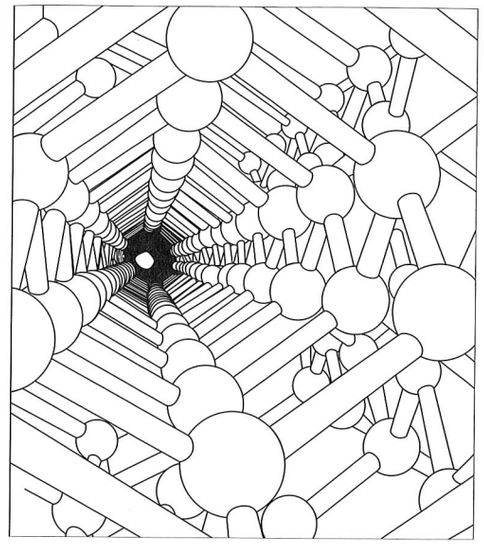


FIGURE 5.7

The silicon lattice viewed along the <110> axis. From *The Architecture of Molecules* by Linus Pauling and Roger Hayward. Copyright © 1964 W. H. Freeman and Company. Reprinted with permission from Refs. [4a] and [4b].

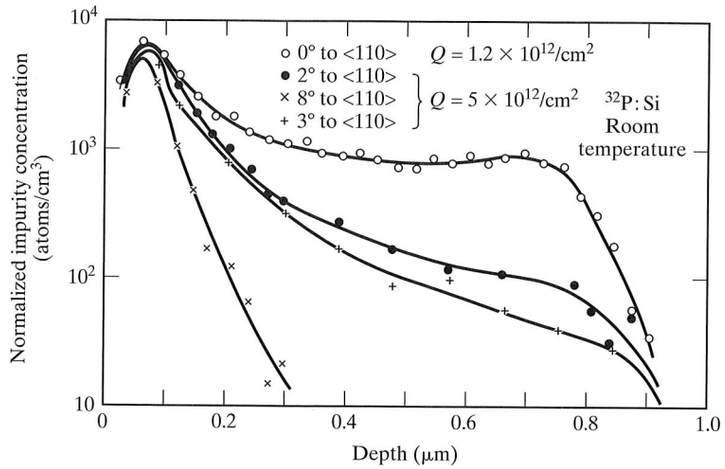


FIGURE 5.8

Phosphorus impurity profiles for 40-keV implantations at various angles from the <110> axis. Copyright 1968 by National Research Council of Canada. Reprinted with permission from Ref. [5].

The effects of channeling are demonstrated in Fig. 5.8. Phosphorus has been implanted at an energy of 40 keV into a silicon target with several orientations of the ion beam relative to the <100> silicon surface. The appearance of a random target can be achieved by tilting <100> silicon approximately 8° relative to the incoming beam. The results are represented by the *x*'s in Fig. 5.8. The range for this case compares well with the LSS calculations presented in Fig. 5.3. The open circles represent the boron profile implanted perpendicular to the <100> surface. Note that the range for the "channeled" case is almost twice that predicted by the LSS theory. Results for two other angles of incidence are given in Fig. 5.8, showing progressively less channeling as the angle is increased.

5.5.2 Lattice Damage and Annealing

During the implantation process, ion impact can knock atoms out of the silicon lattice, damaging the implanted region of the crystal. If the dose is high enough, the implanted layer will become amorphous. Figure 5.9 gives the dose required to produce an amorphous silicon layer for various impurities as a function of substrate temperature. The heavier the impurity, the lower the dose that is required to create an amorphous layer. At sufficiently high temperatures, an amorphous layer can no longer be formed. Note that damage from argon implantation was mentioned as a possible gettering technique at the end of Chapter 4.

Implantation damage can be removed by an "annealing" step. Following implantation, the wafer is heated to a temperature between 800 and 1000 °C for approximately 30 min. At these temperatures, silicon atoms can move back into lattice sites, and impurity atoms can enter substitutional sites in the lattice. After the annealing cycle, nearly all of the implanted dose becomes electrically active, except for impurity concentrations exceeding $10^{19}/cm^3$.

Unfortunately, annealing cycles of 30 min at temperatures approaching 1000 °C can cause considerable spreading of the implant by diffusion. It has been found that truly amorphous layers can actually be annealed at lower temperatures through the process of solid-phase epitaxy. The crystalline substrate seeds recrystallization of the amorphous layer, and epitaxial growth can proceed as rapidly as 500 Å/min at 600 °C. During solid-phase epitaxy, impurity atoms are incorporated into substitutional sites, and full activation is achieved at low temperatures.

Low-energy arsenic implantations produce shallow amorphous layers that can be annealed using solid-phase epitaxy to yield shallow, abrupt junctions that are ideal for

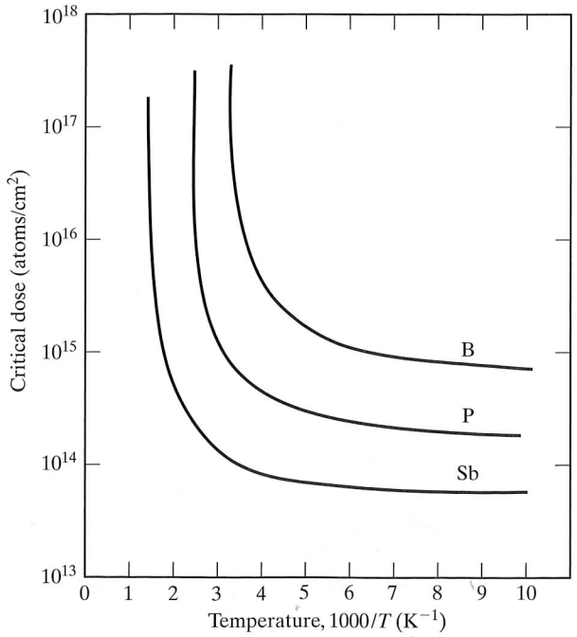


FIGURE 5.9

A plot of the dose required to form an amorphous layer on silicon versus reciprocal target temperature. Arsenic falls between phosphorus and antimony. Copyright 1970 by Plenum Publishing Corporation. Reprinted with permission from Ref. [6].

VLSI structures. Boron, however, is so light that it does not produce an amorphous layer even at relatively high doses, unless the substrate is deliberately cooled. (See Fig. 5.9.) Today, boron is often implanted using ions of the heavier BF_2 molecule. The lower-velocity implant results in shallow layers that can be annealed under solid-phase-epitaxy conditions.

5.5.3 Deviations from the Gaussian Theory

If we take a detailed look at the shape of the implanted impurity distribution, we find deviations from the ideal Gaussian profile. When light ions, such as boron, impact atoms of the silicon target, they experience a relatively large amount of backward scattering and fill in the distribution on the surface side of the peak, as in Fig. 5.10. Heavy atoms, such as arsenic, experience a larger amount of forward scattering and tend to fill in the profile on the substrate side of the peak. A number of methods have been proposed for mathematically modeling this behavior, such as the use of Pearson Type-IV distributions [8]. However, for common implant energies below 200 keV, the Gaussian theory provides a useful model of the impurity distribution. This is particularly true since the forward and backward scattering tend to alter the tails of the distribution where the concentration is well below the peak value.

5.6 SHALLOW IMPLANTATION

Deep submicron MOS devices require heavily doped source–drain regions with junction depths below 20 nm. In order to form these junctions, a new set of manufacturing tools was developed based upon low-energy implantation and rapid thermal annealing. A detailed understanding of a diffusion phenomenon termed Transient Enhanced Diffusion or TED was also required.

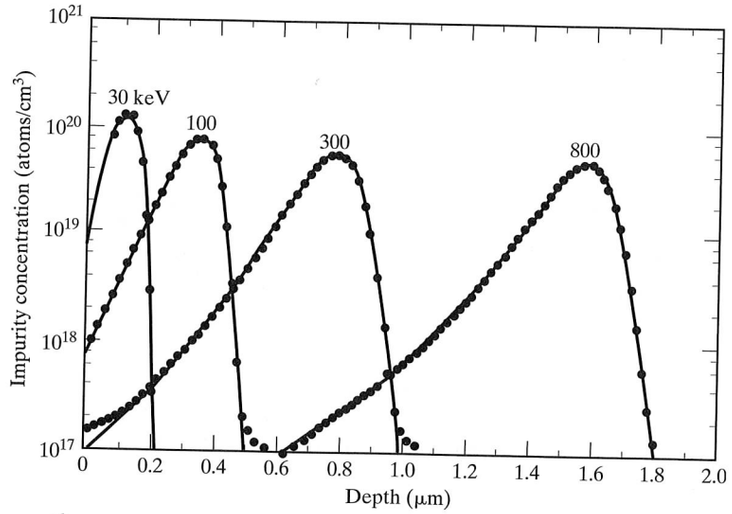


FIGURE 5.10

Measured boron impurity distributions compared with four-moment (Pearson IV) distribution functions. The boron was implanted into amorphous silicon without annealing. Reprinted with permission from Philips Journal of Research [8].

5.6.1 Low-Energy Implantation

To achieve shallow junctions, low-voltage ion implantation with energies in the range of 0.25–5 keV are utilized. Note that the classical ion-implanter described in Section 5.1 is not adequate for these implants, because of the high initial acceleration potential; specialized implanter systems have been developed specifically for low-energy ion implantation. In addition, new implantation species with high mass, such as decaborane $B_{10}H_{14}$ [12], and hence low resulting velocity, are being investigated. The "as-implanted" impurity profile distributions resulting from low-energy implantations can have peaks very near the surface with junction depths of less than 25 nm, as indicated by the SIMS data in Fig. 5.11. Because relatively high doses are used to achieve low sheet resistance for source–drain regions, even low-energy implants cause substantial damage to the crystal near the wafer surface, and this damage must be removed by annealing.

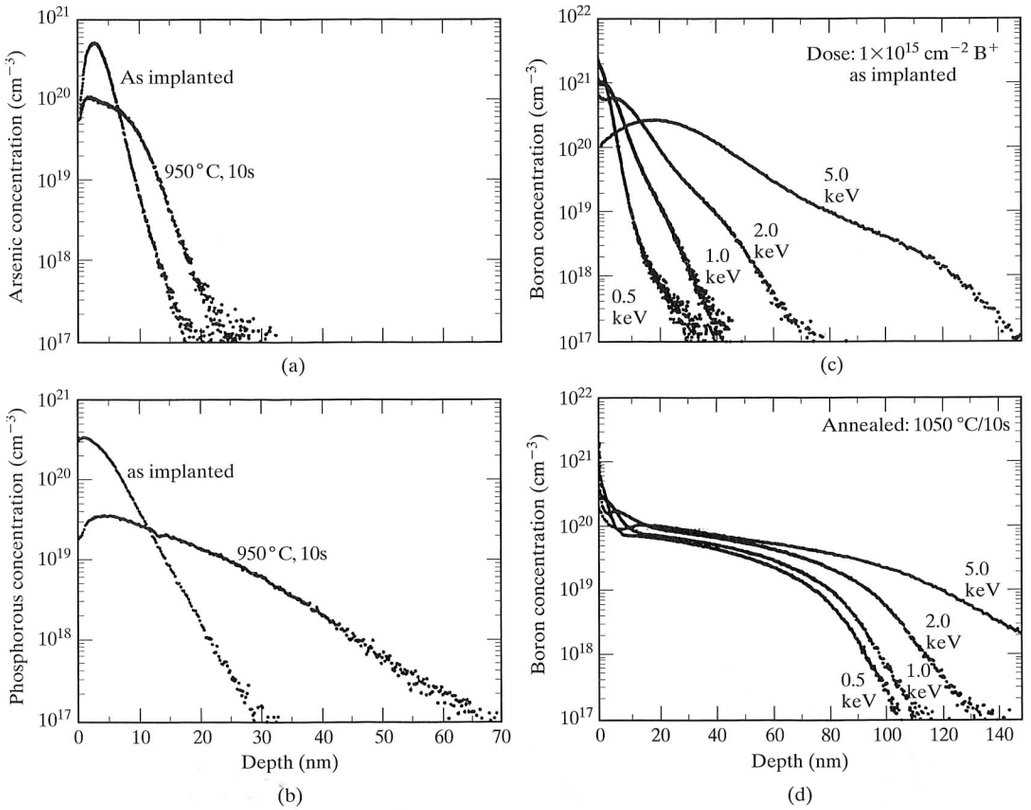


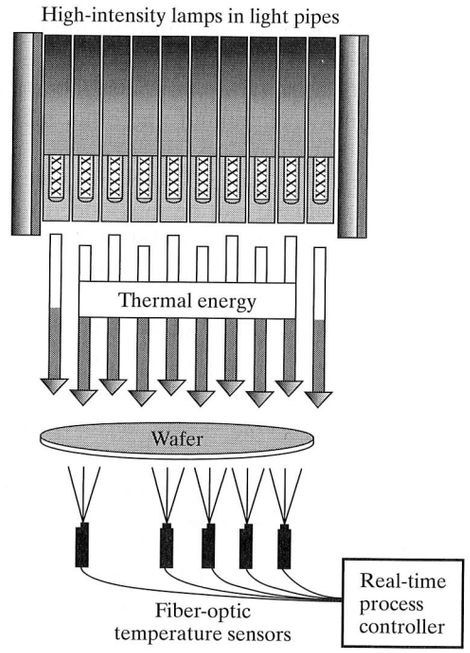
FIGURE 5.11

Examples of transient enhanced diffusion. SIMS data comparing as-implanted and annealed depth profiles from (a) 3 x 10^{14}/cm^2, 2 keV As^+, and (b) 3 x 10^{14}/cm^2, 1 keV P^+. Annealing conditions were 950 °C for 10 sec. SIMS depth profiles of 1 x 10^{15}/cm^2 B implanted at 0.5-, 1-, 2-, and 5-keV (c) as-implanted, and (d) after annealing at 1050 °C for 10 sec. Copyright 1997 IEEE. Reprinted with permission from Ref. [13].

5.6.2 Rapid Thermal Annealing

In addition to removing the damage caused by the implantation, the annealing step is required to electrically activate the implanted impurities. However, in order to minimize diffusion of the shallow implanted profiles, the *Dt* product associated with the annealing process must be kept as small as possible. Rapid Thermal Annealing (RTA) systems can achieve the desired results with annealing times that range from a few minutes down to only a few seconds. High-intensity lamps shown in Fig. 5.12(a) are used to rapidly heat the wafer to the desired annealing temperature (e.g., 950–1050 °C) in a very short time. Extremely rapid temperature ramp-up and ramp-down rates are achieved (e.g., 50 °C/sec or more). Using this rapid thermal-processing technique, the effective *Dt* products can be very small. However, even the short ramp time can be important if the dwell time at the upper temperature is short. (See Problems 5.19–5.22.)

Rapid thermal annealing represents only one form of rapid thermal processing. Similar systems are used to grow very thin oxide and nitride layers using processes termed rapid thermal oxidation (RTO) or rapid thermal nitridation (RTN). Silicide layers, to be discussed in Section 7.5, can also be formed using rapid thermal processing. An example of an RTP system appears in Fig. 5.12(b).



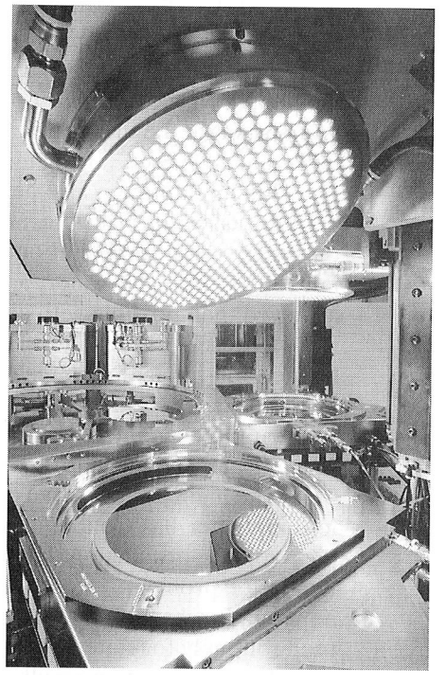

(b)

FIGURE 5.12

(a) Concept of a rapid thermal processing (RTP) system. (b) Applied Materials 300 mm RTP System. (Courtesy Applied Materials, Inc.)

5.6.3 Transient Enhanced Diffusion (TED)

During the investigation of shallow junction formation, it was discovered that the impurities diffuse considerably more than predicted by simple diffusion theory using the values of the *Dt* product calculated for the annealing process. It was found that the presence of damage to the silicon crystal from the implantation temporarily enhances the diffusion coefficient by a factor as large as 5 to 10 times [13–16]. This enhancement is a transient phenomenon which disappears as the damage is annealed out. However, the modification of the impurity profile can be substantial, particularly to the tails of the distribution, and the junction depth can change by a significant amount. Since the dose is constant, the peak concentration also falls, and the sheet resistance changes due to the impurity redistribution. An example of the profile redistribution due to TED is also presented in the SIMS data in Fig. 5.11 [13]. Because of its importance in small geometry devices, modeling of the TED phenomena has been added to many process simulation programs.

SUMMARY

Ion implantation uses a high-voltage accelerator to introduce impurity atoms into the surface of the silicon wafer, and it offers many advantages over deposition by high-temperature diffusion. Ion implantation is a low-temperature process minimizing impurity movement by diffusion, which has become very important to VLSI fabrication. Low-temperature processing also permits the use of a wide variety of materials as barrier layers to mask the implantation. Photoresist, oxide, nitride, aluminum, and other metal films can all be used, adding important increased flexibility to process design.

Ion implantation also permits the use of a much wider range of impurity species than diffusion. In principle, any element that can be ionized can be introduced into the wafer using implantation. Implantation offers much tighter control of the dose introduced into the wafer, and a much wider range of doses can be reproducibly achieved than possible with diffusion.

Diffused profiles almost always have the maximum impurity concentration at the surface. Ion-implantation techniques can be used to produce new profiles with subsurface peaks or retrograde profiles which decrease toward the wafer surface. Implantation can introduce impurities into very shallow layers near the surface, again a significant advantage for VLSI structures.

The main disadvantage of ion implantation is the cost of the equipment. Also, the ion implanter has trouble achieving high doses ($>10^{16}/cm^3$) in a time reasonable for high-volume production. High-current machines have been developed to overcome this latter problem. Overall, the flexibility and process control achievable with ion implantation have far outweighed the disadvantage of cost, and ion implantation is used routinely for state-of-the-art bipolar and MOS integrated-circuit fabrication.

Ion implantation results in profiles that can be modeled by a Gaussian distribution. The depth and width of the distribution depend on both the ion species and the energy of the implantation. To prevent channeling, implantation is normally performed at an angle of approximately 8° off the normal to the wafer surface.

The implantation process damages the surface, and an annealing step is required to remove the effects of the damage. Low doses may result in the need for annealing at 800 to 1000 °C for 30 min. However, if the surface layer has become amorphous, annealing can be achieved through solid-phase epitaxy at temperatures of only 600 °C.

Very shallow implantations, that are required for deep submicron VLSI fabrication, can be achieved using low energy (< 5 keV) ion implantation. Rapid thermal annealing is then used to activate the implantation while maintaining a small Dt product. However, transient enhanced diffusion causes the implantations to spread more deeply than predicted by the Dt value and standard diffusion models.

REFERENCES

[1] J. Lindhard, M. Scharff, and H. Schiott, "Range Concepts in Heavy Ion Ranges," *Mat.-Fys. Med. Dan. Vid. Selsk*, *33*, No. 14, 1963.

[2] J. F. Gibbons, W. S. Johnson, and S. W. Mylroie, *Projected Range in Semiconductors*, 2nd ed., Dowden, Hutchinson, and Ross, New York, 1975.

[3] S. Furukawa, H. Matsumura, and H. Ishiwara, "Lateral Distribution Theory of Implanted Ions," in S. Namba, Ed., *Ion Implantation in Semiconductors*, Japanese Society for the Promotion of Science, Kyoto, pp. 73, 1972.

[4] (a) L. Pauling and R. Hayward, *The Architecture of Molecules*, W. H. Freeman, San Francisco, 1964. (b) S. M. Sze, Ed., *Semiconductor Devices Physics and Technology*, McGraw-Hill, New York, 1985.

[5] G. Dearnaley, J. H. Freeman, G. A. Card, and M. A. Wilkins, "Implantation Profiles of ^{32}P Channeled into Silicon Crystals," *Canadian Journal of Physics, 46*, 587–595 (March 15, 1968).

[6] F. F. Morehead and B. L. Crowder, "A Model for the Formation of Amorphous Si by Ion Implantation," pp. 25–30, in Eisen and Chadderton (see Source Listing 4).

[7] B. L. Crowder and F. F. Morehead, Jr., "Annealing Characteristics of *n*-type Dopants in Ion-Implanted Silicon," *Applied Physics Letters, 14*, 313–315 (May 15, 1969).

[8] W. K. Hofker, "Implantation of Boron in Silicon," *Philips Research Reports Supplements*, No. 8, 1975.

[9] J. F. Gibbons, "Ion-Implantation in Semiconductors—Part I: Range Distribution Theory and Experiment," *Proceedings of the IEEE, 56*, 295–319, March 1968.

[10] J. F. Gibbons, "Ion Implantation in Semiconductors—Part II: Damage Production and Annealing," *Proceedings of the IEEE, 60*, 1062–1096, September 1972.

[11] T. Hirao, G. Fuse, K. Inoue, S. Takayanagi, Y. Yaegashi, S. Ichikawa, and T. Izumi, "Electrical Properties of Si Implanted with As Through SiO_2 Films," *Journal of Applied Physics, 51*, 262–268 (January 1980).

[12] K. Goto, J. Matsuo, Y. Tada, T. Tanaka, Y. Momiyama, T. Sugii, and I. Yamada, "A High-Performance 50 nm PMOSFET Using Decaborane ($B_{10}H_{14}$) Ion Implantation and 2-step Activation Annealing Process," *IEEE IEDM Digest*, pp. 471–474, December 1997.

[13] A. Agarwal, D. J. Eaglesham, H-J. Gossman, L. Pelaz, S. B. Herner, D. C. Jacobson, T. E. Haynes, Y. Erokhin, and R. Simonton, "Boron-Enhanced-Diffusion of Boron: The Limiting Factor for Ultra Shallow Junctions, *IEEE IEDM Digest*, pp. 467–470, December 1997.

[14] A. D. Lilak, S. K. Earles, K. S. Jones, M. E. Law, and M. D. Giles, "A Physics-Based Modeling Approach for the Simulation of Anomalous Boron Diffusion and Clustering Behavior," *IEEE IEDM Digest*, pp. 493–496, December 1997.

[15] K. Suzuki, T. Miyashita, and Y. Tada, "Damage Calibration Concept and Novel B Cluster Reaction Model for B Transient Enhanced Diffusion Over Thermal Process Range from 600 °C (839 h) to 1100 °C (5 s) with Various Ion Implantation Doses and Energies," *IEEE IEDM Digest*, pp. 501–504, December 1997.

[16] S. S. Yu, H. W. Kennel, M. D. Giles, and P. A. Packan, "Simulation of Transient Enhanced Diffusion Using Computationally Efficient Models," *IEEE IEDM Digest*, pp. 509–512, December 1997.

SOURCE LISTING

[1] J. W. Mayer, L. Eriksson, and J. A. Davies, *Ion-Implantation in Semiconductors*, Academic Press, New York, 1970.

[2] G. Dearnaley, J. H. Freeman, R. S. Nelson, and J. Stephen, *Ion-Implantation*, North-Holland, New York, 1973.

[3] G. Carter and W. A. Grant, *Ion-Implantation of Semiconductors*, John Wiley & Sons, New York, 1976.

[4] F. Eisen and L. Chadderton, Eds., *Ion Implantation in Semiconductors*, First International Conference (Thousand Oaks, CA), Gordon and Breach, New York, 1970.

[5] I. Ruge and J. Graul, Eds., *Ion Implantation in Semiconductors*, Second International Conference (Garmisch-Partenkirchen, Germany), Springer-Verlag, Berlin, 1972.

[6] B. L. Crowder, Ed., *Ion Implantation in Semiconductors*, Third International Conference (Yorktown Heights, NY), Plenum, New York, 1973.

[7] S. Namba, Ed., *Ion Implantation in Semiconductors*, Fourth International Conference (Osaka, Japan), Plenum, New York, 1975.

[8] F. Chernow, J. Borders, and D. Bruce, Eds., *Ion Implantation in Semiconductors*, Fifth International Conference (Boulder, CO), Plenum, New York, 1976.

PROBLEMS

5.1 Boron is implanted with an energy of 60 keV through a 0.25-μm layer of silicon dioxide. The implanted dose is $1 \times 10^{14}/\text{cm}^2$.

(a) Find the boron concentration at the silicon–silicon dioxide interface.

(b) Find the dose in silicon.

(c) Determine the junction depth if the background concentration is $3 \times 10^{15}/\text{cm}^3$.

5.2 A measured boron dose of $2 \times 10^{15}/\text{cm}^2$ is implanted into the surface of a silicon wafer at an energy of 10 keV. What are the projected depth and straggle based upon Fig. 5.3? What is the junction depth if the implantation resulted in a Gaussian profile and the background concentration of the wafer is $10^{16}/\text{cm}^3$?

5.3 What energy is required to implant phosphorus through a 1-μm layer of silicon dioxide if the peak of the implant is to be at the Si–SiO_2 interface? What is the straggle?

5.4 An arsenic dose of $1 \times 10^{12}/\text{cm}^2$ is implanted through a 50-nm layer of silicon dioxide with the peak of the distribution at the Si–SiO_2 interface. A silicon nitride film on top of the silicon dioxide is to be used as a barrier material in the regions where arsenic is not desired. How thick should the nitride layer be if the background concentration is $1 \times 10^{15}/\text{cm}^3$?

5.5 An implantation will be used for the predeposition step for a boron base diffusion. The final layer is to be 5 μm deep with a sheet resistance of 125 ohms per square ($N_B = 10^{16}/\text{cm}^3$).

(a) What is the dose required from the ion implanter if the boron will be implanted through a thin silicon dioxide layer so that the peak of the implanted distribution is at the silicon–silicon dioxide interface?

(b) What drive-in time is required to produce the final base layer at a temperature of 1100 °C?

5.6 Repeat Problem 5.5 for a 2-μm-deep diffusion with a sheet resistance of 200 ohms/square.

5.7 Repeat Problem 5.5 for a 0.25-μm-deep diffusion with a sheet resistance of 250 ohms/square.

5.8 A phosphorus dose of $1 \times 10^{15}/\text{cm}^2$ is implanted into the surface of a silicon wafer at an energy of 20 keV. What are the projected depth and straggle based upon Fig. 5.3? What is the junction depth if the implantation resulted in a Gaussian profile and the background concentration of the wafer is $10^{16}/\text{cm}^3$?

5.9 **(a)** Use Irvin's curves to find the sheet resistance of a boron layer implanted completely below the surface in *n*-type silicon ($N_B = 10^{15}/\text{cm}^3$). Assume the layer has a peak concentration of $1 \times 10^{19}/\text{cm}^3$, and the range and straggle are 1.0 μm and 0.11 μm, respectively. (Hint: Think about conductors in parallel.)

(b) What is the dose of this implantation?

(c) What was the energy used for this ion implantation?

(d) At what depths are *pn* junctions located?

5.10 **(a)** Photoresist is used as an implantation barrier during a boron source/drain implantation at 50 keV. How thick a layer of photoresist should be utilized to block the implant?

(b) Repeat the process for a phosphorus implant.

(c) Repeat it for an arsenic implant.

5.11 What are the velocities of the following ions in an ion implanter if they are accelerated through a potential of 5 keV (a) B^+ ions? (b) $(BF_2)^{++}$ ions? (c) $(B_{10}H_{14})^+$ ions?

5.12 The source and drain regions of a self-aligned *n*-channel polysilicon-gate MOS transistor are to be formed using arsenic implantation. The dimensions of a cross section of the device are given in Fig. P5.12. Calculate the channel shrinkage caused by lateral straggle if the peak concentration of the implantation is $10^{20}/\text{cm}^3$ and the substrate doping is $10^{16}/\text{cm}^3$. Assume that the channel region is in the silicon immediately below the oxide. Use $R_p = 0.1$ μm, $\Delta R_p = 0.04$ μm, and $\Delta R_\perp = 0.022$ μm.

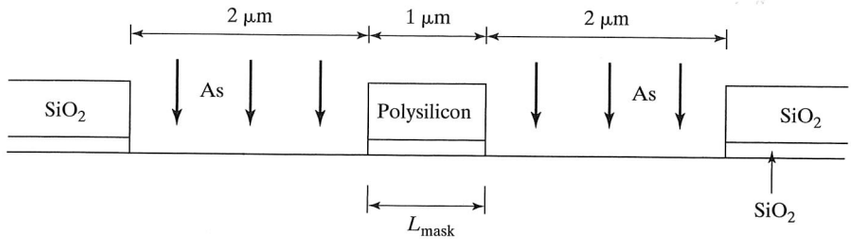


FIGURE 5.12

5.13 An implanted profile is formed by two boron implantations. The first uses an energy of 100 keV and the second an energy of 200 keV. The peak concentration of each distribution is $5 \times 10^{18}/cm^3$. Draw a graph of the composite profile and find the junction depth(s) if the phosphorus background concentration is $10^{16}/cm^3$. What are the doses of the two implant steps?

5.14 A high-energy (5 MeV) is used to implant oxygen deep below the silicon surface in order to form a buried SiO_2 layer. Assume that the desired SiO_2 layer is to be 0.2 μm wide.

(a) What is the oxygen dose required to be implanted in silicon?

(b) What beam current is required if a 200-mm-diameter wafer is to be implanted in 15 min?

(c) How much power is being supplied to the ion beam? Discuss what effects this implantation may have on the wafer.

5.15 The threshold voltage of an NMOS transistor may be increased by ion implantation of boron into the channel region. For shallow implantations, the voltage shift is given approximately by $\Delta V_T = qQ/C_{ox}$, where Q is the boron dose and $C_{ox} = \varepsilon_0/X_0$. X_0 is the oxide thickness and ε_0 is the permittivity of silicon dioxide: $3.9 \times (8.854 \times 10^{-14}$ F/cm). What boron dose is required to shift the threshold by 0.75 V if the oxide thickness is 40 nm?

5.16 An ion implanter has a beam current of 10 μA. How long does it take to implant a boron dose of $10^{15}/cm^2$ into a wafer with a diameter of 200 mm?

5.17 Write a computer program to calculate the sheet resistance of an arbitrary Gaussian layer in silicon.

5.18 A boron dose of $1 \times 10^{15}/cm^2$ is implanted into a silicon wafer. (a)Use Fig. 5.9 to determine the maximum substrate temperature required to insure that an amorphous layer is formed so that solid-state epitaxy is possible. (b) What happens if the implanted species is changed to phosphorus?

5.19 An RTA system goes from 25 to 1050 °C at a rate of 50 °C/sec, and remains at 1050 °C for 1 minute. It then returns to 25 °C at a rate of 50 °C/sec. Numerically calculate the total Dt product for a boron diffusion using the data from Table 4.1 in Chapter 4. What is the Dt product considering only the time spent at 1050 °C?

5.20 Repeat Prob. 5.19 if the time at 1050 °C is reduced to 5 seconds.

5.21 An RTA system goes from 25 to 980 °C at a rate of 40 °C/sec and stays at 980 °C for 2 minutes. It then returns to 25 °C at a rate of 40 °C/sec. Numerically calculate the total Dt product for a phosphorus diffusion using the data from Table 4.1 in Chapter 4. What is the Dt product considering only the time spent at 980 °C?

5.22 Repeat Prob. 5.21 reducing the time at 980 °C to 15 seconds.

CHAPTER 6

Film Deposition

Fabrication processes involve many steps in which thin films of various materials are deposited on the surface of the wafer. This chapter presents a survey of deposition processes, including evaporation, chemical vapor deposition, and sputtering, which are used to deposit metals, silicon and polysilicon, and dielectrics such as silicon dioxide and silicon nitride. Evaporation and sputtering require vacuum systems operating at low pressure, whereas chemical vapor deposition and epitaxy can be performed at either reduced or atmospheric pressure. An overview of vacuum systems and some results from the theory of ideal gases are also presented in this chapter.

6.1 EVAPORATION

Physical evaporation is one of the oldest methods of depositing metal films. Aluminum and gold are heated to the point of vaporization, and then evaporate to form a thin film covering the surface of the silicon wafer. To control the composition of the deposited material, evaporation is performed under vacuum conditions.

Figure 6.1 shows a basic vacuum deposition system consisting of a vacuum chamber, a mechanical roughing pump, a diffusion pump or turbomolecular pump, valves, vacuum gauges, and other instrumentation. In operation, the roughing valve is opened first, and the mechanical pump lowers the vacuum chamber pressure to an intermediate vacuum level of approximately 1 Pascal (Pa[1]). If a higher vacuum level is needed, the roughing valve is closed, and the foreline and high-vacuum valves are opened. The roughing pump now maintains a vacuum on the output of the diffusion pump. A liquid-nitrogen (77 K) cold trap is used with the diffusion pump to reduce the pressure in the vacuum chamber to approximately 10^{-4} Pa. Ion and thermocouple gauges are used to monitor the pressure at a number of points in the vacuum system, and several other valves are used as vents to return the system to atmospheric pressure.

[1] 1 atm = 760 mm Hg = 760 torr = 1.013×10^5 Pa. 1 Pa = 1 N/m^2 = 0.0075 torr.