5.13 An implanted profile is formed by two boron implantations. The first uses an energy of 100 keV and the second an energy of 200 keV. The peak concentration of each distribution is $5 \times 10^{18}/cm^3$. Draw a graph of the composite profile and find the junction depth(s) if the phosphorus background concentration is $10^{16}/cm^3$. What are the doses of the two implant steps?

5.14 A high-energy (5 MeV) is used to implant oxygen deep below the silicon surface in order to form a buried SiO_2 layer. Assume that the desired SiO_2 layer is to be 0.2 μm wide.

(a) What is the oxygen dose required to be implanted in silicon?

(b) What beam current is required if a 200-mm-diameter wafer is to be implanted in 15 min?

(c) How much power is being supplied to the ion beam? Discuss what effects this implantation may have on the wafer.

5.15 The threshold voltage of an NMOS transistor may be increased by ion implantation of boron into the channel region. For shallow implantations, the voltage shift is given approximately by $\Delta V_T = qQ/C_{ox}$, where Q is the boron dose and $C_{ox} = \varepsilon_0/X_0$. X_0 is the oxide thickness and ε_0 is the permittivity of silicon dioxide: $3.9 \times (8.854 \times 10^{-14}$ F/cm). What boron dose is required to shift the threshold by 0.75 V if the oxide thickness is 40 nm?

5.16 An ion implanter has a beam current of 10 μA. How long does it take to implant a boron dose of $10^{15}/cm^2$ into a wafer with a diameter of 200 mm?

5.17 Write a computer program to calculate the sheet resistance of an arbitrary Gaussian layer in silicon.

5.18 A boron dose of $1 \times 10^{15}/cm^2$ is implanted into a silicon wafer. (a)Use Fig. 5.9 to determine the maximum substrate temperature required to insure that an amorphous layer is formed so that solid-state epitaxy is possible. (b) What happens if the implanted species is changed to phosphorus?

5.19 An RTA system goes from 25 to 1050 °C at a rate of 50 °C/sec, and remains at 1050 °C for 1 minute. It then returns to 25 °C at a rate of 50 °C/sec. Numerically calculate the total Dt product for a boron diffusion using the data from Table 4.1 in Chapter 4. What is the Dt product considering only the time spent at 1050 °C?

5.20 Repeat Prob. 5.19 if the time at 1050 °C is reduced to 5 seconds.

5.21 An RTA system goes from 25 to 980 °C at a rate of 40 °C/sec and stays at 980 °C for 2 minutes. It then returns to 25 °C at a rate of 40 °C/sec. Numerically calculate the total Dt product for a phosphorus diffusion using the data from Table 4.1 in Chapter 4. What is the Dt product considering only the time spent at 980 °C?

5.22 Repeat Prob. 5.21 reducing the time at 980 °C to 15 seconds.

CHAPTER 6

Film Deposition

Fabrication processes involve many steps in which thin films of various materials are deposited on the surface of the wafer. This chapter presents a survey of deposition processes, including evaporation, chemical vapor deposition, and sputtering, which are used to deposit metals, silicon and polysilicon, and dielectrics such as silicon dioxide and silicon nitride. Evaporation and sputtering require vacuum systems operating at low pressure, whereas chemical vapor deposition and epitaxy can be performed at either reduced or atmospheric pressure. An overview of vacuum systems and some results from the theory of ideal gases are also presented in this chapter.

6.1 EVAPORATION

Physical evaporation is one of the oldest methods of depositing metal films. Aluminum and gold are heated to the point of vaporization, and then evaporate to form a thin film covering the surface of the silicon wafer. To control the composition of the deposited material, evaporation is performed under vacuum conditions.

Figure 6.1 shows a basic vacuum deposition system consisting of a vacuum chamber, a mechanical roughing pump, a diffusion pump or turbomolecular pump, valves, vacuum gauges, and other instrumentation. In operation, the roughing valve is opened first, and the mechanical pump lowers the vacuum chamber pressure to an intermediate vacuum level of approximately 1 Pascal (Pa[1]). If a higher vacuum level is needed, the roughing valve is closed, and the foreline and high-vacuum valves are opened. The roughing pump now maintains a vacuum on the output of the diffusion pump. A liquid-nitrogen (77 K) cold trap is used with the diffusion pump to reduce the pressure in the vacuum chamber to approximately 10^{-4} Pa. Ion and thermocouple gauges are used to monitor the pressure at a number of points in the vacuum system, and several other valves are used as vents to return the system to atmospheric pressure.

[1] 1 atm = 760 mm Hg = 760 torr = 1.013×10^5 Pa. 1 Pa = 1 N/m^2 = 0.0075 torr.

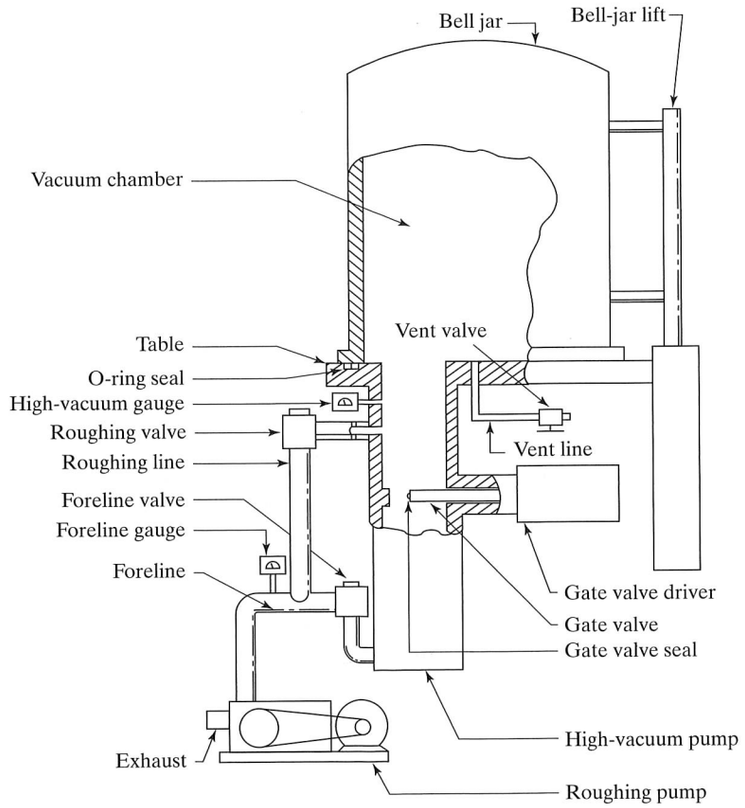

FIGURE 6.1

Typical vacuum system used for evaporation including vacuum chamber, roughing pump, high-vacuum pump, and various valves and vacuum gauges. Copyright 1987 McGraw-Hill Book Company. Reprinted with permission from Ref. [5].

6.1.1 Kinetic Gas Theory

Gases behave in an almost ideal manner at low pressure and are well described by the ideal gas law. Pressure P, volume V, and temperature T of one mole of a gas are related by

$$PV = N_{av}kT \tag{6.1}$$

where k is Boltzmann's constant [2] and N_{av} is Avogadro's number (6.02×10^{23} molecules/mole). The concentration of gas molecules is given by

$$n = \frac{N_{av}}{V} = \frac{P}{kT} \tag{6.2}$$

In some systems, the surface of the substrate must be kept extremely clean prior to deposition. The presence of even a small amount of oxygen or other elements will result in formation of a contamination layer on the surface of the substrate. The rate Φ

[2] k (Boltzmann's constant) $= 1.38 \times 10^{-23}$ J/K $= 1.37 \times 10^{-22}$ atm-cm^3/K.

of formation of this layer is determined from the impingement rate of gas molecules hitting the substrate surface and is related to the pressure by

$$\Phi = \frac{P}{\sqrt{2\pi mkT}} \text{ (molecules/cm}^2\text{-sec)} \tag{6.3}$$

where m is the mass of the molecule. This can be reduced to

$$\Phi = \frac{2.63 \times 10^{20} P}{\sqrt{MT}} \text{ (molecules/cm}^2\text{-sec)} \tag{6.4}$$

where P is the pressure in Pa and M is the molecular weight (e.g., $M = 32$ for oxygen molecules). If we assume that each molecule sticks as it contacts the surface, then the time required to form a monolayer on the surface is given by

$$t = \frac{N_s}{\Phi} = \frac{N_s\sqrt{2\pi mkT}}{P} \tag{6.5}$$

where N_s is the number of molecules/cm^2 in the layer.

Example 6.2

Suppose the residual pressure of oxygen in the vacuum system is 1 Pa. How long does it take to deposit one atomic layer of oxygen on the surface of the wafer at 300 K?

Solution: The radius of an oxygen molecule is approximately 3.6 Å. If we assume close packing of the molecules on the surface, there will be approximately 2.2×10^{14} molecules/cm^2. At 300 K and 1 Pa, the impingement rate for oxygen is 2.7×10^{18} molecules/cm^2-sec. One monolayer is deposited in 82 μ sec (a very short period).

Pressure and temperature also determine another important film-deposition parameter called the *mean free path*, λ. The mean free path of a gas molecule is the average distance the molecule travels before it collides with another molecule. λ is given by

$$\lambda = \frac{kT}{\sqrt{2}\pi pd^2} \tag{6.6}$$

where d is the diameter of the gas molecule and is in the range of 2 to 5 Å. Evaporation is usually done at a background pressure near 10^{-4} Pa. At this pressure, a 4-Å molecule has a mean free path of approximately 60 m. Thus, during aluminum evaporation, for example, aluminum molecules do not interact with the background gases and tend to travel in a straight line from the evaporation source to the deposition target.

On the other hand, sputtering, which will be discussed in Section 6.4, uses argon gas at a pressure of approximately 100 Pa, using the same radius results in a mean free path of only 60 μm. Thus, the material being deposited tends to scatter often with the argon atoms and arrives at the target from random directions.

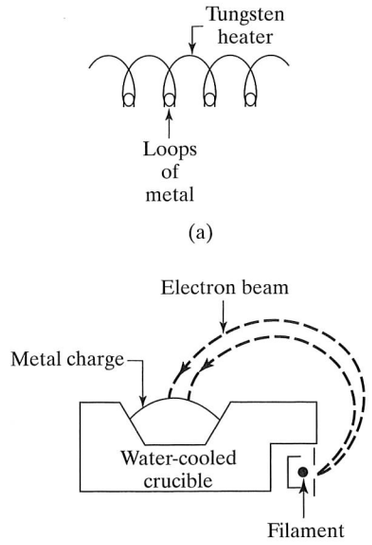

FIGURE 6.2

Two forms of evaporation sources. (a) Filament evaporation, in which loops of wire hang from a heated filament; (b) electron-beam source in which a beam of electrons is focused on a metal charge. The beam is bent in a magnetic field.

6.1.2 Filament Evaporation

The simplest evaporator consists of a vacuum system containing a filament that can be heated to high temperature. In Fig. 6.2(a), small loops of a metal such as aluminum are hung from a filament formed of a refractory (high-temperature) metal such as tungsten. Evaporation is accomplished by gradually increasing the temperature of the filament until the aluminum melts and wets the filament. Filament temperature is then raised to evaporate the aluminum from the filament. The wafers are mounted near the filament and are covered by a thin film of the evaporating material.

Although filament evaporation systems are easy to set up, contamination levels can be high, particularly from the filament material. In addition, evaporation of composite materials cannot be easily controlled using a filament evaporator. The material with the lowest melting point tends to evaporate first, and the deposited film will not have the same composition as the source material. Thick films are difficult to achieve, since a limited supply of material is contained in the metal loops.

6.1.3 Electron-Beam Evaporation

In electron-beam (E-beam) evaporation systems (see Fig. 6.2(b)), the high-temperature filament is replaced with an electron beam. A high-intensity beam of electrons, with an energy up to 15 keV, is focused on a source target containing the material to be evaporated. The energy from the electron beam melts a region of the target. Material evaporates from the source and covers the silicon wafers with a thin layer.

The growth rate using a small planar source is given by

$$G = \frac{m}{\pi\rho r^2}\cos\phi\cos\theta(\text{cm/sec}) \tag{6.7}$$

for the geometrical setup in Fig. 6.3. ϕ is the angle measured from the normal to the

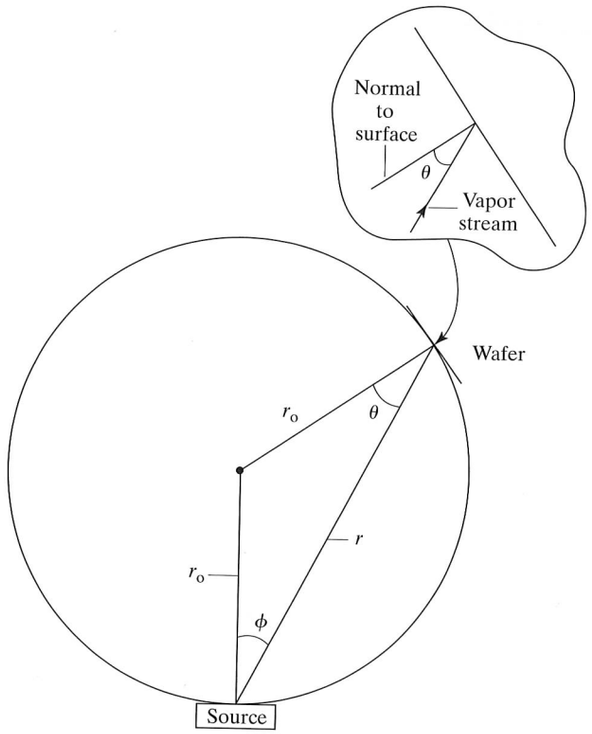

FIGURE 6.3

Geometry for evaporation in a system using a planetary substrate holder.

plane of the source, and θ is the angle of the substrate relative to the vapor stream. ρ and m are the density (g/cm^3) and mass evaporation rate (g/sec), respectively, of the material being deposited.

For batch deposition, a planetary substrate holder (Fig. 6.4) consisting of rotating sections of a sphere is used. Each substrate is positioned tangential to the surface of the sphere with radius r_o, as in Fig. 6.3. Applying some geometry yields

$$\cos\theta = \cos\phi = \frac{r}{2r_o} \tag{6.8}$$

For the planetary substrate holder, G becomes independent of substrate position:

$$G = \frac{m}{4\pi\rho r_o^2} \tag{6.9}$$

The wafers are mounted above the source and are typically rotated around the source during deposition to ensure uniform coverage. The wafers are also often radiantly heated to improve adhesion and uniformity of the evaporated material. The source material sits in a water-cooled crucible, and its surface only comes in contact with the electron beam during the evaporation process. Purity is controlled by the purity of the original source material. The relatively large size of the source provides a virtually unlimited supply of material for evaporation, and the deposition rate is easily controlled by changing the current and energy of the electron beam.

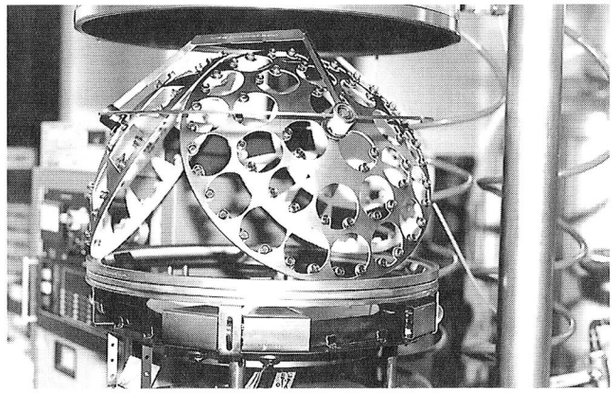

FIGURE 6.4

Photograph of a laboratory E-beam evaporation system with a planetary substrate holder which rotates simultaneously around two axes.

One method of monitoring the deposition rate uses a quartz crystal, which is covered by the evaporating material during deposition. The resonant frequency of the crystal shifts in proportion to the thickness of the deposited film. By monitoring the resonant frequency of the crystal, the deposition rate may be measured with an accuracy of better than 1 Å/sec. Dual electron beams with dual targets may be used to coevaporate composite materials in E-beam evaporation systems.

X-ray radiation can be generated in an electron-beam system for acceleration voltages exceeding 5 to 10 keV, and substrates may suffer some radiation damage from both energetic electrons and X-rays. The damage can usually be annealed out during subsequent process steps. However, the radiation effects are of great concern to MOS process designers, and sputtering has replaced electron-beam evaporation in many steps in manufacturing processes.

6.1.4 Flash Evaporation

Flash evaporation uses a fine wire as the source material, and a high-temperature ceramic bar is used to evaporate the wire. The wire is fed continuously and evaporates on contact with the ceramic bar. Flash evaporation can produce relatively thick films, as in an E-beam system, without problems associated with radiation damage.

6.1.5 Shadowing and Step Coverage

Because of the large mean free paths of gas molecules at low pressure, evaporation techniques tend to be directional in nature, and shadowing of patterns and poor step coverage can occur during deposition. Figure 6.5 illustrates the shadowing phenomenon that can occur with closely spaced features on the surface of an integrated circuit. In the fully shadowed region, there will be little deposition. In the partially shadowed region, there will be variation in film thickness. To minimize these effects, the planetary substrate holder of the electron-beam system continuously rotates the wafers during the film deposition.

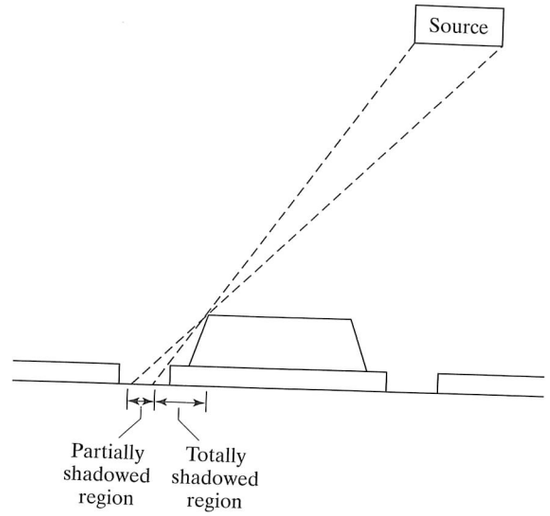

FIGURE 6.5

An example of the shadowing problem that can occur during low-pressure vacuum deposition in which the molecular mean free path is large.

6.2 SPUTTERING

Sputtering is achieved by bombarding a target with energetic ions, typically Ar^+. Atoms at the surface of the target are knocked loose and transported to the substrate, where deposition occurs. Electrically conductive materials such as Al, W, and Ti can use a dc power source, in which the target acts as the cathode in a diode system. Sputtering of dielectrics such as silicon dioxide or aluminum oxide requires an RF power source to supply energy to the argon atoms. A diagram of a sputtering system is shown in Fig. 6.6.

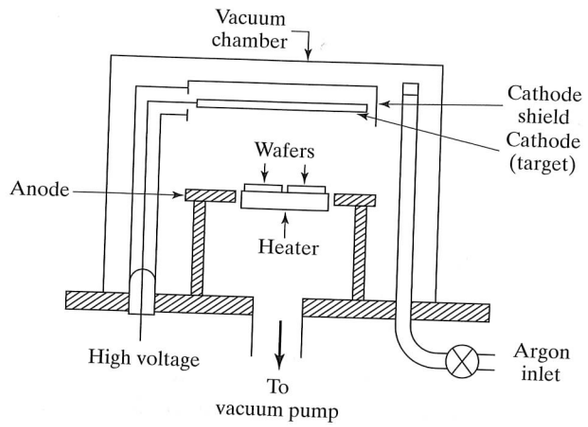

FIGURE 6.6

A dc sputtering system in which the target material acts as the cathode of a diode and the wafers are mounted on the system anode.

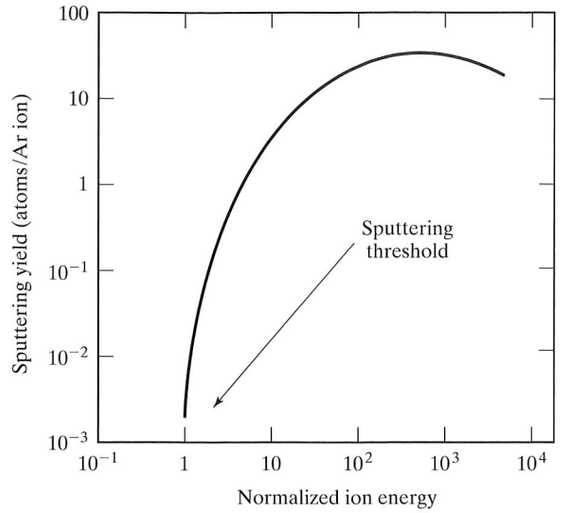

FIGURE 6.7

Sputtering yield versus ion energy for a dc sputtering system using argon.

In sputter deposition, there is a threshold energy that must be exceeded before sputtering occurs. The sputtering yield (Fig. 6.7) represents the number of atoms liberated from the target by each incident atom, and it increases rapidly with energy of the incident ions. Systems are usually operated with an energy large enough to ensure a sputtering yield of at least unity.

Sputtering can be used to deposit a broad range of materials. In addition, alloys may be deposited in which the deposited film has the same composition as the target. An example is the Al–Cu–Si alloy commonly used for metallization in integrated circuits. (We will discuss this alloy in Chapter 7.) As one might expect, sputtering results in the incorporation of some argon into the film, and heating of the substrate up to 350 °C can occur during the deposition process. Sputtering provides excellent coverage of the sharp topologies often encountered in integrated circuits.

Sputter etching (a reversal of the sputter deposition process) can be used to clean the substrate prior to film deposition, and the sputter etching process is often used to clean contact windows prior to metal deposition. Etching removes any residual oxide from the window and improves the contact between the metal and the underlying material.

6.3 CHEMICAL VAPOR DEPOSITION

Chemical vapor deposition (CVD) forms thin films on the surface of a substrate by thermal decomposition or reaction of gaseous compounds. The desired material is deposited directly from the gas phase onto the surface of the substrate. Polysilicon, silicon dioxide, and silicon nitride are routinely deposited using CVD techniques. In addition, refractory metals such as tungsten (W) can also be deposited using CVD.

Chemical vapor deposition can be performed at pressures for which the mean free path for gas molecules is quite small, and the use of relatively high temperatures can result in excellent conformal step coverage over a broad range of topological profiles.

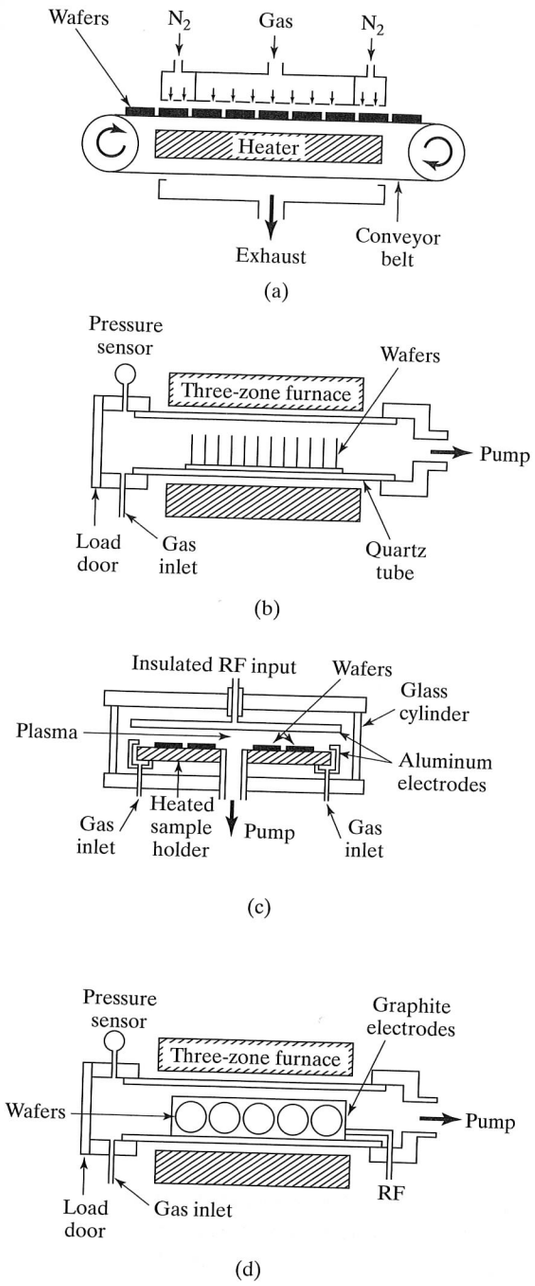

FIGURE 6.8

Four types of chemical vapor deposition (CVD) systems. (a) Atmospheric-pressure reactor; (b) hot-wall LPCVD system using a three-zone furnace tube; (c) parallel-plate plasma-enhanced CVD system; (d) PECVD system using a three-zone furnace tube. Copyright 1983 Bell Telephone Laboratories, Inc. Reprinted by permission from Ref. [2].

6.3.1 CVD Reactors

Several different types of CVD reactor systems are shown in Fig. 6.8. In Fig. 6.8(a), a continuous atmospheric-pressure (APCVD) reactor is shown. This type of reactor has been used for deposition of the silicon dioxide passivation layer as one of the last steps

in IC processing. The reactant gases flow through the center section of the reactor and are contained by nitrogen curtains at the ends. The substrates can be fed continuously through the system, and large-diameter wafers are easily handled. However, high gas-flow rates are required by the atmospheric-pressure reactor.

The hot-wall, low-pressure system of Fig. 6.8(b) is commonly used to deposit polysilicon, silicon dioxide, and silicon nitride and is referred to as a low-pressure CVD (LPCVD) system. The reactant gases are introduced into one end of a three-zone furnace tube and are pumped out the other end. Temperatures range from 300 to 1150 °C, and the pressure is typically 30 to 250 Pa. Excellent uniformity can be obtained with LPCVD systems, and several hundred wafers may be processed in a single run. Hot-wall systems have the disadvantage that the deposited film simultaneously coats the inside of the tube. The tube must be periodically cleaned or replaced to minimize problems with particulate matter. In spite of this problem, hot-wall LPCVD systems are in widespread use throughout the semiconductor industry. Vertical furnaces similar to that depicted in Fig. 3.11(b) are also utilized for chemical vapor deposition.

CVD reactions can also take place in a plasma reactor, as shown in Fig. 6.8(c). Formation of the plasma permits the reaction to take place at low temperatures, which is a primary advantage of plasma-enhanced CVD (PECVD) processes. In the parallel-plate system, the wafers lie on a grounded aluminum plate, which serves as the bottom electrode for establishing the plasma. The wafers can be heated up to 400 °C using high-intensity lamps or resistance heaters. The top electrode is a second aluminum plate placed in close proximity to the wafer surface. Gases are introduced along the outside of the system, flow radially across the wafers, and are pumped through an exhaust in the center. An RF signal is applied to the top plate to establish the plasma. The capacity of this type of system is limited, and wafers must be loaded manually. A major problem in VLSI fabrication is particulate matter that may fall from the upper plate onto the wafers.

The furnace–plasma system in Fig. 6.8(d) can handle a large number of wafers at one time. A special electrode assembly holds the wafers parallel to the gas flow. The plasma is established between alternating groups of electrodes supporting the wafers.

Optical excitation, usually with laser sources, can also be used to assist or replace the thermal energy required for CVD reactions, and this form of processing is referred to as photon-enhanced chemical vapor deposition.

6.3.2 Polysilicon Deposition

Silicon is deposited in an LPCVD system using thermal decomposition of silane:

$$SiH_4 \xrightarrow{600°C} Si + 2H_2 \tag{6.10}$$

Low-pressure systems (25 to 150 Pa) use either 100% silane or 20 to 30% silane diluted with nitrogen. A temperature between 600 and 650 °C results in deposition of polysilicon material at a rate of 100 to 200 Å/min. A less commonly used deposition occurs between 850 and 1050 °C in a hydrogen atmosphere. The higher temperature overcomes a reduction in deposition rate caused by the hydrogen carrier gas.

Polysilicon can be doped by diffusion or ion implantation or during deposition (in situ) by the addition of dopant gases such as phosphine, arsine, or diborane. The addition of diborane greatly increases the deposition rate, whereas the addition of phosphine or arsine substantially reduces the deposition rate.

Polysilicon is often deposited as undoped material and is then doped by diffusion. High-temperature diffusion occurs much more rapidly in polysilicon than in single-crystal silicon, and the polysilicon film is typically saturated with the dopant to achieve as low a resistivity as possible for interconnection purposes. Resistivities of 0.01 to 0.001 ohm-cm can be achieved in diffusion-doped polysilicon. Ion implantation typically yields a lower active-impurity density in the polysilicon film, and ion-implanted polysilicon exhibits a resistivity about 10 times higher than that achieved by high-temperature diffusion.

6.3.3 Silicon Dioxide Deposition

Silicon dioxide films can be deposited using a variety of reactions and temperature ranges, and the films can be doped or undoped. Phosphorus-doped oxide can be used as a passivation layer over a completed integrated circuit or as the insulating medium in multilevel metal processes (which will be discussed in the next chapter). Silicon dioxide containing 6 to 8% phosphorus by weight will soften and flow at temperatures between 1000 and 1100 °C. This "P-glass reflow" process can be used to improve step coverage and provide a smoother topography for later process steps. SiO_2 with lower concentrations of phosphorus will not reflow properly, and higher concentrations can corrode aluminum if moisture is present. Oxide doped with 5 to 15% by weight of various dopants can also be used as a diffusion source.

Deposition of silicon dioxide over aluminum must occur at a temperature below the silicon-aluminum eutectic point of 577 °C. (See Chapter 7.) A reaction between silane and oxygen between 300 and 500 °C is commonly used to deposit SiO_2:

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2 \tag{6.11}$$

The oxide may be doped with phosphorus using phosphine:

$$4PH_3 + 5O_2 \rightarrow 2P_2O_5 + 6H_2 \tag{6.12}$$

Oxide passivation layers can be deposited at atmospheric pressure using the continuous reactor of Fig. 6.8(a), or they can be deposited at reduced pressure in an LPCVD system, as in Fig. 6.8(b).

Deposition of SiO_2 films prior to metallization can be performed at higher temperatures, which gives a wider choice of reactions and results in better uniformity and step coverage. For example, a dichlorosilane reaction with nitrous oxide in an LPCVD system at approximately 900 °C,

$$SiCl_2H_2 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2HCl \tag{6.13}$$

can be used to deposit insulating layers of SiO_2 on wafer surfaces.

Decomposition of the vapor produced from a liquid source, tetraethylorthosilicate (TEOS), can also be used in an LPCVD system between 650 and 750 °C:

$$Si(OC_2H_5)_4 \rightarrow SiO_2 + \text{byproducts} \tag{6.14}$$

Deposition based on the decomposition of TEOS provides excellent uniformity and step coverage. Oxide doping may be accomplished in the LPCVD systems by adding phosphine, arsine, or diborane.

A comparison of some of the properties of various CVD oxides is given in Table 6.1.

6.3.4 Silicon Nitride Deposition

As discussed in Chapter 3, silicon nitride is used as an oxidation mask in recessed oxide processes. Silicon nitride is also used as a final passivation layer, because it provides an excellent barrier to both moisture and sodium contamination. Composite films of oxide and nitride are being investigated for use as very thin gate insulators in scaled VLSI devices, and they are also used as the gate dielectric in electrically programmable memory devices.

Both silane and dichlorosilane will react with ammonia to produce silicon nitride. The silane reaction occurs between 700 and 900 °C at atmospheric pressure:

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2 \tag{6.15}$$

Dichlorosilane is used in an LPCVD system between 700 and 800 °C:

$$3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2 \tag{6.16}$$

Thermal growth of silicon nitride is possible, but not very practical. Silicon nitride will form when silicon is exposed to ammonia at temperatures between 1000 and 1100 °C, but the growth rate is very low.

Plasma systems may be used for the deposition of silicon nitride. Silane will react with a nitrogen discharge to form plasma nitride (SiN):

$$2SiH_4 + N_2 \rightarrow 2SiNH + 3H_2 \tag{6.17}$$

Silane will also react with ammonia in an argon plasma:

$$SiH_4 + NH_3 \rightarrow SiNH + 3H_2 \tag{6.18}$$

LPCVD films are hydrogen-rich, containing up to 8% hydrogen. Plasma deposition does not produce stoichiometric silicon nitride films. Instead, the films contain as much as 20 to 25% hydrogen. LPCVD films have high internal tensile stresses, and

TABLE 6.1 Properties of Various Deposited Oxides (After Ref. [2])

Source	Deposition Temperature (°C)	Composition	Conformal Step Coverage	Dielectric Strength (MV/cm)	Etch Rate (Å/min) [100:1 H_2O:HF]
Silane	450	$SiO_2(H)$	No	8	60
Dichlorosilane	900	$SiO_2(Cl)$	Yes	10	30
TEOS	700	SiO_2	Yes	10	30
Plasma	200	$SiO_{1.9}(H)$	No	5	400

films thicker than 2000 Å may crack because of this stress. On the other hand, plasma-deposited films have much lower tensile stresses.

The resistivity (10^{16} ohm-cm) and dielectric strength (10 MV/cm) of the LPCVD nitride films are better than those of most plasma films. Resistivity of plasma nitride can range from 10^6 to 10^{15} ohm-cm, depending on the amount of nitrogen in the film, while the dielectric strength ranges between 1 and 5 MV/cm.

6.3.5 CVD Metal Deposition

Many metals can be deposited by CVD processes. Molybdenum (Mo), tantalum (Ta), titanium (Ti), and tungsten (W) are all of interest in today's processes, because of their low resistivity and their ability to form silicides with silicon. (See Chapter 7.) Aluminum can be deposited from a metallorganic compound such as tri-isobutyl aluminum, but this technique has not been commonly used because many other excellent methods of aluminum deposition are available. Advanced metallization systems employ copper, and researchers are actively exploring CVD processes for copper deposition. However, at this writing, CVD copper processes suitable for use in manufacturing have not been developed, and copper is still deposited by standard electro- and electrolus plating techniques similar to those utilized to produce printed circuit boards.

Tungsten can be deposited by thermal, plasma, or optically assisted decomposition of WF_6:

$$WF_6 \rightarrow W + 3F_2 \tag{6.19}$$

or through reduction with hydrogen:

$$WF_6 + 3H_2 \rightarrow W + 6HF \tag{6.20}$$

Mo, Ta, and Ti can be deposited in an LPCVD system through reaction with hydrogen. The reaction is the same for all three metals:

$$2MCl_5 + 5H_2 \rightarrow 2M + 10HCl \tag{6.21}$$

Here M stands for any one of the three metals previously mentioned.

6.4 EPITAXY

CVD processes can be used to deposit silicon onto the surface of a silicon wafer. Under appropriate conditions, the silicon wafer acts as a seed crystal, and a single-crystal silicon layer is grown on the surface of the wafer. The growth of a crystalline silicon layer from the vapor phase is called *vapor-phase epitaxy* (VPE), and it is the most common form of epitaxy used in silicon processing. In addition, *liquid-phase epitaxy* (LPE) and *molecular-beam epitaxy* (MBE) are being used widely in compound semiconductor technology.

Epitaxial growth was first used in IC processing to grow single-crystal *n*-type layers on *p*-type substrates for use in standard buried-collector bipolar processing. More recently, it has been introduced into CMOS VLSI processes where lightly doped layers are grown on heavily doped substrates of the same type (*n* on n^+ or *p* on p^+) to help suppress a circuit-failure mode called *latchup*.

6.4.1 VPE

Silicon epitaxial layers are commonly grown with silicon deposited from the gas phase. A basic model for the process is given in Fig. 6.9. At the silicon surface, the flux J_s of gas molecules is determined by

$$J_s = k_s N_s \tag{6.22}$$

where k_s is the surface-reaction rate constant and N_s is the surface concentration of the molecule involved in the reaction. In the steady state, this flux must equal the flux J_g of molecules diffusing in from the gas stream. The flux J_g may be approximated by

$$J_g = (\overline{D_g}/\delta)(N_g - N_s) = h_g(N_g - N_s) \tag{6.23}$$

where $\overline{D}$ is an effective diffusion constant for the gas molecule and δ is the distance over which the diffusion is taking place. The ratio D_g/δ is called the *vapor-phase mass-transfer coefficient*, h_g. Equating J_s and J_g yields the flux impinging on the surface of the wafer. The growth rate v is equal to the flux divided by the number N of molecules incorporated per unit volume of film:

$$v = \frac{J_s}{N} = \frac{k_s h_g}{k_s + h_g}\frac{N_g}{N} \tag{6.24}$$

If $k_s \gg h_g$, then growth is said to be mass-transfer-limited, and

$$v = h_g \frac{N_g}{N} \tag{6.25}$$

If $h_g \gg k_s$, then growth is said to be surface-reaction-limited, and

$$v = k_s \frac{N_g}{N} \tag{6.26}$$

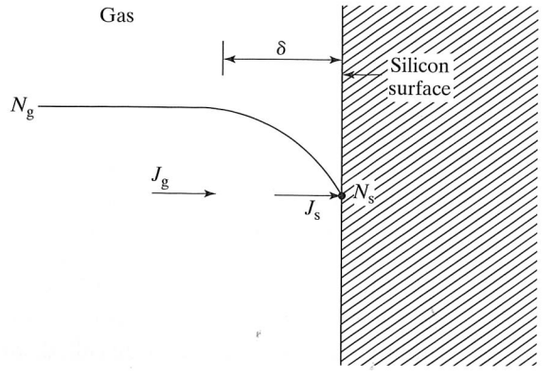

FIGURE 6.9
Model for the epitaxial growth process.

Figure 6.10 shows epitaxial growth rate as a function of temperature. Chemical reactions at the surface tend to follow an Arrhenius relationship characterized by an activation energy E_A, whereas the mass-transfer process tends to be independent of temperature. These two regions show up clearly in this figure. At low temperatures, the growth rate follows an Arrhenius relationship with an activation energy of approximately 1.5 eV. At higher temperatures, the growth rate becomes independent of temperature. To have good growth-rate control and to minimize sensitivity to variations in temperature, epitaxial growth conditions are usually chosen to yield a mass-transfer-limited growth rate.

Three common types of VPE reactors, the horizontal, pancake, and barrel systems, are shown in Fig. 6.11. The susceptor that supports the wafers is made of graphite and is heated by RF induction in the horizontal and vertical reactors and by radiant heating in the barrel reactor.

Silicon tetrachloride ($SiCl_4$), silane (SiH_4), dichlorosilane (SiH_2Cl_2), and trichlorosilane ($SiHCl_3$) have all been used for silicon VPE. Silicon tetrachloride has been widely used in industrial processing:

$$SiCl_4(\text{gas}) + 2H_2(\text{gas}) \leftrightarrow Si(\text{solid}) + 4HCl(\text{gas}) \tag{6.27}$$

This reaction takes place at approximately 1200 °C and is reversible. If the carrier gas coming into the reactor contains hydrochloric acid, etching of the surface of the silicon wafer can occur. This in-situ etching process can be used to clean the wafer prior to the start of epitaxial deposition.

A second reaction competes with the epitaxial deposition process:

$$SiCl_4(\text{gas}) + Si(\text{solid}) \leftrightarrow 2SiCl_2(\text{gas}) \tag{6.28}$$

This second reaction also etches the silicon from the wafer surface. If the concentration of $SiCl_4$ is too high, etching of the wafer surface will take place rather than epitaxial

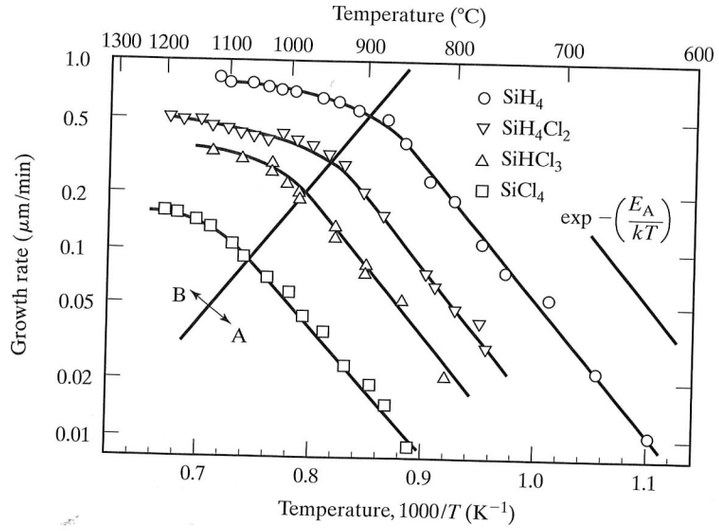

FIGURE 6.10
Temperature dependence of the silicon epitaxial growth process for four different sources. The growth rate is surface-reaction-limited in region A and is mass-transfer-limited in region B. Reprinted with permission from Philips Journal of Research from Ref. [3].

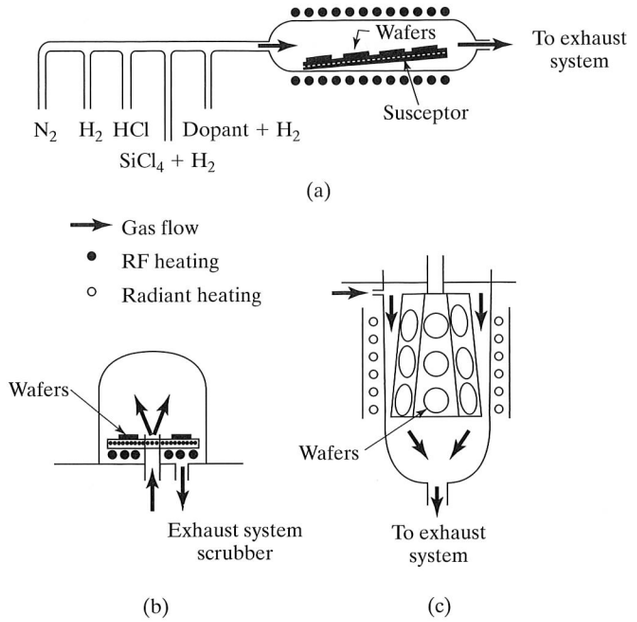

FIGURE 6.11

(a) Horizontal, (b) pancake, and (c) barrel susceptors commonly used for vapor-phase epitaxy. Copyright 1985 John Wiley & Sons, Inc. Reprinted with permission from Ref. [1].

deposition. Figure 6.12 shows the effect of $SiCl_4$ concentration on the growth of epitaxial silicon. The growth rate initially increases with increasing $SiCl_4$ concentration, peaks, and then decreases. Eventually, growth stops and the etching process becomes dominant. If the growth rate is too high, a polysilicon layer is deposited, rather than a layer of single-crystal silicon.

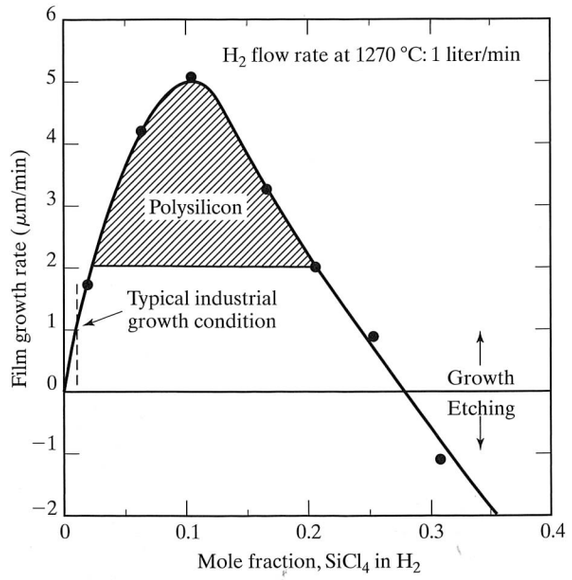

FIGURE 6.12

Silicon epitaxial growth rate as a function of $SiCl_4$ concentration. Polysilicon deposition occurs for growth rates exceeding 2 μm/min. Etching of the surface will occur for mole fraction concentrations exceeding 28%. Copyright 1985 John Wiley & Sons, Inc. Reprinted with permission from Ref. [1].

Epitaxial growth can also be achieved by the pyrolytic decomposition of silane:

$$SiH_4 \xrightarrow{650°C} Si + 2H_2 \tag{6.29}$$

The reaction is not reversible and takes place at low temperatures. In addition, it avoids the formation of HCl gas as a reaction by-product. However, careful control of the reactor is needed to prevent formation of polysilicon rather than single-crystal silicon layers. The presence of any oxidizing species in the reactor can also lead to contamination of the epitaxial layer by silica dust.

6.4.2 Doping of Epitaxial Layers

Epitaxial layers may be doped during the growth process by adding impurities to the gas used for deposition. Arsine, diborane, and phosphine are the most convenient sources of the common impurities. The resistivity of the epitaxial layer is controlled by varying the partial pressure of the dopant species in the gas supplied to the reactor. The addition of arsine or phosphine tends to slow down the rate of epitaxial growth, while the addition of diborane tends to enhance the epitaxial growth rate.

Lightly doped epitaxial layers are often grown on more heavily doped substrates, and autodoping of the epitaxial layer can occur during growth. Impurities can evaporate from the wafer or may be liberated by chlorine etching of the surface during deposition. The impurities are incorporated into the gas stream, resulting in doping of the growing layer. As the epitaxial layer grows, less dopant is released from the wafer into the gas stream, and the impurity profile eventually reaches a constant level determined by the doping in the gas stream.

During deposition, the substrate also acts as a source of impurities which diffuse into the epitaxial layer. This out-diffusion will be discussed more fully in the next section. Both autodoping and out-diffusion cause the transition from the doping level of the substrate to that of the epitaxial layer to be less abrupt than desired. The effects of autodoping and out-diffusion are illustrated in Fig. 6.13.

6.4.3 Buried Layers

Out-diffusion is a common problem that occurs with the buried layer in bipolar transistors. In order to reduce the resistance in series with the collector of the bipolar transistor, heavily doped *n*-type regions are diffused into the substrate prior to the growth of an *n*-type epitaxial layer. During epitaxy, impurities diffuse upward from the heavily doped buried-layer regions.

Diffusion of impurities from the substrate during epitaxial growth is modeled by the diffusion equation with a moving boundary [4], as in Fig. 6.14,

$$D\frac{\partial^2 N}{\partial x^2} = \frac{\partial N}{\partial t} + v_x\frac{\partial N}{\partial x} \tag{6.30}$$

where v_x is the rate of growth of the epitaxial layer.

Two specific solutions of Eq. (6.30) are applicable to epitaxial layer growth. The first case is the growth of an undoped epitaxial layer on a uniformly doped substrate.

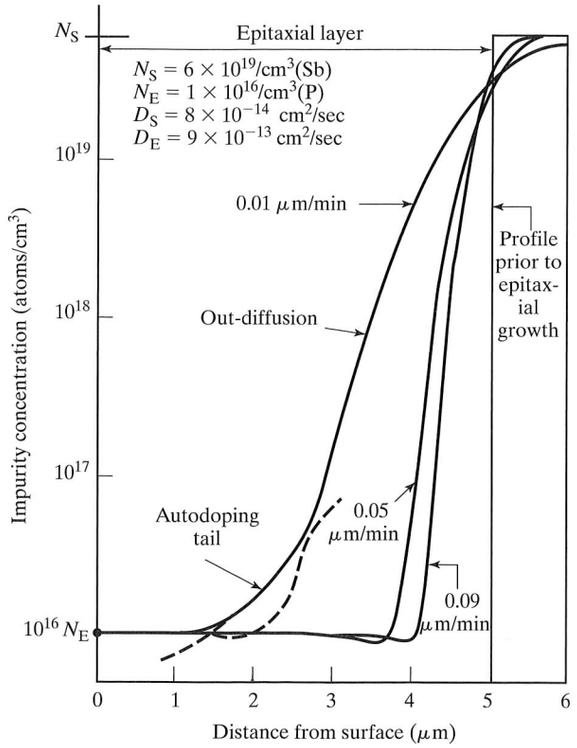

FIGURE 6.13

Redistribution of impurity atoms due to gas-phase autodoping and impurity out-diffusion during epitaxial layer growth. Out-diffusion is calculated using Eq. (6.33) for epitaxial growth of a phosphorus-doped layer at 1150 °C over an antimony-doped buried layer with a surface concentration of 6 x $10^{19}/cm^3$. The three curves are for growth rates of 0.01, 0.05, and 0.09 μm/min. For clarity, the effects of autodoping are shown on only one curve.

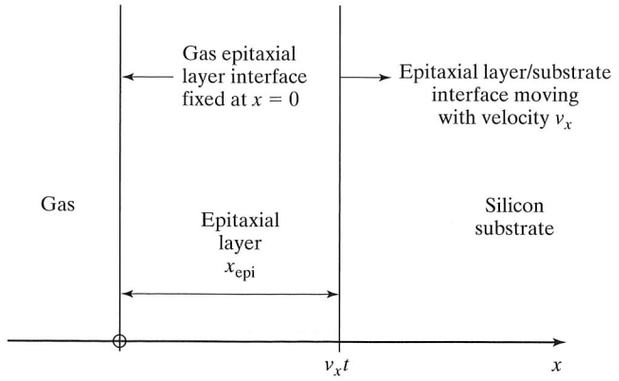

FIGURE 6.14

Geometrical model for the moving boundary value problem which describes the epitaxial growth process.

The boundary conditions are $N(x, 0) = N_s = N(\infty, t)$, and the flux $J_x = (h + v_x)N(0, t)$, where h is the mass-transfer coefficient, which characterizes the escape rate of dopant atoms from the silicon into the gas. Normally, $h \ll v_x$. A change of variables from x to $x' = x - v_x t$ simplifies Eq. (6.30) and gives an approximate solution for $N(x, t)$:

$$N_1(x,t) = \frac{N_s}{2}\left[1 + \text{erf}\frac{x - x_{epi}}{2\sqrt{D_s t}}\right] \tag{6.31}$$

Equation (6.31) assumes that the epitaxial layer growth rate greatly exceeds the rate of movement of the diffusion front. Equation (6.31) is the exact solution for diffusion from one semi-infinite layer into a second semi-infinite layer.

The second case is the growth of a doped epitaxial layer on an undoped substrate. The boundary conditions for this case are $N(0, t) = N_E$, and $N(\infty, t) = 0 = N(x, 0)$. The solution of Eq. (6.30) for these boundary conditions is:

$$N_2(x,t) = \frac{N_E}{2}\left[\text{erfc}\frac{x - x_{epi}}{2\sqrt{D_E t}} + \exp\frac{v_x x}{D_E}\,\text{erfc}\frac{x + x_{epi}}{2\sqrt{D_E t}}\right] \tag{6.32}$$

where $x_{epi} = v_x t$ is the epitaxial layer thickness. Superposition of the solutions for these two cases gives a good approximation to diffusion which occurs during epitaxial growth:

$$N(x,t) = N_1(x,t) + N_2(x,t). \tag{6.33}$$

N_S represents the doping in the substrate, and N_E is the doping intentionally introduced into the epitaxial layer. D_S and D_E represent the diffusion coefficients of the impurity species in the substrate and epitaxial layer, respectively. Figure 6.13 shows diffusion profiles for a phosphorus-doped epitaxial layer grown at various rates on an antimony-doped substrate. The curves were produced using Eq. (6.33).

An additional problem occurs during epitaxial growth. The oxidation and lithographic processing steps used during formation of a buried layer result in a step of as much as 0.2 μm around the perimeter of the buried layer. Epitaxial growth on this non-planar surface causes the pattern to shift during growth, as illustrated in Fig. 6.15. Pattern shift is difficult to predict, may be as large as the epitaxial layer thickness, and must be accounted for during the design of subsequent mask levels.

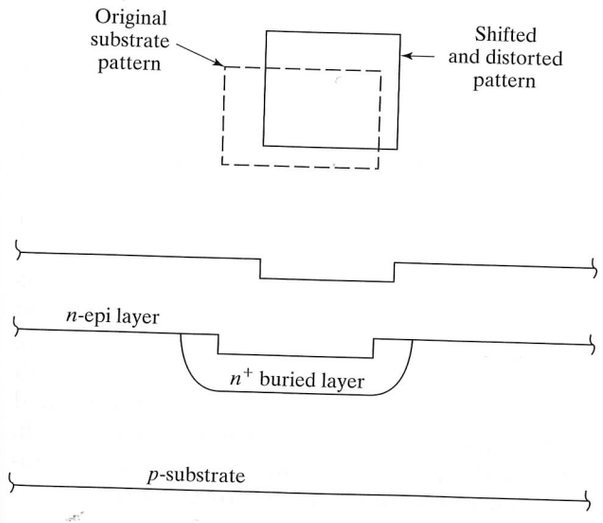

FIGURE 6.15

Pattern shift during epitaxial growth over an n^+ buried layer. The original pattern is shifted and distorted in shape.

6.4.4 Liquid-Phase and Molecular-Beam Epitaxy

In liquid-phase epitaxy, the substrate is brought into contact with a solution containing the material to be deposited in liquid form. The substrate acts as a seed for material crystallizing directly from the solute. Growth rates typically range between 0.1 and 1 μm/min.

In the molecular-beam epitaxy process, the crystalline layer is formed by deposition from a thermal beam of atoms or molecules. Deposition is performed in ultrahigh-vacuum conditions (10^{-8} Pa). Substrate temperatures during MBE range from 400 to 900 °C, and the growth rate is relatively low (0.001 to 0.3 μm/min). The epitaxial layer is grown atomic layer by atomic layer, and many unique device structures can be fabricated by changing the material which is deposited between one layer and the next.

The throughput of MBE is relatively low. Plasma-assisted CVD processes, which promise to give many of the benefits of MBE with much higher throughput, continue to be investigated in research laboratories.

SUMMARY

Thin films of a very broad range of materials are used in IC fabrication. This chapter has presented an overview of film-deposition techniques, including physical evaporation, chemical vapor deposition (CVD), epitaxial growth, and sputtering. Most of these processes are performed at low pressure, and this chapter has presented an introduction to vacuum systems and a review of some important aspects of ideal gas theory.

Physical evaporation using filament or electron-beam evaporators can be used to deposit metals and other materials that can easily be melted. E-beam systems can operate at high power levels and melt high-temperature metals. However, E-beam evaporation may result in radiation damage to thin oxide layers at the surface of the wafer. In addition, it is difficult to deposit material compounds and alloys using evaporation. Finally, gas molecules at low pressures have large mean free paths, and evaporation has problems with shadowing and poor step coverage during film deposition.

Sputtering uses energetic ions such as argon to bombard a target material and dislodge atoms from the surface of the target. The dislodged atoms are deposited on the surface of the wafer. Direct-current sputtering systems can be used to deposit conductive materials, and RF sputtering can be used to deposit insulators. Sputtering can be used to deposit composite materials in which the deposited film maintains the same composition as the source material. Sputtering also uses higher pressures than evaporation. The much shorter mean free paths that result yield a deposition with freedom from shadowing and much better step coverage.

Low-pressure and atmospheric chemical vapor deposition (CVD) systems deposit films from chemical reactions taking place in a gas stream passing over the wafer. Polysilicon, silicon dioxide, silicon nitride, and metals can all be deposited using CVD techniques. A special type of CVD deposition called epitaxy results in the growth of single-crystal silicon films on the surface of silicon wafers. Out-diffusion and autodoping cause problems with impurity profile control during epitaxial layer growth.

In a modern bipolar or MOS fabrication process, one can expect to find evaporation, sputtering, and CVD techniques all used somewhere in the process flow.

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PROBLEMS

6.1 A silicon wafer sits on a bench in the laboratory at a temperature of 300 K and a pressure of 1 atm. Assume that the air consists of 100% oxygen. How long does it take to deposit one atomic layer of oxygen on the wafer surface, assuming 100% adhesion?

6.2 Repeat Problem 6.1, but this time the wafer is kept in a nitrogen-purged cabinet in which the oxygen content is less than 0.1% of the total gas content.

6.3 Calculate the impingement rate and mean free path for oxygen molecules ($M = 32$) at 300 K and a pressure of 10^{-4} Pa. What is this pressure in torr?

6.4 An ultrahigh-vacuum system operates at a pressure of 10^{-8} Pa. What is the concentration of residual air molecules in the chamber at 300 K?

6.5 A high-vacuum system has a residual nitrogen concentration of 1000 molecules/cm^3. What is the gas pressure at 300K?

6.6 The partial pressure of a material being deposited in a vacuum system must be well above the residual background gas pressure if reasonable deposition rates are to be achieved. What must the partial pressure of aluminum be to achieve a deposition rate of 100 nm/min? Assume close packing of spheres with a diameter of 5 Å, 100% adhesion of the impinging aluminum, and a temperature of 300 K.

6.7 A wafer 100 mm in diameter is mounted in an electron-beam evaporation system in which the spherical radius is 40 cm. Use Eq. (6.7) to estimate the worst-case variation in film thickness between the center and edges of the wafer for an evaporated aluminum film 1 μm thick.

6.8 Repeat Problem 6.7 for a 200-mm wafer mounted 50 cm from the e-beam source.

6.9 Electron-beam evaporation is going to be used to deposit a 0.6-μm-thick layer of aluminum on a 300-mm-diameter wafer. The thickness variation between the center and edges of the wafer is desired to be less than 0.05 μm. How far should the wafer be from the source?

6.10 An MBE system must operate under ultrahigh-vacuum conditions to prevent the formation of undesired atomic layers on the surface of the substrate. What pressure of oxygen can be permitted at 300 K if formation of a monolayer of contamination can be permitted after the sample has been in the chamber for no less than 4 hr?

6.11 **(a)** Calculate the growth rate of a silicon layer from an $SiCl_4$ source at 1200 °C. Use $h_g =$ 1 cm/sec, $k_s = 2 \times 10^6 \exp(-1.9/kT)$ cm/sec, and $N_g = 3 \times 10^{16}$ atoms/cm^3. (For silicon, $N = 5 \times 10^{22}$/cm^3.)

(b) What is the change in growth rate if the temperature is increased by 25 °C?

(c) At what temperature does $k_s = h_g$? What is the growth rate at this temperature?

(d) What is the value of E_A in Fig. 6.10?

6.12 Use Eqs. (6.31) and (6.32) to model the case of a 10-μm *n*-type epitaxial layer ($N_E = 1 \times 10^{16}$/cm^3) grown on a *p*-type substrate ($N_S = 1 \times 10^{18}$/cm^3). Plot the impurity profile in the epitaxial layer and substrate assuming that the layer was grown at a rate of 0.2 μm/min at a temperature of 1200 °C. Assume that boron and phosphorus are the impurities. Find the location of the *pn* junction.

6.13 Compare and discuss the advantages and disadvantages of evaporation, sputtering, and chemical vapor deposition.

6.14 **(a)** A 1-kg source of aluminum is used in an E-beam evaporation system. How many 100-mm wafers can be coated with a 1-μm Al film before the source material is exhausted? Assume that 15% of the evaporated aluminum actually coats a wafer. (The rest is deposited on the inside of the electron-beam system.)

(b) Repeat the process for a 300-mm wafer.

6.15 **(a)** A silicon wafer 100 mm in diameter is centered 200 mm above a small planar evaporation source. Calculate the ratio of thickness between the center and edges of the wafer using Eq. (6.7), following a 1-μm film deposition.

(b) Repeat the process for 200- and 300-mm wafers centered 40 cm above the small planar source.

6.16 Advanced CMOS processes often use lightly doped epitaxial layers grown on heavily doped substrates. Use Eq. (6.31) to predict the dopant profile in the epilayer if an intrinsic silicon layer is grown on top of a substrate that has a uniform concentration of 10^{20} As atoms/cm^3. Assume the layer thickness is 1 μm and that it is grown in $SiCl_4$ at 1,100 °C.

6.17 Repeat Problem 6.16 for the case where the intrinsic layer is grown on a substrate that has a uniform concentration of 2×10^{20} B atoms/cm^3. Assume the layer thickness is 2 μm and that it is grown in SiH_4Cl_2 at 950 °C.

CHAPTER 7

Interconnections and Contacts

The previous six chapters focused on the various processes used to fabricate semiconductor devices in the silicon substrate. To complete the formation of an integrated circuit, one must interconnect the devices and finally get connections to the world outside the silicon chip. Until the 1970s, integrated circuits had two possible levels of interconnection: diffusions and metallization. The use of polysilicon as a gate material in MOS devices added a third level useful for interconnecting devices and circuits.

In this chapter, we discuss the various forms of interconnections and the problems associated with making good contacts between metal and silicon. Refractory metal silicides and multilevel metallization used in VLSI processes are discussed, and an additional method for depositing patterned films, called *liftoff*, is also introduced.

Copper has been introduced in IC processing because of its lower resistivity. The CMP process, introduced in Chapter 3, is combined with standard electroplating techniques to achieve highly planar, inlaid copper interconnections referred to as Damascene technology. Low dielectric constant interlevel films are used to reduce the capacitance of the interconnection levels.

7.1 INTERCONNECTIONS IN INTEGRATED CIRCUITS

As we found in previous chapters, aluminum, polysilicon, and diffused regions are all easily isolated from each other using an insulating layer of silicon dioxide. Thus, today's integrated circuits have three different materials that may cross over each other. To be useful as an interconnect, the materials must also provide as low a sheet resistance as possible in order to minimize voltage drops along the interconnect lines, as well as to minimize propagation delay caused by the resistance and capacitance of the line. Finally, low-resistance "ohmic" contacts must be made between the materials, and the interconnection lines must be reliable throughout long-term operation.

Figure 7.1 shows a simple MOS logic circuit illustrating how polysilicon, metal, and diffused interconnections may cross over or contact each other. Aluminum is used