Thesis for the Degree of Doctor of Technology
Sundsvall 2012

A Hybrid Pixel Detector ASIC with Energy Binning for Real-Time, Spectroscopic Dose Measurements

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ISSN 1652-893X

ISBN 978-91-87103-20-9

Mid Sweden University Doctoral Thesis 128

Akademisk avhandling som med tillstånd av Mittuniversitetet i Sundsvall framläggs till offentlig granskning för avläggande av doktors examen i elektronik **onsdagen den 30 maj 2012**, klockan **13.00** i sal **O102**, Mittuniversitetet Sundsvall. Seminariet kommer att hållas på engelska.

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Printed by Kopieringen Mittuniversitetet, Sundsvall, Sweden, 2012

to my parents and my sister

ACKNOWLEDGEMENTS The first page of this thesis was written on the first day of proton-proton collisions in the LHC. No, I didn't work on the LHC, but being at CERN on that very historic day was catalytic.

Dosepix is the result of an enormous team effort. I would like to express my deepest gratitude to everyone who has worked on this project and supported our efforts. It was truly a privilege working with you.

To IBA Dosimetry, the German Federal Ministry of Economics and Technology, and Marie Curie Actions (ELACCO project): thank you for the generous financial support of work on the Dosepix Project.

To the Medipix2 and Medipix3 Collaborations: thank you for sharing your technical expertise and offering many a sympathetic pat on the back.

To Göran, David K., Omi, Anna, and Erik F.: thanks for the lessons on semiconductor physics. Thanks David K. for this beautiful latex template.

To my officemates throughout the years (Cinzia, Sherwood, Sami, Daniel, Nicoletta, and Massimiliano), my comrades in arms (François, Matt, Giulia, Fiete, Ana, Eva, and Ans), and my CERN Medipix colleagues (Timo, Richard and Jérôme): thank you for the technical discussions and moral support. My special thanks to my long-term officemate Rafa for his immense patience in guiding me through analogue design.

To Salim and Jan T.: thank you for inviting me to partake in your paper.

To my colleagues at CERN who attended the two Dosepix design reviews and who met with me offline for detailed discussions (Sandro M., Sandro B., Jan K., Karolina, and Paul): thank you for your suggestions and help in getting the pixel to a sensible state. My thanks to Rui for help during my nocturnal testing sessions, to Bert and Wojciech for their tools support, to Kostas for coordinating the MOSIS run, Bernard for negotiating the contract, Tuomas for helping me with the synthesis, Sandro B. for maintaining the design flow, and to the ever-charming Ian for skilfully wirebonding the first Dosepix samples to their COB boards. My gratitude to David P. for designing the IC Tester interface card, helping me debug my scripts and not running the other way when you saw me in the halls.

To Gabriel and Lukas, thanks for helping me with radiation measurements and for developing the MatLab scripts to fit the data.

To the IBA Dosimetry research partners (Stefan, Ernst, Karl, Uwe, Martin, Norbert K., and Norbert M.): thank you for all the brainstorming sessions, joint measurement efforts, and for a spectacular readout system. To Stefan in particular, it has been a pleasure working with you and the ECAP team to get Dosepix up and running.

To the Erlangen crew (Thilo, Gisela, Mike, Ina, Peter, Thomas, and Wilhelm): thank you for all the ideas, measurements, and laughs. I will never forget the thrill of those first radiation measurements in your lab. To Thilo and Mike especially, thank you for coming up with the concept of Dosepix and drafting the initial specifications.

Special thanks to Paulo for the design of the bandgap voltage reference circuit, Pierpaolo for the design of the Periphery DAC output stages, Rafa for co-designing the pixel frontend, and Xavi for the design of the E-fuse control logic, the Periphery DACs, the TestPulse Buffers, and the PLL. My sincerest gratitude to Rafa, Michael and Xavi for their mentoring.

To Christina of the Mid Sweden University print office, thank you for your very rapid help in getting the final text ready for publication.

To Erik F., thank you for translating my abstract to Swedish and your helpful suggestions during measurements.

To my thesis editors (Christer, Rafa, Michael, Erik H., Thilo, Ina, Peter, and Gabriel): thank you for helping me make this thesis what it is.

To my dissertation opponent Dr. Roberto Dinapoli and PhD committee members: thank you for your evaluation of my work.

To my academic supervisor Prof. Christer Frödjh, thank you for championing my application to become a PhD student and patiently explaining sensor and X-ray tube concepts to me.

To Dr. Erik Heijne, thank you for reading through the many iterations of this thesis over the past three years, and thank you especially for all the endless encouragement, support and kindness, as well as the occasional gentle reminder that there is more to life outside the office walls.

To my CERN supervisor Dr. Michael Campbell, thank you for cutting me slack when things didn't happen quite the way I'd planned, for calming me down and helping me debug when I didn't see 1's and 0's magically appear after plugging Dosepix in for the first time, for your excellent advice on my papers, presentations and thesis, and most of all, for allowing me to participate in all these amazing projects.

Finally, I'd like to thank all my friends and family for cheering me on all these years. To Aunt Gladys, Uncle Peter, Adrian, and Sylvia: thanks for crossing the Atlantic Ocean and North Sea for my dissertation. To Filip and his parents who have made me feel so welcome in their family, *thank you for believing in me.*

Abstract

Hybrid pixel detectors have been demonstrated to provide excellent quality detection of ionising photon radiation, particularly in X-ray imaging. Recently, there has been interest in developing a hybrid pixel detector specifically for photon dosimetry. This thesis is on the design, implementation, and preliminary characterisation of the Dosepix readout chip.

The text starts with an introduction on the concept of ionising radiation and advocates the need for better dose monitoring devices for radiation protection of personnel working in potentially radioactive environments. Chapters 2 and 3 respectively explains and provides examples of hybrid pixel detectors. Chapter 4 presents an overview of the Dosepix chip and its two intended applications (active personal dosimeter and diagnostics tool to assess medical X-ray beam quality), with a discussion on how the chip design was tailored towards these applications. Chapters 5 and 6 present details on the pixel analogue fronted and digital processing blocks, respectively. Chapter 7 reports measurements taken using the Dosepix hybrid pixel detector. Finally, Chapter 8 concludes with a summary.

Dosepix has 256 square pixels of 220 μm side-length, constituting 12.4 mm^2 of photo-sensitive area per detector. The combination of multiple pixels provides many parallel processors with limited input flux, resulting in a radiation dose monitor which can continuously record data and provide a real-time report on personal dose equivalent. Energy measurements are obtained by measuring the time over threshold (ToT) of each photon and a state machine in the pixel sorts the detected photon events into appropriate energy bins. Each pixel contains 16 digital thresholds with 16 registers to store the associated energy bins. Preliminary measurements of Dosepix chips bump bonded to silicon sensors show very promising results. The frontend has an equivalent noise charge of 120 e^-. In low power mode, each chip consumes 15 mW, permitting its use in a portable, battery-powered system. Direct ToT output from the hybrid pixel detector assembly reveal distinctive photo-peaks correctly identifying the nature of incident photons, and verification measurements indicate that the pixel binning state machines accurately categorise charge spectra. Personal dose equivalent reconstruction using this data has a flat response for a large range of photon energies and dose rates.

Sammanfattning

Hybrid pixeldetektorer har visats ge utmärkta resultat för detektering av joniserande strålning, speciellt i röntgenbildstillämpningar. På senare tid har det funnits ett intresse av att utveckla en hybrid pixeldetektor för dosimetri med joniserande fotoner. Den här avhandlingen behandlar design, implementering och preliminär karakterisering av utläsningschipet Dosepix.

Texten börjar men en introduktion till joniserande strålning och visar på ett behov av bättre utrustning för att övervaka stråldosen för personer som arbetar i en potentiellt radioaktiv miljö. Kapitel 2 och 3 förklarar och ger exempel på hybrid pixeldetektorer. Kapitel 4 innehåller översikt över Dosepix och dess tänkta tillämpningar, (personlig dosimeter och ett verktyg för att bedöma kvalitén på strålfältet i medicinska tillämpningar), samt en diskussion hur Dosepix skräddarsytts för att möta dessa tillämpningar. Kapitel 5 och 6 behandlar i detalj pixlarnas analoga respektive digitala delar. Kapitel 7 redovisar mätningar med Dosepix och kapitel 8 avslutar avhandlingen med att kommentera projektets tillstånd och framtid. Avhandlingen innehåller också appendix med extra förklaringar av relevanta koncept.

Dosepix har 256 stycken, 220μm stora kvadratiska pixlar, vilket ger en känslig area på 12,4 mm^2 per detektor. Antalet pixlar ger flera parallella kanaler och håller nere flödet per kanal. Dosepix kan mäta stråldosen kontinuerligt och redovisar den i real tid. Energin mäts genom den tid som pulsen från fotonen är över tröskeln och en tillståndsmaskin sorterar sedan varje detekterad foton till rätt energi korg. Alla pixlar innehåller 16 digitala trösklar och 16 register för att lagra energi korgarna. Preliminära mätningar med Dosepix bumpbondad till en kiselsensor visar mycket lovande resultat. Varje pixel har ett elektronikbrus på 120e$^-$ och effektförbrukningen i lågeffektläget är 15mW vilket möjliggör ett portabelt batteridrivet system. Vid direkt utläsning av tid över tröskel värden syns tydliga fototoppar och jämförande mätningar indikerar att tillståndsmaskinen i pixlarna på ett korrekt sätt kategoriserar laddningsspektra. Rekonstruering av personlig dosekvivalent med dessa data ger jämn respons över ett stort spektrum av fotonenergier och flödeshastighet.

Översättning av Erik Fröjdh

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This thesis is based on the following papers, herein referred to by their Roman numerals:

1 *Ionising Radiation in the Workplace*

Let's say that there was no colour in the world. Or rather, let's say that our vision could only register black, white, and shades of grey. How much information would we miss? Would our ability to identify and differentiate between objects be hindered by our inability to discern between pigments and hues? Take, for example, the photograph in Figure 1.1. Which scoop of ice cream is chocolate?

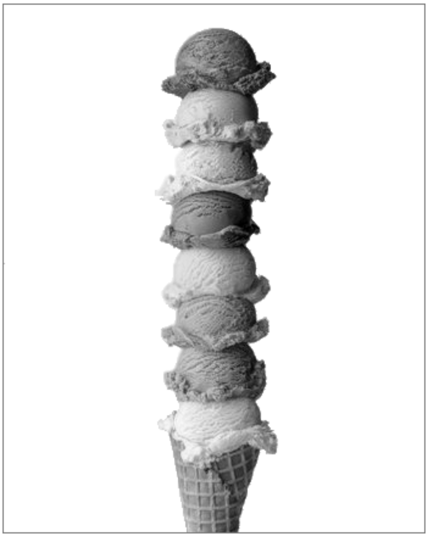


Figure 1.1: Photograph in greyscale

To be fair, we can probably narrow the choice down to two likely candidates based on the shades alone: the top scoop or three scoops down from it. But can we say with absolute certainty which of these two is the correct choice? For that matter, can we even be sure that chocolate is actually present? If your health was somehow linked to finding (or not finding) a particular flavour, would you stake your personal safety on the odds of making the correct guess based on this image in greyscale?

With the addition of colours in Figure 1.2, the answer becomes clear...

...the chocolate is on top.

Colour results from the eye's detection of different wavelengths of visible light. Although colour is only one of several potentially-useful visual cues for identifying objects in a photograph, the addition of colour to a black and white still image can help increase the accuracy of our interpretation of the scene.

X-rays and γ-rays, like visible light, have different wavelengths that affect the way in which these photons interact with matter. If we can differentiate between different wavelengths of X-rays, we can better predict the consequences of the presence of these ionising photons. This would provide us a means to better protect ourselves from the adverse effects of a potentially radioactive environment, such as in an X-ray imaging facility.

Figure 1.2: Photograph in colour
(Photograph from www.free-extras.com.)

This thesis presents the design and implementation of a radiation monitor which can measure the colour (so to speak) of ionising photon radiation, and use that information to calculate dose.

1.1 Ionising Electromagnetic Radiation

Radiation is the emission of energy from a source. The term *electromagnetic radiation* refers to radiation carried by electromagnetic waves (or *photons*), such as radio waves, microwaves, infrared radiation, visible light, ultraviolet light, X-rays, and γ-rays. The last three items on this list constitute the high-frequency end of the electromagnetic spectrum which carries enough energy to ionise atoms. When ionising radiation is absorbed in matter, its interaction can cause the removal of a (previously) bound electron from the atom and turn the atom into a positively-charged ion. Interaction of biological tissue with ionising radiation can damage the tissue; the degree of damage varies based on a number of factors, including the energy of the radiation, its species (or type), its intensity, and the duration of exposure [1; 2]. Nevertheless, when used properly, ionising electromagnetic radiation can have many useful applications. For example, since X-rays can both penetrate and be attenuated by matter, they can be used to capture images of the interior of objects, including the human body. When using X-rays for applications such as medical imaging, it is important to closely monitor the exposure to personnel working in zones of radiation usage.

This thesis presents a novel design targeted at two main applications: 1) active personal dosimeter (specifically for photons), and 2) X-ray tube peak voltage meter. This first chapter advocates the need for active personal dosimeters (which can not only measure personal dose equivalent, but also report instant readings of personal dose equivalent rate) in workplaces where personnel are exposed to ionising photons. The introduction is followed by an explanation of hybrid pixel detectors in Chapter 2, and the description of a series of hybrid pixel detectors, called Medipix, in Chapter 3. Chapter 4 then presents the core topic of the thesis: Dosepix, a hybrid pixel detector ASIC which resolves photon energies and provides data which can be used to calculate personal dose equivalent. The design and implementation of the pixel circuits, which process signals from the detected photon energies, are discussed in Chapters 5 and 6. Chapter 7 then presents measurement results of prototype Dosepix detector assemblies. Finally, the thesis concludes with a review of the design and measurement results and a discussion on the project status and outlook in Chapter 8. A set of appendices provide supplementary explanations of relevant topics.

1.2 CERN

CERN plays two important roles in the introduction to the topics of this thesis. First, it is an example of a workplace which requires radiation monitoring and protection. Second, the advancement of hybrid pixel detectors and the development of discrete photon processing techniques have benefited from the large engineering efforts to meet the requirements of particle tracking in high energy physics experiments.

The *Conseil Européen pour la Recherche Nucléaire*, CERN (*i.e.* the European Council for Nuclear Research), was formed in 1952 following a UNESCO[1] resolution to form a regional research laboratory permitting international scientific collaboration [3]. Two years later, the council evolved into the European Organization for Nuclear Research, which is the present-day entity of CERN.

The CERN facility hosts several particle accelerators for the purpose of conducting HEP experiments. The flagship machine, the Large Hadron Collider (LHC), is capable of producing particle collisions at centre-of-mass energies of (up to) 14 TeV, which would allow the creation of previously unobserved fundamental particles from protons. The LHC arranges high energy collisions between two circulating beams of protons (or during heavy ion experiments, two beams of lead ions). Built in a 27 km circular tunnel approximately 100 m below ground level, the LHC's purpose is to create, and allow the observation of, fundamental particles in order to enrich our understanding of the nature of matter and energy. The LHC successfully circulated controlled proton beams for the first time on September 10, 2008, and the first proton-proton collisions occurred on November 23, 2009 following extensive repairs to the machine after uncontrollable heating and helium leakage in the superconducting magnets.

CERN and its activities have lead to many significant technological innovations. The most famous example is the invention of the World Wide Web by Berners-Lee and Cailliau in 1990, which was intended to facilitate the sharing of information between scientists and engineers in the high energy physics (HEP) community [4; 5]. In 1992, Charpak was awarded the Nobel Prize for Physics for his 1968 invention of the multi-wire proportional chamber [6].

Around 1986, the idea to integrate a nuclear signal processing chain in

[1] UNESCO: United Nations Educational, Scientific and Cultural Organization.

each pixel of a segmented semiconductor detector was proposed at CERN [7], and a first implementation was made in 1989 [8]. Subsequently, both monolithic and hybrid approaches were further investigated in the CERN RD19[2] pixel detector collaboration. From 1992 onward the WA94-97 experiment made tests and installed a telescope of seven double planes of silicon pixel detectors consisting of overlapping ladders. Figure 1.3 illustrates the setup to take images of particle tracks resultant from the bombardment of a ^{208}Pb ion on a Pb target in the WA97 experiment. The event shown in Figure 1.3b allowed the reconstruction of 153 particle tracks [9] which were measured with a precision of the order of 10^{-6} m. The important thing to note is that noise signals were practically suppressed so that each hit (dots in Figure 1.3b) in the figure corresponded to a track which could be traced back to the collision point (*i.e.* no erroneous hits were recorded). The nearly immediate practical use of hybrid pixel detectors in the WA94-97 [10] and DELPHI[3] experiments provided convincing proof of principle and opened the way for larger-scale (*i.e.* with an area of several square metres) adoption in the future LHC experiments.

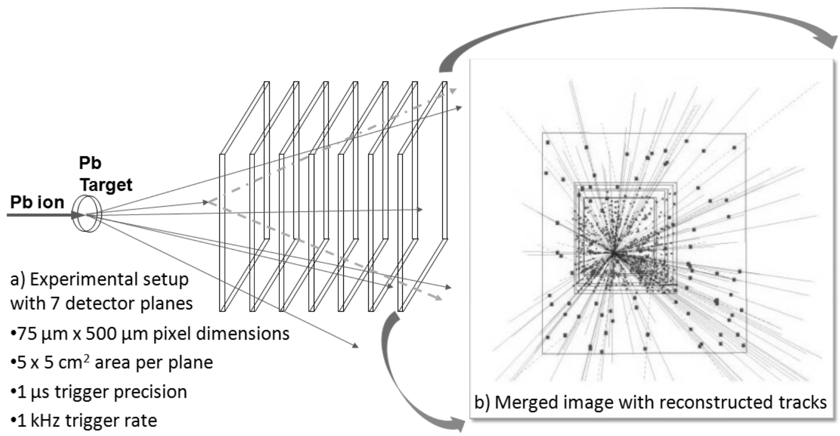


Figure 1.3: Multiple planes of silicon pixel arrays in the WA97 experiment
Data and reconstructed tracks from [9].

[2] RD19 was a research and development collaboration for the development of hybrid and monolithic silicon micropattern detectors.

[3] DELPHI: Detector with Lepton, Photon and Hadron Identification (high energy physics experiment at CERN).

The LHC and the detectors for its experiments took 20+ years in the making. The four large LHC experiments (ALICE, ATLAS, CMS, and LHCb[4]), all rely heavily on segmented semiconductor detectors. ALICE [11], ATLAS [12] and CMS [13], for example, contain pixel arrays in the inner layers of their tracking systems, which require fast and reliable detection of charged particles [14]. LHCb uses a modified version of the ALICE tracker hybrid pixel detector in their ring imaging Cherenkov (RICH) detectors [11; 15] and planes of hybrid pixel detectors are foreseen in their future tracking component upgrades [16]. The development of tracking detectors to meet the demanding requirements of HEP experiments has pushed many new technological advancements, which have lead to the auxiliary evolution of hybrid pixel detectors for X-ray imaging and ultimately, personal dosimetry. These topics will be further explored in the chapters to follow.

1.3 Personal Dosimetry

As in all HEP laboratories, radiation exposure is closely monitored throughout the CERN facility. In addition to monitoring the radioactive byproducts of LHC collisions in the underground experiment caverns, radiation protection measures are also necessary in many of CERN's ground-level laboratories, for example engineering laboratories and beam lines used to develop and characterise the detectors. Prior to installation in the HEP experiments, these detectors must first be validated using radioactive sources and high energy particle beams. Personal dosimeters are worn by all CERN personnel whose work entail exposure to ionising radiation.

Personal dosimetry is the monitoring of individuals whose work necessitate exposure to ionising radiation sources (above natural background levels). Examples of occupations which might involve exposure to electromagnetic radiation include CERN laboratory employees, radiology staff in hospitals and dental offices, medical equipment sterilisation personnel, and nuclear accident response teams. International radiation protection guidelines generally follow the "as low as reasonably achievable" (ALARA) principle, which attempts to find a practical balance between the risks of exposure and beneficial uses of radiation.

[4]ALICE: A Large Ion Collider Experiment; ATLAS: A Toroidal LHC ApparatuS; CMS: Compact Muon Solenoid; LHCb: LHC b-physics.

1.3.1 Overview of Terminology

Absorbed dose, D, is the amount of energy absorbed per unit mass in a material. The level and nature of interaction between incident radiation and the material, however, are not based on radiation energy alone. More meaningful quantities, particularly when discussing the biological impact of irradiation, are the dose equivalent, the personal dose equivalent, and the effective dose equivalent, which measure the effects of energy transferred by ionising radiation to biological tissue. The *dose equivalent*, H, is the amount of (any type of) radiation which, when absorbed in a biological system, results in the same biological effect as one unit of absorbed dose delivered by a low linear energy transfer (LET) radiation (such as electromagnetic radiation), where LET is the local rate of energy deposition along the radiation track. The dose equivalent, H, is determined by weighting the absorbed dose, D, by a quality factor, Q, which is a unitless radiation-species-dependent constant. The *personal dose equivalent*, $\mathrm{H_p(d)}$, is the dose equivalent in soft tissue at a depth, d (in mm), below the body surface. The personal dose equivalent rate, $\dot{\mathrm{H}}_\mathrm{p}(\mathrm{d})$, reports the energy absorbed in mass per unit of time, t. Personal dose equivalent and personal dose equivalent rate are the main quantities of interest in personal dosimetry [17]:

$$\begin{aligned}
\text{Absorbed dose, } D &= \frac{\mathrm{d}\bar{\epsilon}}{\mathrm{d}m} && \text{[Gy]} \quad (1.1)\\
\text{Dose equivalent, } H &= D \times Q && \text{[Sv]} \quad (1.2)\\
\text{Personal dose equivalent, } H_p(d) &= H(\text{at depth } d) && \text{[Sv]} \quad (1.3)
\end{aligned}$$

where $\mathrm{d}\bar{\epsilon}$ is the mean energy from the impinging radiation absorbed in matter of mass, dm, and Q is the unitless quality factor. Typically, personal dosimeters calculate $\mathrm{H_p(0.07)}$ for the personal dose equivalent in skin, and $\mathrm{H_p(10)}$ for the 'whole body equivalent'. The personal dose equivalent rate is:

$$\text{Personal dose equiv. rate, } \dot{H}_p(d) = \frac{\mathrm{d}H_p(d)}{\mathrm{d}t} \qquad \text{[Sv/h]} \quad (1.4)$$

1.3.2 Personal Dosimeters

Personal dosimeters are worn to monitor radiation doses received at work. They comprise radiation sensitive materials which record the energy deposited by ionising radiation and estimate the personal dose equivalent absorbed by their subjects. *Passive personal dosimeters* are devices whose radiation-sensitive materials cannot be directly read out through electronic means. Data acquisition often involves a dedicated reader machine and/or a specialised process to release the radiation-induced signal. These devices tend to be read out infrequently (*e.g.* once per month). *Active personal dosimeters* contain sensors which output radiation-induced signals which can be read out directly and can provide real-time monitoring of the subject. Typically this implies that the radiation-induced signal of an active dosimeter is electronic[5]; this permits immediate radiation dose readings which enable the subject to act on present conditions. Whether passive or active, most solid-state radiation-sensitive materials are not compositionally equivalent to tissue, and therefore the measured energy absorbed by these materials must also be converted to an estimate of the equivalent dose absorbed in tissue. Often metal and/or plastic filters are placed over (parts of) the sensitive material to help improve the personal equivalent dose reconstruction from dose deposited in a sensor.

The biological effects of ionising radiation absorption in tissue depend on many factors, including the overall exposure duration. Cells contain natural repair mechanisms against radiation damage, and over time, they may be able to recover from low radiation doses with little or no long-term effects [18]. While chronic radiation exposure can permit the body time to recover (*e.g.* repair or replace affected cells), acute radiation with the same energy absorbed in the same mass can result in much more severe biological impact. It is therefore important to not only monitor the personal dose equivalent of radiation workers, but also the personal dose equivalent *rate*, as the absorption of 20 mSv concentrated in one minute would likely have much more biological effect than the absorption of the same dose distributed over the course of a year [1]. Moreover, instant dose readings help ensure that a radiation worker is exposed to as low as reasonable radiation levels (ALARA principle). Whereas passive personal dosimeters are read out infrequently and can only report the personal

[5] Active personal dosimeters (APDs) are sometimes called electronic personal dosimeters (EPDs).

dose equivalent, some active personal dosimeters can be read out at steady intervals and provide both the personal dose equivalent and personal dose equivalent rate in real time.

1.3.3 Pixels for Dosimetry

Segmented semiconductor detectors have many attributes useful for dose measurement, including electronic output (for direct readability), high spatial resolution (for image pattern analysis), low input capacitance (for low energy radiation detection), and small sensitive areas associated with individual frontend circuits (for handling high fluxes). There exist several dosimetry projects which employ either hybrid pixel detectors (Paper II, [19; 20; 21; 22]) or monolithic complementary metal oxide semiconductor (CMOS) sensors ([23]) to detect and characterise radiation for dosimetry. In these examples, the high spatial resolution is important for the radiation analysis. In mixed radiation field dosimetry, for example, the geometry of radiation interaction with sensors can be used to help identify radiation species (*e.g.* Paper II, [20; 21; 22]).

Pixels are beneficial for more than capturing spatial information, however. Pixels also act as many individual, parallel processors to handle concurrent radiation signals, permitting, for example, the individual energy measurement of each radiation quantum absorbed by the sensor. The idea of exploiting the energy-resolving capabilities as well as the reduced input flux at each channel of segmented photon counting detectors to implement a photon dosimeter was proposed by [24]. Each pixel would contain photon signal processing circuits and large memory arrays for on-chip spectral analysis to allow for a real-time, energy-resolving photon dosimeter. The combination of many small pixels providing spectral information would permit accurate dose reconstruction in both high and low flux photon radiation environments [25].

1.4 X-Ray Production in Medical Imaging

Medical imaging facilities use X-ray tubes to generate radiation in energy ranges and intensities suitable for diagnostic imaging. Figure 1.4 depicts the main components of an X-ray tube, which consists of a wire filament at the cathode, a target metal at the anode, and an applied potential across the two electrodes.

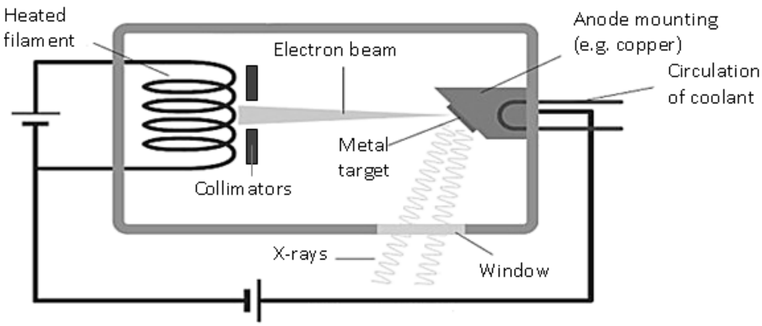


Figure 1.4: Block diagram of an X-ray tube
Illustration based on drawing from [26].

1.4.1 X-ray Tube Spectrum

X-rays are generated through the bombardment of energetic electrons (from the cathode) on a target (at the anode). The cathode is a source of electrons through thermionic emission[6]. A large potential difference (the tube voltage) between the electrodes accelerates the electrons towards the anode. The unit electron-volt (eV) is the amount of energy attained through the acceleration of 1 V; an electron accelerated by 100 kV tube voltage, for example, would have a kinetic energy of 100 keV in a vacuum.

The majority of accelerated electrons striking the target will merely generate heat from collisions. Some electrons, however, will interact close enough to a target atom nucleus in order to be decelerated by the Coulombic forces of the positive nucleus. The kinetic energy lost due to deceleration is emitted as a bremsstrahlung ("braking") photon of energy equal to that lost from the electron. The quantity of energy lost in deceleration depends on interaction proximity to the nucleus (it increases with increasing

[6] Thermionic emission is the emission of charge carriers from a heated surface, such as a tungsten filament heated through current flow [27].

proximity up to the maximum value of the original electron kinetic energy). Thus the emitted bremsstrahlung spectrum is a continuum, with low energy photons filtered at the output by the tube port.

If the kinetic energy of the electron is greater than the characteristic X-ray energy[7] of the anode material, then the tube output spectrum will also contain photon intensity peaks at the characteristic X-ray energies. The chances of characteristic X-ray production increases with higher electron beam kinetic energy, thus the intensity of characteristic X-ray photons (relative to bremsstrahlung intensity) also increases with tube voltage.

The anode material and tube voltages depend on the composition of tissue being imaged. Typical X-ray tubes for radiology are operated between 40 kV to 150 kV, while typical mammography tubes are operated at 25 kV to 40 kV (the optimal ratio of breast imaging contrast over patient dose is attained using 10 keV to 15 keV X-rays) [29]. Figure 1.5 shows the output from an X-ray tube for mammography. As previously explained, the maximum bremsstrahlung photon energy provides an indication of the kinetic energy of the X-ray tube electrons. In these example spectra, Molybdenum and lucite filters have removed most of the high energy photons from the output spectra, however it can be seen that the maximum bremsstrahlung photon energy, as well as relative characteristic X-ray intensity over bremsstrahlung intensity, depends on tube voltage.

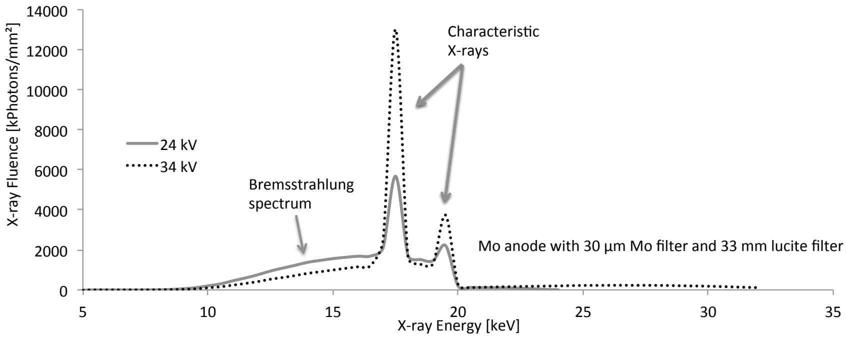


Figure 1.5: Example mammography X-ray spectra
X-ray tube spectra when the tube voltage is 24 kV and 34 kV. The characteristic X-ray energies of the molybdenum anode are at 17.4 keV and 19.6 keV. Data from [29].

[7]Characteristic X-rays have discrete energy values corresponding to the difference in binding energies between electron shells in an atom. Characteristic X-rays (also called fluorescence photons) are emitted during the rearrangement of electrons to an energetically stable state after ionisation [28].

1.4.2 X-ray Tube Voltage

The voltage potential used to accelerate electrons between X-ray tube electrodes is parameterised by two quantities: kilovolt peak (kVp) and voltage ripple.

An X-ray generator typically consists of a step-up transformer to provide current at a high voltage from an AC[8] input. In order to generate a DC tube voltage, the transformer output is rectified and smoothed with capacitances. The X-ray tube voltage ripple is the percentage variation in tube voltage [30]:

$$\%\text{ Voltage Ripple} \quad = \quad \frac{V_{peak} - V_{min}}{V_{peak}} \times 100$$

Modern X-ray generators typically output signals with 3-25% voltage ripple depending on the circuit implementation [29]. Constant potential generators with less than 2% ripple exist but are expensive and not commonplace.

The peak voltage (V_{peak}) or the more commonly used term, kilovolt peak (kVp), is an operation parameter of the X-ray tube, along with the tube current and exposure time.

1.4.3 kVp Meters

A kVp meter measures the peak accelerating voltage of an X-ray tube. An invasive kVp meter determines the tube voltage through a direct connection to the voltage generator circuit with a voltage divider connected to an oscilloscope. However, this setup is impractical for routine use in imaging facilities. An alternative method to determine tube voltage is to use a device which can extrapolate the tube voltage through analysis of the output spectra. A non-invasive kVp meter is an X-ray tube quality assurance tool which measures and analyses the tube spectra, which can vary with time if the tube voltage is not constant (*e.g.* due to voltage ripple, pulsed operation, or temperature variations).

[8] AC: alternating current; DC: direct current.

1.5 Summary of Publications and Personal Contributions

This thesis is on the design, implementation, and verification of a hybrid pixel detector chip called Dosepix. A number of publications related to this work are included at the end of the thesis:

Paper I, *Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements* (presented at the Vienna Conference on Instrumentation in 2007), introduces the Timepix hybrid pixel detector, which was used to take the preliminary photon dose data for the definition of Dosepix specifications. The thesis author developed a Verilog description of the Timepix digital circuits and ran detailed simulations of the digital part of the pixel matrix.

Paper II, *Smart dosimetry by pattern recognition using a single photon counting detector system in time over threshold mode* (presented at the International Workshop on Radiation Imaging Detectors in 2011), describes a method of image analysis to identify radiation species in mixed-field dosimetry applications using a Timepix detector. The thesis author wrote the background on dosimetry for this paper and provided advice on chip calibration to improve the energy measurement.

Paper III, *Design considerations for area-constrained in-pixel photon counting in Medipix3* (presented at the Topical Workshop on Electronics for Particle Physics in 2008), discusses methods of optimising transistor layout in designs with high functional requirements and severe area constraints. The thesis author designed the manual layout of the Medipix3.0 and Medipix3.1 digital counters and devised a method to optimally utilise the available pixel area to realise the complete set of features requested by the Medipix3 Collaboration members.

Papers IV, V, & VI, *Medipix3: A 64 k pixel detector readout chip working in single photon counting mode with improved spectrometric performance* and *Characterization of the Medipix3 pixel readout chip* (presented at the International Workshop on Radiation Imaging Detectors in 2009 and 2010, respectively) and *Counter architectures for a single photon-counting pixel detector such as Medipix3*, (presented at the International Summer School on Nuclear Physics Methods and Accelerators in Biology and Medicine in 2007), introduce the Medipix3 hybrid pixel detector and describe the fully custom-designed digital counters of Medipix3.0 and Medipix3.1. The thesis author designed the full-custom digital circuits of the Medipix3.0 and Medipix3.1 digital counters, starting at the transistor level. This included the development of detailed analogue models of the digital circuits (including the counters and charge summing arbitration logic) which were incorporated into the Verilog descriptions of each custom-designed logic gate. The thesis author created a library of these custom digital blocks.

Papers VII & VIII, *A pixel detector ASIC for dosimetry using time-over-threshold energy measurements* (presented at the Solid State Dosimetry Conference in 2010) and *Electrical measurements of a multi-mode hybrid pixel detector ASIC for radiation detection* (presented at the International Workshop on Radiation Imaging Detectors in 2011), discuss the design and electrical measurements of the Dosepix hybrid pixel detector chip with in-pixel energy spectrum analysers. The thesis author designed the digital part of the Dosepix pixel, the end of column blocks, and the matrix/periphery "glue" logic, including the column-level clock-gating scheme which reduces power consumption, permitting the chip to be used in a portable battery-powered device. The design of the digital blocks of the Dosepix pixel is the core of this thesis work. The author also co-designed and fully implemented (in schematic and layout) the analogue part of the pixel and manually laid out the full chip. All initial chip and hybrid pixel assembly measurements (including the results presented in these papers and in this thesis) were made by the thesis author.

2

Hybrid Pixel Detectors and Quantum Processing Systems

> *"The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas... Integrated electronics will make electronic techniques more generally available through all of society, performing many functions that presently are done inadequately by other techniques or not done at all."*
>
> Gordon E. Moore, 1965 [31]

In his seminal article of 1965, Moore predicted that the satisfaction of societal demands would require technology to progress at a rate for which the density of integrated electronic components would double every 18 months for the ten years to follow. He noted that such a rate could be realistically sustainable given the then recent advances in multilayer metallisation techniques to free up interconnect area for active devices [31]. Ten years later, Moore adjusted his prediction to state that transistor densities would double every 24 months [32]. This projection of microelectronics industry trends, commonly referred to as "Moore's Law", has been used as a guideline for planning the semiconductor industry roadmap. Adhering to the pace set by Moore, technological advancements over the past 40+ years have indeed miniaturised transistor feature sizes exponentially. The smaller transistors have enabled faster, lower power and more complex circuits, and have permitted the realisation of inventions for new applications, such as compact portable computers, mobile phones, mp3 players, and global positioning systems.

Although semiconductor companies continue to invent ways to manufacture smaller transistors, the rate of device dimension scaling has diminished in recent years, particularly as minimum achievable dimensions approach atomic units. Recently, the International Technology Roadmap for Semiconductors (ITRS) released a white paper outlining the concept of "More-than-Moore" (MtM) which focuses on the trend of functional diversification [33]. While Moore's Law addressed the geometric scaling of transistors on a common substrate, MtM considers modern approaches to realising integrated *systems*, with functions implemented by components which complement the electronics chip. Notably, the MtM white paper cites image sensors based on hybrid pixel detector technologies as prime examples of MtM systems, where the highly integrated readout electronics provide processing functions, while photon sensing is achieved by a sensor which is connected to, but not part of the chip. MtM systems such as hybrid pixel detectors provide new potential to realise functionally dense systems in small packages.

2.0.1 Hybrid Pixel Detectors

A hybrid pixel detector is an electronics system with a semiconductor sensor, such as a silicon diode, electrically connected to dedicated readout electronics via balls of solder called bump bonds. Both the sensor and readout electronics are segmented into many small channels (typically referred to as pixels), and each channel (on both the sensor and readout electronics) has an electrode to which the bump bond forms an electrical connection. Figure 2.1 illustrates the cross-section of such a hybrid pixel, and Figure 2.2 shows an array of solder bumps. The term *hybrid* refers the fact that the sensor and readout application-specific integrated circuit (ASIC) are distinct components (rather than a single monolithic piece), and as such the sensor and ASIC can be separately optimised. The composition of the sensor material, for example, can be chosen for its sensitivity to detect a targeted range of energies. Currently silicon is the most commonly used semiconductor sensor material. Silicon is a relatively plentiful material (and therefore cost-effective), and pn junction diodes made from Si are suitable for the detection of low energy photons. However, there is much interest, particularly in the medical imaging community, in the evaluation of sensors made of high-Z (*i.e.* high atomic number) materials such as GaAs, CdTe, or CdZnTe [34; 35; 36; 37], which have much better efficiencies to capture high energy photons. On the ASIC side, modern deep sub-micron technologies offer the opportunity to achieve high functional density, thereby permitting complex photon processing, such as photon counting or online event binning, to be realised within small pixel areas. Figure 2.3 shows an example of a hybrid pixel detector, with the ASIC glued and wirebonded to the readout board, and the semiconductor sensor bump-bonded on top of the ASIC.

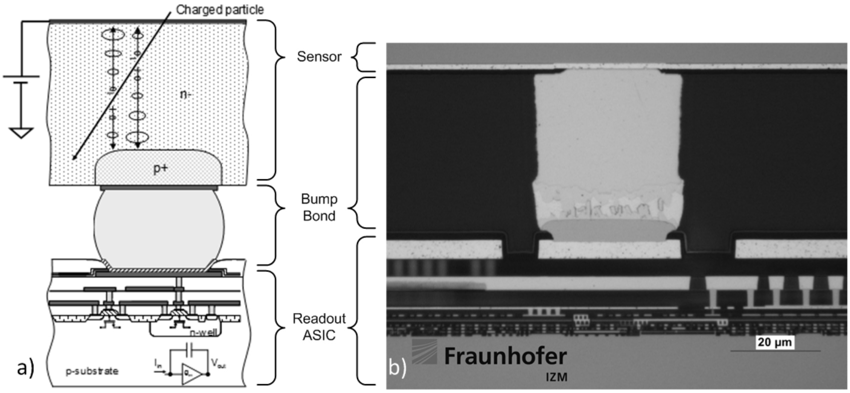


Figure 2.1: Cross-section of a pixel in a hybrid pixel detector

a) Cross-section of a semiconductor pn junction sensor bump bonded to the frontend of a readout ASIC. Illustration courtesy of R. Ballabriga, CERN [38]. **b)** Photograph of a silicon sensor connected by a type of bump bond called copper pillar to the input electrode of a pixel in the Dosepix readout ASIC. The ASIC was implemented in an 130 nm CMOS process with 8 metal layers. Photograph printed with permission from Fraunhofer IZM.

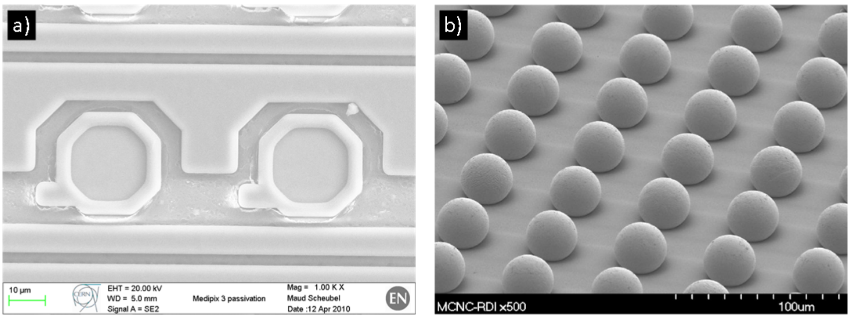


Figure 2.2: Bump bonds and electrodes

a) SEM (scanning electron microscope) image of two bump bond electrodes on a Medipix3 ASIC. While the rest of the chip is protected by a layer of SiN, the electrodes are exposed with passivation layer openings 20 µm in diameter and 55 µm apart. **b)** SEM image of an array of tin-lead solder bumps on a Medipix2 ASIC prior to flip-chip assembly with the sensor. Image courtesy of A. Huffman, Research Triangle Institute.

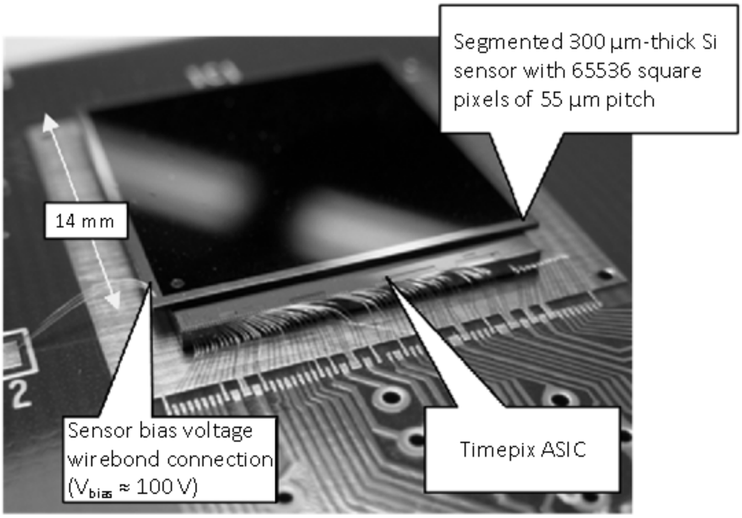


Figure 2.3: Photograph of a hybrid pixel detector and its readout board

This photograph shows a Timepix hybrid pixel detector mounted on its readout board. All of the wirebond connection pads are arranged along a single edge of the readout ASIC; this allows tiling with other detectors along the three other edges. The wirebonds connected to the top of the sensor provides a bias (depletion) voltage across the pn junction of the silicon sensor. Photograph courtesy of J. Jakůbek, Czech Technical University [39].

2.1 The Sensor

A pn junction diode consists of a transition in the material composition from one doping level to another level. Because of the sharp gradient in charge carrier concentrations across the junction, electrons on the n-type side close to the junction diffuse to the p-type side, while holes on the p-type side diffuse to the n-type. These carriers quickly recombine and disappear, but they leave behind positive ions within the n-type and negative ions in the p-type. This creates a region of space-charge in the device, *i.e.* the depletion region, with a built-in voltage potential due to the charge gradient. If a voltage in the same polarity as the built-in potential is applied to electrodes at the two surfaces, then the augmented electric field depletes the junction even further. Usually the applied bias voltage ensures full depletion across the sensor volume.

When a photon impinges onto a pixel, one of four forms of interactions with the sensor material can result: 1) photoelectric absorption (also known as the photoelectric effect[1]), 2) Compton scattering, 3) pair production, and/or 4) coherent scattering. Photoelectric absorption is desirable for efficient photon detection because the quantity of charge generated in the sensor is directly proportional to the incident energy. The likelihood of a form of interaction depends on the atomic number of the sensor material as well as the energy of the incident photon. Figure 2.4 indicates the dominant form of interaction given the absorber atomic number and photon energy.

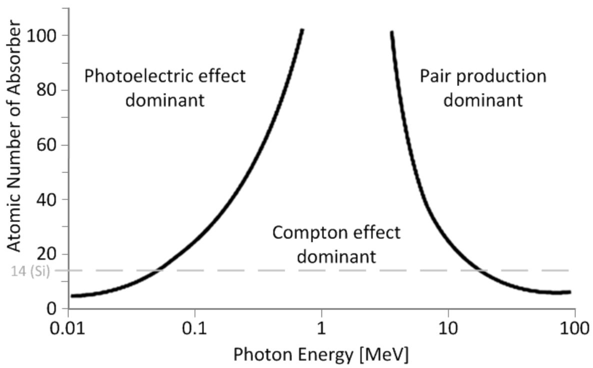


Figure 2.4: Interaction of γ-ray photons with matter

The atomic number of silicon (14) is indicated. Plotted based on data from [28].

During photoelectric absorption, the energy from the incident photon is *completely transferred to the sensor material*. The absorption of incident energy causes the ejection of a photoelectron from a sensor atom, and the photoelectron obtains the kinetic energy:

$$\begin{aligned} E_{e^-} &= E_\gamma - E_{binding} \\ &= h\nu - E_{binding} \end{aligned} \tag{2.1}$$

where the Planck's constant, h, times the incident wave frequency, ν, is the incident energy, E_γ.

[1] Einstein was awarded the Nobel Prize for Physics in 1921 for his explanation of the photoelectric effect [40] which had been observed by Hertz and Lenard during their cathode ray (electron beam) experiments. Lenard had also received the Nobel Prize for Physics in 1905 for his work on cathode rays [41].

The vacancy in the inner shell (left by the ejection of the photoelectron) leaves the atom in an energetically undesirable state. To stabilise the atom, this inner-shell vacancy is filled by an electron from an outer shell, which in turn is filled by an electron of a shell even further from the nucleus. The surplus of energy liberated during the rearrangement of electrons between shells results in the emission of either a characteristic X-ray (with energy, $E_X = E_K - E_L$, in an example where a K-shell vacancy is filled by an L-shell electron), or an Auger electron (with energy, $E_{Auger} = E_K - 2E_L$, for the same example). By conservation of energy, the kinetic energies carried by the photoelectron, characteristic X-rays, and/or Auger electrons sum up to E_γ. Interaction of the photoelectron and characteristic X-ray/Auger electron with other atoms in the sensor material cause the generation of electron-hole pairs *which form the signal to be processed by the associated electronics*. While it is possible that a characteristic X-ray (or Auger electron) will escape the sensor material, characteristic X-rays in silicon have short mean free paths and are likely to be reabsorbed by the sensor material. Thus the number of electron-hole pairs in silicon is usually proportional to the absorbed energy.

When Compton scattering occurs, the photon is deflected at an angle Θ, and the photon energy is *partially transferred to the recoil electron*. The quantity of energy transfer depends on Θ, but in Compton scattering, at least some of the original energy is retained by the scattered photon, which may then leave the material without further interaction, or remain in the material and undergo a subsequent interaction (such as photoelectric absorption, another Compton scattering, or coherent scattering).

In pair production, the energy of the photon is *fully transformed to an electron-positron pair*. The photon disappears if the incident photon energy is greater than twice the rest-mass energy of an electron (1.02 MeV), and thus pair production occurs only during the interaction of very high energy photons with the sensor (in the Coulomb field of sensor nuclei or electrons). All the excess energy goes into kinetic energy shared by the electron and the positron (neglecting momentum transfer to the nucleus). The latter will annihilate after slowing down in the sensor material.

The last form of interaction, coherent scattering, modifies the photon direction but with no [42] energy transfer.

The ability of a detector system to resolve energies depends greatly on the probability and form of interaction between the incident photon and the sensor material. The linear attenuation coefficient, μ, is the probability (per path length) that a photon interacts with the sensor material, whether by absorption or scattering. It is the sum of the individual probabilities of occurrence of the four interactions listed above:

$$\mu_{total} = \mu_{photoelectric} + \mu_{Compton} + \mu_{pair} + \mu_{coherent} \tag{2.2}$$

and the average distance travelled by a photon through the sensor prior to interaction is called the mean free path, λ :

$$\lambda = \frac{1}{\mu} \tag{2.3}$$

For a beam of monoenergetic photons, the linear attenuation coefficient relates the number of photons incident on the sensor, I_o, with the intensity of photons which *pass through the detector without interaction*, $I_{transmitted}$:

$$I_{transmitted} = I_o e^{-\mu t} \quad \text{or alternatively,} \tag{2.4}$$

$$I_{transmitted} = I_o e^{-(\mu/\rho)\times(\rho t)} \quad \text{and thus,} \tag{2.5}$$

$$I_{interacted} = I_o - I_{transmitted} \tag{2.6}$$

where t is the sensor thickness, ρ is its density, μ/ρ is called the mass attenuation coefficient, and the term ρt is called the mass-thickness. Equation 2.5 is parameterised by the mass-thickness, since the degree of photon attenuation depends on the density of atoms in the sensor material and its thickness. Figure 2.5 shows the mass attenuation coefficients as a function of photon energy for the different forms of interaction in silicon. It should be noted that μ_{total}/ρ does not differ by any noticeable amount with or without coherent scattering. Up to ~40 keV, photoelectric absorption dominates the overall effects; beyond ~60 keV, Compton scattering takes over as the dominant form of interaction. For the range of energies shown in Figure 2.5, $\mu_{pair}/\rho = 0$.

The energy deposited in the depleted pixel sensor volume (either by absorption or partial transfer during scattering), creates electron-hole pairs. The number of electron-hole pairs generated by a silicon diode sensor is determined by the deposited energy, $E_{absorbed}$ and the sensor material ionisation energy, ϵ_i:

$$n = \frac{E_{absorbed}}{\epsilon_i} \tag{2.7}$$

where the average ionisation energy, ϵ_i, in Si is 3.62 eV at 300 K [28].

The electric field applied across the sensor causes the electrons and holes to separate, and the resultant current flow instantaneously induces

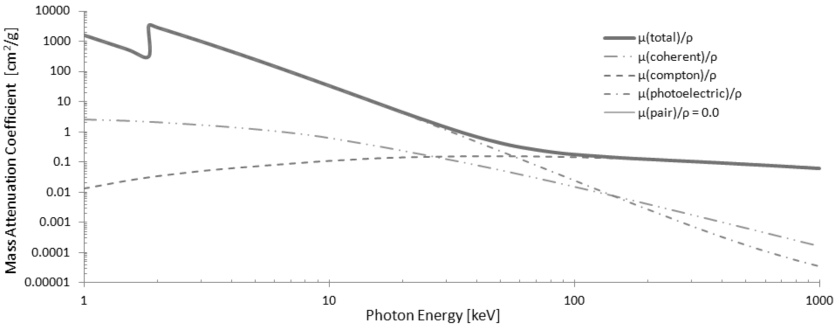


Figure 2.5: Mass attenuation coefficients of photons in silicon

Note: the density of silicon is $\rho = 2.3296\ \mathrm{g/cm^3}$. Data from the National Institute of Standards and Technology XCOM database [42].

charges in the contact electrodes (Shockley-Ramo theorem [43; 44]). While the charge is progressively collected by the electrode at the sensor pixel output, this current decays until charge collection is complete. The signal current is transmitted through the bump bond to the low impedance input of the associate pixel in the readout electronics. The amplifier is usually charge-sensitive and integrates the signal current.

2.1.1 Charge Sharing

When photon energy is absorbed by the sensor material, the generated electron-hole pairs form a three-dimensional cloud in the pixel volume. Ideally, the electric field across the sensor would contain the charge cloud within the pixel and guide all the charge carriers directly to its electrode. Charge carriers undergo diffusion during drift, and some of the carriers may be collected in neighbouring pixels. This effect increases with lower electric field and longer charge carrier collection time.

Charge sharing, in the context of segmented semiconductor sensors, can occur where the signal associated with energy deposited in the pixel is instead collected by the electrode of a neighbour. Various phenomena can cause charge sharing:

- Charge carrier diffusion (even in the presence of an electric field),
- Photoelectrons crossing pixel boundaries, and
- Fluorescence photons crossing pixel boundaries

Charge sharing not only degrades the signal seen by the original pixel, but can also cause adjacent pixels to falsely record their partial signals. In segmented detectors, the degree of charge sharing increases with decreasing ratio of pixel area over sensor thickness. Similarly, the occurrence of charge sharing increases in sensor materials whose fluorescence photons have long mean free paths.

2.1.2 Detector Capacitance and Its Influence on Readout Noise

The n-type and p-type electrodes of the pn junction diode form parallel plates insulated by the depletion region, with the capacitance:

$$C_{junction} = \epsilon \frac{A}{W} \tag{2.8}$$

where ϵ is the silicon dielectric constant times the permittivity of free space ($\epsilon_{Si} \times \epsilon_0$), and A is the parallel plate area. The depletion width, W, is:

$$W = \sqrt{\frac{2\epsilon(V_{bias} + V_{bi})}{qN}} \tag{2.9}$$

where q is the electron charge magnitude, N the dopant concentration in the bulk, V_{bi} the built-in potential across the depletion region, and V_{bias} the voltage applied across the diode. The junction capacitance is thus [45]:

$$C_{junction} = A\sqrt{\frac{\epsilon qN}{2(V_{bias} + V_{bi})}} \tag{2.10}$$

Equation 2.13 indicates that $C_{junction}$ depends on doping levels and also sensor bias voltage, particularly when V_{bias} » V_{bi}.

Figure 2.6a illustrates the various sources of capacitance at the input of the readout electronics. In addition to junction capacitance, there is also capacitance between directly adjacent bump bond electrodes, C_{side}, and capacitance between bump bond electrodes of diagonally-neighbouring pixels, $C_{diagonal}$ (see Figure 2.6b). The total interpixel capacitance, $C_{interpixel}$, seen by a central pixel electrode (*i.e.* grey electrode of Figure 2.6b) of diameter, 2r, with an electrode implantation depth, d, and separated from its side neighbours by a gap distance, g, can be calculated by [46]:

$$\begin{aligned} C_{interpixel} &= 4C_{diagonal} + 4C_{side} \\ &= 4C_{diagonal} + \frac{4\pi\epsilon 2r}{ln\left(\frac{g}{d} + \sqrt{\frac{g}{d}^2 - 1}\right)} \end{aligned} \tag{2.11}$$

Capacitive contributions from pixels further than the direct neighbours are neglible [46].

On the readout electronics side, there is also capacitance between the input electrode and the metal layers below connecting it to the frontend input. For an input electrode of diameter = 25 μm in the readout electronics, the electrode capacitance, C_{pad}, is[2]:

$$C_{pad} \simeq 50 \text{ fF} \tag{2.12}$$

The total input capacitance of a pixel with four equidistant side neighbours is consequently:

$$C_{det} = C_{junction} + C_{interpixel} + C_{pad} \tag{2.13}$$

As can be seen in Figure 2.7a, C_{det} increases with pixel pitch. One major advantage of segmented semiconductor detectors, such as hybrid pixel detectors, is the reduction of capacitance at the input of each analogue frontend. While the frontends presented in this thesis utilise topologies for which the preamplifier gain is independent of C_{det}, Figure 2.7b shows that the system noise nevertheless increases with C_{det} (which depends on the pixel pitch and bump bond pad size). Segmentation therefore allows the realisation of low-noise frontend systems by reducing the sensor area associated with each frontend[3].

[2]Determined through the circuit extraction of a pixel implemented in a commercial 130 nm CMOS process [47].

[3]It should be noted that the calculations shown in this section are not intended to be rigorous. The intention of this section is to demonstrate the general effects of detector capacitance on frontend performance, and to explain how C_{det} was calculated for the simulations of Appendix B.

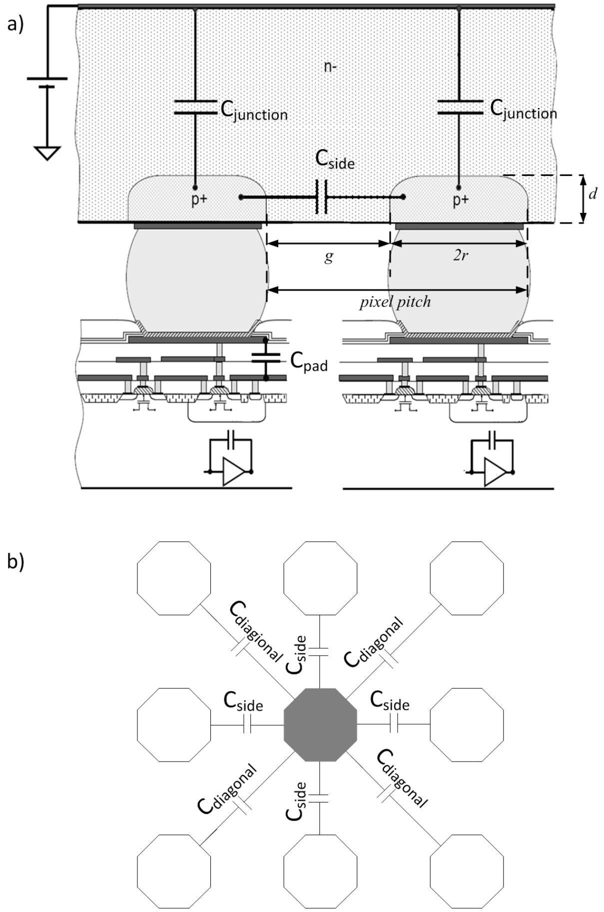


Figure 2.6: Input capacitance to readout electronics

a) Illustration of parasitic capacitance at the input of a pixel frontend. Drawing courtesy of R. Ballabriga, CERN [47]. **b)** Interpixel capacitances.

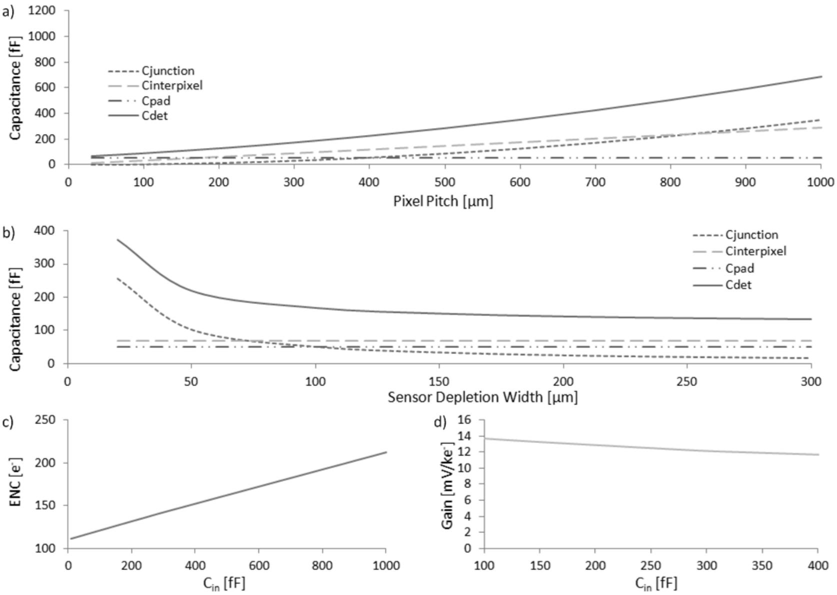


Figure 2.7: Input capacitance to readout electronics

a) Calculation of C_{det} from a Si sensor versus pixel pitch. In these calculations, W = 300 µm, g = 0.5 µm, 2r = 25 µm, and $C_{diagonal}$ = 3.2 fF[4]. **b)** Calculation of C_{det} from a Si sensor versus sensor depletion width. In this calculations, the square pixel is 220 µm in side-length. **c)** Extracted simulation of the influence of C_{det} on the Dosepix frontend noise without any sensor leakage current. This demonstrates how the choice of pixel and pad sizes can affect system performance. **d)** Extracted simulation of the influence of C_{det} on the Dosepix *charge sensitive* preamplifier gain. The x-axis is limited to the range of C_{det} based on the values plotted in **c**. As intended for a charge sensitive preamplifier, the gain does not change by much with C_{det}.

[4]Determined through an empirical fit [46].

2.2 The ASIC

As its name implies, an application-specific integrated circuit (ASIC) is an electronics chip designed to perform dedicated tasks. The ASIC component of a hybrid pixel detector is often referred to as the readout chip (ROC), because the ASIC traditionally provided the means to acquire an amplified electrical signal from the sensor. Modern hybrid pixel detectors however, perform many complex processing functions in addition to readout capability. A presentation of the variety of functions which can be performed by hybrid pixel detector ASICs is an extensive topic and beyond the scope of this thesis. Instead, this explanation of the role of readout electronics will focus on the functions which are provided by the Medipix family of hybrid pixel detectors, as well as the Dosepix chip.

A major advantage of hybrid pixel detectors, compared to active pixel sensors for example, is that the entire pixel area on the ASIC can be utilised for functionality (*i.e.* 100% fill factor[5]). As Moore predicted, each generation of transistor technology maturation has permitted the realisation of increasingly dense and lower power circuits. Medipix represents a set of chips which have benefited from the miniaturisation trends of the CMOS industry. The small, low power transistors available in deep submicron technologies have enabled the combination of robust analogue frontend circuits with complex digital processing blocks within compact pixel areas, permitting high levels of functionality as well as high spatial resolution detectors. Figure 2.8 shows the progression of transistor and data densities in the various generations of Medipix (and related) hybrid pixel detectors.

2.2.1 *System Architecture*

Hybrid pixel detectors are very often intended for imaging, and typically contain a matrix of segmented pixels arranged in a grid formation in order to provide position-sensitive information. High spatial resolution requires compact areas and pixel chips tend to be structured to optimise hardware resources. Figure 2.9 depicts an example of how a hybrid pixel detector ASIC might be organised.

[5]Fill factor is the percentage of pixel area which is sensitive to the energy deposited by photons.

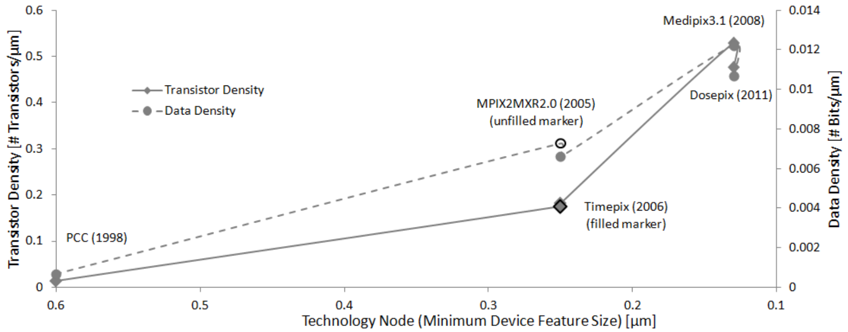


Figure 2.8: Transistor and data density evolution in hybrid pixel detectors

Both transistor and data densities inside pixel areas are plotted here to indicate functional density trends in hybrid pixel detectors implemented at different standard CMOS technology nodes. The plots are connected in chronological order of the design. Except for Dosepix, these detectors contain pixels whose layouts were completely custom designed and manually laid out. Paper III studies the level of extra functional density which can be achieved from custom design over automatic layout generation. The Dosepix pixel layout was partially done manually and partially done with automatic place and route tools as a compromise between achieving optimal functional density and practical design time. The plot of data density indicates the number of data storage elements (including configuration bits, counters, shift registers, and digital thresholds) per unit area. To be fair, while transistor size scaling plays the predominant role in effecting these trends, it is not the only factor. Choice of block architectures, such as latches versus flip-flops, resettable versus non-resettable flip-flops, and linear feedback shift registers (LFSR) versus reconfigurable binary counters, also determines the level of functional density which can be realised within pixel areas.

Columns are defined along the axis of data transfer in a pixel matrix. During operation, charge from the sensor is processed by the analogue frontend and converted to a digital format for storage and readout. During readout, the digital data is transferred down the column to be handled by end of column blocks. Typically, data is shifted down the column in a single serial chain through the pixels; this is the simplest and most area-efficient way to transfer the data, albeit not the fastest. Alternatively, a data bus could be used to expedite the data transfer at the expense of routing resources, area and perhaps also power.

The area below the matrix is called the chip periphery and the transistors located in that region constitute the periphery circuits. These circuits are necessary to provide chip-level control and readout coordination, however the area occupied by the periphery cannot be used to detect photons. The periphery circuits are therefore often arranged at a single edge of the hybrid pixel detector, allowing tiling of other hybrid pixel detectors along the remaining three edges to increase the photo-sensitive surface. The periphery can contain digital to analogue conversion circuits (DACs) which allow the user to program the operating points of analogue circuits, such as the pixel frontend. The periphery might also include test or diagnostics blocks, reference circuits, global chip control signals, readout coordination circuits, and digital programming memories. Close to the border to the pixel matrix are the end of column blocks which provide specific control and processing for input and output signals in each column of pixels.

Finally, the wirebond pads provide connection points to wires on a printed circuit board[6]. The chip IO includes data transfer lines, control signals, power supplies, and ground connections. Multiple power domains are often necessary to isolate analogue and digital circuits on the chip.

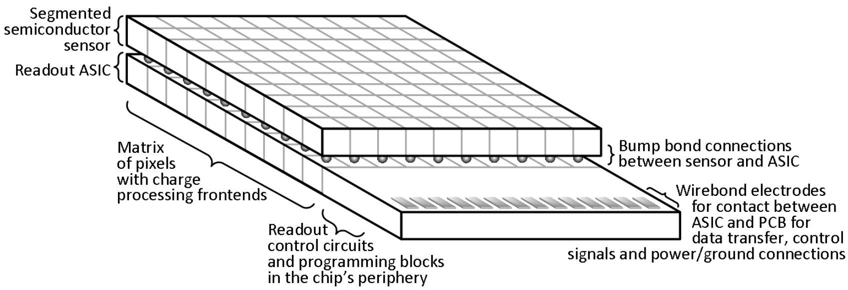


Figure 2.9: The main elements of a hybrid pixel detector ASIC

[6] An emerging technology, called through silicon vias (TSV), is being developed which would remove the need for wirebond connections in hybrid pixel detectors (*e.g.* [48]). Instead, the chip to board connections would be made using ball grid array (BGA) bump bonds connecting the board to vias at the underside of the chip. The removal of the wirebond pad area would reduce the inactive area of a hybrid pixel detector, and perhaps allow tiling at all four sides. Projects such as [49], aim to butt hybrid pixel detectors on all four edges, with the array of ASICs bump bonded to large-area sensors on one surface and bump bonded to the common readout system on the other surface.

2.3 Quantum Processing in Pixels

There are numerous approaches to extract information regarding an incident photon using CMOS circuits, particularly as transistor density limitations become less restrictive and permit increasingly complex circuits within small pixel areas. Three methods of charge processing are presented here: 1) signal integration, 2) discrete photon counting, and 3) time over threshold measurements.

The operation of an integrating detector is depicted in Figure 2.10a. In this example, the pixel circuit contains a capacitance which is precharged to a reset voltage. During the integration period, $T_{\mathrm{Integration}}$, a parallel current discharges the capacitance. This current is the summation of a photocurrent, I_{photo} (from the charge generated through photoelectric absorption of photon energy) and a dark current, I_{dark} (a thermally generated signal which flows irrespective of the presence of photons)[50; 51]. The rate of discharge depends on the magnitude of the current, and thus the integrated current can be determined by sampling (an amplified version of) the voltage across the capacitor at the end of $T_{\mathrm{integration}}$. *Thus, an integrating detector is intended to measure the overall integrated energy deposited during $T_{Integration}$.*

An alternate approach is to count the number of photons absorbed by the sensor diode during a defined period. In the example of Figure 2.10b, the charge generated in the diode is converted to a voltage pulse whose amplitude is proportional to the magnitude of charge. The voltage pulse is not a clean signal however; the amplified charge signal is overlaid with background electronics noise. The amplitude of the pulse is compared with a threshold voltage. If the threshold voltage is set higher than the noise signal, then the resultant discriminator output pulse is asserted for the detection of charge from energy deposited in the sensor. This circuit outputs a digital count of the number of these discriminated pulses, which represents the detected number of photons during the open electronic shutter period, $T_{\mathrm{OpenShutter}}$. *Thus, a photon counting detector is intended to measure the intensity of photons during $T_{OpenShutter}$.*

The final approach, the measurement of an amplified charge signal's time over threshold (ToT), is a variant of the analogue-to-digital conversion technique proposed by Wilkinson in 1950, which recorded the shaped voltage pulse discharge time [52]. ToT is a special case of photon counting which exploits the fact that the *width*, as well as the amplitude, of the

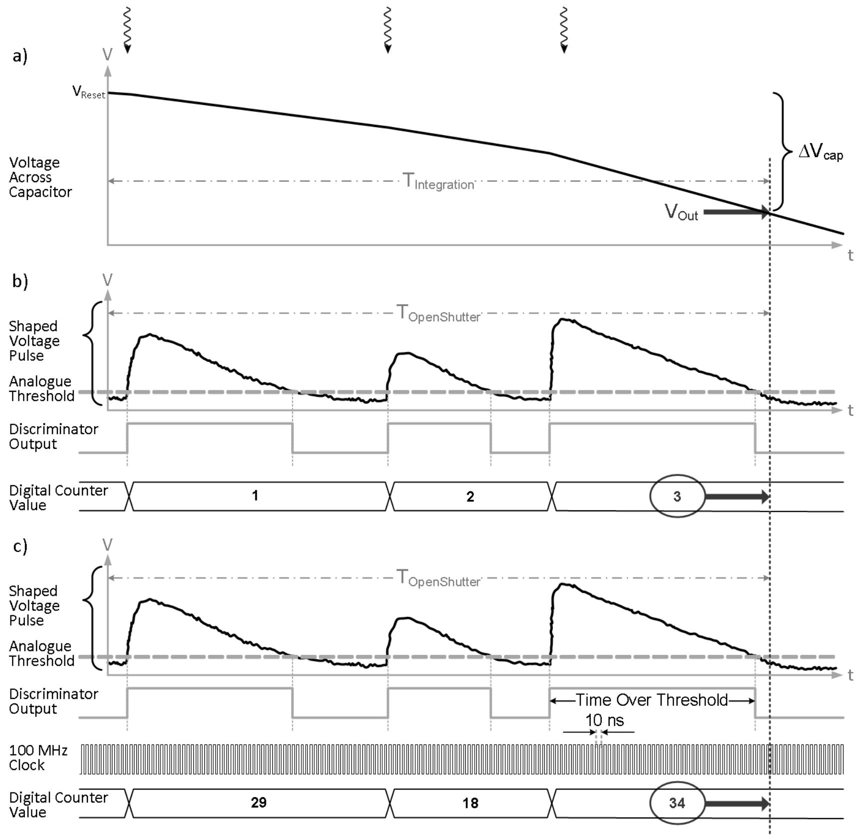


Figure 2.10: Charge processing in pixels

Processing of charge generated by the deposition of energy from three photons. **a)** Charge integration. **b)** Discrete photon counting. **c)** Time over threshold (ToT) measurement.

shaped voltage pulse is proportional to the quantity of input charge. Figure 2.10c shows a counter measuring the number of digital clock periods coincident with the discriminator output. This provides the duration of the discriminator pulse, which is also the time during which the shaped voltage is over the threshold. In this example, the counter is overwritten by the ToT value of the most recent photon event. *Thus, a ToT detector is intended to measure the energy deposited in the sensor. In this example implementation, it measures the energy deposited by a single photon.*

The appropriate choice of charge processing technique depends on the application and available resources. For example, signal integration with an analogue output can be realised in as few as three transistors [53; 54], resulting in an extremely compact, low area and low power design. This alone however, is not a compelling argument in a discussion of hybrid pixel detectors, which offer the opportunity to realise many transistors within the pixel. The main advantage of the signal integration approach is that it can handle the detection of high fluxes, provided that $T_{\text{Integration}}$ is shorter than the time it takes for the integrated signal to saturate the electronics. Photon counting, on the other hand, can experience pileup of the shaped pulses in the presence of high flux, immediately causing a form of saturation which would result in missed photon counts. Nevertheless, due to the suppression of noise and low energy fluorescence signals from threshold discrimination, photon counting provides excellent noise immunity resulting in very high quality photon detection systems whose dynamic ranges are limited only by the digital counter depth. The conclusion therefore, is that energy integrating systems can be suitable for very high flux applications; otherwise, photon counting detectors provide much higher dynamic range images. Chapter 6 will present a type of integrating photon detection mode which utilises the benefits of photon counting.

2.3.1 Analogue Frontend for Photon Counting

Figure 2.11 lists the various charge processing functions and components of the analogue frontend of a discrete photon processing system [55; 38; 45; 28].

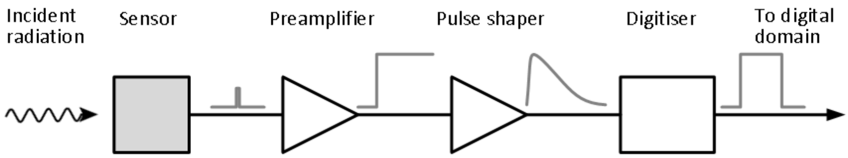


Figure 2.11: Typical components of an analogue frontend
Based on a diagram in [45].

The signal induced from the sensor is rather small and needs to first be amplified by the aptly-named preamplifier circuit. An optional shaper follows to tailor the frontend bandwidth to increase the signal to noise ratio (SNR). Finally, a digitiser converts the amplified analogue signals into a digital signal. The output of the analogue frontend feeds into digital circuits whose basic functions are to store and transfer data to the end of column.

2.3.2 Charge-Sensitive Preamplifier

The charge resultant from photon energy deposition in a silicon sensor is quite small (*e.g.* 6.14 ke$^-$ or 0.98 fC from 22.101 keV deposited by a silver Kα fluorescence photon) and collected over a very short time (a few ns). The role of the preamplifier is therefore to amplify and stretch the input signal prior to further processing by the rest of the pixel analogue frontend. Although various amplification topologies can be used to realise a preamplifier, it would be desirable to design the preamplifier to be *charge-sensitive*, such that the output depends on the input charge, and is insensitive to variable system parameters, such as detector capacitance, operating temperatures, and power consumption. Figure 2.12a demonstrates a charge-sensitive preamplifier consisting of an inverting operational amplifier (opamp) and a feedback capacitance, which results in an output voltage proportional to the input charge.

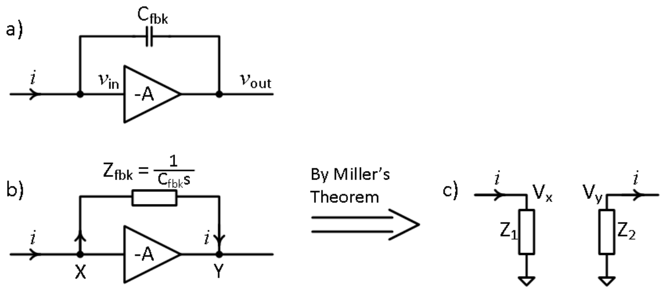


Figure 2.12: Charge sensitive amplifier with feedback capacitance

If the input of the opamp (node X in Figure 2.12) has a very high impedance (*e.g.* it is the gate of a MOSFET), then it can be assumed that all the current at X flows through the feedback path and is integrated by the feedback capacitance, C_{fbk}.

From the equivalent circuit derived from Miller's Theorem [56]:

$$Z_1 = \frac{Z}{1 - \frac{V_y}{V_x}} \tag{2.14}$$

But from Figure 2.12b,

$$V_y = -AV_x \tag{2.15}$$

where A is the opamp gain. Combining Equations 2.14 and 2.15:

$$Z_1 = \frac{\frac{1}{C_{fbk}s}}{1 - \frac{-AV_x}{V_x}} = \frac{1}{C_{fbk}s(1+A)} \tag{2.16}$$

Hence the equivalent input capacitance of Figure 2.12 is:

$$C_{in} = C_{fbk}(1+A) \tag{2.17}$$

When electron-hole pairs in the sensor separate and move towards the oppositely-charged electrodes, they induce a net current parallel to the detector capacitance. Thus the sensor can be modelled as a current source, i_{det}, in parallel with C_{det} (of Equation 2.13). Figure 2.13 shows the equivalent circuit of a charge sensitive preamplifier connected to a pn junction diode sensor.

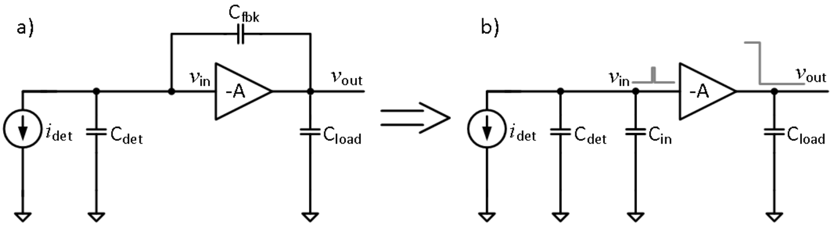


Figure 2.13: CSA with detector model

Recalling that $V = \frac{\int idt}{C} = \frac{Q}{C}$, the input voltage of Figure 2.13 is:

$$v_{in} = \frac{\int i_{det}dt}{C_{det} + C_{in}} = \frac{\int i_{det}dt}{C_{det} + C_{fbk}(1+A)} \tag{2.18}$$

The output voltage is therefore:

$$v_{out} = -Av_{in} = -A\left[\frac{\int i_{det}dt}{C_{det} + C_{fbk}(1+A)}\right] \tag{2.19}$$

If A is sufficiently large such that $C_{det} \ll C_{fbk}(1+A)$:

$$\begin{aligned} v_{out} &\simeq -A\left[\frac{\int i_{det}dt}{C_{fbk}(1+A)}\right] \\ &\simeq -\frac{\int i_{det}dt}{C_{fbk}} \qquad \text{(since A} \gg 1\text{)} \\ &\simeq -\frac{Q_{det}}{C_{fbk}} \end{aligned} \tag{2.20}$$

Thus, the output of the preamplifier is a voltage step whose amplitude is proportional to the ratio of charge induced in the sensor over a *fixed* feedback capacitance, and independent of the detector capacitance. The CSA performance is also independent of how the opamp is implemented, so long as it is correctly biased and its gain is sufficiently large to satisfy the condition $C_{det} \ll C_{fbk}(1+A)$.

Injection of test charge In addition to robustness against variable system parameters, a secondary but significant advantage of the topology depicted in Figure 2.13, is that a circuit can be added to inject a controlled quantity of charge into the preamplifier input. Consider the addition of a small capacitance, C_{test}, and a step voltage source, Δv_{test}, in parallel with the detector capacitance (Figure 2.14):

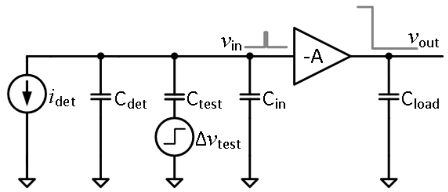


Figure 2.14: CSA with test charge injection

A controlled test charge, $Q_{test} = C_{test}\Delta v_{test}$, can thus be injected into the frontend input for test and calibration. It should be noted that C_{test} should be designed to be small to minimise its influence on the regular performance of the frontend.

Resetting the preamplified signal The charge sensitive preamplifier circuit of Figure 2.13 provides a step voltage output in response to a delta input. The addition of a parallel resistance in the feedback path, shown in Figure 2.15, provides a means to discharge the preamplifier voltage to its baseline DC value.

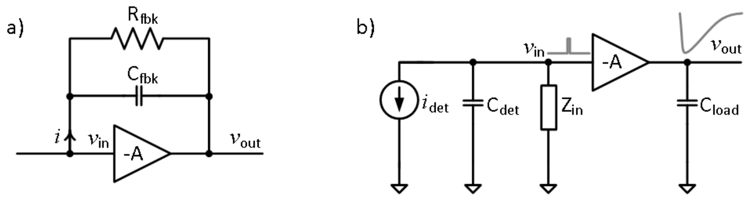


Figure 2.15: CSA with feedback resistance for pulse shaping

The rate of discharge depends on the overall impedance in the feedback path:

$$Z_{fbk} = R_{fbk} \parallel \frac{1}{C_{fbk}s} = \frac{R_{fbk}}{1 + R_{fbk}C_{fbk}s} \tag{2.21}$$

By Miller's Theorem and applying Equation 2.14, the input impedance of Figure 2.15b is:

$$Z_{in} = \frac{R_{fbk}}{(1 + R_{fbk}C_{fbk}s)(1 + A)} \tag{2.22}$$

And its output voltage is:

$$\begin{aligned} v_{out} &= -Av_{in} \\ &= -Ai\left[\frac{R_{fbk}}{(1 + R_{fbk}C_{fbk}s)(1 + A)}\right] \\ &\simeq \frac{-iR_{fbk}}{1 + \tau s} \qquad \text{if A » 1} \end{aligned} \tag{2.23}$$

The preamplifier output then becomes a voltage pulse with decay $\sim e^{(\frac{t}{\tau})}$ and the decay time constant $\tau = R_{fbk}C_{fbk}$. Typically, the faster the time constant, the higher the electronics noise.

An important characteristic of this circuit is that the rate of discharge is constant for constant feedback impedance, and hence *the width of the preamplifier output pulse is proportional to the input charge*. Although the amplitude of the preamplifier voltage pulse depends on the input charge, it also eventually reaches an upper limit depending on the preamplifier voltage headroom. Even after the output pulse has reached the maximum amplitude however, the feedback capacitor continues to integrate the remaining input charge and the output does not discharge until after the entire input signal has been integrated in C_{fbk}. Consequently, the width of the preamplifier output pulse of the circuit in Figure 2.15 is proportional to the quantity of input charge, *even beyond the linear range of the preamplifier output amplitude*.

frontend pileup Frontend pileup occurs when multiple photons arrive within a short interval, such that multiple pulses overlap before the preamplifier output is discharged to the baseline voltage. The pileup of two preamplifier pulses is depicted in Figure 2.16. There are two classifications of frontend systems with respect to pileup: paralysable and non-paralysable [28]. Paralysable systems are those for which there is no special mechanism to separate or ignore a piled-up event; thus piled-up and regularly-spaced events are treated identically. Non-paralysable systems, on the other hand, can detect the occurrence of pileup and contain extra circuits which remove a piled-up event from the processing chain. The architectures presented in this thesis are of the paralysable category. It should also be noted however that the pixels presented here are small enough to limit input flux and thus pileup is rare enough to not hinder the intended applications.

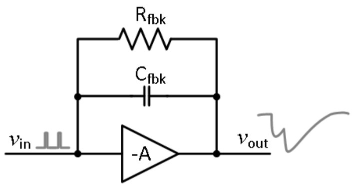


Figure 2.16: Pileup in the CSA

frontend noise Electronics noise arise from random fluctuations, such as those described in Appendix A. Often the frontend noise is quantified as an equivalent noise charge (ENC), which is the quantity of charge at the input of the preamplifier which would result in an output signal equivalent to the noise magnitude. The ENC of a frontend system depends on several factors, including the detector capacitance and the frontend shaping time. Detailed explanations on the parallel and series noise of pixel frontends can be found in [57; 58; 59; 38].

2.3.3 Pulse Shaping

The pulse shaper is a chain of filters which tailor the system bandwidth to a range of frequencies which are favourable for the signal but cut off the low frequency noise. The circuit's name stems from the fact that its bandpass filter alters the time domain shape of the preamplifier output voltage pulse.

While shapers are commonly used in hybrid pixel detector frontends targeted towards high energy physics measurements, some hybrid pixel detectors which are intended for imaging may skip the pulse shaping step. In small pixels with small detector capacitances, for example, the electronics noise may already be low enough to warrant the exclusion of a shaper, particularly since a shaper would occupy area and consume power. Furthermore, in systems which measure the preamplifier output time over threshold, the addition of a pulse shaper would reduce the system's useful range since a shaper output pulse width is not proportional to the input charge beyond the preamplifier linear range. Therefore, in small pixels (*i.e.* pixels with low input capacitance and hence low noise), particularly those which measure ToT, the output of the circuit in Figure 2.15 can be directly input to the digitiser block.

2.3.4 Analogue to Digital Conversion

One of the major benefits of the photon counting charge processing technique is that the output is digital. The digitiser is an analogue comparator which discriminates the shaper/preamplifier output pulse against a threshold voltage. The digital signal is asserted when the shaper (preamplifier) output exceeds the threshold voltage. The output of this block becomes the input to the digital domain, where the circuits process the threshold-discriminated signal according to the requirements of the applications (*e.g.* photon counting, ToT measurements, photon arrival time-stamping, energy binning, etc.).

The most important argument for photon counting frontends however, is the fact that the threshold voltage serves to truncate the signal to ignore the noise which lies below the threshold. It is for this reason that photon counting charge processing systems are often referred to as practically "noise-free" [60; 24], because the digital photon count excludes false counts resultant from noise.

3 The Medipix Family of Detectors

Modern high energy physics (HEP) experiments require a combination of specialised detectors to observe the many characteristics of particles resultant from high energy collisions. Most HEP experiments employ segmented semiconductor detectors in the components which are tasked to record particle tracks. Hybrid pixel technology provides a means to quickly, cleanly, and accurately record the presence of particles. By the end of the 1990's, several hybrid pixel readout chips had been developed and were successfully taking measurements at CERN [8; 61; 62; 63]. Since γ-ray sources had been used to calibrate these hybrid pixel detectors, it stood to reason that the detectors could also be used for γ-ray detection and ultimately, imaging. However, as the specifications for CERN's HEP experiments required rectangular pixels and external triggering, these particular detectors were not quite appropriate for imaging, for which square pixels and electronic shuttering would be better suited.

The Photon Counting pixel readout Chip (PCC), which would later be known as Medipix1 [64], was thus developed in 1997 as a prototype to demonstrate that a photon counting, hybrid pixel detector could be used in X-ray imaging applications. The project involved a collaboration of several institutes, of which CERN was a member. The readout ASIC was implemented in a 1 µm Self-Aligned Contact CMOS process (which at the time was the highest density commercial process available with component densities comparable to those of standard 0.6 µm CMOS processes [65]), and consisted of 64 by 64 square pixels measuring 170 µm in side-length. Each pixel contained a preamplifier, a voltage threshold discriminator, and a 15-bit counter which recorded the number of preamplifier output pulses whose amplitudes exceeded the threshold voltage. The 15-bit counter was implemented as a linear feedback shift register (LFSR) whose output was a pseudo-random code[1]. Each PCC image reported the intensity of photons

[1] Digital data is typically encoded in binary code, which is a universally understood pattern. A pseudo-random pattern, however, does not correspond to conventional binary code and digital operations (such as arithmetic) cannot be directly performed on the data without first decoding it to a standard binary format. The advantage of the LFSR structure is that the same register can be used for data transfer with minimal hardware reconfiguration; the drawback is that because the LFSR increments in a pseudo-random code, its output must be decoded off-chip, usually using a lookup table. Depending on the readout system resources, this extra decoding step could be considered a burden.

incident on each pixel by providing a count of the number of times charge collected from the sensor exceeded a threshold value. If the threshold was programmed to be higher than the electronics noise floor, then the number stored in the counter corresponded to signals which genuinely resulted from photon detection, rather than false signals resultant from noise. Because of this, the exposure time could be set for very long periods to obtain high contrast images without risk that contributions from noise or dark currents would saturate the pixel storage structures. Furthermore, because the data was digitised within the pixel, the data did not degrade during transfer.

Images taken using PCC, such as the example shown in Figure 3.1b, proved that a photon counting hybrid pixel detector specified for imaging could provide clean (*i.e.* more or less free of noise counts) images with a very high dynamic range. Measurements confirmed that the removal of background and noise contributions from the signal through threshold discrimination meant that different material densities, even in low-contrast objects, could be discerned using much lower X-ray doses to achieve comparable image quality as integrating detector technologies [66]. These promising results lead to a series of hybrid pixel detectors under the project name Medipix.

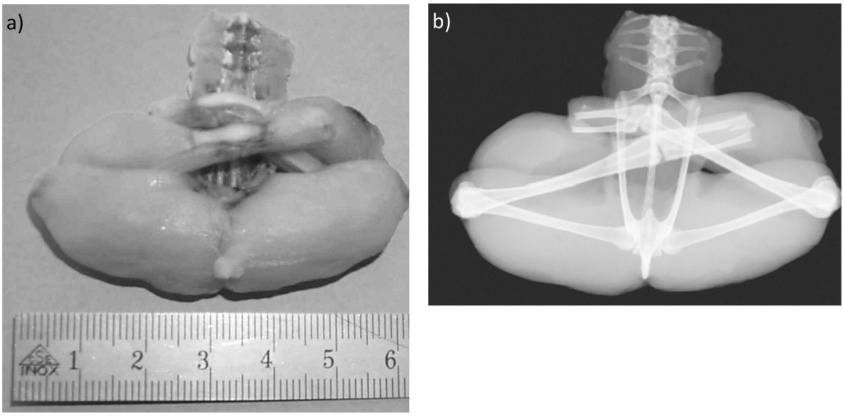


Figure 3.1: X-ray image taken with PCC

X-ray image taken using the Photon Counting Chip bump bonded to a silicon sensor [67]. **a)** Photograph of the original specimen (frog legs). **b)** X-ray image taken with PCC (Medipix1).

3.1 Medipix2 and Timepix

Following the successful demonstration of hybrid pixel detector-based X-ray imaging using PCC, the Medipix2 Collaboration was formed to develop a new chip with many more and much smaller pixels. The first Medipix2 ASIC [68] was designed in 2000 for a 0.25 μm standard CMOS process, with 256 by 256 square pixels originally targeted to occupy an area of 50 μm by 50 μm but later increased to a 55 μm side-length to accommodate an overflow prevention circuit[2]. Each pixel contains a preamplifier (which can be programmed to accept either positive or negative charge input), two threshold discriminators, and a single 13-bit LFSR counter which increments for every preamplifier output pulse whose amplitude lies within the energy window defined by the two discriminators. A slightly modified version (a "respin") of the design was released in 2001, followed by two fully revised designs called Mpix2MXR1.0 and Mpix2MXR2.0, with improved temperature and radiation dose insensitivity, and digital glitch recovery [69]. Since its release in 2005, the Mpix2MXR2.0 ASIC been used in a multitude of charge processing detector systems, including hybrid pixel detectors with semiconductor sensors, but also systems in which the bare Medipix2 ASIC pixel electrodes were left exposed to collect charge generated by photons incident on a microchannel plate placed above the ASIC [70], or to collect charge generated in photon interaction with ionising gas above the ASIC [71; 72]. An overview of Medipix2, its history and its applications, along with a list of associated projects and their publications, can be found in [60].

The Timepix ASIC (Paper I, [73]) is a variant of Mpx2MXR2.0 with complementary features implemented with the addition of a digital clock. Its design in 2006 was at the request of the European Union's Detector R&D Towards the International Linear Collider (EUDet) Collaboration, who required an ASIC which would act as the anode in prototype gas-filled detectors [60; 74]. The Timepix ASIC utilises most of the analogue frontend from Mpix2MXR2.0, but has one, rather than two, threshold discriminator. The digital blocks, containing a 14-bit LFSR counter, can be programmed to operate in one of three operation modes: photon counting mode, time of arrival (ToA) mode, and time over threshold (ToT) mode. In ToA mode, the counter commences counting of (up to) 100 MHz digital clock cycles

[2] The 55 μm pitch has since become somewhat of a standard amongst Medipix chips.

at the assertion of the threshold discriminator output to timestamp the arrival of a photon. In ToT mode, the counter counts the number of 100 MHz digital clock cycles coincident with the asserted discriminator output pulse to record the width of the preamplifier output, which is proportional to the sensor signal.

The versatility of the Mpx2MXR2.0 and Timepix ASICs (*e.g.* compatibility with a variety of semiconductor sensors and gas-filled detectors), along with the ability to tile multiple chips for larger area arrays, has permitted many evaluation studies of new sensor materials and detector configurations. For example, Figure 3.2 is an image taken using a two by two array of tiled Timepix ASICs bump bonded to CdTe.

Figure 3.2: X-ray image taken with Timepix CdTe quad

In Medipix nomenclature, a quad consists of four readout ASICs tiled in a two by two array and bump-bonded to a large area sensor. The X-ray image here was taken by a quad of Timepix ASICs bump-bonded to a CdTe sensor. The ASICs were programmed to operate in photon counting mode. The high dynamic range of the detector is demonstrated by the imaging of different materials attenuating the photons. It should be noted that CdTe is an extremely difficult material to grow and the point defects in the image are due to the fact that the sensor technology is still under research and development. However, this also clearly demonstrates that the Medipix family of chips are used to prototype systems with new sensor materials. Image courtesy of M. Fiederle, Albert-Ludwigs-Universität Freiburg.

3.2 Medipix3

The occurrence of charge sharing (where the charge generated by energy deposition from a single photon is collected by a cluster of pixels) poses a limitation on both the spatial and energy resolutions of finely segmented semiconductor detectors. This is particularly an issue in systems which wish to extract information regarding the deposited spectra, as charge sharing distorts the proportional relationship between the charge which is processed by a frontend, and the energy which had actually been deposited in its associated pn junction volume [75; 76]. A prototype ASIC was developed in 2006 which contained a network of eight by eight small pixels with inter-pixel communication [77]. The pixel networks were able to accumulate the charge collected by a neighbourhood cluster of pixels, and then assign the full set of charge to a single pixel frontend using a winner-take-all algorithm. Evaluation of this novel scheme using charge injected by test pulses demonstrated that it could successfully mitigate charge sharing effects to reconstruct a much more accurate record of the deposited spectra.

The Medipix3 Collaboration was formed in 2006 to establish a new member of the Medipix family: Medipix3 (Papers III to VI, [78; 79; 80; 81]), a photon counting hybrid pixel detector with inter-pixel communication and charge-summing capabilities. Like its predecessors, Medipix3 contains 256 by 256 pixels of 55 μm pitch. In order to accommodate the many new complex features and modes, Medipix3 is implemented in a standard CMOS 130 nm process, which permits much higher transistor densities than the 250 nm technology used by the previous Medipix chips. The Medipix3 frontend consists of a preamplifier, a shaper (to convert the preamplifier output to currents which can then be summed with currents from neighbouring pixels), and two threshold discriminators. Details on the Medipix3 frontend and the charge summing algorithm are presented in [38]. This thesis will focus on an explanation of the compact reconfigurable digital counters which were designed for the Medipix3.0 and Medipix3.1[3] ASICs.

[3] Medipix3.1 is a slightly modified version of Medipix3.0, with changes to three mask layers to disconnect a leaky electrostatic discharge protection diode and to raise the threshold voltage of transistors in analogue multiplexors in order to reduce leakage current. These modifications affect the analogue frontend but the digital counters are identical in both versions.

3.2.1 The Medipix3 Photon Counters

The Medipix3.0 ASIC was submitted for fabrication in 2008. Each pixel contains data structures designed to provide the following user-specified functional requirements:

- Selectable counting and serial shifting modes
- Configurable depth (2x1-bit, 2x4-bit, 2x12-bit, or 1x24-bit)
- Counter overflow prevention
- Continuous open shutter capability
- Fast clearing
- Binary format output

Figure 3.3 depicts the basic architecture of a four-bit binary ripple counter which can be reconfigured for serial shifting using multiplexors (MUX) at the inputs of the flip flops. The pixel consists of 24 such custom-designed flop flops, arranged as two 12-bit chains (Paper VI, [81]). Each chain is associated with the output of one of the two pixel analogue threshold discriminators. When a 1-bit counter depth is selected, the multiplexed pixel output selects the least significant bit of the structure and ignores the higher order bits. Similarly, when a 4-bit depth is selected, the pixel output MUX taps the Q port of the 4th flip flop. When the 24-bit depth is selected, the outputs of the 12th bit of one counter connects to the inputs of the 1st bit of the other counter using an extra set of MUXes at the input of the latter counter; the entire 24-bit chain is then associated with the output of a single analogue discriminator (the other discriminator is ignored).

In *counting mode* (Figure 3.3b), the discriminator output is used as the CountClk and the connected flip flops increment in a conventional binary code format for each photon detected by the frontend. In *serial shifting mode* (Figure 3.3c), the Q output of each flip flop is connected to the D input of its successor, and the values shift through the flip flops with an external ShiftClk signal. In a special mode called *continuous read-write (CRW) mode*, the two flip flop chains alternate between counting and serial shifting, such that there is no readout "deadtime" (*i.e.* the electronic shutter need not close while reading out the pixel data). In this mode, both counters are associated with the same discriminator output.

To economise on the physical area occupied by a flip flop, each bit is implemented in the custom-designed structure shown in the schematic of Figure 3.5b. Special care must be taken in the control of this circuit when switching between the various modes and configurations. Although the operation of these counters is quite complex and requires rather complicated control circuits both within the pixel and at the end of column blocks, its major advantage is that it meets all the feature requirements listed on page 47 and with meticulous manual layout, fits in the allocated area. Details on the design and layout of these counters are presented in Papers III & VI, as well as [82]. Figure 3.4 shows the layout of the counters and their control circuits.

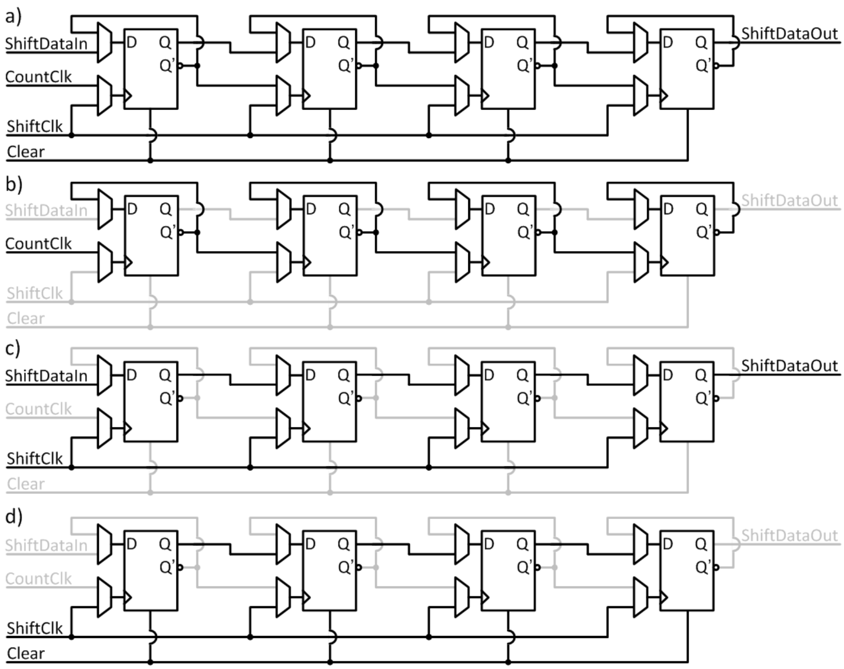


Figure 3.3: Configurable binary ripple counters/shift registers

a) 4 D-type flip flops with 2-to-1 multiplexors (MUX) at each input to select between binary ripple counting or serial shifting. **b)** Binary ripple counter mode. **c)** Serial shift register mode. **d)** Clearing the flip flops in serial shift register mode.

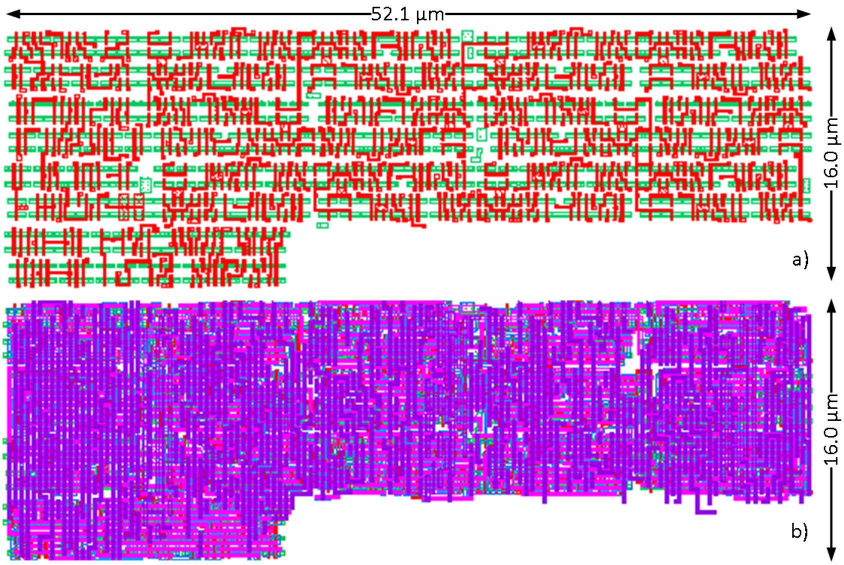


Figure 3.4: Layout of the Medipix3 counters

Layout of the Medipix3.0 counters and control logic. These ∼1350 transistors occupy 23.4% of the 55^2 μm^2 pixel area, with a local device density of 1.9 transistors/μm^2. Each cell was custom-designed and manually placed and routed in the optimal density method described in Paper III. **a)** RX and PC (active area and polysilicon) visible. **b)** RX, PC, M1, M2, and M3 (active area, polysilicon, and first 3 out of 8 metal layers) visible.

COUNTER DESIGN ISSUES Several design issues were observed during testing of the Medipix3.0 ASIC, including corrupted initialisation of the digital counters at the beginning of frames. Figure 3.5b shows the gate-level schematic of a single bit. The Mode signal selects the MUX paths which determine whether the structure is in counting mode or serial shifting mode. When Mode = 1′b0, the bit chain is a serial shift register; when Mode = 1′b1, the chain is a binary ripple counter. The D flip flop is implemented as a pair of master-slave loops. Each loop consists of back-to-back inverters which store a static digital value until the path is overwritten by a value driven through the transmission gate switches whose states are controlled by the flip flop Clk input. The Mode and ShiftClk signals are generated by control circuits in the pixel based on column signals from the end of column block.

The MUXes and logical switches of Figure 3.5 are implemented as transmission gates, which occupy much less layout area than their static CMOS logic gate counterparts, but suffer from signal feedthrough[4] due to their inherent bidirectional nature. Due to limited layout area, some signal paths contain several transmission gates in series without intermediate buffering.

Consider the schematic of the Figure 3.5c. Because ShiftClk comes from a combinational circuit in the pixel composed of static CMOS logic gates, its drive strength is stronger than the signal through the Q′(n) node, which must drive TG7 (transmission gate 7) as well as TG5 followed by TG1. When the transmission gates are fully open or closed, this difference in drive strength does not affect the circuit function. However, during the transition between modes, when the transmission gates are all partially open, the difference in drive strength can leak enough signal through TG8 to reverse the signal direction of TG7 and result in a random value at nodes Clk(n+1) and Q′(n). The randomness of the resultant value also depends on the magnitude of digital voltage supply drop due to instantaneous power consumption while the counters are switching modes. This signal contention occurs whenever the structure switches from *serial shifting mode to counting mode*: during serial shifting, all the bits are loaded with 1′b0 at Q (and hence Q′ = 1′b1), and during the transition between serial shifting and counting, ShiftClk is always 1′b0 by design. However, Figure 3.5d indicates that the signal contention *does not* occur when a Clear command is inserted *between* serial shifting (for data readout) and counting mode (for photon counting). Also by design of the pixel control circuits, ShiftClk is always held high during the falling edge of the Clear signal, and thus there is no contention between TG7 and TG8 during the transition from the Clear command to counting mode.

Therefore, the workaround against data corruption between readout and photon counting operations is to execute a Clear command prior to each frame. While this workaround reliably initialises the counters in sequential read-write operation, it unfortunately cannot be used in CRW mode since the assertion of the Clear signal resets *all* counter bits to 24′b0. Thus CRW mode operation is disabled in Medipix3.0 and Medipix3.1.

[4]In proper electronics engineering terminology, the correct term for this effect should be "charge sharing". However, since the same term is already used in this thesis to describe a phenomenon in the sensor, we use the unusual term "signal feedthrough" to describe charge sharing in transmission gates to avoid confusion.

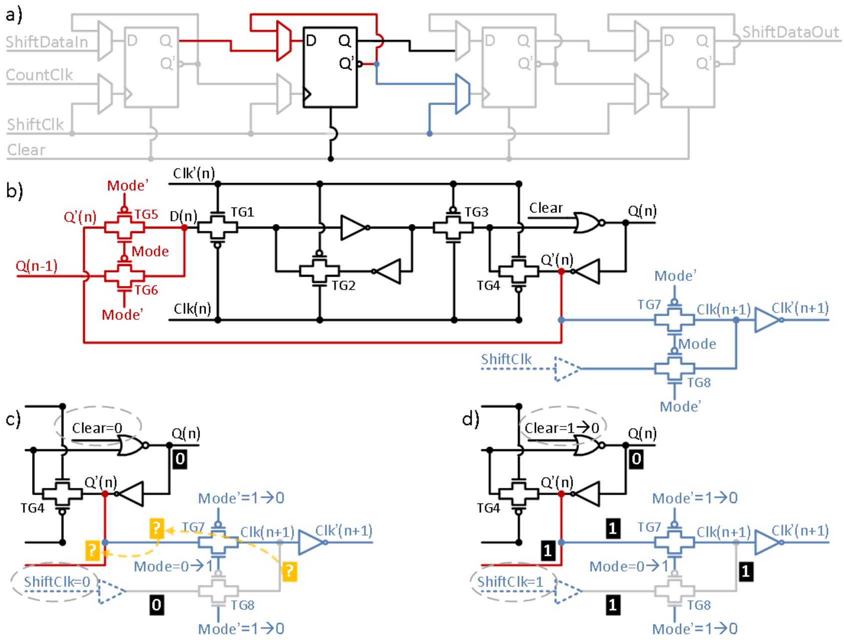


Figure 3.5: Schematic of a custom-designed bit of the Medipix3 counters

a) Block-level schematic of a chain of Medipix3 counter bits. **b)** Gate-level schematic of a Medipix3 counter bit. **c)** Signal propagation in the Clk input MUX of the (n+1)th bit after a transition from serial shifting (readout) mode to counting mode. **d)** Signal propagation in the Clk input MUX of the (n+1)th bit after a transition from Clear mode to counting mode. When the active high Clear signal is asserted, the configuration MUXes place each bit in serial shifting mode, and a "0" is written to the slave loop of the D flip flop via the NOR gate. A single toggle of the ShiftClk then pushes that "0" to the master loop of the subsequent bit to initialise both loops in the flip flops.

In spite of the need to disable CRW mode, the counters in Medipix3.0 and Medipix3.1nevertheless function reliably in sequential read-write operation with this workaround, and high dynamic range images such as that in Figure 3.6 can be taken with a 24-bit counter depth and very long open shutter periods.

Figure 3.6: X-ray image taken with Medipix3.1

Image composed of 12 tiled X-ray images of a flower. Each tile was taken using a Medipix3.1 assembly bump bonded in fine pitch mode with a 300 μm silicon sensor. In each tile, the flower was irradiated by an X-ray tube with a W anode and 150 μm Be window set to 20 kV and 1 s exposure time. The detector was programmed to run in high gain mode [38] with the threshold set to 7 keV and counter depth configured for a 24-bit length to provide high dynamic range. Image courtesy of S. Procz, Albert-Ludwigs-Universität Freiburg [83].

proposed solution A potential solution to the counter data corruption which is caused by signal feedthrough incorporates the already proven workaround described in the previous subsection. In the existing layout (shown in Figure 3.4), the column-level Clear signal is buffered at the pixel level, and to reduce the instantaneous current consumption during a Clear command, the column-level Clear signal is copied into two separate signals which *separately control* each of the 12-bit counter chains in the pixel. The proposed solution is to add an extra Clear signal in the global column lines in order to separately reset the two 12-bit chains. In this way, the two 12-bit chains can be independently reset at the beginning of each frame during CRW mode. This solution would require no modifications to the existing transistor layout in the pixel and minor changes to the routing of the existing Clear signal buffers, as well as a change in logic in the end of column buffers.

3.3 Summary of Medipix ASICs

Table 3.1 summarises the various Medipix chips. Although Dosepix is not strictly speaking a member of the Medipix chipset, it originated from the Medipix project and is included as a final row in the table.

Chip	Technology Node	No. of Pixels & Pixel Pitch	Active Area	Buttable	No. of Acquisition Modes	Special Modes	Deadtime-Free Readout	Counter Over-flow Control	Fast Data Reset	Digital Output Format	No. of Energy Thresh.	Event Memory Size per Pixel	Main Function(s)
Medipix1	0.6 µm (equiv.), 2 metal layers	4096 of 170 µm	1.18 cm^2	No	1	No	No	No	No	Pseudo random	1	32766	**Imaging** by single photon counting
Medipix2*	0.25 µm, 6 metal layers	65536 of 55 µm	1.98 cm^2	3 sides	1	No	No	Yes	No	Pseudo random	2	11810	**Imaging** by single photon counting with energy window discrimination
Timepix	0.25 µm, 6 metal layers	65536 of 55 µm	1.98 cm^2	3 sides	3	No	No	Yes	No	Pseudo random	1	1† or 11810	**Imaging** by single photon counting, **particle tracking** by particle arrival timestamping, or time over threshold measurements
Medipix3*	0.13 µm, 8 metal layers	65536 of 55 µm or 16384 of 110 µm	1.98 cm^2	2, 3 or 4 sides	2‡	2 gain modes	Disabled	Yes	Yes	Binary	1, 2, 4, or 8	1, 16, 4096, or 16.8M	**Imaging** by single photon counting with interpixel communication to mitigate charge sharing effects
Dosepix	0.13 µm, 8 metal layers	256 of 220 µm	12.4 mm^2	3 sides	3	2 power modes	Yes	Yes*	Yes	Binary	1 analogue and 16 digital	1M, 256, or 1**	**Dosimetry** by time over threshold measurements and online energy binning

Table 3.1: Main attributes of the Medipix chipset

*Multiple iterations of the Medipix2 and Medipix3 designs exist. The values reported here are based on Mpix2MXR2.0 and Medipix3.1.

†Only one event per frame is recorded in ToA and ToT modes.

‡Single pixel mode and charge summing mode. The other combinations of Medipix3 modes are taken into account in the other columns.

*In energy binning mode.

**In energy binning mode, photon counting mode and energy integration mode, respectively.

4

A Hybrid Pixel Detector for Personal Dosimetry and kVp Metering

The previous chapters demonstrated the utility of hybrid pixel detectors for the clean detection of X-rays and γ radiation. The fact that the sensor and the ASIC are two distinct components allows separate optimisation of both modules. The implementation of the ASIC in a deep sub-micron technology, for example, permits high transistor densities while keeping the power budget low. Moreover, the availability of the entire pixel area for photon signal processing presents the opportunity to implement complex circuits which provide clean photon detection through quantum counting, as well as spectroscopic information on the deposited energy through time over threshold (ToT) measurement. Segmentation of the detector into small channels reduces the flux and input capacitance at each frontend input, while achieving a larger overall sensitive area when combining the data of many pixels. Hybrid pixel detectors are in fact suitable for versatile radiation detection in both high and low flux environments because the flux at each frontend is limited to permit accurate energy measurements in high flux cases, while the larger overall sensitive area provides sufficient sampling of statistics in low flux cases. Due to the small detector capacitance at the frontend input, the frontend noise is also very low, which permits reliable detection of a large X-ray energy range. Accurate, reliable, and real-time knowledge of the intensity and energy of impinging photons could certainly be extended to applications beyond X-ray imaging.

This chapter explores the application of hybrid pixel detector photon processing capabilities towards 1) personal dosimetry and 2) quality assessment of medical X-ray tubes (in particular, X-ray tubes for mammography). The second half of the chapter will present the ASIC of Dosepix, a hybrid pixel detector designed to be used in an active personal dosimeter (APD) and in an X-ray tube peak voltage (kVp) meter.

4.1 Requirements of an Active Personal Dosimeter

An active personal dosimeter (APD) is a portable radiation monitor which is worn by personnel whose work activities involve exposure to ionising radiation, for example at medical diagnostics facilities. Recalling the discussion of Chapter 1, APDs provide immediate radiation dose and dose rate readings. Most countries have government groups which regulate radiation protection practices. While the exact rules regarding radiation protection differ between countries, most governments refer to guidelines and recommendations outlined by the International Commission on Radiological Protection (ICRP), use radiation dose data published by the International Commission on Radiation Units and Measurement (ICRU), and when assessing new radiation monitoring devices, adhere to the standards defined by the International Electrotechnical Commission (IEC) and the International Standards Organization (ISO).

Radiation monitoring devices fall under a large range of categories. The principal application proposed in this thesis focuses on an APD which provides real-time readings of personal dose equivalent, $H_p(d)$, and personal dose equivalent rate, $\dot{H}_p(d)$, *specifically for ionising photon dose*. The term active implies that the dosimeter should provide an immediate dose (or dose rate) reading, without the need for a separate reader machine. The APD design of this thesis is intended to:

- be a portable device to be worn on the person,
- measure the personal dose equivalents, $H_p(10)$ and $H_p(0.07)$, and the personal dose equivalent rates, $\dot{H}_p(10)$ and $\dot{H}_p(0.07)$, from external X and γ radiation,
- provide a digital reading of real-time dose measurements, and
- sound alarms in case of abnormal readings.

Table 4.1 lists some of the technical requirements of the hybrid pixel detector-based APD design with the above features and compliant with IEC standards regarding directly readable personal dosimeters for photon radiation [84].

The idea of using a photon counting, segmented semiconductor detector such as Medipix to implement a low energy personal dosimeter was studied in [24], leading to the proposal for a new hybrid pixel detector (Paper VII, [85]) to be designed specifically for this, and related, applications

	Design Requirement	Target Specification	Response Tolerance	Comments
1	Battery operated	100 h continuous operation on battery		Single battery to supply all components in the APD
2	Form factor	Maximum dimensions: $15\,\mathrm{cm} \times 3\,\mathrm{cm} \times 8\,\mathrm{cm}$ Maximum volume: $300\ \mathrm{cm}^3$		
3	Mass	Maximum mass: 350 g		
4	Dose measurements of low energy X-rays	20 keV to 150 keV, for 0^o to $60\ ^o$ incidence angles	-29% to +67%	Workplace example: medical diagnostics facility
5	Dose measurements of high energy X and γ rays	80 keV to 1.5 MeV, for 0^o to $60\ ^o$ incidence angles	-29% to +67%	Workplace example: industrial polymer modification facility
6	Dose rates	0.5 µSv/h to 1 Sv/h	$\pm$20%	
7	Ambient temperature	Indoor use: 5^oC to 40^o, outdoor use: -10^oC to 40^o	$\pm$15%	
8	Alarm and response time	$\leq$10 s waiting time to alert $\dot{H}_p(10) \geq 100\,\mu\mathrm{Sv/h}$	$\pm$20%, (if delay >1 s, extra dose <10 µSv)	
9	Readout deadtime	0 s		APD may not halt dose detection, even during readout

Table 4.1: APD design requirements

Note: target specifications and tolerances as defined by international standards [84].

[86; 87]. Design parameter choices for the hybrid pixel detector-based APD depend on the requirements of Table 4.1. The appropriate pixel size, for example, depends on tradeoffs between limiting frontend input flux (to avoid frontend pileup), reducing the frontend noise (to improve energy resolution and detection of very low energy X-rays), and providing adequate physical area to realise the required functionality. Similarly, the number of pixels in the matrix is a tradeoff between the contending need for sufficient overall sensitive area to sample the radiation field, and the need to limit power consumption.

The APD will consist of multiple hybrid pixel detectors bump bonded to 300 μm silicon sensors. Some of the sensors will be covered by filter materials to filter out low energy photons from the photons which reach the detector (to improve measurements of high energy photons). The geometry of the filter is designed to account for different angles of incidence, and the energy deposited in the silicon by photons arriving at an angle with respect to the sensor are well modelled in the proposed dose reconstruction [25; 88]. The following subsections provide a discussion leading to the design specifications of the energy binning mode of the APD hybrid pixel detector ASIC.

4.1.1 *Photon Interaction with Tissue*

The International Commission on Radiation Units and Measurement (ICRU) definition of a tissue-equivalent phantom has a density of 1 g/cm^3 and is composed of 76.2% oxygen, 11.1% carbon, 10.1% hydrogen, and 2.6% nitrogen [89]. Figure 4.1 shows the energy-dependent mass attenuation coefficients for tissue with this composition. Since photon interaction with silicon is different from photon interaction with tissue, knowledge of the number of incident photons as well as the deposited photon energy are important in the accurate reconstruction of personal dose equivalent and personal dose equivalent rate using a silicon-sensor-based dosimeter.

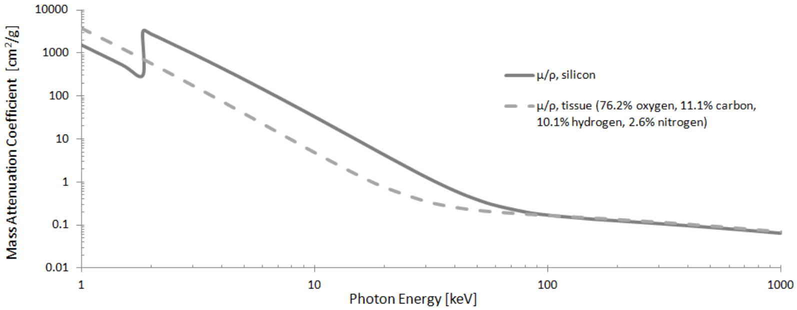


Figure 4.1: Photon attenuation in tissue and silicon

Total mass attenuation coefficients (including coherent scattering) of photon interaction with tissue and silicon. Tissue density (1 g/cm^3) and composition as defined by the ICRU [17]. Data from the National Institute of Standards and Technology XCOM database [42]

4.1.2 Typical Photon Fluxes to be Handled by APDs

Figure 4.2a plots the personal dose equivalent of photons reported by the ICRU [17]. This data is provided as a ratio of personal dose equivalent at a given tissue depth over photon fluence, where the fluence, Φ, is the number of photons incident per unit area [17]. Using the ICRU-reported data of Figure 4.2a, the photon flux absorbed by the tissue, $\dot{I}_{\mathrm{tissue}}$, can be derived for a given tissue depth, d, dose rate, $\dot{H}$, and photon energy:

$$\begin{aligned} \dot{I}_{tissue} &= \frac{I_{tissue}}{t} \\ &= \frac{\Phi A}{t} \\ &= \left[\frac{H_p(d)}{\Phi}\right]^{-1} A\dot{H} \end{aligned} \tag{4.1}$$

where I_{tissue} is photon intensity absorbed by tissue. Dividing the intensity by time, t, provides the photon rate (*i.e.* the flux). Recalling Equation 2.6 from Chapter 2, the incident photon flux, $\dot{I}_o$, can be backcalculated from the absorbed flux:

$$\dot{I}_o = \frac{\dot{I}_{tissue}}{1 - e^{-(\frac{\mu}{\rho})\rho d}} \tag{4.2}$$

where (μ/ρ) is the absorber mass attenuation coefficient, ρ is the absorber density, and d is the absorption depth. $\dot{I}_o$ is plotted as a function of photon energy in Figure 4.2b for an example dose rate $\dot{H}$ = 1 Sv/h.

With knowledge of $\dot{I}_o$, the flux of 25 keV photons (for example) arriving at the frontend of square pixels with different areas is shown in Figure 4.2c. The smaller the pixel area, the lower the flux to be processed by the associated frontend. The probability of frontend pileup, P_{pileup}, can be roughly approximated by [90]:

$$\begin{aligned} P_{pileup}(L) &= 1 - P_0(L) \\ &\approx 1 - \left[\frac{\lambda}{(\lambda - \lambda^2\delta)[1 + \delta(\lambda - \lambda^2\delta)]} e^{-\lambda^2 \delta L}\right] \end{aligned} \tag{4.3}$$

where $P_0(L)$ is the probability of no pulses coinciding when there are λ Poisson-distributed pulses of width δ occurring during the interval L. The secondary plot in Figure 4.2c plots Equation 4.3 for 25 keV photons incident on a 300 µm-thick silicon sensor, for various side-lengths of square pixels. When pileup occurs, the frontend output pulses of multiple photons become merged. In the dose reconstruction algorithm which will be discussed later in this chapter, occasional pileup does not affect the accuracy of the estimated dose, however when pileup becomes frequent, it can lead to an overestimate in dose.

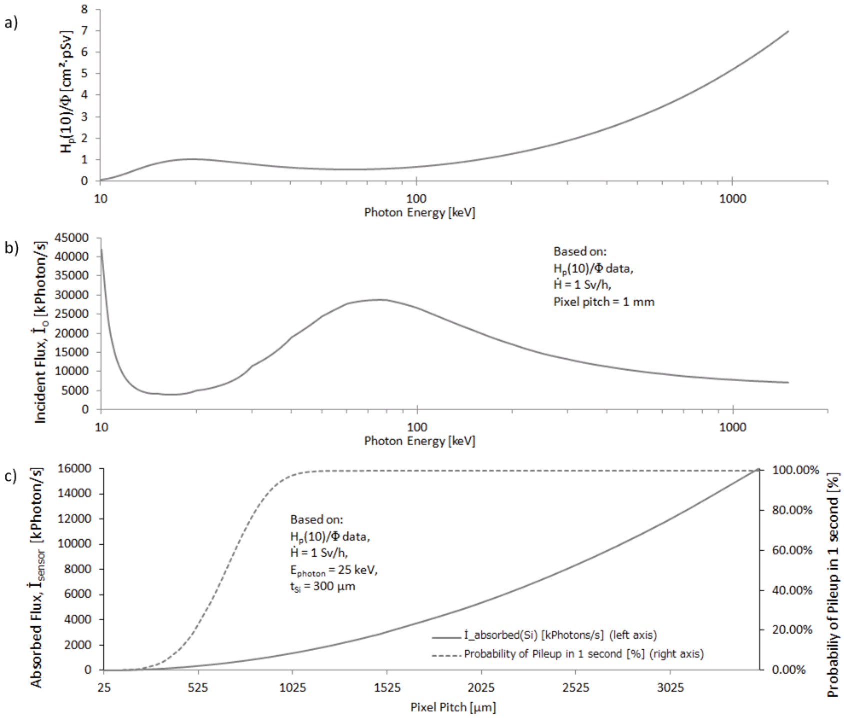


Figure 4.2: Personal dose equivalent of photons

a) Plot of $H_p(10)/\Phi$ versus photon energy. Angle of incidence = 0^o. Data from the ICRU [17]. **b)** Photon flux incident on a 1.0 mm^2 pixel for an example dose rate of 1 Sv/h, calculated from Equations 4.1 and 4.2. The tissue material composition and mass attenuation coefficients are based on the values outlined in Figure 4.1. Note: y-axis presented in 1000 Photons/s. **c)** Flux absorbed by a 300 µm thick silicon sensor, calculated from Equation 2.6 based on $H_p(10)/\Phi$ data for 25 keV photons depositing 1 Sv/h. The probability of frontend pileup from Equation 4.3 is shown on the right axis. For this plot, $\lambda = \dot{I}_{sensor}$, $\delta = T_{pulse} = 2$ µs (the frontend pulse processing time for charge from a 25 keV photon), and L = 1 second. The plot indicates that, for 25 keV photons depositing 1 Sv/h, there is more than 10% probability of pileup in pixels with side-lengths greater than 420 µm, assuming square geometry.

4.1.3 Dose Reconstruction from Deposited Energy Spectra in a Sensor

The APD design aims to reconstruct personal dose equivalent and personal dose equivalent rate using multiple hybrid pixel detectors which record photon energies deposited in 300 µm-thick silicon sensors through time over threshold (ToT) measurements. A method of dose reconstruction was developed in [25].

Figure 4.3a shows a simulation of the spectrum of energy deposited in a 220 µm by 220 µm pixel. This simulation of photons from an ^{241}Am source depositing their energies in a 300 µm silicon sensor takes into account the different interaction mechanisms between photons and silicon, including absorption, scattering, fluorescence, and charge sharing. The dose reconstruction method of [25] was devised using simulation data such as this, in combination with measurement data using a Timepix assembly with silicon.

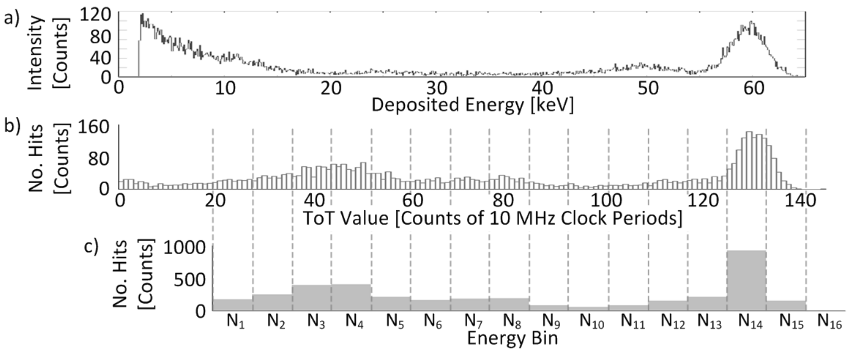


Figure 4.3: Binning ToT measurements to reconstruct dose

a) Simulation of the spectrum of energy deposited in a 220 µm by 220 µm by 300 µm silicon sensor, when irradiated by an^{241}Am source. Data from Gabor [91]. **b)** A histogram of data from 4000 ToT measurements recorded by a single Dosepix pixel with a 300 µm thick silicon sensor, irradiated by an ^{241}Am source. These ToT measurements are based on a 10 MHz reference clock. Example energy bin definitions are presented. **c)** The data from **b** sorted into 16 energy bins.

Figure 4.3b plots measured ToT data from a hybrid pixel detector with a silicon sensor without any filters. Since ToT is proportional to energy deposited in the sensor, this ToT information can be used to estimate the photon energy deposited in the tissue of the APD wearer. Practically speaking, off-chip processing of the data in Figure 4.3b would consume a lot of time and system resources. The APD will therefore contain on-chip circuits which automatically pre-sort the data into energy bins, where the energy bin limits are defined by digital ToT threshold values. The output of the chip energy bin registers would provide a count of the total number of photons absorbed by the sensor, as well as the spectroscopic classification of each photon. Figure 4.3c shows the data of Figure 4.3b sorted into an example of 16 energy bins. The equivalent dose of energy deposited in tissue can be estimated by a combination of the number of counts in each bin, N_i, of the APD hybrid pixel detector assemblies with various filters on top of the silicon sensors [25]:

$$D = \sum_{i=1}^{16} \alpha_i \cdot N_i^{air} + \sum_{i=1}^{16} \beta_i \cdot N_i^{Filter_1} + \sum_{i=1}^{16} \gamma_i \cdot N_i^{Filter_2} + ... + \sum_{i=1}^{16} \zeta_i \cdot N_i^{Filter_{n-1}} \tag{4.4}$$

The automatic on-chip pre-classification of detected photons into energy bins allows a microcontroller to quickly and accurately reconstruct personal dose equivalent [25; 88; 91; 92]. Moreover, frequent readout of chip data (*e.g.* once per 10 s) with controlled exposure periods (*i.e.* controlled with an electronic shutter) permits the real-time calculation of personal dose equivalent rate.

4.1.4 Dose Reconstruction Response

Figure 4.4 shows the response of simulated reconstructed doses which would be measured by a 220 µm by 220 µm pixel with a 300 µm silicon sensor. The response, R, is the ratio of reconstructed dose over actual dose. The pixel model is based on frontend pulse durations from schematic simulations of the frontend which will later be presented in Chapter 5, as well as predictions on the detector energy resolution based on measurements from Timepix in time over threshold (ToT) mode [25]. The reconstructed dose in the pixels overestimates the real dose in cases of high flux because of the superposition of preamplifier pulses from frontend pileup results in false ToT detection of high energy photons, which skews the dose estimate to a higher value. However, Figure 4.4a shows that, for the IEC-specified photon energy ranges and dose rates (of Table 4.1), the reconstructed dose has an extremely flat response which lies well within tolerable deviations from unity. In fact, Figure 4.4b shows that the reconstructed dose continues to be within IEC limits for extreme dose rates beyond 5 Sv/h, which is *five times the maximum rate* required by the IEC [84].

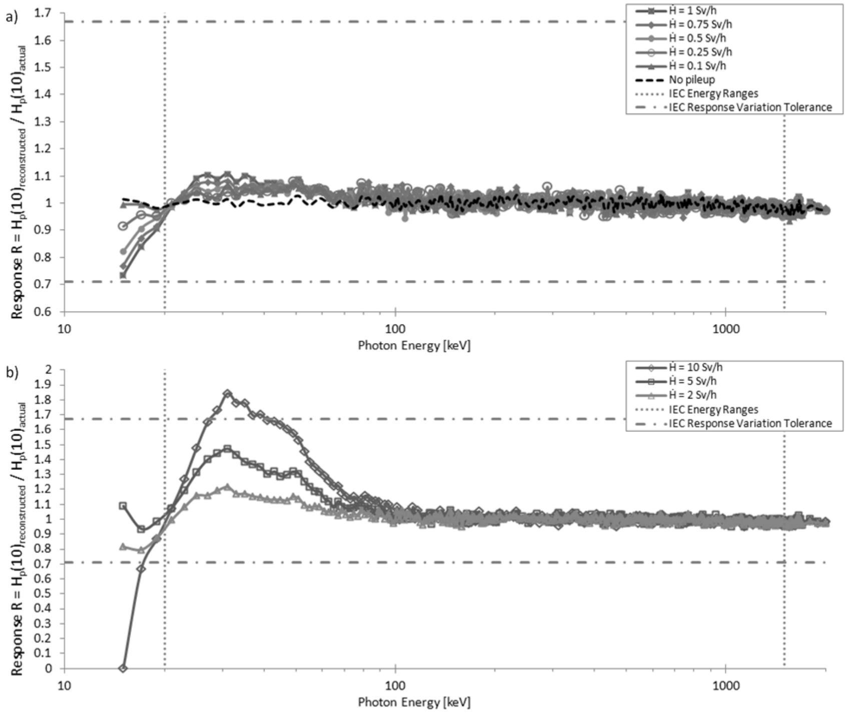


Figure 4.4: Dosepix personal dose reconstruction response

Plot of responses reconstructed from simulated energy measurements by a modelled 220 μm by 220 μm pixel with a 300 μm silicon sensor. IEC-specified limits are indicated. Plot **a** shows the response for the dose rate requirements of the IEC. Plot **b** shows the response for dose rates above IEC requirements. Data courtesy of M. Böhnel, Friedrich-Alexander Universität Erlangen-Nürnberg [25]. IEC limits defined in [84].

4.1.5 ASIC Specifications Based on APD Requirements

Table 4.2 provides a list of hybrid pixel detector ASIC specifications based on the proposed dose reconstruction method, the APD requirements of Table 4.1, and dose reconstruction response evaluation from [25].

Analogue voltage supply value:	1.5 V
Digital voltage supply value:	1.5 V
Max. chip current consumption:	5 mA
Overall photo-sensitive area:	12.4 mm^2
Dose measurement deadtime:	0 s
Data-based alarm from chip:	yes
Square pixel side-length:	220 μm
No. pixels:	256
Matrix power budget:	4.5 mW
Pixel power budget:	17.5 μW/pixel
Pixel output data:	Select most recent ToT value or binned photon counts
No. energy thresholds	
Analogue:	1/pixel
Digital:	16/pixel
ToT counter depth:	12 bits
ToT counter overflow detection:	yes (to flag high energy photon detection or pileup)
ToT data output format:	Conventional binary code
ToT reference clock frequency:	up to 100 MHz
ToT linear range:	from <10 keV to >1.5 MeV
No. energy bins:	16
Energy bin register depth:	16
Energy bin output format:	Conventional binary code
Serial readout clock frequency	up to 10 MHz

Table 4.2: Target specifications for the APD application

These specifications are based on the requirements outlined in Table 4.1, frontend pileup influence on dose reconstruction, ToT measurement resolution, microcontroller compatibility (*e.g.* byte-sized data word-lengths, single voltage supply value, etc.), and reduction of off-chip computation complexity (to permit real-time dose and dose rate reconstruction).

4.2 Requirements of a kVp Meter

The second targeted application for the new hybrid pixel detector design of this thesis is a kVp meter: an instrument used to assess X-ray tubes for medical imaging. The term *kVp* (kilovolt peak) refers to the maximum tube voltage used to accelerate electrons from the tube cathode to the anode target. The hybrid pixel detector is foreseen for use in a kVp meter, specifically to assess the quality of X-ray tubes for mammography.

Recalling from Chapter 1, the tube output spectrum depends on the accelerating voltage, which supplies the kinetic energy of the tube electrons and sets the upper limit of bremsstrahlung photon energy emitted from the anode. Figure 4.5 illustrates the relationship between tube voltage and output spectra. Measurement of the tube spectrum provides a lookup table for tube voltage. It should be noted that each spectrum in Figure 4.5 corresponds to a specific tube voltage value, which is not necessarily the peak voltage. The voltage of an X-ray tube is typically the output of a rectified AC signal and time-variant. Moreover, during mammography, the tube voltage is typically a pulse whose rise and fall-times depend on tube temperature. The kVp meter should therefore take many fast measurements of the output spectra in order to capture the spectral changes due to varying tube voltage. Evaluation of the exact kVp spectra measurement and analysis method will be the topic of future work, thus the new hybrid pixel detector ASIC should be programmable and reconfigurable to permit the investigation of different techniques.

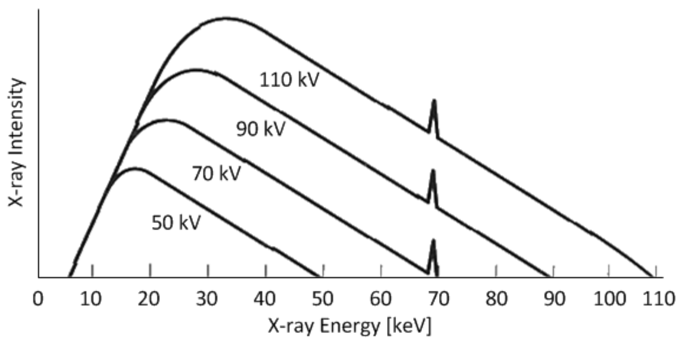


Figure 4.5: X-ray tube spectra dependence on tube voltage

The spectrum emitted from an X-ray tube depends on the voltage accelerating electrons in the tube. The example illustrated here are the different output spectra for different tube voltage values. Illustration redrawn from [93].

4.2.1 ASIC Specifications Based on kVp Meter Requirements

Based on the requirements discussed in the previous section, and a number of practical considerations, Table 4.3 provides a list of hybrid pixel detector ASIC specifications based on the requirements of the kVp meter application.

Analogue voltage supply value:	1.5 V
Digital voltage supply value:	1.5 V
Readout framerate:	∼4800 frames per second
Preamplifier linear range:	up to >160 keV
Pixel output data:	Detected photon intensity
Event counter depth:	8 bits
Event counter output format:	Conventional binary code
Serial readout clock frequency:	up to 10 MHz

Table 4.3: Target specifications for the kVp meter application
These specifications are based on preliminary estimates of tube voltage variation rate and a maximum targeted kVp setting of 160 kV [94; 95].

4.3 Dosepix

Dosepix is the custom-designed ASIC of a hybrid pixel detector with the combined specifications of Tables 4.2 and 4.3, designed within the framework of a research and development partnership between CERN, Friedrich-Alexander University Erlangen-Nuremberg, and IBA Dosimetry [96]. As an APD component, Dosepix will be in a portable, energy-resolving radiation monitor which outputs pre-binned digitised values representing energy spectra deposited in the sensor. This spectroscopic data can immediately be converted to a tissue-equivalent dose by a linear combination of the gathered statistics. As a kVp meter component, the Dosepix hybrid pixel detector will be used to analyse X-ray tube spectra for a given kVp setting.

4.3.1 System Overview

The Dosepix ASIC was implemented in a 130 nm standard CMOS process with eight metal layers for routing. It contains a matrix of 16 by 16 identically-designed square pixels measuring 220 µm in side-length. The pixel area was chosen as the result of a tradeoff between a photo-sensitive area which is small enough to limit the flux at the frontend input, but at the same time sufficiently large to accommodate the many elaborate features of the digital processing blocks [25]. The combination of many channels results in an overall sensitive area of 12.4 mm^2 in order to gather statistics to sample the radiation field.

Each pixel has three modes of data acquisition. In energy binning mode, the pixel measures the time over threshold (ToT) corresponding to a detected photon and records the event in one of 16 energy bin registers which are defined by digital energy thresholds. The output of photon counting mode is a record of the total number of photons which have deposited energies higher than the analogue threshold. The output of the energy integration mode is the cumulative ToT count of charge generated during an open shutter period. Details on these modes will be presented in Chapter 6.

Figure 4.6 depicts the system concept of the Dosepix APD [86; 87], which consists of multiple Dosepix detector assemblies. The ASICs connect to the serial port interface (SPI) ports of a microcontroller, which not only provides control signals for the chips, but also calculates dose based on the data. One of the Dosepix detectors will comprise an uncovered silicon sensor, while the remaining detectors will have filters placed above the sensors. The various filters stop low energy photons to reduce the flux transmitted to the silicon sensor [94], allowing for better dose reconstruction of high energy photons. Equivalent doses can be estimated from the binned charge spectra using a linear combination of the data read out of the multiple chips. The exact number of Dosepix detectors which will be used in the APD will be determined through a tradeoff between system power consumption and the accuracy of dose reconstruction [25; 88].

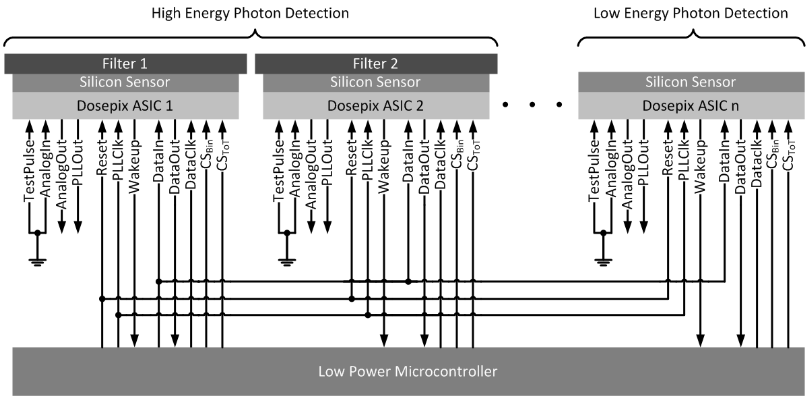


Figure 4.6: Overview of the personal dosimeter system

4.3.2 Chip Architecture

The photograph of the Dosepix ASIC in Figure 4.7a provides a floorplan of the major blocks on the chip: wirebond pads, the pixel matrix, the end of column (EoC) blocks, the periphery-level digital to analogue converters (DACs), the electronic fuses, and the PLL. The following sections briefly describe the roles of these blocks.

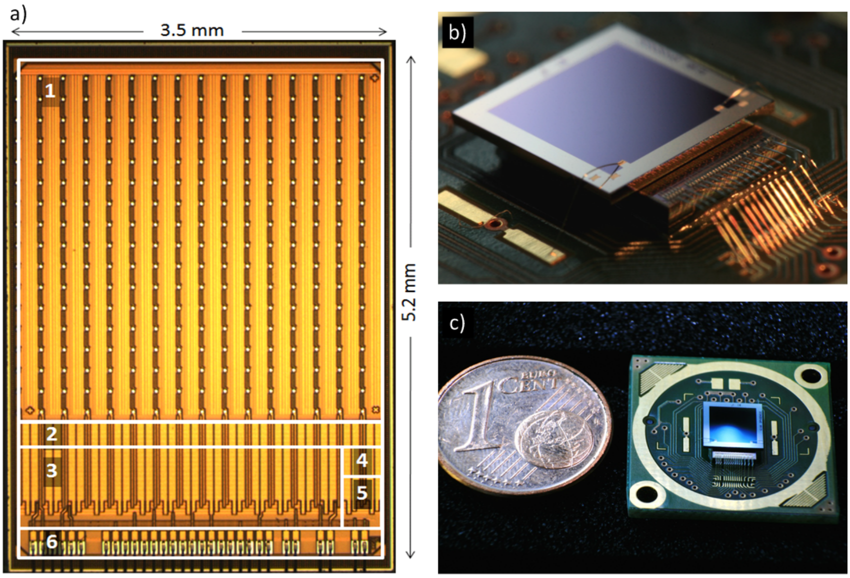


Figure 4.7: Photographs of Dosepix

a) The Dosepix ASIC surface (without sensor). **1:** 16 columns by 16 rows of pixels. A 17th row of bump bond pads provides the ground connection for the sensor. **2:** 16 end of column readout and control logic blocks, including analogue test pulse buffers. **3:** 14 programmable DAC circuits. **4:** Electronic fuse control circuit for unique chip identification serial numbers. **5:** Programmable frequency PLL. **6:** Wirebond pads. **b)** The Dosepix hybrid pixel assembly (silicon sensor bump bonded to the top of the ASIC) and its wirebond connections to a daughterboard. **c)** The daughterboard, which has a socket underneath to connect to various readout systems. Photographs of **b & c** courtesy of T. Gabor, Friedrich-Alexander Universität Erlangen-Nürnberg [91].

4.3.3 Inputs and Outputs

The Dosepix ASIC has 30 single-ended CMOS wirebond pads along the bottom edge for communication with a printed circuit board. Table 4.4 lists the chip input and output signals, excluding power and ground lines.

Signal Name	**Function**
AnalogIn	External analogue override input
AnalogOut	Buffered analogue output from one of the Periphery DACs or reference circuits (*e.g.* temperature sensor)
DataClk	Data clock (input)
DataIn	Serial input data (input)
DataOut	Digital serial output data (output)
CS_{ToT}	Chip select for the ToT data stream (input)
CS_{Bin}	Chip select for the Energy Bin data stream (input)
Reset	Reset signal (input)
TestPulse	Test pulse timing signal (input)
Wakeup	Digital wakeup alert for microcontroller (output)
PLLClk	Reference input clock for the PLL (input)
PLLOut	Digital output (for diagnosis) of the PLL (output)

Table 4.4: Input and output signals of the Dosepix ASIC

4.3.4 Pixel Matrix

The Dosepix ASIC contains 16 columns by 16 rows of identically designed pixels which process charge collected from the sensor. Each channel occupies an area of 220×220 μm^2; details of the pixel implementation will be presented later in Chapters 5 and 6. Figure 4.8 shows digital inter-pixel data communication lines along the columns.

4.3.5 End of Column (EoC) Blocks

Each column of pixels has an associated End of Column (EoC) Block which provides the column-level control signals (based on the chip mode and programming registers), and manages data stream multiplexing between the ToT and Bin readout streams, and the chip programming mode stream.

The EoC blocks also contain column-level buffers to drive the analogue test pulse up the column if one (or more) pixels has its analogue test configuration bit enabled.

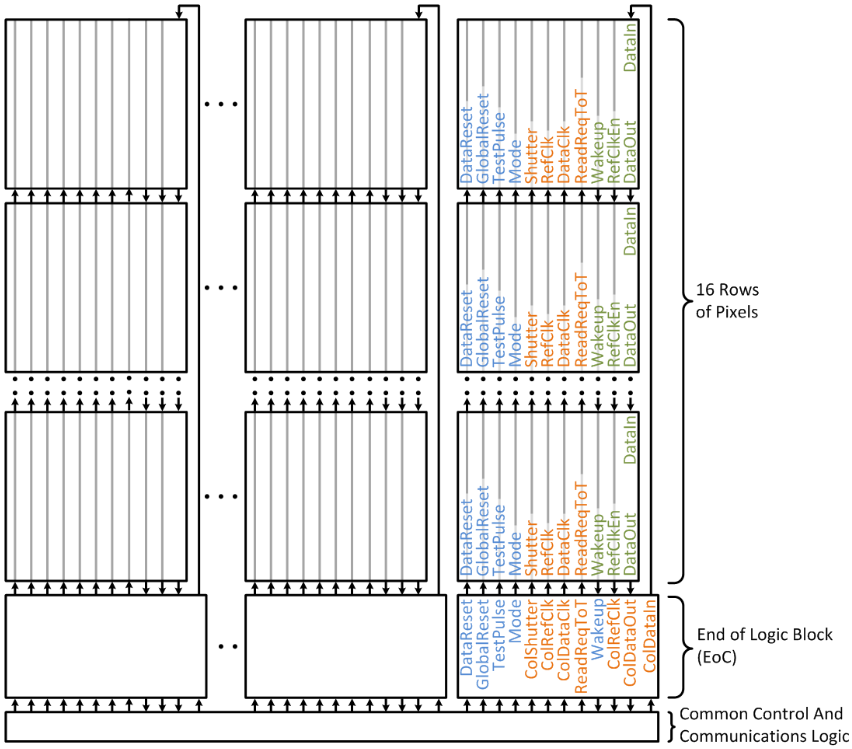


Figure 4.8: Digital connections between pixels along the column

Blue: global signals common to all pixels in the matrix. **Orange**: signals generated (or handled) by the End of Column Block; these are common to all pixels in the column. **Green**: signals which are generated in each pixel and propagated down to the End of Column Block.

4.3.6 *Chip Programming*

To maintain a simple, low power wirebond interface, digital communications between the Dosepix ASIC and its readout board are limited to a single SPI (serial peripheral interface)-compatible 5-bit bus consisting of CS_{ToT} (chip select for the ToT data stream), CS_{Bin} (chip select for the energy bin data stream), DataClk, DataIn and DataOut. Both chip select signals are active low and are used by the microcontroller to set the chip in a specific data mode.

The microcontroller on the readout board can write (and read back) programming data in the following registers on the Dosepix ASIC by setting CS_{ToT} and CS_{Bin} to place the chip into a Chip Programming Mode and following the programming protocol outlined in [95]:

- Operation Mode Register (OMR) (24 bits)
- Periphery DAC Register (128 bits)
- Column Analogue Test Pulse Enable Register (16 bits)
- Column Select for Bin Readout (4 bits)
- Configuration Bits (3 bits per pixel)
- Threshold Adjustment Bits (6 bits per pixel)
- Digital Threshold Registers (192 bits per pixel)

4.3.7 Periphery-Level Digital to Analogue Converters

The periphery-level digital to analogue converters (DACs) in the Dosepix ASIC were originally designed for the Medipix3.0 ASIC, and the DAC output stages have been modified to compensate for the high levels of MOSFET gate leakage currents observed in using Medipix3.0. To avoid confusion with the Threshold Adjustment DAC which is within the pixels themselves, these global DACs are referred to as the Periphery DACs. There are 14 Periphery DACs which provide the biasing voltages and currents for the analogue frontend, and reference signals for the analogue test pulse.

4.3.8 Electronic Fuses and Chip Serial Number

The Dosepix ASIC contains a set of 32 fuses which can individually be burnt electronically by sending in a large current using a controlled pulse. A fuse which has been permanently burnt outputs a 1'b1 while a fuse which is still intact outputs a 1'b0. The digital vector encoded by the set of fuses provide 32 bits for unique chip identification. The fuses are a commercial IP core block and their control circuits (for burning and reading) were originally designed for Medipix3.0.

4.3.9 Phase Lock Loop (PLL)

A PLL with programmable output frequency provides the reference clock which is copied into the EoC clocks for distribution to the pixel matrix. This reference clock is used to control the pixel finite state machines, and to provide a timing reference for ToT measurements.

4.3.10 Rolling Shutter for "Always On" Requirement

An active personal dosimeter is not permitted to pause dose monitoring when worn by its user. Therefore, in energy binning mode, the global electronic shutter is always on, even during readout. The Dosepix ASIC has two streams of data: the ToT data stream and the Energy Bin data stream. Chapter 6 will explain that there is a ToT Register for readout of ToT data, which is separate from the ToT Counter. When a read command for ToT data is initiated, an entire frame (*i.e.* data from all ToT Counters from every row and column) can be read out from the chip *without interrupting* ToT measurements and energy bin assignments of photons which arrive during the readout time. The Energy Bin Registers however, utilise the same set of flip flops for both counting and serial shifting, which means that counting must necessarily pause during readout of the Bin data stream. The Bin data is therefore output one column per read request from the wirebond signal CS_{Bin}. During the readout of the column which is addressed by the programmable Column Select Register, the remaining 15 columns continue to measure ToT and bin detected charge.

4.3.11 Low Power Considerations for Device Portability

In the APD application, a single battery (*e.g.* 1200-1500 mAh, 3.7 V Li-ion) will be used to power all device components. Each Dosepix ASIC targets a power budget of 5 mA at 1.5 V. The Dosepix ASIC includes a number of power-saving constructs.

wakeup alert for microcontroller The IEC requirement for APD alarm delay is for a response in less than 10 s (recall Table 4.1). For the Dosepix APD, this means that the energy bin data needs to be read out and calculated into a dose at least once every 10 s. Depending on the incident photon flux, the APD may require more frequent readouts than the 10 s requirement to prevent the pixel memory structures from being filled. A Wakeup alert signal is output from the Dosepix ASIC which indicates that a readout is required (either because an unusually large quantity of charge has been detected or because at least one Energy Bin Register is close to full). The Wakeup signal permits the microcontroller to enter a low power sleep mode when a readout is not required. Details on the implementation of the Wakeup signal will be discussed in Chapter 6.

PROGRAMMABLE PHASE LOCK LOOP (PLL) In order to save system-level power, the Dosepix ASIC contains a low power programmable phase lock loop (PLL) which takes a 10 MHz input reference clock and generates a nominally 100 MHz output clock for ToT measurements. Using the operation mode register (OMR), the PLL can alternatively be programmed to output 50 MHz, 25 MHz, 16.6 MHz, 12.5 MHz, 10 MHz, and 8.3 MHz, or the PLL can be bypassed to output the 10 MHz input reference clock. The PLL is designed to consume a constant ∼300 µW.

COLUMN CLOCK GATING The dynamic digital power of a circuit is given by:

$$P = CV^2 f \tag{4.5}$$

where f is the digital switching frequency. Since the power consumption scales with frequency, it would be desirable to turn off the digital clock whenever it is not needed in order to conserve power, particularly when measuring low fluxes, where only a small portion of the overall measurement time is spent processing charge. Although gating the ToT reference clock (RefClk) at each pixel reduces some power consumption, the column-level clock buffers still unnecessarily consume a large amount of energy when the pixels are waiting for photons to arrive. When enabled, the column-level clock gating (CCG) scheme depicted in Figure 4.9 manages clock distribution in the EoC block so that the pixels receive RefClk only when there is activity in at least one row.

Details on how the reference clock is used in the pixels are presented in the chapters which follow.

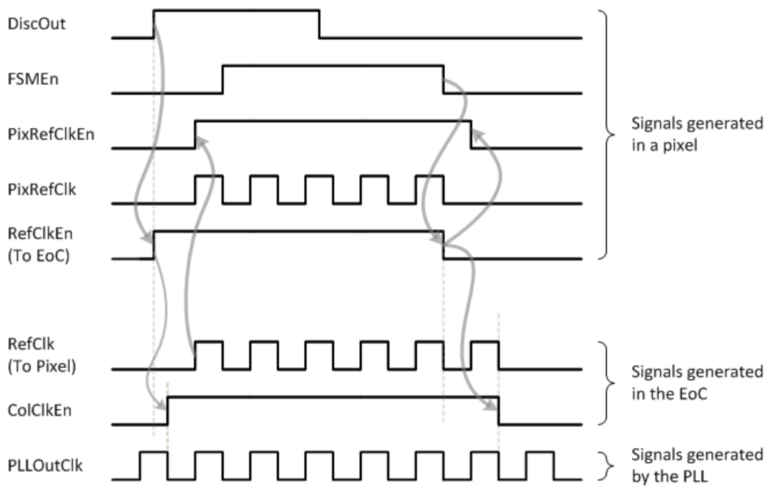


Figure 4.9: Column clock gating scheme

When there is no activity in a pixel (*i.e.* no output from the Discriminator), the pixels wait in an idle state. When the Discriminator output (DiscOut) asserts, the associated pixel generates a reference clock request called RefClkEn, which is the ORed value of DiscOut and the finite state machine enable (FSMEn) of the Binning State Machine. All the RefClkEn signals in the column are then ORed and sent down to the EoC to generate a combined column reference clock enable, ColClkEn, which waits to assert at the next falling edge of the constantly toggling PLLOutClk. The EoC then generates a new reference clock and sends RefClk = PLLOutClk && ColClkEn up to the pixels. On the rising edge of RefClk, the pixels which have activity generate a local PixRefClkEn and PixRefClk = RefClk && PixRefClkEn. The pixel circuits operate on PixRefClk. Using this scheme, RefClk only toggles when there is activity in at least one pixel in the column. This scheme, along with the interface circuits in the Event Selection Block, is designed to avoid glitches in the generated gated clocks, and takes into account the fact that DiscOut is asynchronous, randomly occurring, and variable in duration.

5

The Dosepix Pixel: Analogue Frontend

The art and challenge of pixel design is to find the means to physically accommodate many complex charge-processing components within an extremely compact area, and at the same time balance the design tradeoffs between the analogue and digital circuits.

The Dosepix readout ASIC contains 16 columns by 16 rows of 256 identically designed pixels. As mentioned in Chapter 4, the pixel is implemented in a 130 nm CMOS process and utilises eight metal layers for high density routing. The very demanding list of complex feature requirements, along with the need to share resources between multiple modes of operation, posed several challenges during the design cycle, which also had very tight project timeline constraints. Moreover, the pixel layout was restricted to an area of 220 µm by 220 µm, required to consolidate digital blocks driven by two separate clock domains (a DataClk which is *up to but not fixed at* 10 MHz, and a RefClk which is *up to but not fixed at* 100 MHz), and targeted to consume a maximum of 12 µA (combined analogue and digital power consumption).

The discussion on the Dosepix pixel design is divided into two chapters. This chapter describes the analogue frontend, which processes the signal induced by the bump-bonded sensor segment. Following the analogue frontend, the Discriminator output is processed by the digital blocks, which will be presented in the next chapter. The overall pixel layout will be shown in Chapter 6. Both Chapters 5 and 6 will conclude with a summary of their respective design targets. A set of selected frontend simulations to complement the pixel design discussion can be found in Appendix B.

5.1 Conceptual Overview of the Analogue Frontend

When a photon impinges onto a pixel sensor volume, its energy is absorbed by the sensor. Due to the photoelectric effect (assuming no energy loss from fluorescence photon escape and neglecting Compton scattering and pair production), the resultant quantity of charge is proportional to the deposited energy. The charge movement induces a signal at the input of the Preamplifier in the corresponding pixel of the ASIC. Figure 5.1a shows the different components which constitute the pixel analogue frontend. The Preamplifier integrates the charge and outputs a voltage pulse whose amplitude and duration are proportional to the input charge (see Figure 5.1b). The Discriminator compares the Preamplifier output voltage with a threshold voltage; its output is a digital pulse whose width corresponds to the time during which the *Preamplifier output exceeds the threshold voltage*.

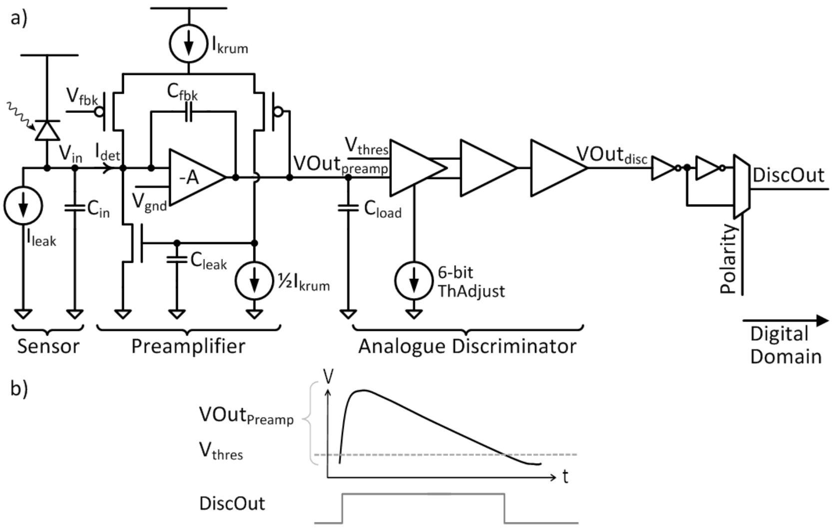


Figure 5.1: Analogue frontend

a) Analogue frontend schematic. b) Illustration of analogue charge processing. Note: $VOut_{Preamp}$ is drawn in this polarity to demonstrate the conceptual overview of the frontend. The true direction of polarity is further discussed in the following sections.

The analogue frontend consists of three main elements: a Preamplifier which integrates the charge from the sensor, an Analogue Threshold Voltage Discriminator which compares the Preamplifier output with a threshold voltage, and a Threshold Adjustment DAC which provides local (pixel-level) corrections for differences in offsets at the Discriminator input.

5.2 The Preamplifier

The Preamplifier in Dosepix was adapted from the preamplifier of the Medipix3 pixel [38], with the feedback capacitance chosen for the linear range requirements of the Dosepix applications and transistor sizes re-optimised based on circuit simulation results given the layout area available in the Dosepix pixel.

The Preamplifier depicted in Figure 5.2a is based on a charge sensitive amplifier architecture with leakage current compensation proposed by Krummenacher [97]. This preamplifier circuit consists of a differential operational amplifier (opamp) with a parallel feedback capacitance, C_{fbk}, which integrates a photo-induced signal from the sensor. It generates a voltage pulse whose amplitude is proportional to the input charge. A differential transistor pair, T_3 & T_4, with tuneable transconductances (due to a programmable bias current source, T_5 & T_6) parallel to C_{fbk} provides the means to discharge the voltage pulse back to the baseline DC voltage, V_{fbk}, at a constant rate. Thus the width of the voltage pulse is also proportional to the input charge. Additionally, this preamplifier architecture includes a leakage current compensation network (C_{leak}, T_1 & T_2) which sinks or sources parasitic DC current leaked from the sensor. C_{leak} is made large to help dampen the Preamplifier output, reducing its overshoot, $V_{Overshoot}$, and consequently the time to return to the baseline DC voltage (V_{fbk}). The effects of the overshoot will be explained later in Figure 5.6 during the discussion on frontend pileup.

Using appropriate values for the baseline DC reference voltages V_{gnd} and V_{fbk}[1], this Preamplifier topology can accept either holes or electrons as input. The polarity of input charge depends on the sensor material and design. To satisfy Equation 2.17 of Chapter 3, the opamp shown in Figure 5.2b is an inverting amplifier. When the Preamplifier integrates positive input charges (holes), the output is a negative voltage pulse. When

[1] V_{fbk} (the feedback voltage), sets the baseline DC voltage of the Preamplifier output. V_{gnd} (the virtual ground voltage), sets the DC voltage at the Preamplifier input.

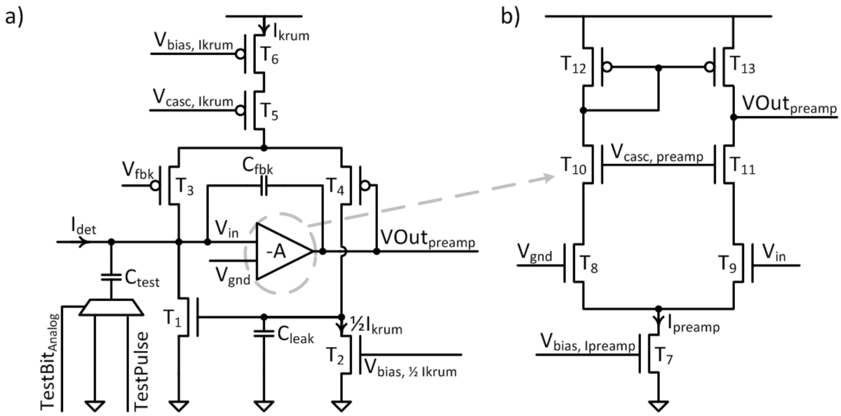


Figure 5.2: Charge sensitive preamplifier

the Preamplifier integrates negative input charges (electrons), the output is a positive voltage pulse. Table 5.1 lists some of the design parameters of the Dosepix Preamplifier.

C_{fbk}:	11.11 fF $\pm 1.8\%_{rms}$[2]
C_{test}:	7.32 fF $\pm 2.1\%_{rms}$
I_{Preamp}:	3 µA
I_{Krum}:	2 nA
-A (OTA):	-214 V/V
CSA gain:	12.3 mV/ke$^-$

Table 5.1: Preamplifier design values

From Equation 2.13 of Chapter 3, C_{det} is calculated to be 145 fF. This design satisfies the charge sensitive condition of Equation 2.20:

$$\begin{aligned} C_{fbk}(1+A) &\gg C_{det} \\ 11.11(1+214) &\gg 145 \end{aligned}$$

[2] According to Monte Carlo simulations of 128 channels on the same chip, see Appendix B.

5.3 The Analogue Threshold Voltage Discriminator

The Analogue Threshold Voltage Discriminator converts the analogue Preamplifier output into a signal which can be processed by the pixel digital blocks. The Discriminator designed for the Dosepix frontend is different from the architectures used in the Medipix and Timepix [69; 38] chips. The Dosepix Discriminator circuit topology was chosen for its robustness against temperature variations.

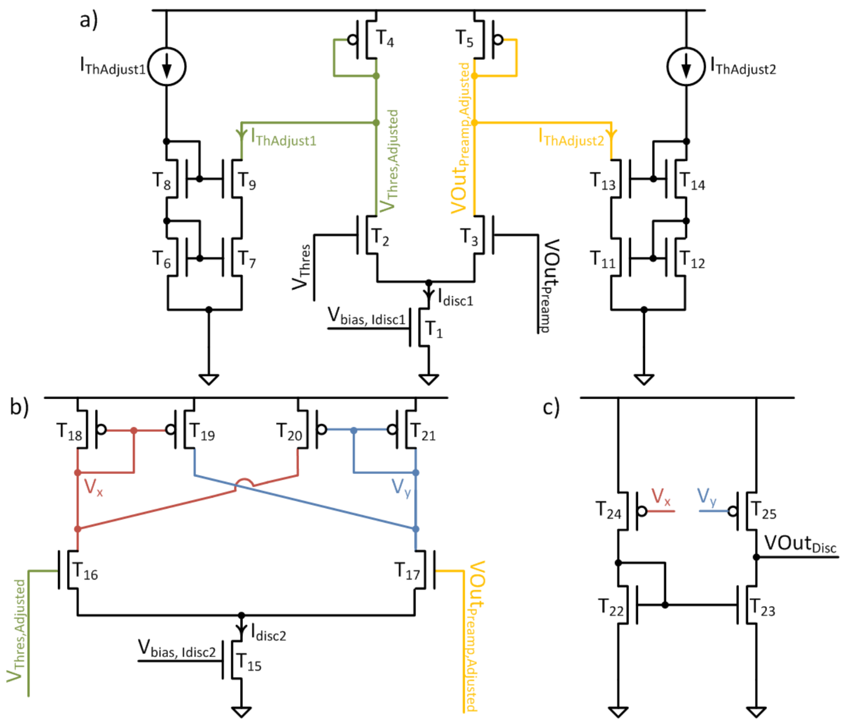


Figure 5.3: Analogue threshold discriminator

The Discriminator consists of the three amplifier stages of Figure 5.3. The 1st stage (Figure 5.3a), permits local tuning of V_{thres}, which is a global signal (*i.e.* the same for all pixels in the matrix). In this stage, the DC offset between V_{thres} and $VOut_{Preamp}$ can be adjusted by tuning the amount of current flowing through T_2 and T_3, which is controlled by programming the local 6-bit DAC to provide the two complementary currents $I_{Adjust1}$ and $I_{Adjust2}$. The main pulse discrimination functionality is achieved in the 2nd stage (Figure 5.3b), in which the amount of current flowing through the two differential branches depends on the difference in gate voltages at the input of T_{16} and T_{17}. Since the Preamplifier output is inverted, the analogue discrimination is also inverted. When $VOut_{Preamp} > V_{thres}$ (*i.e.* no activity from the inverting Preamplifier), T_{17}, T_{20} and T_{21} are off, while T_{19} operates in the triode region, and $VOut_{Disc} = V_{SS}$. When $VOut_{Preamp} < V_{thres}$ (*i.e.* charge is being integrated in the Preamplifier), T_{16}, T_{18} and T_{19} turn off while T_{20} operates in the triode region, and $VOut_{Disc} = V_{DD}$. The 3rd stage (Figure 5.3c) is a gain stage whose output is input to a digital inverter which corrects the polarity of the inverted analogue frontend output.

5.4 Local Threshold Adjustment

Although all pixels in the matrix are designed to be identical, there are always process variations which cause mismatch between real transistors [98; 99; 100]. A 6-bit Threshold Adjustment digital to analogue converter (DAC) provides individual threshold mismatch correction capability in each pixel. This local DAC outputs adjustment currents which are sunk from the differential branches of the Discriminator (the 1st stage of Figure 5.3a) to compensate for the DC offset between $VOut_{Preamp}$ and V_{thres}. The number of DAC bits was chosen based on area available in the pixel.

Figure 5.4 shows the two complementary output currents, $I_{Adjust1}$ and $I_{Adjust2}$, of the Threshold Adjustment DAC (Figure 5.5). The amount of current, $I_{pixeldac}$, given by the least significant bit (LSB) of the pixel-level Threshold Adjustment DAC is determined by a global DAC in the chip periphery. By design, $I_{Adjust1} + I_{Adjust2} = 62 \times I_{pixeldac}$ (*i.e.* the Threshold Adjustment DAC power consumption is independent the digital code). When the digital code is set to the midrange values of 6′b011111[3] or 6′b100000, $I_{Adjust1} = I_{Adjust2} = 31 \times I_{pixeldac}$; these two codes effectively turn off the Threshold Adjustment since the two Discriminator branches receive the same adjustment current (see Figure 5.4). When the Threshold Adjustment DAC bits are set to 6′b011110 or less, $I_{Adjust1} > I_{Adjust2}$; the lower the code, the greater the difference between the two adjustment currents. When the Threshold Adjustment DAC bits are set to 6′b100001 or more, $I_{Adjust1} < I_{Adjust2}$; the higher the code, the greater the difference between the two adjustment currents.

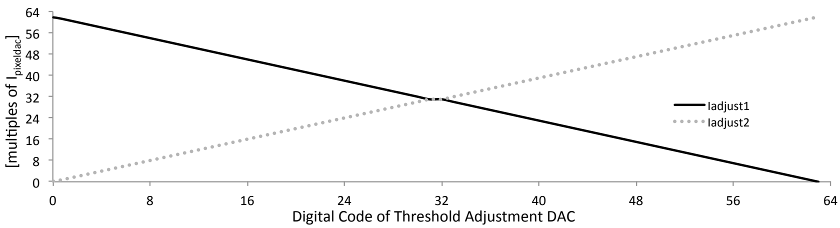


Figure 5.4: Threshold adjustment currents

[3]The prefix "n′b" indicates that the n following digits are represented in binary format. All numbers in this thesis are in decimal format unless otherwise indicated using this Verilog syntax. Similarly, hexidecimal numbers will be denoted by the prefix "n′h".

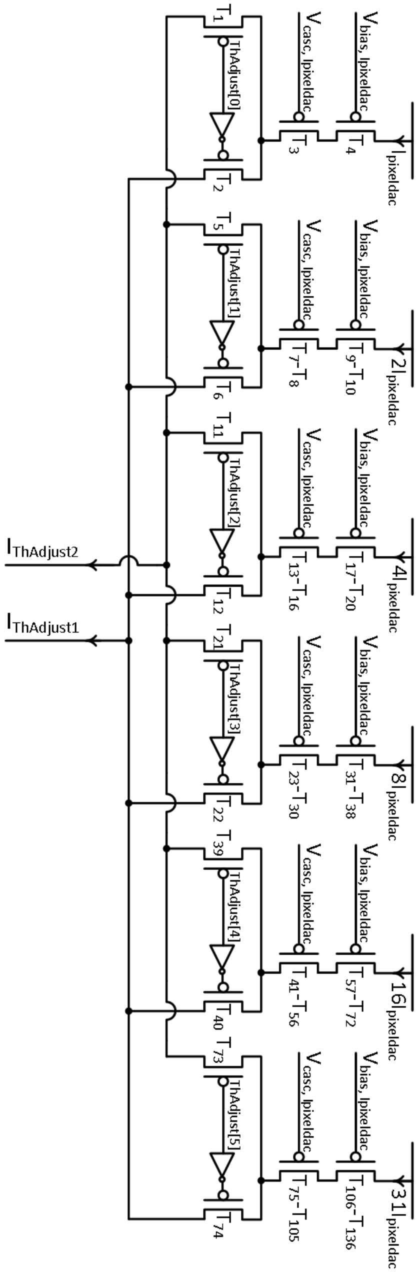


Figure 5.5: Local threshold adjustment DAC

5.5 Analogue TestPulse

The pixel frontend can be configured to either accept input from the bump bond electrode or an analogue test signal. When a pixel is configured for analogue test pulse input, the TestPulse Block in the End of Column Block (EoC) generates a voltage pulse which, when applied to a test capacitance (C_{test}) in the pixel, induces a charge at the input of the Preamplifier to simulate the sensor signal. The simulated charge is given by:

$$Q_{test} = \Delta V \times C_{test} \tag{5.1}$$

where ΔV is the difference in testpulse reference voltages set by two DACs in the chip periphery, and C_{test} = 7.3 fF $\pm$ 2.1%$_{rms}$ (from simulation, see Appendix B). Q_{test} is generated on each edge of TestPulse (the polarity of the charge depends on whether the TestPulse edge is rising or falling).

5.6 Frontend Pileup

Figure 5.6a shows the Preamplifier and Discriminator responses to charge from the sensor due to the interaction of a single photon. In this example, the pulse duration to process 13.9 ke$^-$ is approximately 3 µs. Figure 5.6a begins with the processing of the charge resultant from the detection of a photon, but a second photon arrives 0.8 µs later, during the pulse duration of the charge from the first photon. The $VOut_{Preamp}$ responses from the two sets of charge superimpose, resulting in a single long DiscOut pulse. Pileup in the analogue frontend occurs when more than one photon impinge on the pixel in rapid succession, overlapping the pulse durations in the frontend.

At the end of its discharge, $VOut_{Preamp}$ overshoots its baseline DC voltage by an amount, $V_{Overshoot}$ (see Figure 5.6d). The overshot $VOut_{Preamp}$ then slowly returns to the DC value. The magnitude of $V_{Overshoot}$ and the time to return to the baseline DC value depend on the quantity of charge being processed by the Preamplifier: the higher the input charge, the greater the overshoot.

5.7 Frontend Simulations

Appendix B presents a selected set of frontend simulations for reference.

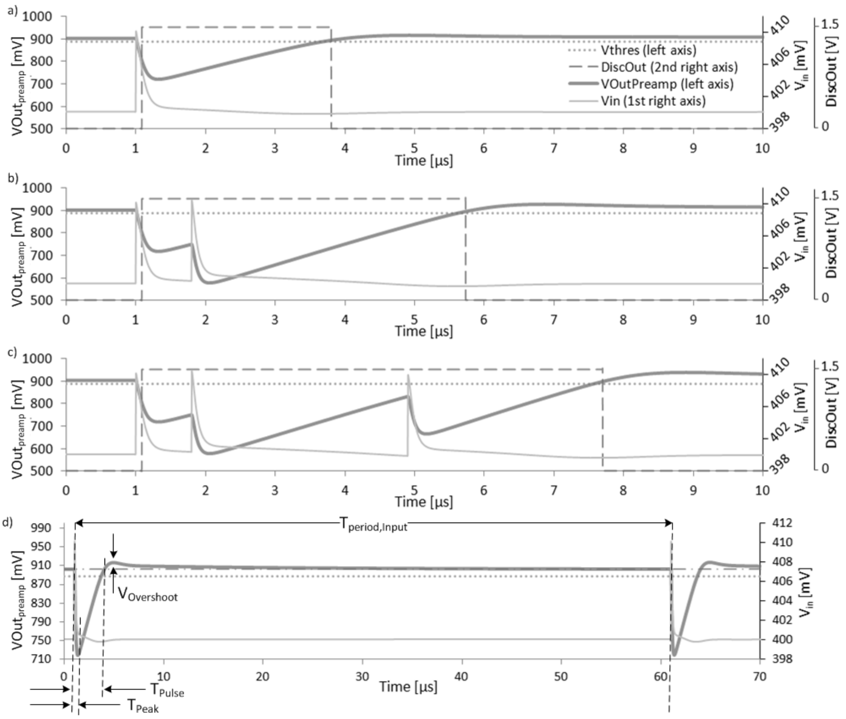


Figure 5.6: Pileup of events in the frontend

a) The charge from a single photon impinging on the pixel area is integrated in the Preamplifier, producing an *inverted* VOut$_{Preamp}$ pulse. The Discriminator outputs a digital pulse, DiscOut, whose high value corresponds to the time during which VOut$_{Preamp}$ exceeds the threshold voltage. **b)** Pileup from a 2nd pulse arriving during the pulse duration. A single long DiscOut pulse results. **c)** Pileup from 3 closely-spaced input pulses. **d)** Illustration of the terms: T_{Period}, T_{Pulse}, T_{Peak}, and $V_{Overshoot}$.

5.8 Pixel Performance Summary (Analogue)

Table 5.2 summarises the salient performance parameters of the Dosepix pixel analogue frontend. Examples at input charge quantities of 6.14 ke^- (22.101 keV)[4] and 44.4 ke^- (160 keV)[5] are reported as "typical" values expected for the personal dosimeter and kVp meter applications, respectively. The performance values reported here are based on simulation conditions listed in Table B.1 and/or described in the figure captions of Appendix B.

Analogue Frontend	
ENC (with sensor):	150 e^-_{rms}
Preamplifier gain:	12.3 mV/ke^-
Gain variation:	0.16 mV_{rms}
Preamplifier linear range:	0.9 ke^- to 47 ke^-
Preamp. peaking time, T_{Peak}	
@ Q_{in}=6.14 ke^-:	347 ns
@ Q_{in}=44.4 ke^-:	287 ns
Preamp. pulse duration, T_{Pulse}	
@ Q_{in}=6.14 ke^-:	2.2 µs
@ Q_{in}=44.4 ke^-:	6.1 µs
ToT linear range:	2.78 ke^- to 55.56 ke^-
ToT monotonic range:	0.98 ke^- to >138.89 ke^-
ToT temp. sensitivity (-10°C to 40°C):	<9% variation, 1.25 ke^- to 27.8 ke^-
Threshold offset variation:	3.1 mV_{rms}
ToT variation @ Q_{in}=6.14 ke^-:	0.04 μs_{rms} (with threshold adjustment)
Minimum resolvable threshold:	~900 e^-
Analogue testpulse Q_{test} range:	~0.25 ke^- to 47 ke^-
Analogue power consumption:	12.4 µW/frontend

Table 5.2: Pixel performance summary (analogue)

[4] A study of ToT measurements using Timepix to evaluate dose reconstruction methods used fluorescence photons of 8.040 keV (Cu-kα), 10.550 keV (Pb-kβ), 17.441 keV (Mo-kα), and 22.101 keV (Ag-kα), and isotope photons of 59.500 keV (^{241}Am) [101; 25].

[5] The expected range of photon energy output from X-ray tubes for the kVp Meter application are 40-160 keV with W anodes and 20-40 keV with Mo anodes [94].

6 The Dosepix Pixel: Digital Processing Circuits

Using the 3-bit Mode bus of Figure 6.1, the pixels can be programmed to run in one of three data acquisition modes, or one of seven programming (or diagnostics) modes. During readout or programming, flip flops in the pixels are daisy-chained to shift data serially down the column. During regular operation, the same flip flops are used for data storage or counting. When a pixel is set to run in a data acquisition mode, it can also be configured either to accept input from the analogue frontend or to bypass the frontend with a digital TestPulse from the End of Column Block. The data acquisition modes are:

1. Energy Binning Mode
2. Photon Counting Mode
3. Energy Integration Mode

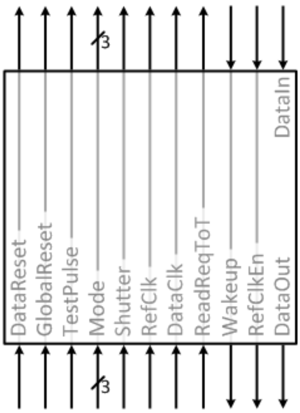


Figure 6.1: Digital interface of a Dosepix Pixel

6.1 Energy Binning Mode

purpose To provide online binning of energy spectra.

operation The pixel records the energy of each incident photon by measuring its ToT. The event is automatically classified into energy bins.

example application of the data Real-time dose reconstruction in a personal dosimeter. Sample ToT measurements can optionally be read out without disrupting energy binning.

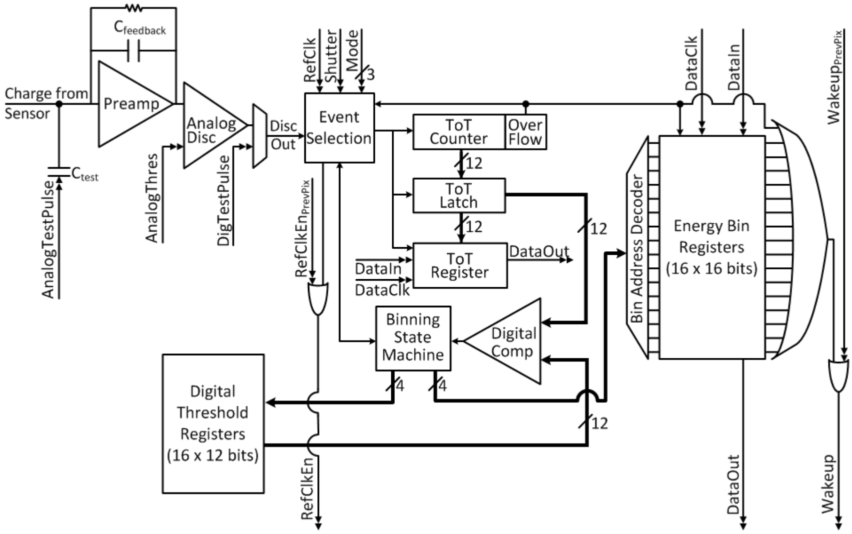


Figure 6.2: Block diagram of the pixel in energy binning mode

overview of the operations Figure 6.2 is a diagram of the major blocks in the pixel while configured to run in energy binning mode. The output of the Analogue Discriminator is the input of a 12-bit digital ToT Counter, which records the number of 100 MHz reference clock (RefClk) pulses coincident with DiscOut. The time over threshold (ToT) provides a measurement of the quantity of charge resultant from the energy deposited onto the sensor. The ToT value is then compared with 16 programmable Digital Thresholds which define the upper and lower limits of 16 energy bins. An array of 16 Energy Bin Registers tallies the number of ToT measurements within each energy window. This provides a charge spectrum of the energy deposited onto the sensor.

6.1.1 Main Digital Blocks

EVENT SELECTION The Event Selection Block is the interface between the analogue frontend and the digital domain. In addition to choosing valid DiscOut events (*i.e.* those which have occurred during the open Shutter period and those whose widths are greater than one RefClk period), the Event Selection Block provides the control signals for the various pixel data acquisition and programming modes. The waveforms of Figure 6.3 illustrate the various cases taken into account by the Event Selection Block. This block also controls the timing of control signals going into the various data structures in the pixel, for example the Event Selection Block provides the control signal telling the ToT Latch to load data from the ToT Counter, and the control signal indicating to the ToT Register to load data from the ToT Latch during a ToT read request. Very short DiscOut pulses lasting less than one RefClk cycle (*e.g.* from setting the analogue threshold too close to the noise floor or from analogue frontend distortions due to pileup) are ignored.

TOT COUNTER The 12-bit ToT Counter outputs a binary value representing the number of 100 MHz (*i.e.* 10 ns) RefClk periods coincident with the DiscOut pulse width.

TOT LATCH At the falling edge of DiscOut, the value in the ToT Counter is parallel-loaded to the ToT Latch. This temporary storage structure allows the ToT Counter to process the next DiscOut event while the Binning State Machine is still evaluating the energy bin assignment.

TOT REGISTER Following a read request for ToT data, the 16-bit ToT Register loads the most recent complete ToT measurement from the ToT Latch into its 12 lower bits, and pads the four upper bits with 4'b0. Its data is then shifted out serially at the toggling of the DataClk. ToT Register allows a readout of the ToT (energy) measurement of photon events *without interrupting energy binning or ToT counting of subsequent DiscOut events*. The occasionally sampled contents of the ToT Register provide measurements of the energy deposited by individual photons and permit the identification of isotopes.

DIGITAL COMPARATOR The Digital Comparator takes two 12-bit binary words and outputs a greater-than-or-equal-to flag. This output is used by the Binning State Machine to assign the event to the appropriate Energy Bin.

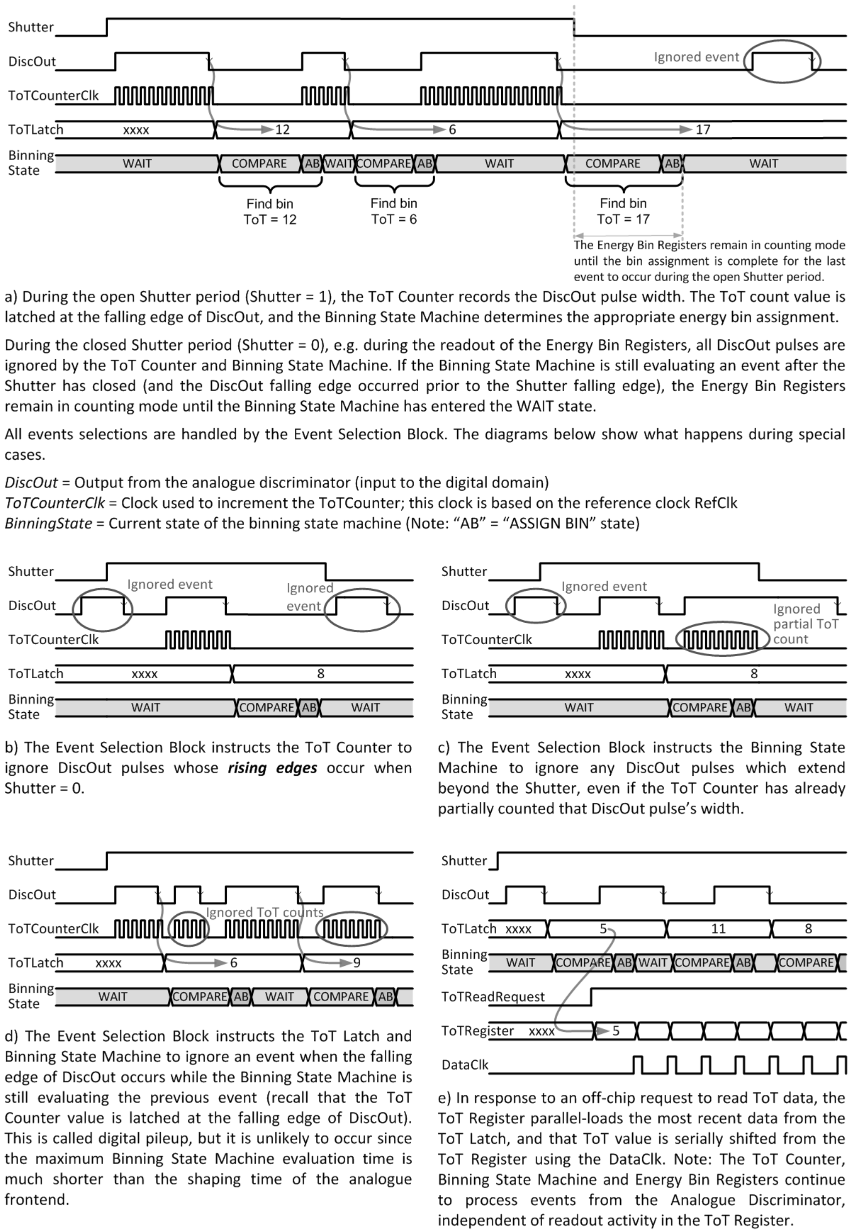


Figure 6.3: Event selection and control in energy binning mode

BINNING STATE MACHINE The Binning State Machine determines the appropriate Energy Bin Register to assign the event measured by the ToT Counter. On the falling edge of DiscOut, the ToT Latch is updated and the Digital Comparator compares the ToT value with a 12-bit Digital Threshold from the address provided by the Binning State Machine. As the Digital Threshold Register values are sorted in ascending order, the Binning State Machine increments the bin address until the Digital Comparator indicates that a Digital Threshold has been found which is less than the value stored in the ToT Latch. The waveforms in Figure 6.3 depict the timing between DiscOut event detection and states in the Binning State Machine. If the Shutter closes while the Binning State Machine is still active, the state machine is permitted to complete processing before the Energy Bin Registers are configured into serial shift register mode. The states are:

WAIT STATE: The state machine waits for the falling edge of DiscOut.

COMPARE STATE: The Digital Comparator compares the ToT Latch value with the Digital Threshold Register output (address provided in ascending order by the Binning State Machine). The Binning State Machine loops in this state until the appropriate Energy Bin address is found. ToT values less than the minimum Digital Threshold are ignored. ToT values greater than the maximum Digital Threshold are assigned to the highest Energy Bin.

ASSIGN BIN STATE: The Bin Address Decoder is enabled.

DIGITAL THRESHOLD REGISTERS Each pixel contains 16×12-bit Digital Threshold Registers, which store ToT values corresponding to the lower and upper limits of the energy windows which define the bins of the Energy Bin Registers. The Digital Threshold Registers are implemented as an array of non-resettable D-type latches. The 16 sets of latches share a single 12-bit data bus for read and write access, and are addressable using a 4-bit bin address encoded in Gray code[1].

BIN ADDRESS DECODER The Bin Address Decoder takes the 4-bit bin address and asserts one of the 16 output lines according to the value encoded in bin address. The 16 lines output from the Bin Address Decoder provide the clock inputs to the Energy Bin Registers when they are configured in counting mode.

[1] Gray code is digital code where only one bit changes for each neighbouring value in a list of sorted values. This prevents uncontrolled intermediate states from occurring in the 12-bit data bus of the Digital Threshold Registers during bin address transitions.

energy bin registers Each pixel contains 16×16-bit Energy Bin Registers. They can be configured to operate in 1) counting mode (*i.e.* to count photon events and construct the charge spectrum) or 2) serial shift mode. While an LFSR structure with pseudo-random output would provide the most compact realisation of a reconfigurable counter and shift register, the Energy Bin Registers were specified to output binary codes in order to simplify off-chip data processing. The Energy Bin Registers were therefore implemented as a series of D flip flops with multiplexors on each of the D and clock inputs. This is very similar to the block-level architecture which was used in the Medipix3.0 counters presented in Chapter 3, however the lower level logic was implemented using standard cell static CMOS logic gates, rather than minimal-size custom blocks. Also to reduce area occupation, the flip flops are not themselves resettable, but upon DataReset or GlobalReset, the Energy Bin Registers are configured in serial shifting mode and the input to each 16-bit register is set to 1′b0, which is then shifted to subsequent bits by the toggling of DataClk. Very special care must be taken in the End of Column logic when changing the clocks between the output of the Bin Address Decoder and the DataClk. Figure 6.4 depicts the basic architecture of the reconfigurable Energy Bin Registers.

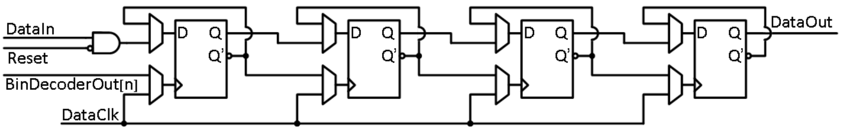


Figure 6.4: Energy bin registers

Only four bits are shown for demonstration of the architecture. The actual structures contain 16 bits. Each 16-bit register chain has an AND gate at its input. When the Reset signal is asserted (during GlobalReset or DataReset commands), it forces a "0" at the beginning of each chain and 16 DataClks are toggled to shift that "0" through all the bits.

When in counting mode, most of the registers are arranged as 16-bit binary ripple counters. The register associated with the highest energy bin, however, is a 15-bit binary ripple counter. The remaining bit is connected to the ToT Counter overflow indicator and is used to set an alarm in case of the detection of a very large input charge.

When in serial shifting mode, the 256 flip-flops of the Energy Bin Registers are daisy-chained and connected to the DataClk.

WAKEUP The Wakeup signal is the output of a 17-input OR gate whose inputs are the 2nd MSB[2] of the 16 Energy Bin Registers and the overflow flag (13th bit) of the ToT Counter. The signal indicates that at least one Energy Bin Register is close to full, or that at least one ToT Counter has measured a ToT value surpassing 4095 (*i.e.* $2^{12} - 1$) which would either mean that the frontend has experienced event pileup, or an especially energetic photon has been detected. The Wakeup signal is connected through a network of OR gates to every pixel and is output off-chip. This allows the readout system components to remain in a sleep mode until it is necessary to read data from the chip. It also provides an alarm in case the dosimeter has suddenly detected a large quantity of radiation. The 17-input OR gate which controls the Wakeup signal is disabled during Energy Bin readout to prevent false toggling on the chip-level Wakeup output while data is shifting through the Energy Bin flip flops.

[2]MSB: Most Significant Bit

6.2 Photon Counting Mode

purpose To measure the number of photons during an exposure time controlled by the electronic Shutter.

operation The pixel records the number of packets of deposited energy which exceed the analogue threshold.

example application of the data To determine X-ray tube voltage from spectra measurements (*e.g.* using threshold scans).

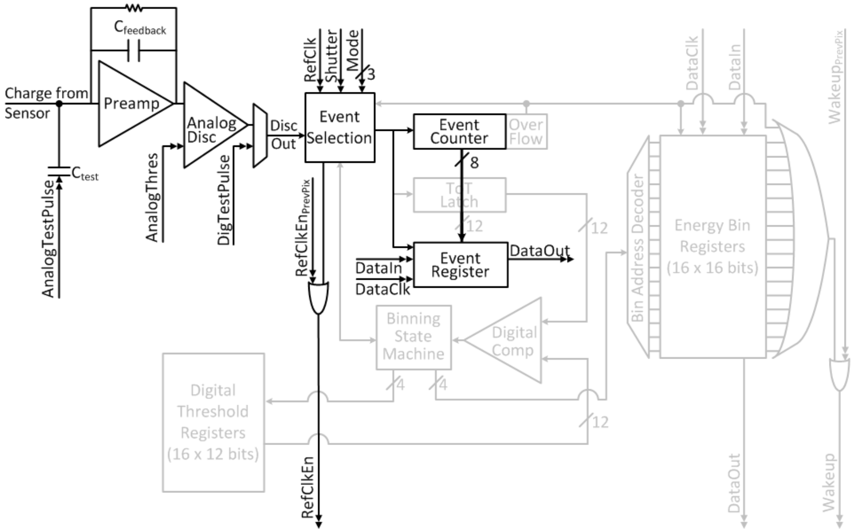
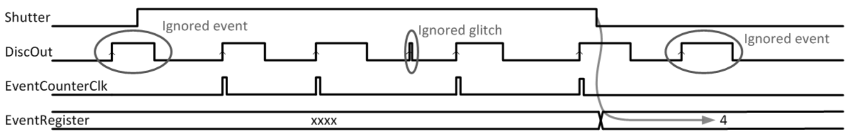


Figure 6.5: Block diagram of the pixel in photon counting mode

overview of the operations Figure 6.5 is a diagram of the major blocks in the pixel while configured to run in photon counting mode. The output of the Analogue Discriminator is the input of an 8-bit digital Event Counter, which records the number of Discriminator output pulses occurring during the open Shutter period. This provides a measurement of the intensity of photons with energies above the analogue threshold. Photon counting mode can also be used to characterise the frontend performance (using techniques explained in Chapter 7).

6.2.1 Main Digital Blocks

EVENT SELECTION The Event Selection Block is the interface between the analogue frontend and digital processing blocks, and provides controls for the various data acquisition and programming modes within the pixel. The waveforms of Figure 6.6 illustrate the various cases taken into account by the Event Selection Block when the pixel is programmed to operate in photon counting mode. Any DiscOut events whose rising edges occur outside of the open Shutter period, and/or any DiscOut events whose durations are less than one RefClk cycle, are ignored.



The Event Counter records the discrete number of events from the Analogue Discriminator. The Event Selection Block selects those events whose ***rising edges*** occur while the Shutter is open (Shutter = 1). Also, the Event Selection Block uses the 100 MHz RefClk to filter out Discriminator output pulses which last for less than the reference clock period of 10 ns.

Figure 6.6: Event selection in photon counting mode

EVENT COUNTER The 8-bit Event Counter outputs a binary value representing the number of DiscOut pulses which have occurred during the open Shutter period.

EVENT REGISTER The 8-bit Event Register serially shifts the value loaded in parallel from the Event Counter.

6.3 Energy Integration Mode

purpose To measure the total energy deposited during an exposure time controlled by the electronic Shutter.
operation Accumulates the total ToT counts.
example application of the data To be used to monitor radiation in environments where the flux is too high to permit single photon processing due to frontend pileup.

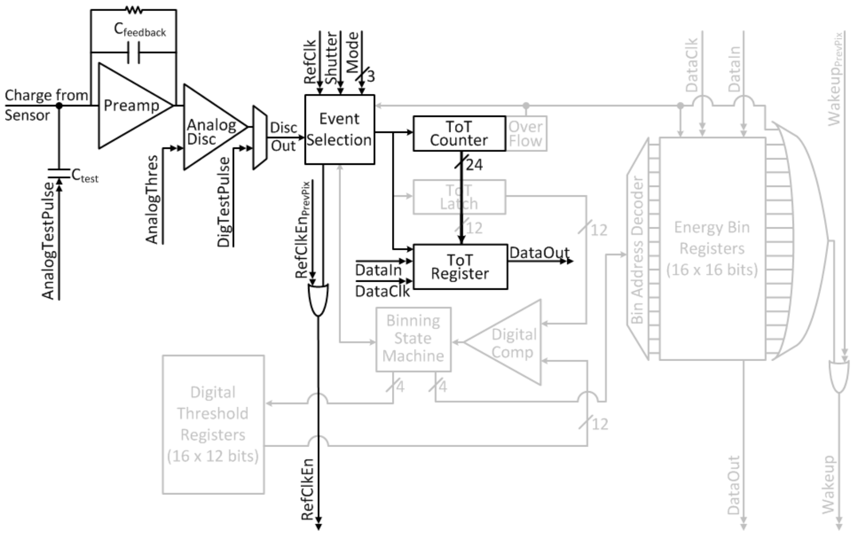
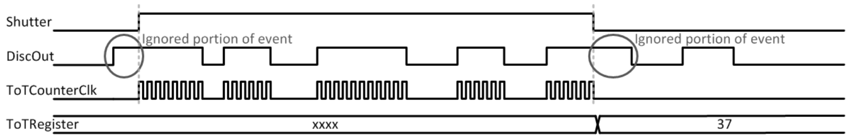


Figure 6.7: Block diagram of the pixel in energy integration mode

overview of the operations Figure 6.7 is a diagram of the major blocks in the pixel while configured to run in energy integration mode. The output of the Analogue Discriminator is the input of a 24-bit digital ToT Counter, which records the number of 100 MHz RefClk coincident with Discriminator output pulses. Since the ToT Counter is not cleared between DiscOut pulses, the ToT value accumulates over the entire open Shutter period. The output of the pixel in this mode is *similar to that of an integrating diode detector, except that noise and dark currents are excluded.*

6.3.1 Main Digital Blocks

EVENT SELECTION The Event Selection Block is the interface between the analogue frontend and digital processing blocks, and provides controls for the various pixel data acquisition and programming modes. The waveforms of Figure 6.8 illustrate the various cases taken into account by the Event Selection Block when the pixel is programmed to operate in energy integration mode. Only the DiscOut events (or the partial events) which occur within the open Shutter period are included in the integrated energy count. Any DiscOut events whose durations are less than one RefClk cycle are ignored.



The ToT Counter records cumulative 100 MHz RefClk cycles for all Analogue Discriminator output pulses which occur while the Shutter is open (Shutter = 1). Any portions of DiscOut which arrive prior to, or extend beyond, the open Shutter will be ignored.

Figure 6.8: Event selection in energy integration mode

TOT COUNTER The 24-bit ToT Counter outputs a binary value representing the cumulative ToT value during the open Shutter period.

TOT REGISTER The 24-bit ToT Register serially shifts the value loaded in parallel from the ToT Counter.

6.4 Other Digital Operation Modes

In addition to the regular data acquisition modes, the pixels can be configured in one of the following programming modes:

- Set Digital Threshold Registers Mode
- Set Configuration Bits Mode
- Set ThAdjust Bits Mode

Or one of the following diagnostics modes:

- Get Digital Threshold Registers Mode
- Get Configuration Bits Mode
- Get ThAdjust Bits Mode
- Test Wakeup Signal Mode

6.4.1 Set and Get Digital Threshold Registers Modes

This section combines the discussion on two separate modes: Set Digital Threshold Registers Mode, and Get Digital Threshold Registers Mode. **Set** Digital Threshold Registers Mode is used to program valid Digital Threshold values into the pixel memory. **Get** Digital Threshold Registers Mode is used to verify the values already stored in the memory. While the two modes utilise many of the same hardware resources, their implementations are quite different. In Set Digital Threshold Registers Mode, Digital Threshold values are input to the pixels one Digital Threshold value at a time according to the Digital Threshold address location which is provided by the chip user. In Get Digital Threshold Registers Mode, the pixels internally generate the addresses (in ascending order) and provide the Digital Threshold value corresponding to each address. A counter in the End of Column Block counts the number of bits which have been shifted out of the column and provides an increment address command to the pixels when all the values from a single Digital Threshold address have been shifted out.

The Digital Threshold Registers are implemented as an array of 16$\times$12-bit, non-resettable latches sharing a single 12-bit bus for read and write access. It should be noted that these latches cannot be automatically initialised using the GlobalReset and DataReset chip commands: the Digital Threshold Registers need to have values explicitly written to them. Since the 12-bit parallel data bus is only accessible by components within the pixel, the ToT Register is borrowed during Set/Get Digital Threshold Registers Mode to provide temporary access to the Digital Threshold Register memory from outside the pixel. Figure 6.9 shows the block diagram of the pixel when it is configured for external access to the Digital Threshold Registers. In these modes, the ToT Register is 16-bits long; the four most significant bits contain the address of the Digital Threshold Register associated with the 12-bit Digital Threshold word stored in the 12 lower bits of the ToT Register. The Binning State Machine and control circuits use RefClk while serial data shifting occurs on DataClk. It is imperative that the DataClk frequency is at least 10× slower than the RefClk frequency in order to ensure that control signals are in place prior to serial data shifting. Furthermore, in order to avoid glitching when accessing the Digital Thresholds in energy binning mode, the Digital Threshold addresses (in any mode) are encoded in Gray Code, where each subsequent address value differs from the previous value by a single bit.

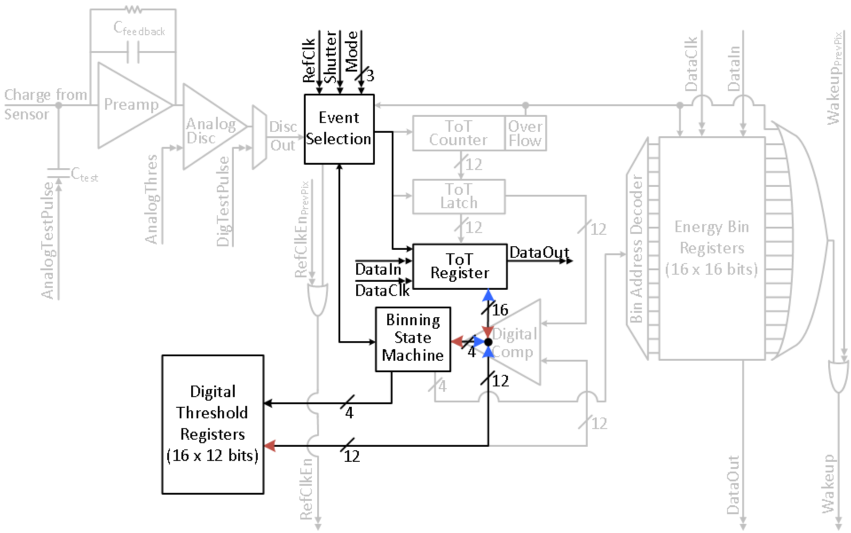


Figure 6.9: External access to the Digital Threshold Registers

Note: Both Set and Get Digital Threshold Registers Modes are shown in this diagram. The red arrows indicate the direction of data flow when writing to the Digital Threshold Registers, and the blue arrows indicate the direction when reading from the memory array. Black arrows indicate the direction of data flow common to both modes.

In Set Digital Threshold Registers Mode, each Digital Threshold value is addressed and written to separately (*i.e.* the write cycle must be repeated 16 separate times in order to write to all Digital Threshold locations in a given pixel). The value stored in the lower 12 bits of the 16-bit ToT Register is written to the Digital Threshold addressed by the upper 4 bits in the ToT Register. Note that a unique Digital Threshold value can be assigned to Digital Threshold Register of each pixel.

In Get Digital Threshold Registers Mode, the Binning State Machine provides the Digital Threshold address, starting at address 0. This address is sent to the Digital Threshold Register array as well as loaded in parallel to the upper 4 bits of the ToT Register. The 12-bit Digital Threshold value corresponding to the address location is loaded in parallel to the lower 12 bits of the ToT Register. The 16-bit ToT Register is then configured as a serial shift register and its value is serially shifted through the daisy chained ToT Registers down the column. A counter in the End of Column Block keeps track of how many bits have been shifted out of the column. After all the bits for a single Digital Threshold location have been shifted out from all the pixels in the column, the End of Column Block sends a control signal to the pixels to increment the Digital Threshold address. The cycle is then repeated: the Binning State Machine provides the next sequential address and the corresponding Digital Threshold value is loaded into the ToT Register.

6.4.2 *Set and Get Configuration Bits Modes*

Some control signals, such as GlobalReset, DataReset and Mode, are common to all pixels in the matrix. Similarly, signals such as RefClk, DataClk and Shutter, are common to all pixels which share a column. The Configuration Bits and the Analogue Threshold Adjustment Bits however, are unique to each pixel. These values are stored in resettable latches in the pixels.

This section combines the discussion on two separate modes: Set Configuration Bits Mode, and Get Configuration Bits Mode. **Set** Configuration Bits Mode is used to program the Configuration Bit Latches. **Get** Configuration Bits Mode is used to verify the values already stored in the pixel.

Each pixel contains a set of Configuration Bits which provide unique programming in individual pixels (*e.g.* selection between analogue test pulse or sensor signal input to the Preamplifier). Since the Configuration Latches cannot serially shift data, both Set and Get Configuration Bits Modes borrow the ToT Register for external access to the data. During these two modes, the ToT Register is configured for an 8-bit word size, where the upper five bits are padded with 5′b00000 (or ignored) and the lower three bits contain the MaskBit, $\mathrm{TestBit}_{\mathrm{Analog}}$ and $\mathrm{TestBit}_{\mathrm{Digital}}$, respectively. Figure 6.10a shows the arrangement of components in the pixel during Set and Get Configuration Bits Modes.

During Set Configuration Bits Mode, the pattern from the user is shifted through the pixel matrix. Counters in the End of Column Blocks keep track of how many bits have shifted through each column. Once the expected total of bits have shifted into the pixels, the Configuration Latches parallel-load the Configuration Bits from ToT Registers, and the pixels assume their new programming.

During Get Configuration Bits Mode, the ToT Register parallel-loads the Configuration Latch values into its lower three bits, while its upper five bits are padded with 5′b00000. The ToT Register contents are then serially shifted off-chip with DataClk.

6.4.3 Set and Get Threshold Adjustment Bits Modes

Like the Configuration Bits, the Analogue Threshold Adjustment (ThAdjust) Bits provide unique programming for each pixel and are stored in resettable latches. The Analogue Threshold Adjustment Bits provide the digital input for the DAC circuit within each pixel, described in §5.4.

This section combines the discussion on two separate modes: Set ThAdjust Bits Mode, and Get ThAdjust Bits Mode. **Set** ThAdjust Bits Mode is used to program the Analogue Threshold Adjustment Latches. **Get** ThAdjust Bits Mode is used to verify those values.

Since the Analogue Threshold Adjust Laches cannot serially shift data, both Set and Get ThAdjust Bits Modes borrow the ToT Register for external access to the data. During these two modes, the ToT Register is configured for an 8-bit word size, where the upper two bits are padded with 2′b0 (or ignored) and the lower six bits contain the digital code for the Threshold Adjustment DAC. Figure 6.10b shows the arrangement of components in the pixel during Set and Get ThAdjust Bits Modes. The mechanisms involved in writing to or reading from the ThAdjust Bits are the same as those described in §6.4.2.

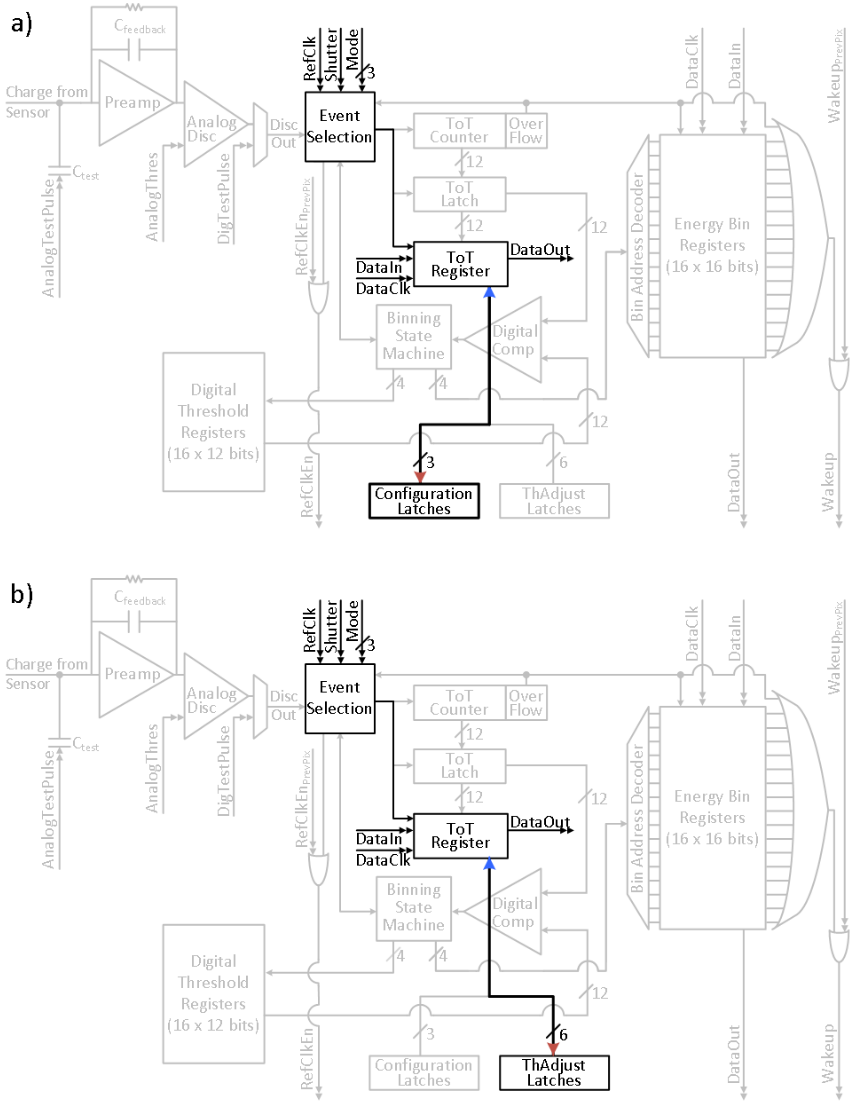


Figure 6.10: External access to pixel configuration settings

a) Both Set and Get Configuration Bits Modes are shown here. The red arrows indicate the direction of data flow during writing and the blue arrows indicate the direction during reading. Black arrows indicate the direction of data flow common to both modes. **b)** Set and Get Analogue Threshold Adjustment Bits Modes.

6.4.4 Test Wakeup Signal Mode

The Test Wakeup Signal Mode utilises the same schematic as that of energy binning mode (Figure 6.2). In energy binning mode, the 17-bit OR gate in each pixel is disabled during readout to avoid constant toggling of the chip Wakeup output. In Test Wakeup Signal Mode, the 17-bit OR gate is left enabled during readout so that test vectors can be shifted through the daisy-chained Energy Bin Registers to verify the Wakeup output.

6.5 Layout of the Pixel

Figure 6.11 shows the layout of the Dosepix pixel. The frontend is laid out in Regions 1, 2, and 3. The digital circuits in Region 4b were placed and routed manually in order to optimise their area occupation, and consist of static digital circuits (*e.g.* Configuration Latches, Analogue Threshold Adjustment Code Latches, etc.). A generous portion of the 220 μm by 220 μm pixel area was allocated to the analogue frontend in order to isolate the bump bond electrode from the 100 MHz digital clock. All analogue bias and power lines are routed over Regions 1, 2, 3, and 4b. The extra isolation of the analogue frontend and bias lines meant a large penalty in the area available to lay out the complex digital circuits.

The analogue circuits were completely custom designed. Their transistors were sized to optimise between the user specifications (*e.g.* ENC, Preamplifier linear range, ToT linear range, etc.), channel-to-channel matching, differential amplifier offsets, and radiation robustness. The most sensitive nodes in the frontend were laid out in an enclosed layout transistor geometry; this technique requires a lot of area and restricts the transistor aspect ratio, but protects the transistor against the creation of radiation-induced charge traps in the oxide [102; 103]. Guard-rings and dummy transistors are also placed throughout the analogue frontend layout in order to improve matching between transistors. The Preamplifier feedback capacitance, C_{fbk}, and test capacitance, C_{test}, were implemented as vertical natural capacitors (VNCAP), and the leakage compensation capacitance, C_{leak}, was implemented as a metal-insulator-metal capacitor (MIMCAP). Both types of capacitors are parameterised cells and are well modelled in circuit simulators.

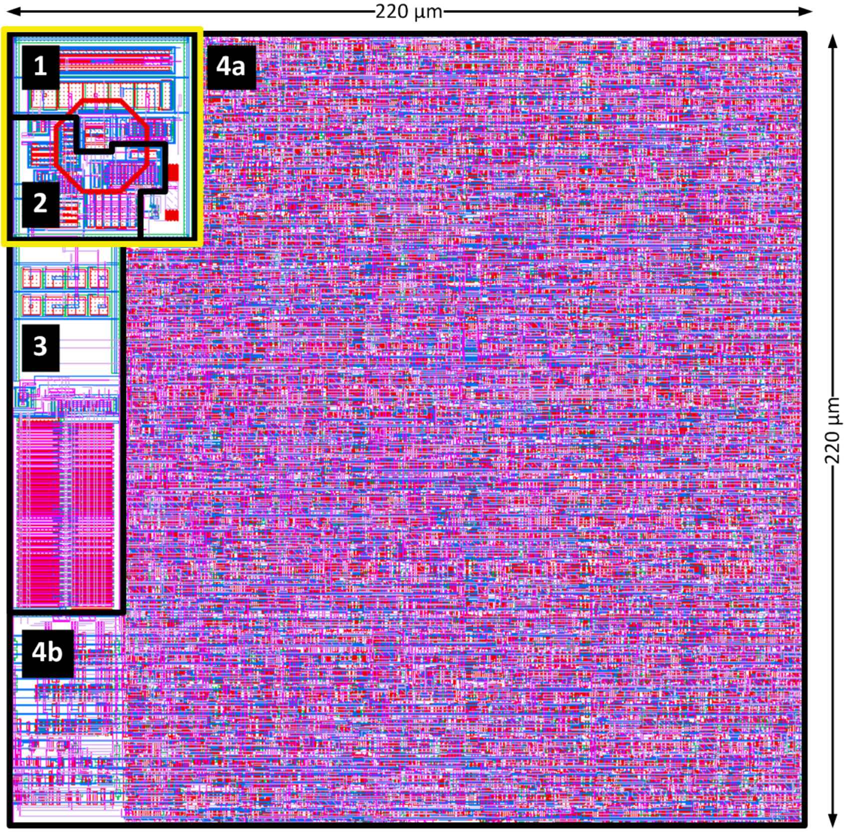


Figure 6.11: Layout of a Dosepix pixel

Metal 1-3: VNCAPs (analogue). **Metal 1-4**: internal routing (both analogue and digital). **Metal 5**: column-level biasing (analogue), and control (digital) lines. **Metal 6 & 7**: MIM-CAPs (analogue). **Metal 6 & 7**: power/ground lines and shielding (digital). **Metal 6, 7, & 8**: power/ground lines and shielding, and bump bond electrode (analogue). Note: Only the lower 3 out of 8 metal layers are displayed to simplify the figure. The yellow box indicates the magnified region of Figure 6.12. **1)** Charge Sensitive Preamplifier. **2)** Analogue Threshold Voltage Discriminator. **3)** 6-bit Analogue Threshold Adjustment DAC. **4a)** Synthesised and automatically placed and routed digital circuits. **4b)** Manually placed and routed digital blocks.

The design of the digital circuits was a mixture of manually-drawn high-level block schematics and synthesised low-level descriptions of individual blocks whose functions were specified in the Verilog hardware description language. With the exception of a few static blocks which were placed and routed manually, the majority of the digital circuits were automatically placed and routed using a commercial 130 nm standard CMOS cell library implemented with regular threshold voltage transistors.

Figure 6.12 shows a magnified view of Regions 1 and 2 of Figure 6.11 in order to better display the dimensions of the bump bond electrode and its isolation from the fast switching digital circuits.

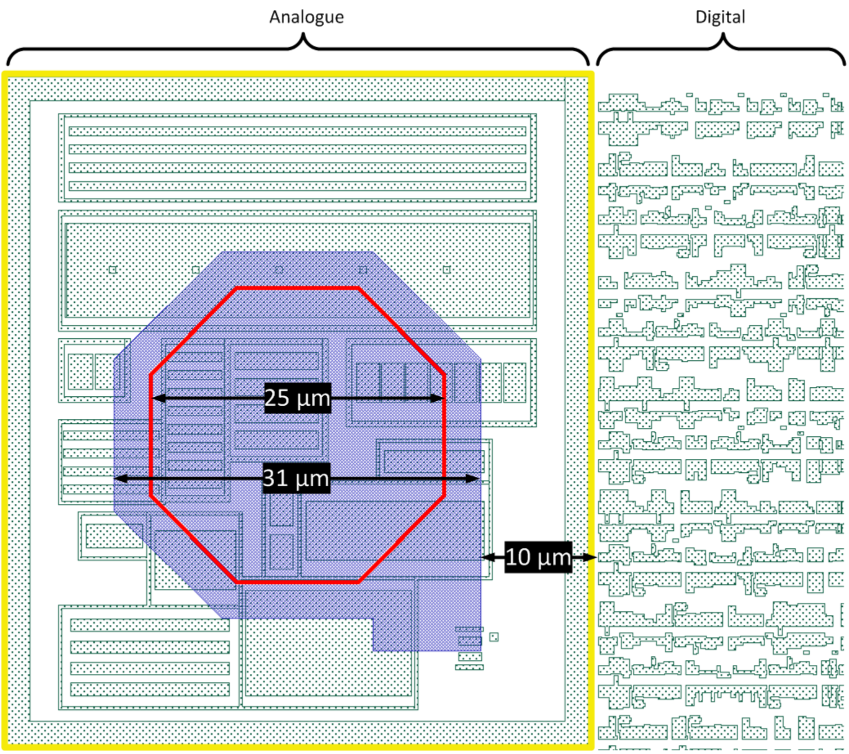


Figure 6.12: Layout of the bump bond electrode in Dosepix

Magnified regions 1 & 2 from Figure 6.11 (yellow box). **Green**: active layer (RX). **Purple**: Metal 8 (MA). **Red**: passivation layer opening (DV).

6.6 Pixel Performance Summary (Digital)

Table 6.1 summarises the main design parameters of the Dosepix pixel digital processing blocks.

Digital Blocks	
ToT counter depth	
Energy binning mode:	12 bits
Photon counting mode:	8 bits
Energy integration mode:	24 bits
Digital thresholds (energy binning mode):	16 thresholds (12-bit ToT value)
No. energy bins (energy binning mode):	16 energy bins
Bin counter depth (energy binning mode):	16 bits
Bin assignment time (energy binning mode):	up to 16 RefClk cycles
DataClk frequency:	up to 10 MHz
RefClk frequency:	8.3 MHz to 100 MHz
ToT measurement resolution:	10 ns to 120 ns
Number of data streams:	2 (ToT data and energy bin data)
ToT readout deadtime @ 10 MHz	
Energy binning mode:	0 s
Photon counting mode:	0.21 ms
Energy integration mode:	0.61 ms
Bin readout deadtime @ 10 MHz	
Energy binning mode:	0.41 ms/column
Static digital power consumption:	6.98 µW/pixel
Total digital power consumption[3]	
@ 13.5 kPhotons/sec (22.101 keV)	
Without column clock gating:	978 µW/column
With column clock gating:	213 µW/column
@ 0.135 Photons/sec (22.101 keV)	
Without column clock gating:	529 µW/column
With column clock gating:	112 µW/column

Table 6.1: Pixel performance summary (digital)

6.7 Chip Power Consumption

From simulation and estimation, the Dosepix ASIC consumes 7.5 mW under typical APD flux conditions when column clock gating is enabled.

[3]Based on calculation of photon flux for $H_p(10)$ measurements of 0.1 Sv/h and 1 µSv/h, respectively.

7 Measurements with the Dosepix Detector

Dosepix can be tested in a number of ways. The electrical performance of the pixel frontend can be studied through the injection of controlled charge signals using the analogue test pulse whose magnitude is programmable using the Periphery DACs. The digital state machines and various data acquisition modes can also be verified using the digital test pulse whose width is determined by the TestPulse input pad. The two forms of test pulses can be used to evaluate the electrical performance of bare ASICs or to complement the characterisation of full hybrid assemblies (*i.e.* ASIC bump bonded to sensor). The results reported in this chapter begin with electrical measurements of a bare ASIC using test pulses. In the latter half of the chapter, results are presented from measurements on a full hybrid assembly exposed to characteristic X-rays. The chapter concludes with a table summarising the main figures of merit. It should be noted that the measurements presented in this chapter and in Paper VIII [104] are intended to demonstrate the Dosepix ASIC functionality; full characterisation of the Dosepix assembly as an ionising photon detector and dosimeter are beyond the scope of this work.

7.1 Readout Systems

Readout of Dosepix is implemented as a chip-on-board (COB) system, where the Dosepix ASIC (or full hybrid assembly) is glued to the COB daughterboard, shown in Figure 7.1, with wirebond connections between the COB board and chip IO pads. The COB board acts as an intermediate interface which can connect to various readout systems via an off-the-shelf data socket, allowing versatile readout and testing.

There are currently two readout systems for Dosepix communications and control: the Credence Sapphire integrated circuit (IC) tester and the Dosepix testboard.

The IC tester is the automated test equipment (ATE) shown in Figure 7.2a. Figures 7.2b and 7.2c show a bare Dosepix ASIC mounted on the COB board, which is connected to various interface cards to communicate

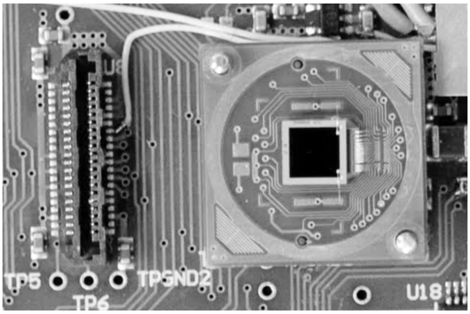


Figure 7.1: Dosepix chip-on-board

The COB daughterboard (designed by N. Kochanski, IBA Dosimetry) allows Dosepix to interface with different readout systems. The COB board in this photo is connected to the Dosepix testboard underneath. To its left is an open socket which can be connected to another COB for simultaneous operation of multiple Dosepixes.

with the IC tester instruments. The Verilog testbenches which were used during the design of Dosepix digital circuits were modified to output test vectors for the IC tester.

The Dosepix testboard contains multiple COB-compatible data sockets to simultaneously test several Dosepix assemblies. A low power microcontroller executes the firmware for hardware control. The testboard connects to the universal serial bus (USB) port of a computer and the microcontroller firmware interfaces with the software utility DPSim. Figure 7.3 shows a photograph of a Dosepix assembly with its COB mounted on a Dosepix testboard irradiated by a radiation source.

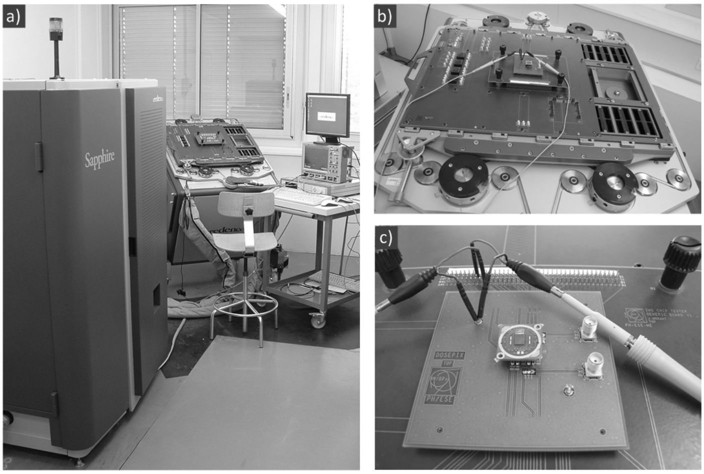


Figure 7.2: Electrical measurements with the IC tester

The Credence Sapphire test platform in the microelectronics section at CERN. This test system allows the user full control of signal voltage levels and precise timing manipulation. The interface cards were designed by D. Porret and J. Morant, CERN.

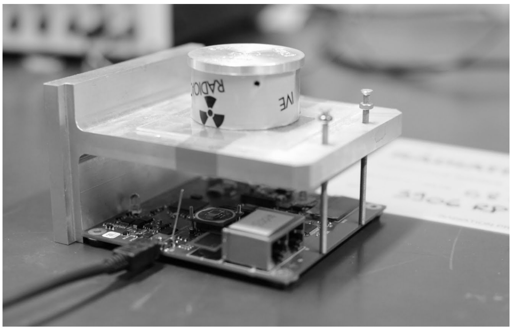


Figure 7.3: Radiation measurements with the Dosepix testboard

The Dosepix testboard (designed by N. Kochanski, IBA Dosimetry) is a portable system which connects to a computer via USB. Firmware (written by M. Jentsch of IBA Dosimetry and W. Haas of Friedrich-Alexander Universität Erlangen-Nürnberg) in the 32-bit microcontroller provides control signals to the multiple Dosepixes which can be connected to the testboard via COB daughterboards. The DPSim software (written by S. Wölfel, IBA Dosimetry) reads programming scripts to operate the testboard and writes data from the Dosepixes into text files for offline analysis. In this photo, the testboard with a single Dosepix hybrid assembly is placed under a ^{109}Cd source for the measurement of photons.

7.2 Electrical Measurements with Test Pulses

Prior to the availability of full Dosepix assemblies, initial tests were conducted on bare Dosepix ASICs connected to COBs interfaced with the IC tester readout system. The S-curve measurement of Figure 7.4 provides a method to measure frontend pulse heights in response to input charge, and also the electronic noise of the frontend system. The measurement (with the pixels operating in photon counting mode) sweeps through a range of V_{thres} DAC values and many test pulses are asserted per threshold voltage setting. The Preamplifier outputs inverted voltage pulses in response to the two polarities of electrostatic charge injected by the test pulse. When V_{thres} is set at ①, the Event Counter (of the schematic in Figure 6.5) records zero counts. As V_{thres} nears ②, DiscOut asserts whenever $VOut_{Preamp}$ crosses V_{thres}; however, this only occurs for a fraction of test-pulse events, as the $VOut_{Preamp}$ peak fluctuates with the electronics noise. When V_{thres} is fully within the $VOut_{Preamp}$ height (*e.g.* at ③), then DiscOut asserts for 100% of the test pulses. When the threshold voltage is at the baseline DC voltage of the Preamplifier output node (④), the Discriminator asserts each time the noise causes $VOut_{Preamp}$ to cross V_{thres}; this region is called the "pedestal". When V_{thres} is set at ⑤, the threshold is fully within the pulses in response to the injection of negative charges.

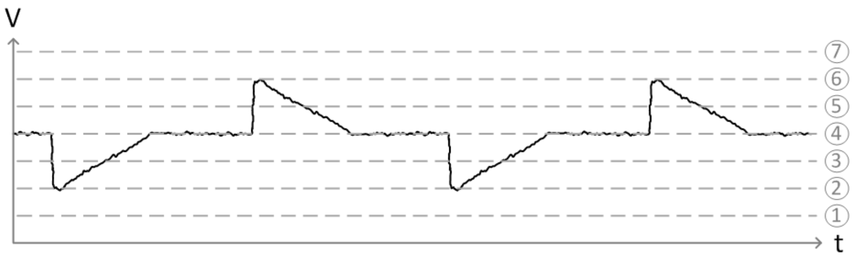


Figure 7.4: S-curve measurement method

Illustration of the S-curve measurement method with test charge injection to the frontend input using the analogue test pulse.

Figure 7.5 shows S-curve measurement results of a single Dosepix pixel on a bare ASIC, with the pixel configured in photon counting mode. Since the analogue test pulse can inject both positive and negative charges, the S-curve in Figure 7.5a shows the frontend response to both polarities of input. Plotting pulse height versus quantity of injected charge provides the frontend gain (Figure 7.5b).

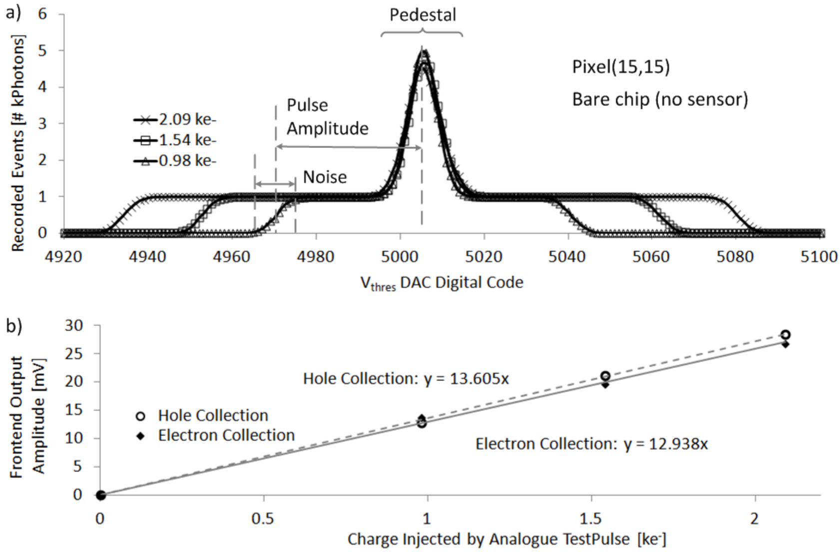


Figure 7.5: S-curve measurements with the analogue test pulse

a) Output of the Event Counter in response to analogue test pulse input for a range of threshold voltage settings. The output of a single pixel from a bare Dosepix ASIC is shown here. 1000 test pulses are injected for each V_{thres} value over 50 frames. The measurement is repeated for three different quantities of injected charge. The Preamplifier output pulse height in response to each input charge quantity can be determined by fitting the S-curve to an error function; the pulse height is the voltage difference between the pedestal mean and the S-curve inflection point. **b)** The frontend gain is the slope of the plot of pulse height versus input charge.

7.2.1 *Analogue Threshold Equalisation*

As explained in Chapter 5, physical variations in manufactured transistors cause mismatch between identically-designed transistors in different pixels. This channel-to-channel mismatch results in different effective threshold voltages of the Analogue Discriminator. The ToT versus input charge measurements from 16 pixels of the same chip demonstrate the analogue threshold offset between these 16 pixels. In Figure 7.6, the analogue threshold is programmed nominally at ∼7.5 ke$^-$. The input charge where each Analogue Discriminator actually sees the analogue threshold is located at the point at which the ToT Counter starts to record non-zero values. The different effective analogue thresholds seen by these 16 pixels is due to offset in the Analogue Discriminators.

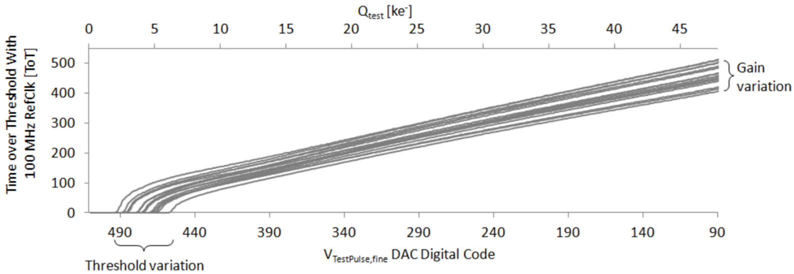


Figure 7.6: ToT calibration curves from an unequalised chip

A 6-bit current DAC in each pixel provides a means to tune the effective threshold of each channel to achieve a more uniform behaviour in the entire pixel matrix. The appropriate digital value of the six trim bits can be found in a number of ways, for example by determining the native (unadjusted) pedestal mean of each pixel using analogue test pulses or radioactive sources, or by determining the edge of the Gaussian noise distribution by counting discriminated noise-threshold crossings without any external input stimulus. Each of these methods involves two sets of sweeps through a range of V_{thres} values with the chip placed in photon counting mode. In each sweep, all pixels are programmed with their threshold adjustment (ThAdjust) bits set to the maximum (or minimum) digital value. The effective threshold of each pixel with the maximum (or minimum) ThAdjust code is then determined by examining the Event Counter contents for each V_{thres} setting. The quantity of current encoded in the least significant bit (LSB) of the Threshold Adjustment DAC is chosen such that the threshold distributions resultant from the two extreme ThAdjust codes overlap by a single threshold value. This overlap value is used as the target threshold. Assuming linear threshold adjustment behaviour, the appropriate ThAdjust code for each pixel is calculated by interpolating the effective threshold at each extreme ThAdjust code to find the code which would shift the Discriminator response towards the target threshold. Figure 7.7 shows the two distributions of pixel noise edges for the maximum and minimum trim bit codes, and the final distribution of pixel noise edge when each pixel is assigned an unique ThAdjust code.

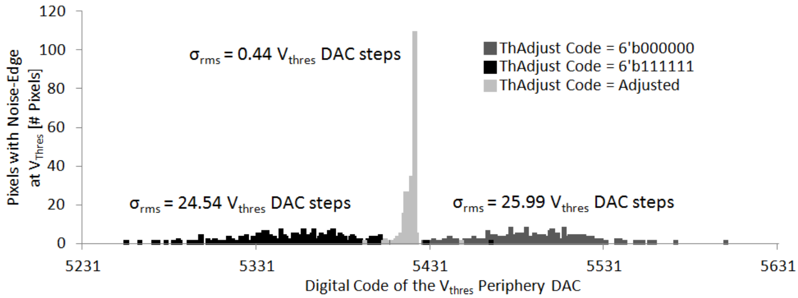


Figure 7.7: Threshold equalisation of a Dosepix assembly

Using the adjusted analogue thresholds of Figure 7.7, Figure 7.8 shows the ToT versus input charge measurement from the same set of pixels as Figure 7.6, but with the analogue thresholds equalised and the effective analogue threshold programmed to 2.2 ke$^-$. The spread of effective analogue thresholds seen by the pixels is greatly reduced by the analogue threshold equalisation. However, there remains a variation in frontend gain, which is apparent from the difference in slopes of the ToT curves. The gain variation can be corrected by the digital threshold equalisation presented in the next section.

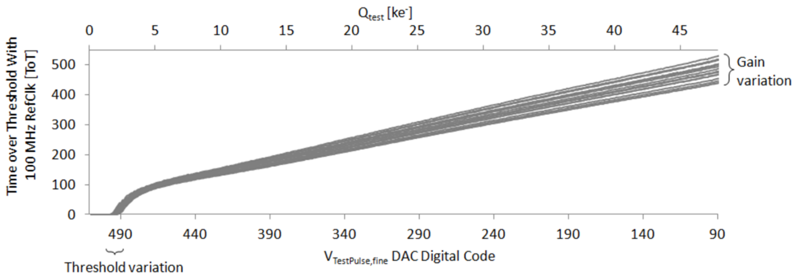


Figure 7.8: ToT calibration curves from an equalised chip

7.2.2 *Digital Threshold Equalisation*

The analogue threshold equalisation presented in the previous section reduces the threshold offsets, but does not correct for frontend gain variations. Since Dosepix has 16 digital thresholds per pixel, gain variations can also be adjusted through *digital threshold equalisation*.

Figure 7.9 shows the output of the Energy Bin Registers of the 16 pixels of Figure 7.8, which have had their analogue thresholds equalised, after 15 minutes of irradiation from an ^{241}Am source (with α particles filtered out). In this measurement, all pixels contain the same set of 16 digital thresholds. The gain variation causes a broadening of the photopeak.

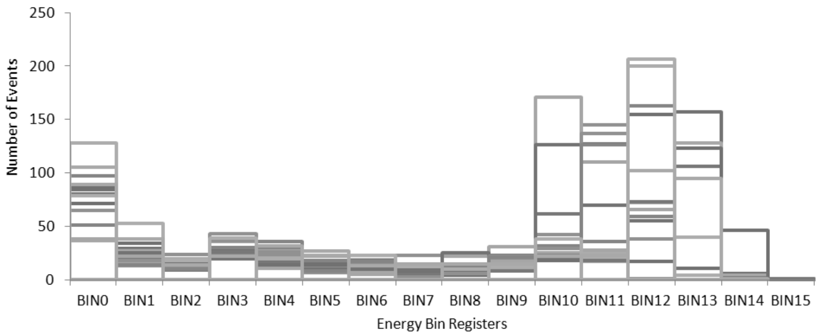


Figure 7.9: Energy binning with analogue but not digital threshold tuning

Energy bin measurements measured in 16 pixels of a Dosepix ASIC bump bonded to a 300 μm thick silicon sensor irradiated with photons from an ^{241}Am source for 15 minutes. The *analogue threshold* was equalised, but the *digital thresholds* were untuned.

Digital threshold equalisation of the chip involves assigning a unique set of digital thresholds to each pixel. Figure 7.10 shows the distribution of ToT values corresponding to 16 frontend input charge signals injected by the analogue testpulse. These 16 input charge values were chosen to define 16 energy bins spaced 4 keV apart, starting at 10 keV. Using the data from this measurement to define a unique set of 16 digital thresholds for each pixel, Figure 7.11 shows the same measurement as Figure 7.9, but with the digital thresholds equalised to define the same energy ranges for each pixel.

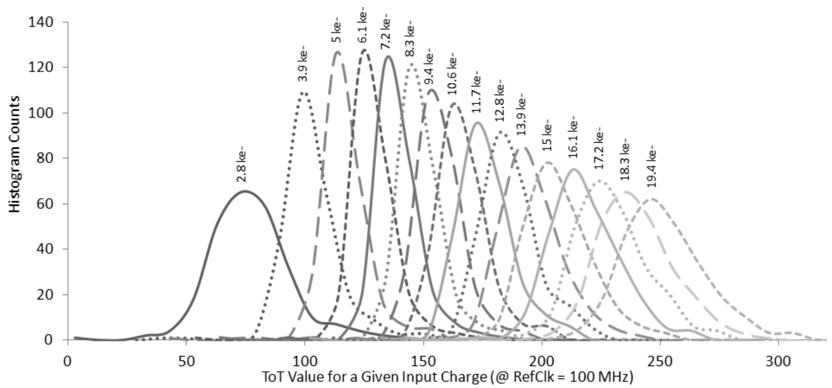


Figure 7.10: Digital threshold distributions of 256 pixels on the same chip

The ToT value recorded by each of the 256 pixels on a single Dosepix assembly (with equalised analogue threshold) for 16 values of frontend input charge (from the analogue test pulse) which define energy bins spaced 4 keV apart, starting at 10 keV (2.7 ke$^-$).

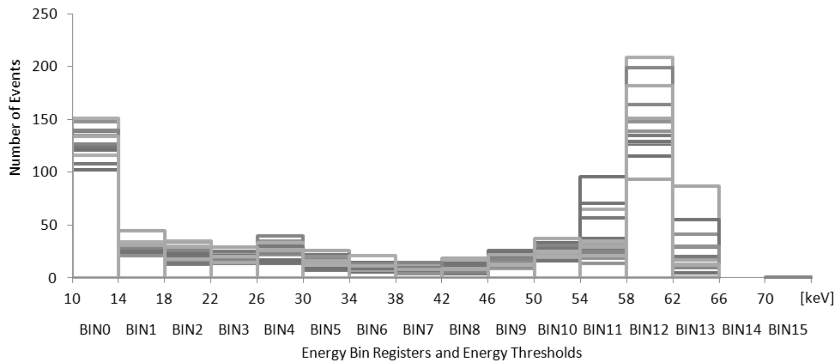


Figure 7.11: Energy binning with analogue and digital threshold tuning

Energy bin measurements measured in 16 pixels of a Dosepix ASIC bump bonded to a 300 μm thick silicon sensor irradiated with photons from an ^{241}Am source for 15 minutes. The analogue threshold was equalised using the data of Figure 7.7 and the digital thresholds were equalised using the data of Figure 7.10. The analogue threshold is set at 8 keV. The ^{241}Am source provides 59.5 keV γ-rays; the α particles have been filtered.

7.3 Characterisation with Sensor

Characterisation of the Dosepix detector assembly (*i.e.* Dosepix ASIC with silicon sensor) requires many monoenergetic photons. Although a radioisotope source placed close to the detector (such as in the setup shown in Figure 7.3) would provide monoenergetic photons, the flux escaping the source would be too low to be of practical use for characterisation. Therefore, the Dosepix detector assembly was characterised by measuring fluorescence photons escaping various target materials in the setup depicted in Figure 7.12.

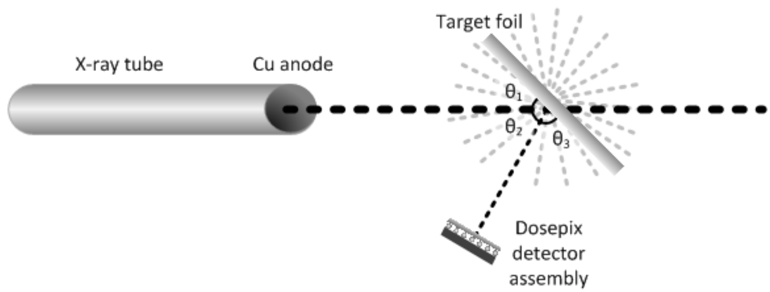


Figure 7.12: Setup to measure fluorescence photons

In this measurement setup, the direct beam from an X-ray tube impinges on a target foil placed a few centimetres from the tube anode. The beam X-rays activate the atoms in the foil, causing the release of fluorescence photons. Although these fluorescence photons escape the target material in all directions, the optimal placement of a detector is at an angle from the front face of the target. In the measurements reported in the following sections, the Dosepix detector assembly was placed a few centimetres from the target at $\Theta_2 \simeq 45^{\circ}$.

Table 7.1 lists the characteristic X-ray energies of anode and target materials commonly used in medical imaging. The energies listed in this table were used to calculate the figures of merit reported in the following sections.

		Relative Intensity of Photons Leaving Target		Photon Energy [keV]		
Z	Element	Kα	Kβ	Kα	Kβ	K(α,β)
29	Cu	0.882	0.118	8.040	8.904	8.140
42	Mo	0.838	0.141	17.441	19.605	17.685
46	Pd	0.830	0.146	21.121	23.815	21.433
48	Cd	0.826	0.148	23.106	26.091	23.456
49	In	0.823	0.150	24.136	27.271	24.509
52	Te	0.817	0.152	27.377	30.990	27.816

Table 7.1: Characteristic anode and target fluorescence lines

When activated (such as by the setup shown in Figure 7.12), a target atom releases a fluorescence photon when the electron from an outer shell fills an inner shell vacancy caused by ionisation from impinging X-rays. The characteristic fluorescence photon carries the difference in binding energies between the two electron shells. Typically, ionisation causes the removal of an electron from the K-shell. If the vacancy in the K-shell is filled by an electron from the adjacent L-shell, the resultant characteristic fluorescence photon is called a Kα photon. Otherwise, when the vacancy is filled by an electron from one of the other shells, the fluorescence photon is called a Kβ photon. This table lists the Kα and Kβ energies of X-ray anode and target materials often used in medical imaging, and the relative intensities of each type of fluorescence photon escaping the target. The final column shows the weighted average characteristic photon energy, K(α,β), which is calculated by weighting the energies of the Kα and Kβ photons with their relative intensities absorbed by a 300 μm-thick silicon sensor. The data analysis in the following sections use this weighted average whenever the detector cannot resolve between the Kα and Kβ energies. Data from [105].

The figures on the following pages show example measurements made using a Dosepix assembly under the conditions listed in Table 7.2 and using the setup depicted in Figure 7.12. Figure 7.13 shows S-curve measurements taken by scanning through V_{thres} values while irradiating the Dosepix assembly with fluorescence photons from each target and from the Cu anode of the x-ray tube. Figure 7.14 plots the results of the fitted data from measurements with different target foils to determine the frontend gain of each pixel.

X-ray tube anode material:	Cu
Target foil materials:	Pd, Cd and In
Tube current:	40 mA
Tube kVp:	45 kV
Readout system:	Dosepix testboard
Readout software:	DPSim version 1.3
Sensor (of full hybrid assembly):	300 μm-thick silicon with collection of holes
Analogue voltage supply ($V_{DD,analog}$):	1.5 V
Threshold voltage (V_{thres}) for ToT measurements:	1.7 ke$^-$
Preamp OTA bias current (I_{preamp}):	6 μA/pixel
Preamp reset/leakage compensation current (I_{krum}):	0.5 nA/pixel
ToT RefClk frequency:	10 MHz (direct from testboard, bypass PLL)

Table 7.2: Dosepix detector assembly measurement parameters

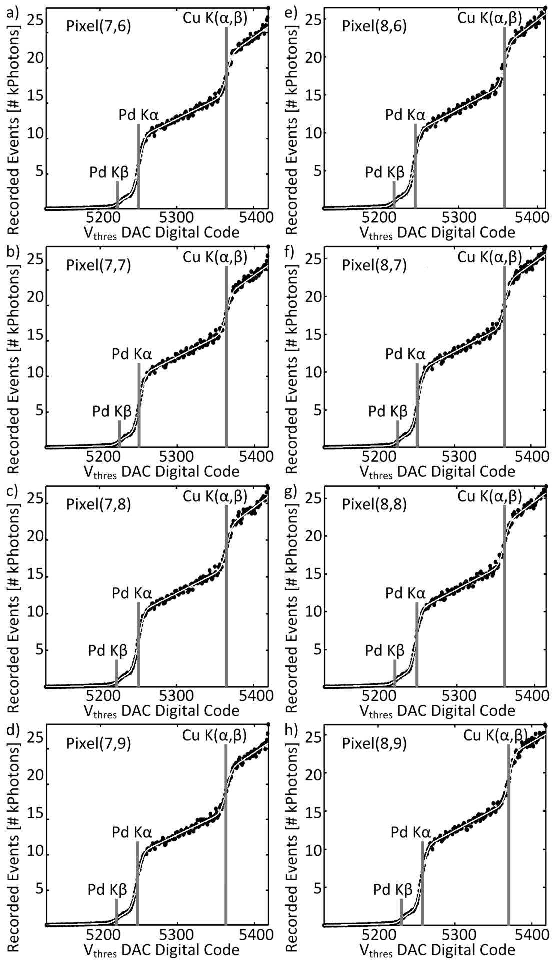


Figure 7.13: S-curve measurements of fluorescence photons

Using the measurement setup of Figure 7.12, the S-curves (see explanation of Figure 7.5a) were measured for V_{thres} scans; three separate scans were done with the Dosepix assembly irradiated with fluorescence photons from Pd, Cd and In. Example S-curves are shown for the central pixel cluster detecting fluorescence photons from a Pd target bombarded by a beam from an X-ray tube with a Cu anode. The Dosepix assembly is able to resolve the Pd Kα and Pd Kβ characteristic X-ray energies, and a single combined Cu K(α,β) characteristic X-ray energy. This data is combined from 1200 Event Counter readouts (with the pixels set in photon counting mode) for each V_{thres} setting. Curve fitting courtesy of G. Blaj, CERN.

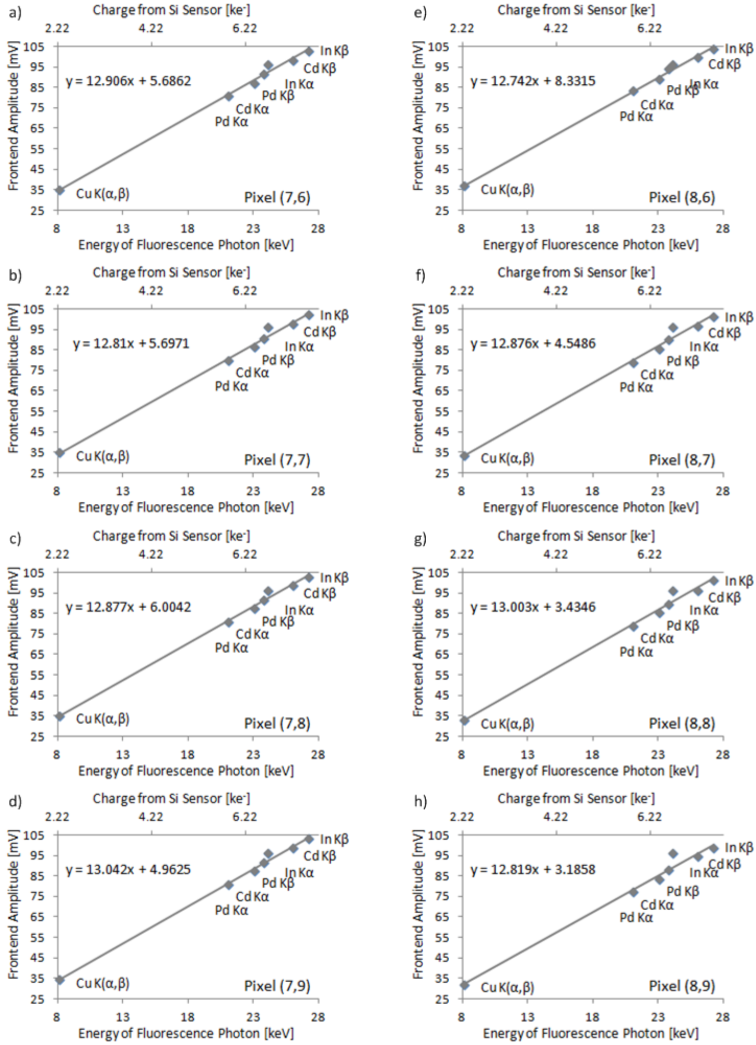


Figure 7.14: Frontend amplitude versus deposited energy

Plot of results from the S-curve fits of Figure 7.13 versus known characteristic X-ray energies, for three sets of S-curve measurements using Pd, Cd and In target foils (curve fitting courtesy of G. Blaj, CERN). The location of each S-curve inflection point is converted to an equivalent voltage using the V_{thres} Periphery DAC gain of 0.4 mV/DAC step. The pedestal mean of each pixel had already been determined during the threshold equalisation of this Dosepix assembly. The slope of the linear fit of pulse height versus injected charge provides each pixel frontend gain in mV per ke$^-$.

Figure 7.15 presents ToT spectra taken using the setup of Figure 7.12. The spectrum of ToT data read from the ToT Register is plotted with data read from the Energy Bin Registers for comparison. The automatic event binning and in-pixel data storage of the Energy Bin Registers drastically reduces the overhead of reading out detected events. For example, in Figure 7.15a, 23% more photons were recorded in a single readout of the Energy Bin Registers after a 6000 ms exposure than in 6000 1 ms-exposure readouts of the ToT Register. Figure 7.15a includes a plot an off-chip binning of the 6000 frames of ToT Register data and Figure 7.15b presents the normalised relative number of counts between the Energy Bin Register data and the binned ToT Register data. Figure 7.16 shows the same measurement, but with Column Clock Gating (CCG) enabled. CCG turns off the RefClk signal being driven up the column when the RefClk signal is not needed, thereby greatly reducing the chip digital power consumption. Differences in the recorded ToT values between running the chip with CCG disabled and enabled are studied in Figure 7.17. In Figure 7.17b, photo-peak locations determined from fitting the ToT spectra of measurements using Pd, Cd, and In target foils are plotted for CCG off and on cases to show the relationship between ToT counts and photon energy.

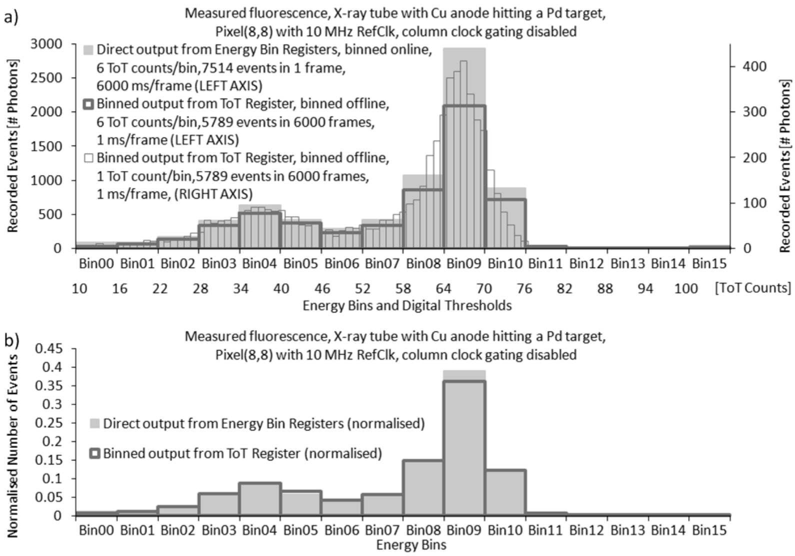


Figure 7.15: ToT spectra without column clock gating

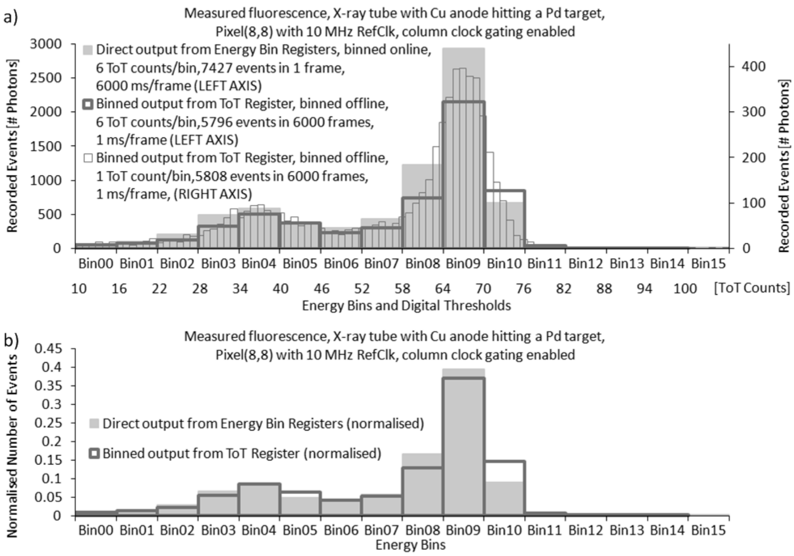


Figure 7.16: ToT spectra with column clock gating

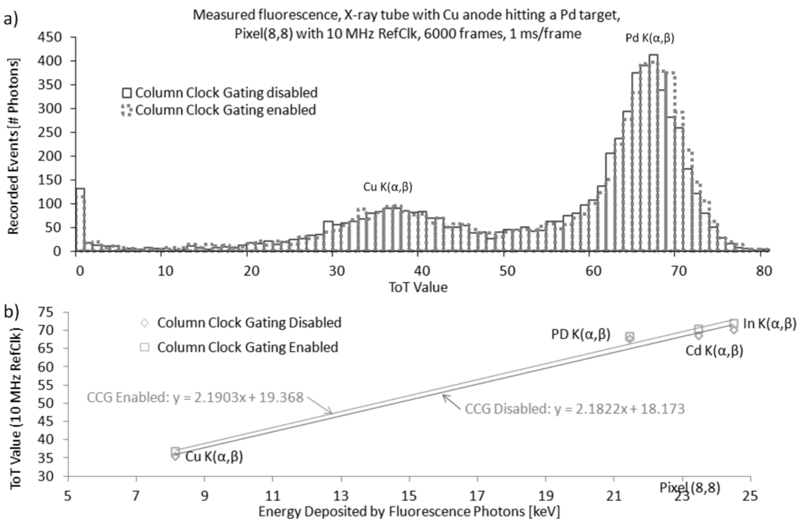


Figure 7.17: ToT spectra shift due to column clock gating

a) ToT Register data after irradiation with fluorescence photons. **b)** Plot of photopeaks from ToT data which were fit to determine the ToT value corresponding to the photopeak of the Cu anode and photopeaks from separate measurements of fluorescence photons from Pd, In and Cd targets (Gaussian fits courtesy of G. Blaj, CERN).

7.4 Chip Measurement Summary

Table 7.3 summarises the main values measured from the Dosepix ASIC and Dosepix ASIC assembly with 300 μm silicon sensor.

Dosepix ASIC	
ENC	
Bare chip:	85 e^-_{rms}
With sensor:	120 e^-_{rms}
Frontend gain:	12.7 mV/ke^-
Gain variation:	0.19 mV_{rms}
Maximum analogue test pulse charge, Q_{test}:	49 ke^-
ToT monotonic range:	>49 ke^- (176 keV)
DiscOut width @ Q_{in}=5.96 ke^-	
CCG disabled:	67.7 10-MHz-ToT counts
CCG enabled:	68.3 10-MHz-ToT counts
ToT spectrum offset due to CCG:	+1.2 10-MHz-ToT counts
Threshold variation	
Before tuning:	760 e^-_{rms}
After tuning:	14 e^-_{rms}
Chip analogue power consumption[1]:	5.8 mW
Chip digital power consumption[2]	
CCG disabled:	40.7 mW
CCG enabled:	9.0 mW
PLL power consumption[3]:	481 μW
Total power consumption:	15.3 mW

Table 7.3: Dosepix measurement summary

[1] Note: the analogue biasing settings for this measurement were not optimised for power consumption; rather the biasing conditions were deliberately placed at conservative values for initial measurements.

[2] With 100 MHz RefClk and constant 100 kHz digital test pulses sent to every pixel. These power consumption conditions are unrealistically high, particularly for the APD application.

[3] Note: the PLL was designed to lock for a 10 MHz input clock, but this power measurement was taken for a PLL locking for a 20 MHz input clock; thus the PLL consumes more power than originally foreseen.

8 Summary

This thesis has presented the design, implementation, and functional testing of a low power hybrid pixel detector ASIC intended for use in an active personal dosimeter and in a kVp meter. Hybrid pixel detectors consist of separate semiconductor sensor and quantum processing ASIC components, permitting the separate optimisation of both modules for radiation detection. Modern deep sub-micron technologies permit the realisation of high transistor and functional densities with low power consumption, enabling a complete signal processing chain to be implemented at the signal collection node. Hybrid pixel detector technology has been successfully used in high energy physics experiments at CERN and in X-ray imaging projects such as the Medipix2 and Medipix3 Collaborations. Exploiting the inherently low noise characteristics of small pixels, photon counting detectors such as the Medipix chipset are able to suppress noise and reliably process a very large dynamic range of energy signals.

The Dosepix ASIC, developed as a joint research project between CERN, Friedrich-Alexander University Erlangen-Nuremberg, and IBA Dosimetry, was implemented in a 0.13 μm CMOS technology for the purpose of personal dosimetry and general radiation detection of photons. The ASIC contains 16×16 square pixels of 220 μm side-length, with a total 12.4 mm^2 sensitive area. The small sensor areas of the parallel channels limit the signal flux to be processed by each pixel frontend to permit accurate dose measurements in both high and low flux radiation environments. Furthermore, the low power consumption allows the Dosepix hybrid pixel detector to be used as a component in a compact portable dosimeter.

The specifications for the chip were determined through studies of photon dose reconstruction [25] and compliance with international standards [84]. Each pixel acts as an individual energy spectrum analyser and contains various data memory structures to permit concurrent chip data measurement and readout. Because of the individual energy measurement of discrete photons (through time over threshold, ToT), the personal dose equivalent reconstructed from (simulations of) the chip output exhibit a very flat response over the entire range of photon energies relevant to personal dosimetry [25].

Each pixel has three modes of data acquisition. In energy binning mode, the pixels each contain 16 digital energy bins to store the pre-sorted count of the number of photons detected during the open (electronic) shutter period. Column-addressable readout permits constant photon processing of at least 15 columns at all times. A Wakeup digital output signal provides alerts to the readout system. Last-recorded single pulse ToT values can be read out without disrupting ToT measurements and energy bin assignments. In photon counting mode, the pixels record the number of detected photons during the open electronic shutter period. This mode has been used for the preliminary characterisation of the ASIC bump-bonded to a 300 μm-thick silicon sensor. In energy integration mode, a 24-bit ToT counter records the cumulative energy deposited in the sensor.

Following the promising results of personal dose equivalent accurately reconstructed from simulation data [25], and the demonstrated performance of the Dosepix ASIC bump bonded to a silicon sensor, the project team plans to investigate prototype implementations of a portable dosimeter consisting of multiple Dosepix assemblies with various filters over the silicon sensors to permit the reliable reconstruction of dose for a large range of photon energies. Development of a kVp meter using Dosepix will subsequently follow. The Dosepix detector will also be used as a tool for physics students and researchers to study photon detection and energy spectrum analysis.

In summary, the Dosepix hybrid pixel detector is a low power semiconductor photon dosimeter which measures the energy of individual photons while suppressing noise and background signals. The Dosepix ASIC continuously records pre-binned spectral measurements in real time, and the combination of many small pixels processing photo-induced signals in parallel permits reliable performance in both low and high flux radiation environments. Table 8.1 summarises the key features and measured values of the Dosepix hybrid pixel assembly prototype.

Square pixel side-length:	220 μm
No. pixels:	256
Sensor:	300 μm-thick silicon
Overall sensitive area:	12.4 mm^2
Chip dimensions:	3.5 mm × 5.2 mm
No. wirebond pads:	30 (single-ended CMOS)
Data readout interface:	SPI
Alert for readout:	Energy Bin(s) full or large charge detected
No. global DACs:	14
No. analogue threshold settings:	8192
PLL input reference frequency:	20 MHz[1]
PLL output frequencies:	16.6, 20, 25, 33.2, 50, 100, or 200 MHz
Charge carrier polarity:	Configurable (holes or electrons)
No. trim bits (threshold offset):	6 bits
Gain variation correction:	12-bit digital threshold tuning
ToT counter depth	
Energy binning mode:	12 bits
Photon counting mode:	8 bits
Energy integration mode:	24 bits
Digital thresholds (energy binning mode):	16 thresholds (12-bit ToT value)
No. energy bins (energy binning mode):	16 energy bins
Bin counter depth (energy binning mode):	16 bits
DataClk frequency:	up to 10 MHz
Pulse processing duration:	of the order of μs[2]
ToT measurement resolution:	5 ns to 60 ns
Number of data streams:	2 (ToT data and energy bin data)
ToT readout deadtime @ 10 MHz	
Energy binning mode:	0 s/frame
Photon counting mode:	0.21 ms/frame
Energy integration mode:	0.61 ms/frame
Bin readout deadtime @ 10 MHz	
Energy binning mode:	0.41 ms/column (but there are always at least 15 columns recording data)
ENC with sensor:	120 e^-_{rms}
Frontend gain:	12.7 mV/ke^-
Gain variation before digital corrections:	0.19 mV_{rms}
Threshold variation after tuning:	14 e^-_{rms}
Chip analogue power consumption:	5.8 mW
Chip digital power consumption with CCG:	9.0 mW
PLL power consumption:	481 μW
Total power consumption:	15.3 mW[3]

Table 8.1: Overall Dosepix summary

[1]The PLL locks at 20 MHz rather than the 10 MHz design value. The Dosepix testboard has been modified to provide a 20 MHz PLLClk.

[2]The exact value depends on the input charge and Periphery DAC settings.

[3]The power consumption reported here is based on conditions which are appropriate for preliminary measurements but are not the optimal settings for low power operation. The digital power consumption was also measured with a constant high frequency digital test pulse sent to all pixels, but this high rate of input would not occur in the APD application.

A

Noise Sources

Noise results from random fluctuations which randomly modify the frontend signal. This appendix presents a brief overview of the main noise contributions from MOSFET transistors (since MOSFETs are the main building blocks of the Dosepix frontend) and from the sensor leakage current. Detailed calculations of frontend noise can be found in [57; 58; 38] and an explanation on input-referred equivalent noise charge (ENC) of a pixel frontend is presented in [59].

Main MOSFET Noise Sources

Thermal Noise

Thermal noise in resistive circuit components result from thermal fluctuations in the motions of charge carriers in the resistor, independent of the current flowing through the resistors [57; 58]. When modelled as a voltage source in series with the resistor, the thermal noise power spectral density of the resistor is:

$$\frac{\overline{v^2}}{\Delta f} = 4kTR \qquad [\mathrm{V}^2/\mathrm{Hz}] \tag{A.1}$$

where k is the Boltzmann constant, T is the absolute temperature, R is the resistance, and Δf is the system bandwidth.

In the frontend systems described in this thesis, there is thermal noise from the resistive transistor elements, and from the MOSFET channel. Of the resistive gate, source, drain, and bulk, the thermal noise from the polysilicon gate dominates. The thermal noise power spectral density from the gate is:

$$\frac{\overline{v^2}}{\Delta f} = 4kTR_G \qquad [\mathrm{V}^2/\mathrm{Hz}] \tag{A.2}$$

where R_G is the gate resistance.

The thermal noise power spectral densities in the channel of a MOSFET biased in strong inversion and in weak inversion, respectively, are [106]:

$$\frac{\overline{v^2}}{\Delta f} = 4kTn\frac{2}{3}\frac{1}{g_m} \qquad \text{in strong inversion } [\mathrm{V}^2/\mathrm{Hz}] \tag{A.3}$$

$$\frac{\overline{v^2}}{\Delta f} = 4kTn\frac{1}{2}\frac{1}{g_m} \qquad \text{in weak inversion } [\mathrm{V}^2/\mathrm{Hz}] \tag{A.4}$$

where the slope factor n is the derivative of the gate voltage over the pinch-off voltage [107] and g_m is the gate to source transconductance.

Flicker ($\frac{1}{f}$) Noise

The exact mechanisms which cause flicker noise are not fully understood [108]. Flicker noise is believed to be due to the random capture and release of mobile carriers in charge traps due to silicon crystal defects or extra energy states in the silicon interface with the gate oxide. The model of flicker noise is a voltage source in series with the MOSFET gate [108]:

$$\frac{\overline{v^2}}{\Delta f} = \frac{K_f}{C_{ox}^2 WLf} \qquad [\mathrm{V}^2/\mathrm{Hz}] \tag{A.5}$$

where K_f is the technology-dependent flicker noise coefficient, C_{ox} is the gate oxide capacitance, W is the transistor width, L is the transistor length, and f is the frequency. Flicker noise is independent of DC biasing and measurements show that the flicker noise in NMOS transistors is an order of magnitude higher than in PMOS devices [108].

Noise from the Senor Leakage Current

Shot Noise

Shot noise occurs due to random fluctuations in the current flowing through a device, such as a pn junction diode. The net current in a forward-biased diode results from majority carriers which gain sufficient energy to cross the potential barrier at the junction and diffuse as minority carriers [27]. Random fluctuations in the net current are a consequence of fluctuations in the number of majority carriers on each side of the junction with sufficient energy to cross the potential barrier [59]. The shot noise due to the sensor leakage current of a hybrid pixel detector is:

$$\frac{\overline{i^2}}{\Delta f} = 2qI_d \qquad [\mathrm{A}^2/\mathrm{Hz}] \tag{A.6}$$

where q is electron charge and I_d is the average value of the sensor leakage current.

Simulations of the Analogue Frontend B

The selected set of simulations presented in this appendix demonstrate frontend functionality. Unless otherwise indicated, all frontend simulations presented in this thesis were done using the conditions listed in Table B.1.

Simulator/device models:	Spectre
Simulated view:	Schematic[1]
Temperature:	27°C
Process parameters:	Typical-typical
Analogue voltage supply ($V_{DD,analog}$):	1.5 V
Analogue power consumption:	12.4 μW/pixel
Threshold voltage (V_{thres}):	12.1 mV (980 e$^-$)
Preamp OTA bias current (I_{preamp}):	3 μA/pixel
Preamp reset/leakage compensation current (I_{krum}):	2 nA/pixel
Capacitance from the sensor (C_{det}):	145 fF/pixel
Leakage current from the sensor (I_{leak}):	400 pA/pixel

Table B.1: Nominal frontend simulation conditions

Figure B.1 depicts the general operation of the analogue frontend. Figure B.2 demonstrates the effects of biasing conditions (and power consumption) on the system noise. Figure B.3 presents the effects of modifying I_{krum}. Figure B.4 shows the frontend linear range. Figure B.5 studies variations in the ToT measurement under different temperature conditions. Figure B.6 shows the effects of mismatch between pixels.

[1] An extracted view of the circuit includes the parasitic resistances and capacitances based on the circuit layout. Simulations based on the extracted view are more realistic than simulations of the schematic. However, the extracted view is not available until after the layout is complete. The frontend design was therefore based on schematic simulations, while extracted simulations were used for post-layout verification.

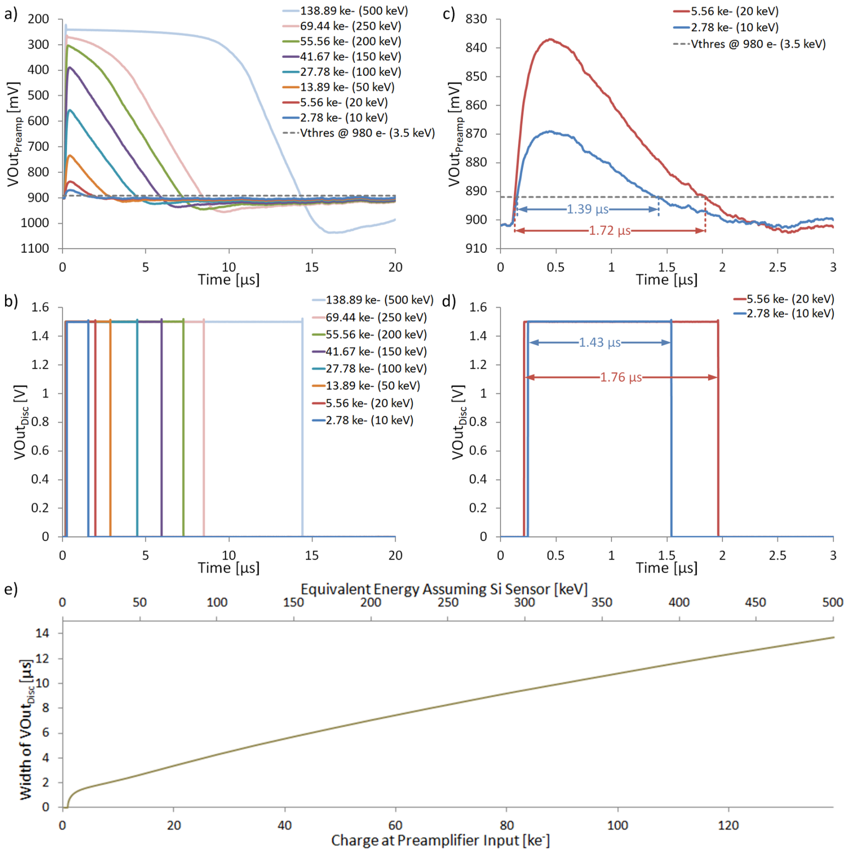


Figure B.1: General simulation of the frontend

Simulation of the frontend with charge from a silicon sensor input to the Preamplifier. **a)** Eight simulations of various quantities of charge collected at the Preamplifier input. The simulations include transient noise and the same noise seed is used in each simulation set. VOut$_{Preamp}$ reaches a maximum voltage for $Q_{in} > \sim 50$ ke$^-$. (See Figure B.4 for a more detailed demonstration of the Preamplifier linear range.) **b)** VOut$_{Disc}$ corresponding to the curves of **a**. **c&d)** Two simulations selected from the set shown in **a&b**. Note the relationship between Q_{in} and ToT. **e)** Discriminator output pulse width versus Q_{in}. Note: although the VOut$_{Preamp}$ amplitude no longer increases with input charge beyond $\sim$50 ke$^-$, the width of VOut$_{Preamp}$, and consequently the width of VOut$_{Disc}$, continues to have a linear relationship with Q_{in} beyond the Preamplifier saturation level.

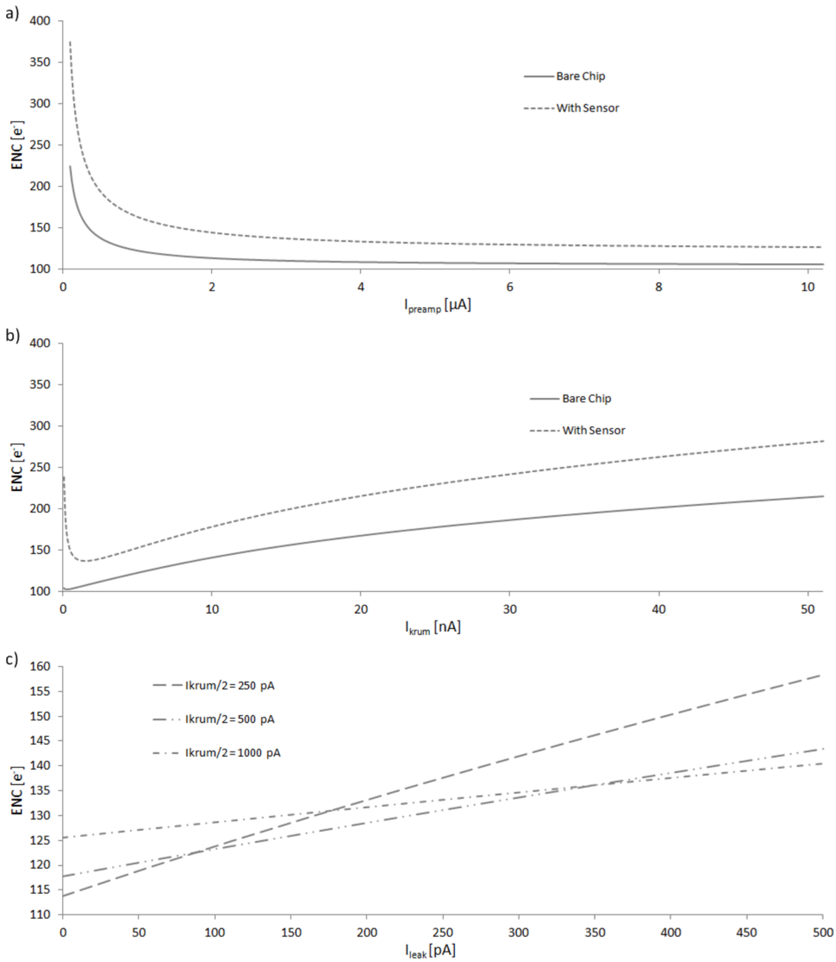


Figure B.2: Simulation of the equivalent noise charge

The sensor component of the pixel is modelled as a 145 fF capacitance in series with an input charge source (*i.e.* a current source delivering a δ(t) pulse with an integral equal to the charge), along with a leakage current source in parallel to the input. Simulations of both schematic and extracted views are shown for comparison. **a)** Equivalent noise charge (ENC) versus the bias current (I_{preamp}) of the Preamplifier OTA, with and without the sensor model. **b)** ENC versus the bias current (I_{krum}) of the Preamplifier reset and leakage compensation network, with and without the sensor model. **c)** ENC versus the sensor leakage current (I_{leak}), for two values of I_{krum}. Here, I_{preamp} = 3 μA and C_{in} = 145 fF.

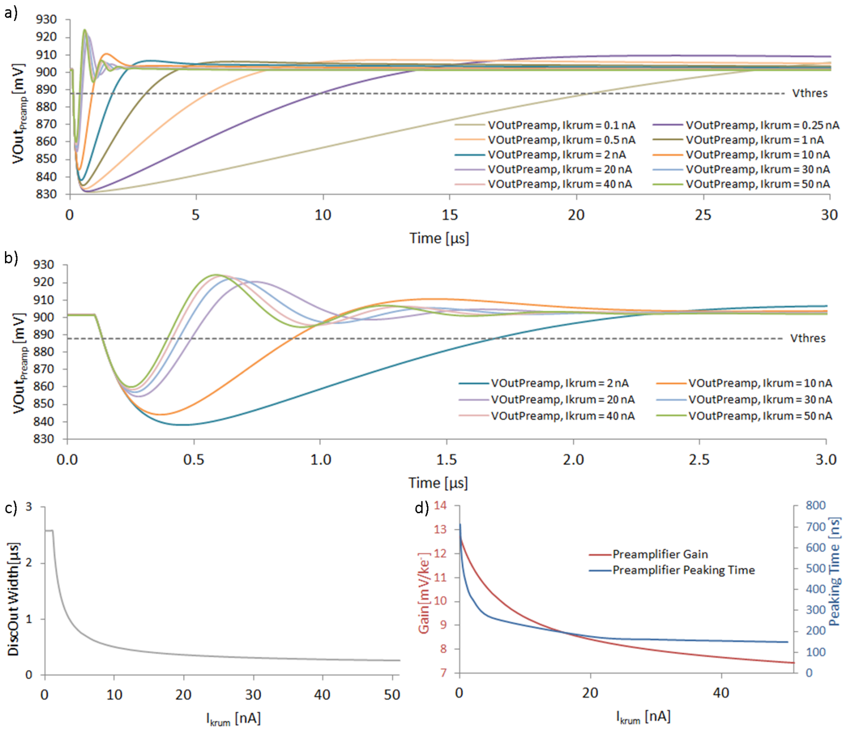


Figure B.3: Simulation of frontend with varying I_{krum}

The Preamplifier pulse duration depends on I_{krum}, the bias current which determines the transconductance in the reset loop. The larger the I_{krum}, the faster T_{Pulse}. However, for large values of I_{krum}, the Preamplifier output shows some oscillations. All the simulations shown here used Q_{in} = 5.56 ke$^-$ (20 keV). **a)** $VOut_{Preamp}$ for different values of I_{krum}. The Periphery DAC can be programmed to provide I_{krum} from 0 nA to 51 nA. **b)** A subset of the curves from **a**. Note the ringing in $VOut_{Preamp}$ which occurs when I_{krum} = 20 nA or higher. **c)** The width of the Discriminator output pulse decreases for increasing I_{krum}. **d)** The Preamplifier output amplitude, and consequently also its gain, are affected by changes in I_{krum}.

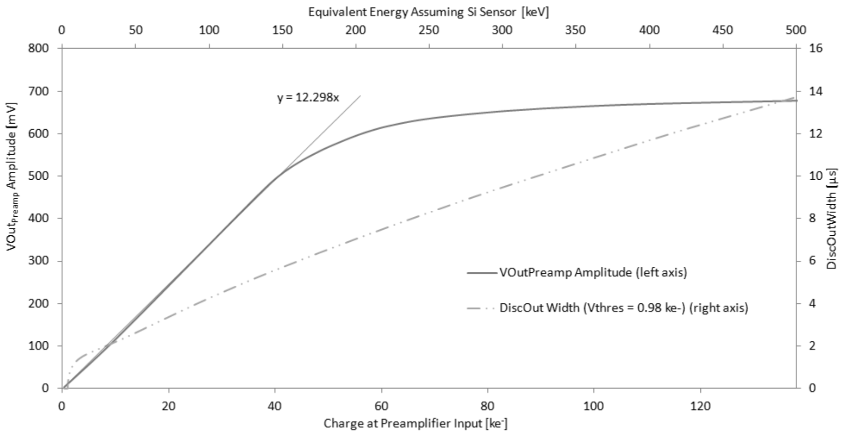


Figure B.4: Simulation of the frontend linear range

The slope of the linear region of the preamplifer output gives the gain: 12.3 mV/ke$^-$. The $VOut_{Preamp}$ amplitude begins to deviate from the linear line by more than 5% after 47.2 ke$^-$; this sets the upper limit of the programmable V_{thres} for photon counting. The width of DiscOut is plotted on the secondary axis for the same input charge range. This demonstrates that the time over threshold increases with Q_{in} even after the $VOut_{Preamp}$ amplitude has saturated. It should be noted that this is a simulation of a single pixel without taking into account any effects of capacitive coupling with adjacent pixels.

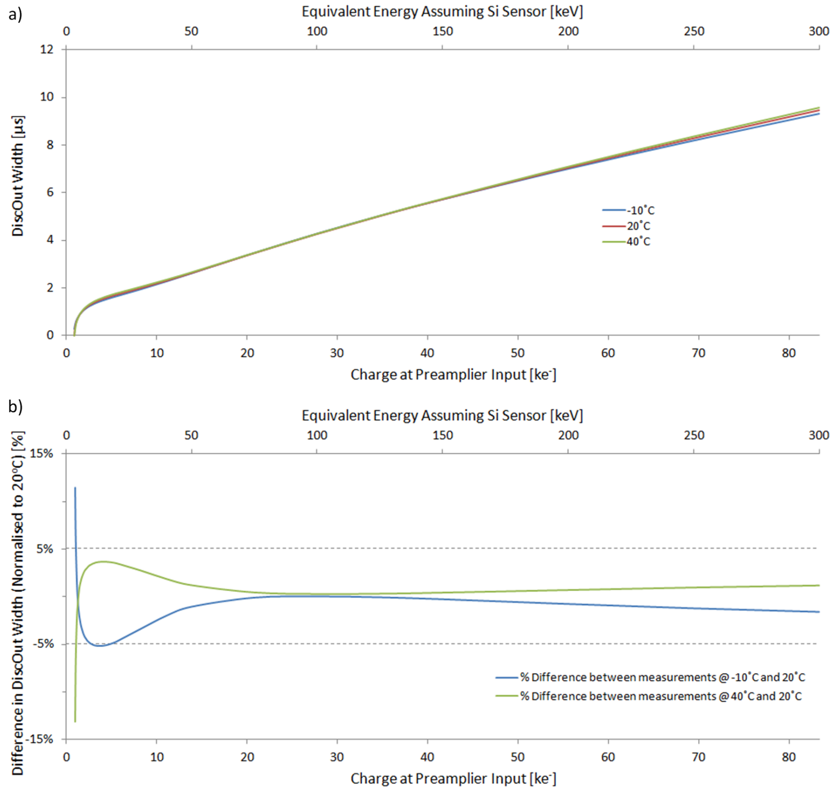


Figure B.5: Simulation of ToT sensitivity to temperature variations

a) Three simulations of ToT versus input charge under different temperature conditions. The temperature ranges simulated here are based on the required ambient temperature ranges for active personal dosimeters[84]. **b)** A comparison between the ToT values measured under the different temperature conditions, normalised to percentages with respect to the values measured at 20°C. For input charge quantities > 1.25 ke-, the Discriminator output pulse widths of a frontend operating at -10°C are within 9% of the pulse widths of the same frontend operating at 40°C.

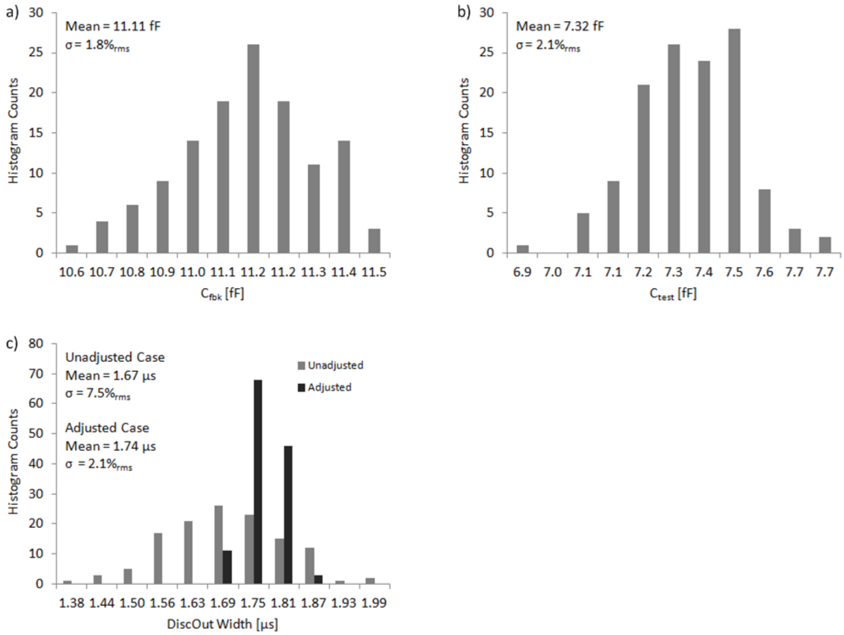


Figure B.6: Simulation of capacitance and gain variations

Monte Carlo mismatch simulation of capacitance and gain variations between different pixels of the same chip, run in Spectre MDL and using the Spectre netlist of the frontend schematic. Each run consists of a transient simulation with 6.14 ke$^-$ injected into the Preamplifier input. Data from 128 Monte Carlo runs are shown here. **a)** Variations in the feedback capacitance, C_{fbk}. **b)** Variations in the Analogue TestPulse capacitance, C_{test}. **c)** Variations in the time over threshold. The simulation is conducted twice. In the unadjusted case, the Threshold Adjustment code is fixed at 6'b100000. the adjusted case simulation, unique Threshold Adjustment codes for each pixel are determined by running a sucessive approximation search (in SpectreMDL, a measurement description language) prior to the transient simulation. It should be noted that this Threshold Adjustment scheme only works to correct for threshold offsets and does not correct for gain variations.

Acronyms

ADC: Analogue to Digital Convertor
ALARA: As Low As Reasonably Achievable (radiation protection guideline)
ALICE: A Large Ion Collider Experiment (LHC experiment)
APD: Active Personal Dosimeter
APS: (CMOS) Active Pixel Sensor
ASIC: Application-Specific Integrated Circuit
ATLAS: A Toroidal LHC ApparatuS (LHC experiment)
BGA: Ball Grid Array
CCG: Column Clock Gating
CERN: European Organization for Nuclear Research
CMOS: Complementary MOSFET
CMS: Compact Muon Solenoid (LHC experiment)
CRW: Continuous Read/Write (Medipix3 readout mode)
CSA: Charge Sensitive Preamplifier
DAC: Digital to Analogue Converter
DELPHI: DEtector with Lepton, Photon and Hadron Identification (experiment at CERN)
DFF: D-type Flip Flop
ENC: Equivalent Noise Charge
EoC: End of Column logic
HEP: High Energy Physics
IC: Integrated Circuit
ICRP: International Commission on Radiological Protection
ICRU: International Commission on Radiation Units and Measurements
ISO: International Standards Organization
ITRS: International Technology Roadmap for Semiconductors
kVp: kilovolt peak (X-ray tubes)
LET: Linear Energy Transfer
LFSR: Linear Feedback Shift Register
LHC: Large Hadron Collider
LHCb: LHC *b*-physics (LHC experiment)
LSB: Least Significant Bit
MDL: Measurement Description Language (Spectre)
MIMCAP: Metal Insulator Metal CAPacitor
MIP: Minimum Ionising Particle
MOSFET: Metal Oxide Semiconductor Field Effect Transistor
MSB: Most Significant Bit
MtM: More-than-Moore
MUX: Multiplexor
NMOS: n-type MOSFET
OTA: Operational Transconductance Amplifier
PCB: Printed Circuit Board
PCC: Photon Counting Chip (Medipix1)
PMOS: p-type MOSFET
PS: Proton Synchrotron
RICH: Ring Imaging CHerenkov detector
rms: Root Mean Squared
ROC: Readout Chip (of a hybrid pixel detector)
SEM: Scanning Electron Microscope
SI: Standard International (units of measurement)
SPI: Serial Peripheral Interface
SPS: Super Proton Synchrotron
SRW: Sequential Read/Write (Medipix3 readout mode)
ToA: Time of Arrival
ToT: Time over Threshold
USB: Universal Serial Bus
VHDL: VHSIC Hardware Description Language
VHSIC: Very High Speed Integrated Circuit
VNCAP: Vertical Natural CAPacitor
WA97: West Area 97 (experiment at CERN)

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