# Planarized Patterning of Y-Ba-Cu-O Thin Films for Multilayer Technology

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*Abstract* —**Planarized layers of $YBa_2Cu_3O_7$ (YBCO) were made by etching trenches in $SrTiO_3$ (STO) substrates, laser depositing a YBCO film and mechanically polishing the film down to the substrate surface. These structures exhibited critical temperatures ($T_c$) of 88 K and a critical current density ($J_c$) of $10^6$ A/cm$^2$ at 77 K. The planarized surface was smooth, with a maximum height difference between the YBCO and STO of 20 nm. The surfaces were used as templates for epitaxial growth of multilayer insulators of STO and $PrBa_2Cu_3O_7$ (PBCO) and top YBCO layers. Complete crossovers, free of superconducting shorts, with $T_c$ of 86 K and critical current density ($J_c$) of $2x10^5$ A/cm$^2$ were made.**

## I. Introduction

In the realization of high critical temperature ($T_c$) integrated circuits, e.g. integrated SQUID magnetometers, it is often necessary to be able to make multilayer superconducting circuits in a controlled way. The identified key elements in such circuits are crossovers (two crossing superconducting lines separated by an insulator) and vias (superconducting connections between two superconducting layers through an insulator). The making of such structures are discussed in a recent review article by the Berkeley group[1]. A key problem to solve, is how to avoid the high angle grain boundaries that can occur in the top superconducting layer. These grain boundaries severely reduce the critical current density ($J_c$) of the film and are due to the growth across the edges of the lower layer film structures. This is a problem which we have also noticed in our earlier work [2]. A way to solve this problem is of course to planarize the underlying layer. Here, we report results from a simple polishing process that both produces a planar bottom layer film and removes outgrowths and boulders from the film surface.

## II. Experiments

The multilayer patterns were defined with photolithography on $SrTiO_3$ (STO) substrates. The bottom $YBa_2Cu_3O_7$ (YBCO) layer was planarized before the insulator layer and top YBCO layer were deposited.

To planarize the bottom layer, we began by etching trenches in the bare STO substrates. To pattern the trenches, we used a photoresist (Microposit AZ 5214E) which was baked at 170°C. The high baking temperature caused the resist to float slightly and the edges of the resist pattern were rounded. The 400-600 nm deep trenches in the substrate were then made by ion milling at an incidence angle to the surface normal of 60°. The substrates were rotated during the ion milling and the incidence angle together with the rounded resist edges assured that the edges of the trenches in the STO substrate became smooth.

A 400-600 nm thick YBCO film was then deposited on the cleaned substrate in a standard laser deposition process [3]. In this case we used a substrate temperature of 835 °C and an oxygen pressure of 0.8 mbar. The samples were polished mechanically by hand with a 0.25 μm diamond spray (Strues) until YBCO only remained in the trenches. This surface was thoroughly cleaned and ion milled for 5 minutes at 60° incidence angle in order to remove a surface layer that was damaged from the polishing. This process resulted in a flat surface for the subsequent growth of the insulator layer, where the YBCO film was in level with the substrate.

For the insulator layer, we chose to use a multilayer of STO and $PrBa_2Cu_3O_7$ (PBCO). We have shown earlier [4] that the use of multilayer insulation layers gives better surface coverage than single layer insulators. The multilayer consisted of 5 STO layers with a thickness of 16 nm interspaced with 4 PBCO layers of 60 nm thickness. The layers were made with laser deposition. The deposition temperature was 745°C for STO and 835°C for PBCO. The oxygen pressure was 0.8 mbar in both cases. Window contacts were then opened in the insulator layer. The windows were patterned with photoresist (Microposit 1813) that was baked at 170° to get smooth edges. The openings in the insulator were made by ion milling (at 60° incidence angle) and the milling was done all the way down to the substrate, through the bottom YBCO layer, in order to expose the ab-planes of this layer. The resist was then removed in an oxygen plasma and the surface was ion milled for 5 minutes to assure that all resist residues and a possible damaged surface layer was removed.

The top YBCO layer was deposited at a lower substrate temperature (780°C) in order to minimize diffusion problems. The oxygen pressure was 0.4 mbar and a film thickness of 250 nm was used. The top layer was covered with an in-situ gold layer which was used for contacts to assure low resistances. The gold was also deposited with laser. There was no separate contacting step to get access to the bottom layer, it was connected from the top layer through window contacts. This assured that all connections to the YBCO had a low resistance. The top layer and the in situ gold contacts were patterned in two separate photo lithography steps with ion milling.

For a summary of the processing steps for the trilayer structures, see Fig. 1.

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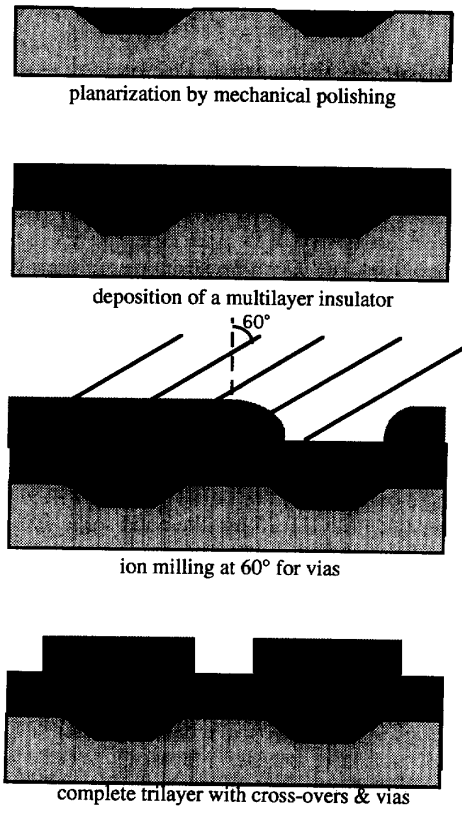


Fig. 1. Processing steps for the trilayer structures. All patterning was made with photo lithography. The trenches in the substrate before the polishing step were made by ion milling at an angle.

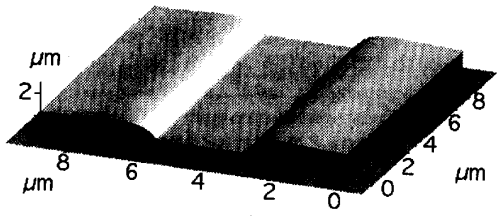


Fig. 2. AFM image of photo resist on a $SrTiO_3$ substrate. The resist has been baked for 30 minutes at 170°C in order to make the edges smooth.

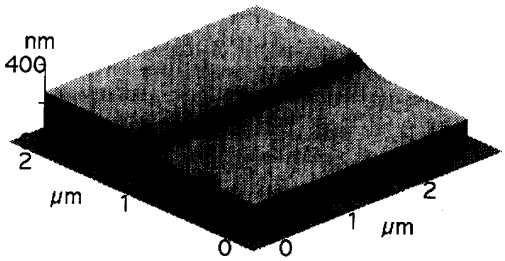


Fig. 3. AFM image of a trench edge on an ion milled $SrTiO_3$ substrate. The maximum angle of the slope is 35° to the surface.

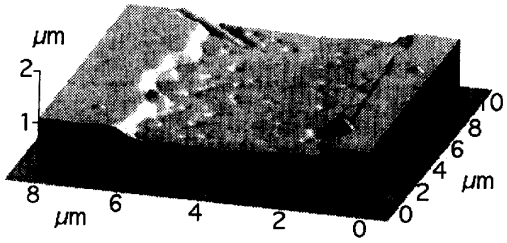


Fig. 4. AFM image of a trench in a substrate covered by a $YBa_2Cu_3O_7$ film. The pinholes in the film surface were more pronounced inside the trenches than in the film grown on the unetched substrate surface.

## III. Results

### A. Structure

The chips were examined by atomic force microscopy (AFM) after each processing step. They were also examined by transmission electron microscopy (TEM).

The profile of the photoresist was examined with AFM after the baking at high temperature. As can be seen in Fig. 2, the edges of the resist became rounded due to floating. The maximum edge angle was 45° to the substrate surface.

The pattern edges in the substrate after ion milling were rounded, and in this case the maximum slope angle was 35° (Fig. 3). This angle should be low enough to assure c-axis growth of the YBCO film across the edge of the trench, something which was proved in later TEM investigations. The ion milling induced a surface roughness. Small 'bumps' about 20 nm high and a few hundred nm wide appeared.

The laser deposited YBCO bottom layer grew c-axis oriented on all parts of the prepared substrate. In the trenches, the YBCO film had more pinholes than the other parts of the film (Fig. 4). The depth of the pinholes were of the order of 10 nm as seen by AFM. The reason for this surface roughness were probably the 'bumps' mentioned earlier.

The polishing of the surface removed most of the particles and pinholes from the YBCO film surface. This indicates that the pinholes did not go through all of the film, but were rather shallow and close to the surface. The height difference of the STO substrate and the YBCO film was less than 20 nm as measured by AFM after 30 minutes of polishing (Fig. 5). In some places on the chip, there were macroscopic scratches, easily seen in an optical microscope. The cause of this was probably that pieces of the substrate edge were broken off during the simple hand polishing procedure and scratched the film surface.

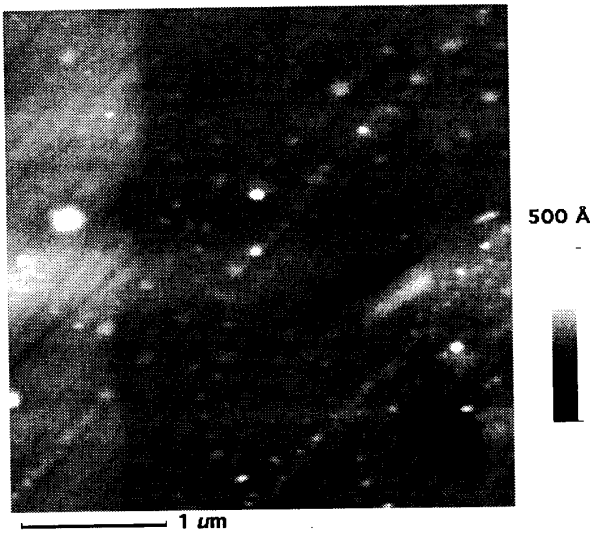


Fig. 5. AFM image of a polished sample. The vertical line in the left part of the picture is the border between STO (to the left) and YBCO. The surface of the sample after planarization is smooth. Outgrowths and pinholes that appeared during the deposition process are partially removed. Some extra polishing could remove them completely, but the number of scratches on the surface would increase. The gray scale (from black to white) indicates a height difference of 50 nm.

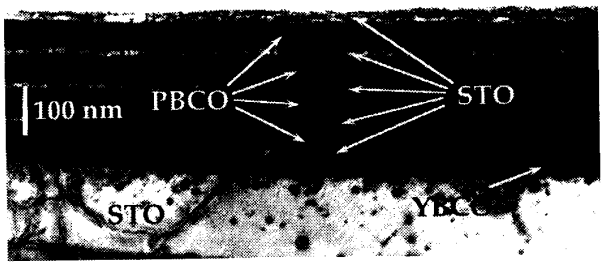


Fig. 6. TEM micrograph of an insulating multilayer grown on the planarized bottom layer. The insulator grows c-axis oriented on the planarized surface and forms a good base for c-axis growth of the $YBa_2Cu_3O_7$ top layer.

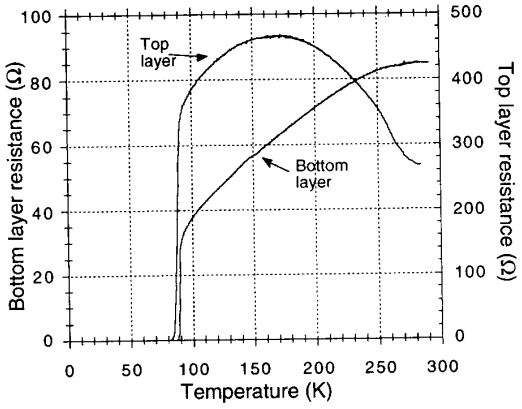


Fig. 7. Resistance of top and bottom layers of a crossover. The shape of the top-layer curve at high temperature is due to the parallel connection with the semiconducting $PrBa_2Cu_3O_7$ layer.

The insulator layer grew continuously across the planarized YBCO patterns. TEM investigations showed that the epitaxy was kept in the insulating layer, with a c-axis orientation at all places, also at the edge of the trenches (Fig. 6). The STO and PBCO layers grew parallel and horizontal and formed a good base for the top layer. In some places local defects, like particles on the planarized surface were observed in the TEM. This inhibited the ordered growth of the insulator layer locally.

The window contacts in the insulator were examined with AFM, and the slope angle was less than 20° to the surface. This low angle should ensures c-axis growth of the top layer film in the window areas [5], and TEM-studies are under way to examine this point.

The YBCO top layer grew c-axis oriented on the insulator without any disruptions.

*B. Electrical characterization*

The critical temperature of the bare polished bottom layer was measured with a four probe method. In this process, gold contacts for wire bonding were deposited on the YBCO film and annealed at 300 °C in oxygen. For the first chips, the bottom layer was destroyed in this process; The $T_c$ was reduced to below 70 K. It was found that a 5 minute ion milling of the YBCO surface was enough to preserve the film, and this process gave bottom layer patterns with a $T_c$ of 88 K and a 77 K $J_c$ of $10^6$ A/cm$^2$. Thus, there existed a contaminated surface layer on the bottom layer YBCO which was removed by the ion milling.

The bottom layer of the completed trilayer chip was also measured, and in this case the $T_c$ was up to 86.9 K with a $J_c$ of $\leq 2.5 \times 10^5$ A/cm$^2$ at 77 K. The bottom layer was thus slightly degraded by the subsequent processing steps. There were also large local variations in the quality of the bottom layer.

It should be mentioned that the bottom layers in the complete structure were measured through via-contacts from the top layer. The contact resistance were low, which indicates that the vias are of reasonable quality. However, we have so far not made any real four probe measurements on separate via connections.

The insulation between the top and bottom layer of a crossover was measured and a resistance of 310 Ω was found for a 200 μm$^2$ area at 77 K. There were no superconducting connections through the crossover. We believe that this relatively low resistance was caused by the low resistivity of PBCO, which formed most of the insulation layer. The parallel connection to the PBCO layer was also seen in the critical temperature measurements of layers in the crossover structures (Fig. 7.).

The YBCO top layer had a $T_c$ of up to 86.5 K and a 77 K $J_c$ of $\leq 7x10^5$ A/cm$^2$. This relatively high quality of the top layer confirms that the epitaxy is kept throughout the layers, from the bottom YBCO layer through the insulator up to the top YBCO layer. The top layer is thus also free of high angle grain boundaries.

## III. Conclusions

We have shown the possibility of using mechanical polishing to produce planarized superconducting structures without significant loss of the superconducting properties. The planarized layers served well as templates for epitaxial growth of an insulator layer and a top superconducting layer. Crossovers, free of high angle grain boundaries, were demonstrated. Our samples showed large local variations. The reason is probably our simple hand polishing method that in some cases produced large scratches in the patterns. A more refined polishing method would certainly give more reproducible results.

## References

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