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Behavioral Level Simulation Methods for Early Noise Coupling Quantification in Mixed-Signal Systems

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**In memory of my grandfather, who always inspired
me to learn new things.**

ABSTRACT

In this thesis, noise coupling simulation is introduced into the behavioral level. Methods and models for simulating on-chip noise coupling at a behavioral level in a design flow are presented and verified for accuracy and validity. Today, designs of electronic systems are becoming denser and more and more mixed-signal systems such as System-on-Chip (SoC) are being devised. This raises problems when the electronics components start to interfere with each other. Often, digital components disturb analog components, introducing noise into the system causing degradation of the performance or even introducing errors into the functionality of the system.

Today, these effects can only be simulated at a very late stage in the design process, causing large design iterations and increased costs if the designers are required to return and make alterations, which may have occurred at a very early stage in the process.

This is why the focus of this work is centered on extracting noise coupling simulation models that can be used at a very early design stage such as the behavioral level and then follow the design through the various design stages. To realize this, SystemC is selected as a platform and implementation example for the behavioral level models. SystemC supports design refinement, which means that when designs are being refined and are crossing the design levels, the noise coupling models can also be refined to suit the current design.

This new way of thinking in primarily mixed-signal designs is called Behavioral level Noise Coupling (BeNoC) simulation and shows great promise in enabling a reduction in the costs of design iterations due to component cross-talk and simplifies the work for mixed-signal system designers.

SAMMANDRAG

I denna avhandling introduceras brussimulering i mikrochip på en beteendenivå. Metoder och modeller för brussimulering i chip presenteras och verifieras för noggrannhet och funktionalitet på en beteendenivå i designflödet. I dagsläget blir elektroniska system tätare och tätare på chippen och fler och fler system görs med både analog och digital elektronik såsom System-on-Chip (SoC). Detta skapar problem när komponenter börjar störa varandra. Oftast är det digitala komponenter som stör de analoga, vilket introducerar brus i systemet som reducerar prestanda eller till och med inför fel i funktionen hos systemet.

Idag kan dessa effekter simuleras i ett mycket sent skede i designflödet, betyder att om fel upptäcks måste designern kanske gå tillbaka många steg i flödet. Detta kostar mycket tid och pengar.

Därför ligger fokus i detta arbete på att extrahera brussimuleringsmodeller som kan användas i ett tidigt skede såsom på beteendenivå och sedan följa designen genom senare skeden i designflödet. För att realisera detta har SystemC valts som en plattform och som ett implementationsexempel för beteendenivåmodellerna. SystemC har stöd för förfining av designer vilket betyder att ett system kan börja beskrivas på en hög nivå för att sedan förfinas för att nå lägre nivåer. Detta gör det möjligt för brusmodellerna att också förfinas i takt med systemdesignen.

Detta nya sätt att tänka på i designprocessen av i huvudsak analog/digital-integrerade system kallas Behavioral level Noise Coupling (BeNoC) simulering och bådär gott för att reducera kostnader för designiterationer på grund av brus mellan komponenter, och gör arbetet enklare för analog/digital- (mixed-signal) designers.

ACKNOWLEDGEMENTS

Ever since my childhood, I have wanted to become either a research scientist or a musician. Today, I do research in my work and play woodwinds in my spare time. A fair compromise since I think it would be quite a challenge to be a fulltime musician and do research in my spare time. There are many I would like to thank for the opportunities I have gotten and the support I have received.

I would like to start by thanking my supervisors Docent Mattias O’Nils, Docent Bengt Oelmann, Professor Hans-Erik Nilsson and Professor Trond Ytterdal for their tireless help, guidance and for the opportunity to fulfill an old boys dream in becoming a research scientist. To my colleagues at the Mid Sweden University Electronics Design Division I send thanks for their support but mostly for three years filled with laughs.

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Last but not least I would like to thank my parents, my brother and my grandparents who all had a hand in my upbringing, which has made me who I am today.

Sundsvall, February 2005

A handwritten signature in dark ink, appearing to read 'Jan Lundgren', with a stylized, flowing script.

Jan Lundgren

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ABBREVIATIONS AND ACRONYMS

GENERAL

CMOS.....	Complementary Metal Oxide Semiconductor
MOSFET.....	Metal Oxide Semiconductor Field Effect Transistor
NMOS.....	Negative-channel Metal Oxide Semiconductor
PMOS.....	Positive-channel Metal Oxide Semiconductor
SoC.....	System on Chip
VLSI.....	Very Large Scale Integration

RESEARCH GROUPS AND APPROACHES

BeNoC.....	Behavioral level Noise Coupling simulation, developed at Mid Sweden University.
IMEC.....	Interuniversity MicroElectronics Center, Belgium.
SPACE.....	Accurate layout-to-circuit extractor for deep submicron technologies, developed at Delft University of Technology.

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LIST OF PAPERS

This thesis base mainly upon the following four papers, herein referred to by their Roman numerals:

- Paper I **Behavioral Simulation of Power Line Noise Coupling in Mixed-Signal Systems using SystemC**
Jan Lundgren, Bengt Oelmann, Trond Ytterdal, Patrik Eriksson, Munir Abdalla and Mattias O'Nils,
Proceedings of the IEEE Computer Society Annual Symposium on VLSI, Tampa, Florida,
February 20-21, 2003.
- Paper II **A Power-line Noise Coupling Estimation Methodology for Architectural Exploration of Mixed-Signal Systems**
Jan Lundgren, Trond Ytterdal, Patrik Eriksson, Bengt Oelmann, Munir Abdalla and Mattias O'Nils,
Proceedings of the Southwest Symposium on Mixed-Signal Design, Las Vegas, Nevada,
February 23-25, 2003.
- Paper III **Taking Mixed-Signal Substrate Noise Coupling Simulation to the Behavioral level using SystemC**
Jan Lundgren, Trond Ytterdal, Kristian Vonbun and Mattias O'Nils,
Proceedings of the 4th IEEE International Workshop on System-on-Chip for Real-Time Applications, Banff, Alberta,
July 19-21, 2004.
- Paper IV **Noise Injection Models for Behavioral level Noise Coupling Simulations in SystemC**
Jan Lundgren, Trond Ytterdal and Mattias O'Nils,
Submitted for the 7th International Workshop on System Level Interconnect Prediction, San Francisco, California,
April 2-3, 2005.

Related paper not included in the thesis:

A SystemC Extension for Behavioral level Quantification of Noise Coupling in Mixed-Signal Systems
Mattias O'Nils, Jan Lundgren, Bengt Oelmann,
Proceedings of the 2003 International Symposium on Circuits and Systems (ISCAS'03), Pages:III-898 - III-901 vol.3, Bangkok, Thailand,
May 25-28, 2003.

1. INTRODUCTION

1.1 THESIS BACKGROUND

The development of mixed-signal systems and Systems on a Chip (SoC) has become more and more common, and the future for system design is believed to lie within the area of the integration of systems on a single chip. The advantages of this design methodology are obvious; the systems can be made smaller, the high-inductive bond wires between chips are removed and the overall cost of systems can be reduced. However, the integration of analog and digital systems on a single chip causes significant problems relating to noise coupling, which appear in switching currents that couple from digital logic to sensitive analog nodes [1]. The two largest coupling connections are those which occur through the substrate and over the power distribution network, but not necessarily in that order. There are recorded cases when the largest coupling source is the power distribution network, for example in a Bluetooth design [2]. Coupling over the power distribution network is often reduced by wiring separate power distribution networks to the analog and the digital components. This is however not always possible since this separation consumes a great deal of space on the chip and with a tight integration of small analog and digital blocks, a joined power distribution network may be required. Even if the power distribution network can be separated, the shared substrate still provides a coupling path, regardless how far apart the digital and analog blocks are located in the floorplan. The research in reducing substrate coupling has resulted in a variety of design solutions, including utilization of guard rings, chip trenches and via contact Faraday cages [3][4][5].

The problem at hand is to define how to simulate noise coupling throughout an entire design flow, since the only simulation tools available for noise coupling work at the layout level. The result of the noise coupling simulation at the layout level may show that the design is required to be returned to an architectural level, for instance, causing large iterations in the design flow and thus resulting in the consumption of both time and money. This problem is depicted in Figure 1. The solution would be the development of a noise coupling simulation tool, independent of design level, thus enabling designers to simulate noise coupling at any stage in the design flow. Simulation at an early stage can offer a great deal of information as regards to how the design should proceed through the design levels, hence reducing iterations in the design flow [6].

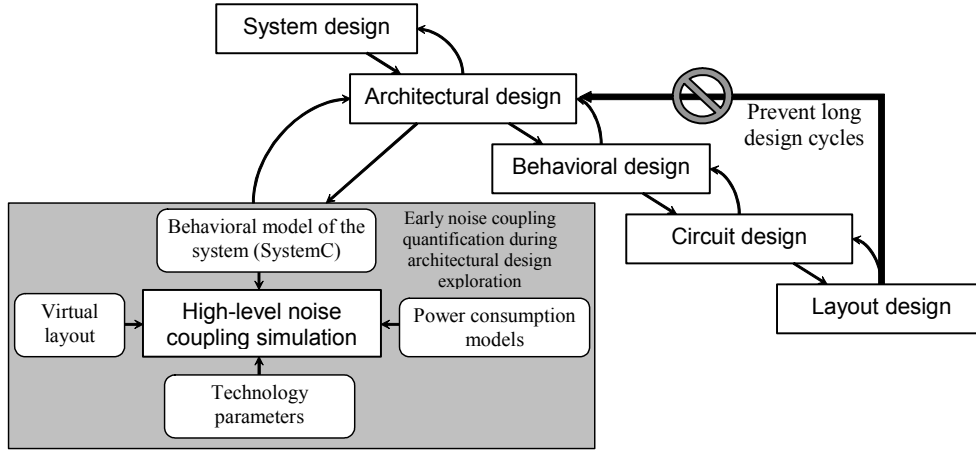


Figure 1. Example of modification to the design flow, where noise coupling simulation can be made at a behavioral level.

1.2 NEEDS AND CONSTRAINTS

The choice of simulation model is of course highly dependant on the needs and constraints of the application. For a highly optimized application, very low level noise coupling simulations may be required. However, modern design is pushing for faster and faster design flow, increasing the demands of good system level design simulators. Because of this, the choosing of a simulation model for behavioral/system level simulations becomes a delicate problem. To set fixed simulation models to different design levels would be one way of creating a standard for macromodels. However, when crossing between design levels in a design flow, a complete re-implementation of simulation models may have to be made. Another solution would be a more open and powerful simulation methodology, where a very high-level simulation model is implemented at an early stage in the design flow and is gradually refined while advancing through the design flow. This methodology requires that the model is implemented in a simulation tool that supports design refinement. It also places more power in the hands of the designer and thus increasing the demands made upon him/her.

1.3 THESIS OUTLINE

Section 2 presents previous research related to the modeling of power distribution networks and substrate, including modeling techniques, approximations, algorithms and implementations. Section 3 presents the Behavioral level Noise Coupling (BeNoC) simulation modeling technique, which is the main contribution of this thesis. Section 4 summarizes the work covered by all papers included in the thesis. Section 5 summarizes and concludes the contributions of the thesis. The papers presenting the original contributions to this thesis can be found in the appendix.

2 NOISE COUPLING MODELING FOR SIMULATION

This section is intended to give the reader a background insight into previous research in the field of noise coupling modeling.

2.1 POWER DISTRIBUTION NETWORK MODELING

The basic idea of a power distribution network coupling is described in Figure 2. A noise generating source module is connected to the power distribution network model. The noise current is transferred and thereby shaped by the network model, then fed into the receiving sink module which is, in turn, affected by the coupled current.

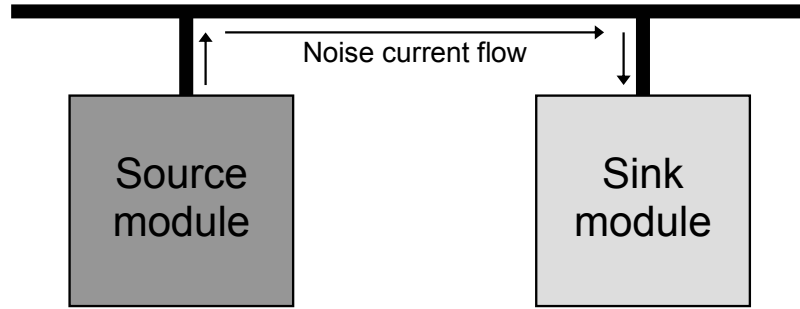


Figure 2. Basic idea of the power distribution network modeling technique. The noise current is coupled over the network model from a source module to a sink module.

The models of power distribution networks have changed significantly over the years. When the gate delay was dominant, the interconnections were modeled as short-circuits. However, when the interconnect capacitances became comparable to those of the gate capacitances, the interconnections were modeled as capacitances to ground $C_{line} = C \cdot l$, where C have approximate values of the distributed capacitances, as shown in Figure 3.

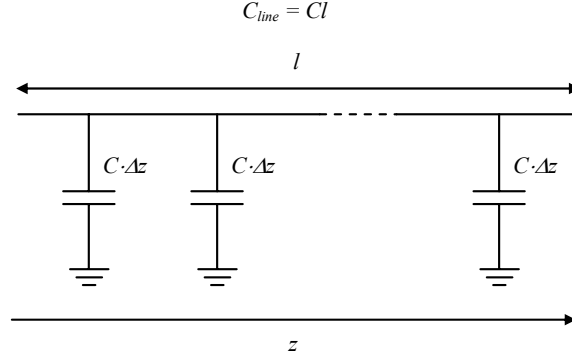


Figure 3. Early capacitance interconnect model.

The two more recent and currently dominant models are the RC and the RLC models [7], which will be discussed in greater detail in the next two sections. There are also considerations to be made about capacitances and inductances in and between power lines in a layout design [8][9], but this will only be handled briefly in this thesis.

2.1.1 RC interconnect model

With time, the resistance of interconnections became comparable to those of the open resistance for a transistor, and with this a new interconnect model had to be considered – the RC model. Since the resistances in the interconnections became significant, a resistance was added in series with the capacitance from Figure 3, forming the RC model shown in Figure 4, where R and C are approximations of the distributed values. This model is sufficient for clocked signal transition times $t_r > 2T_0$, where T_0 is the time of flight [10].

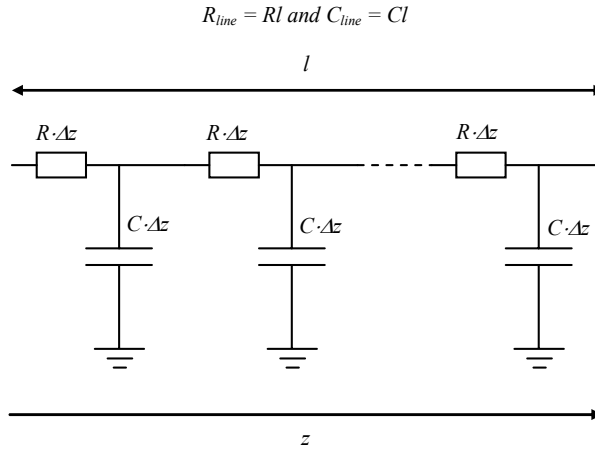


Figure 4. RC interconnect model.

2.1.2 RLC interconnect model

Even the RC model is now beginning to become obsolete for certain applications. There are factors that support the expansion of the RC model into an RLC model having an inductance in series with the RC link, as shown in Figure 5. These factors are:

- Transition times are much shorter
- Wider lines at higher metal layers
 - Decreases interconnect resistance
- Introduction of lower resistance materials for interconnect

$$\rho_{Copper} \cong \frac{1}{2} \rho_{Aluminum}$$

- Faster devices

$$R_{line} = Rl, L_{line} = Ll \text{ and } C_{line} = Cl$$

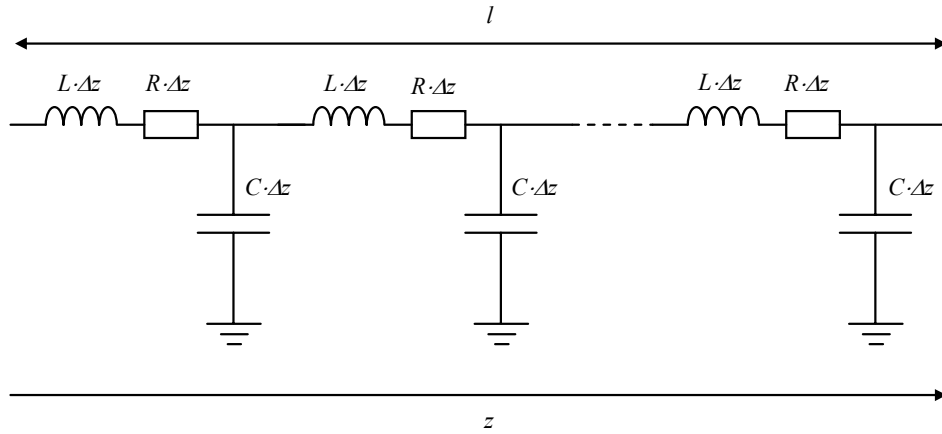


Figure 5. RLC interconnect model.

R , L and C are as in the earlier models approximations of the distributed vales.

2.1.3 Which model should be used?

For present applications, the RC model and the RLC model are those in use. So, what model should be used for a given application? According to Ismail et al. [10] the RC model is sufficiently accurate if one of the two following statements is satisfied:

$$\frac{R_{line} l}{2} \sqrt{\frac{C_{line}}{L_{line}}} > 1 \quad (1)$$

That is, the attenuation is sufficiently large to make reflections negligible. l is the length of the interconnection.

$$t_r > 2l\sqrt{L_{line}C_{line}} = 2T_0 \quad (2)$$

That is, the waveform transition time is slower than twice the time of flight. This results in a range of l for which the inductance in the RLC model is significant:

$$\frac{t_r}{2\sqrt{L_{line}C_{line}}} < l < \frac{2}{R_{line}}\sqrt{\frac{L_{line}}{C_{line}}} \quad (3)$$

Where t_r is the transition time. These conditions are also graphically displayed in Figure 6 [10].

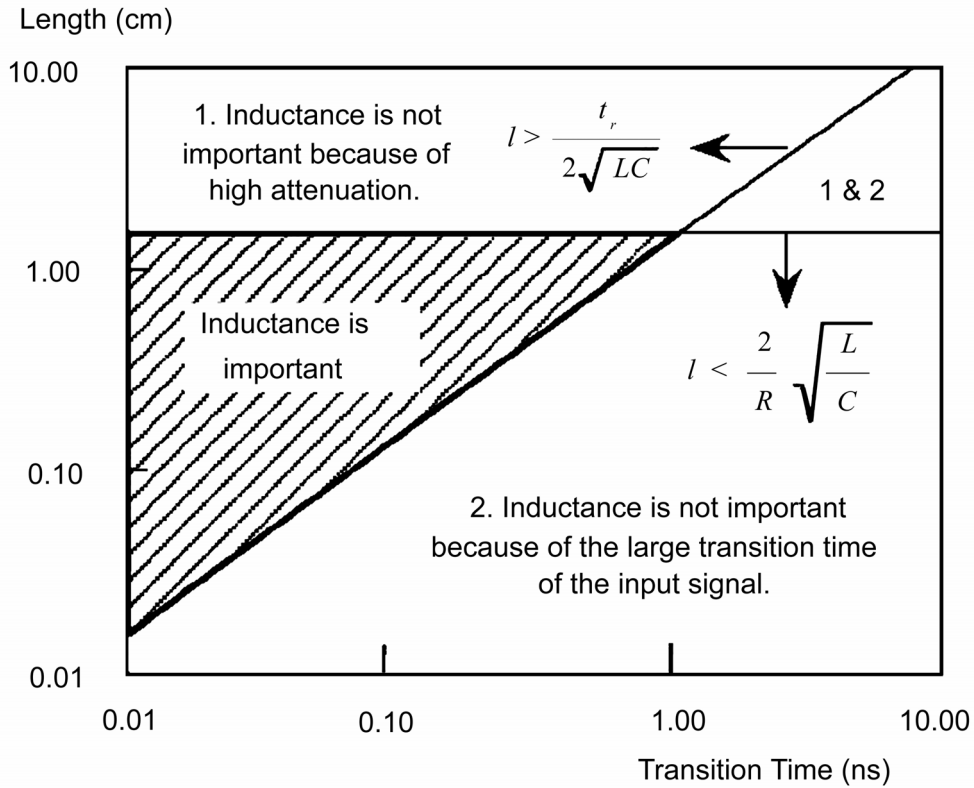


Figure 6. Transition time t_r versus the length of the interconnect line l . The crosshatched area denotes the region where inductance is important.

2.1.4 Modeling bond wires and leadframe pins

Apart from on-chip wires, there are other parts of the power distribution network that need to be included in the simulation models. Figure 7 shows a packaged chip in profile, where gold bond wires and copper leadframe wires are connected to the on-chip bond pads. These all have to be carefully modeled to make accurate power distribution network simulations.

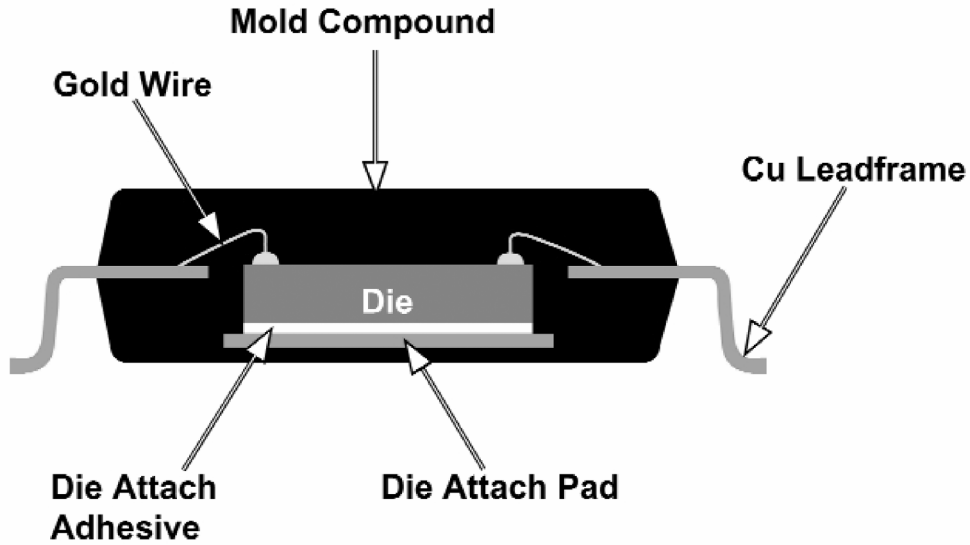


Figure 7. Profile cross section of a Thin Shrink Small Outline Package (TSSOP) where the bond wires and leadframes are shown. Courtesy of Amkor Technology.

Bond wires and leadframe pins are both very low resistive and very high inductive in comparison to on-chip wires and thus are usually modeled as inductors [1], as shown in Figure 8.

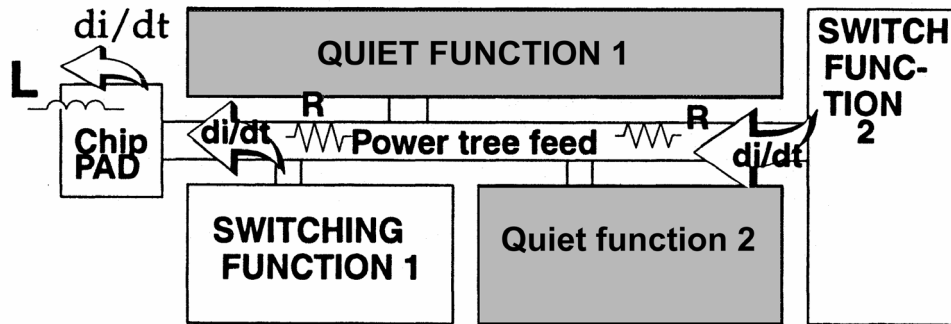


Figure 8. Tree power distribution network design example. The pad, bond wire and leadframe are modeled as one resulting inductance.

To offer a motivation for this inductive model, the calculated examples of self inductance and mutual inductance – inductive coupling between wires – in Table 1 can be perused, which clearly show the inductive dominance in bond wires and leadframes over chip wires [11]. They also shows that self inductive bounce voltage amplitudes become quite large even at moderate currents, and that these amplitudes are considerably larger in bond wires and leadframes than in on-chip wires, because of the larger parasitic inductances. This shows that the reduced number of pins in SoC systems is a great improvement over the older systems.

Table 1. Inductive coupling from chip wires, bond wires and 68 pin PLCC package leads.

Conditions:	self inductance (nano henry (nh))	mutual-L (nano henry (nh))	mutual-L coupling from 10mA rms @ 50MHz	mutual-L coupling from 100mA rms @ 50MHz	self-L bounce from 100mA rms @ 50MHz
1mm long chip wire. 3u width and spaced 1u above a ground plane	0.42	.037	0.16mV	1.6mV	18.6mV
Wirebond wire only, corner bond	3.0	1.4	6.2mV	62mV	133mV
Wirebond wire only, center bond	2.24				99.5mV
Leadframe wire only, corner lead	11.0	4.2	18.7mV	187mV	489mV
Leadframe wire only, center lead	7.9				351mV
Total corner lead and no nearby grounded pin	14	5.6	24.9mV	249mV	622mV
Total corner lead with every other package lead grounded	5.0				222mV

2.2 SUBSTRATE MODELING

In substrate modeling, some work has been undertaken within a few abstraction levels, but not at the behavioral level. There exist different models spanning from resistive network models with one common ground node, all the way down to device simulation models. The different physical issues causing noise coupling will be characterized first and then several different macromodels that have been developed for substrate modeling on circuit and layout levels will be investigated.

2.2.1 Physical properties causing noise coupling

The first and most obvious physical property is the resistivity of the substrate which can be modeled as resistors in a substrate mesh cell (see Figure 9a). This is a simple and fast substrate model to simulate since DC analysis can be used. A more complex and accurate model is the one shown in Figure 9b, which includes capacitors in the substrate mesh cell [12]. There are several places where the capacitors become more vital, for example between gate and substrate, and between wells and surrounding substrate. This makes it possible to reduce the number of capacitors by only including those that are more vital [13][14].

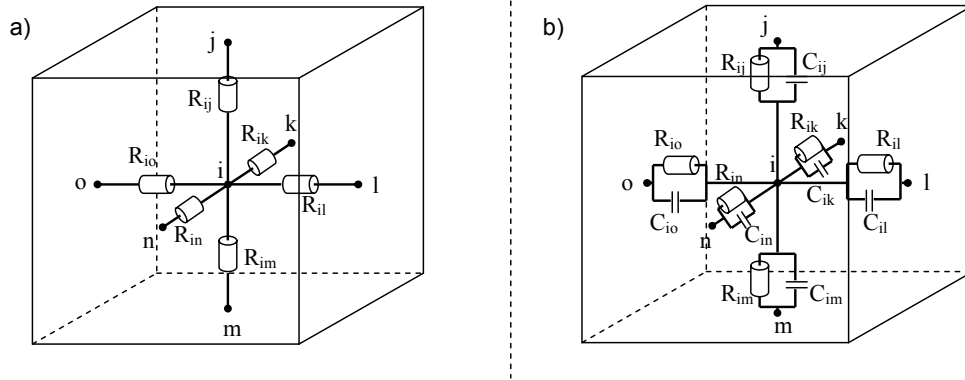


Figure 9. Comparison between a) resistive substrate mesh cell model and b) resistive/capacitive substrate mesh cell model.

2.2.2 Substrate macromodels

2.2.2.1 Asymptotic Waveform Evaluation (AWE) macromodel

The AWE macromodel is based on a nodal analysis approach, solving the equation:

$$\sum_j \left[R_{ij} (\Psi_i - \Psi_j) + C_{ij} \left(\frac{\partial \Psi_i}{\partial t} - \frac{\partial \Psi_j}{\partial t} \right) \right] = 0 \quad (4)$$

Where Ψ_i and Ψ_j are the potentials in the nodes i and j from Figure 9b [15]. The substrate macromodel is computed as an $n \times n$ admittance matrix:

$$\begin{bmatrix} y_{11}(s) & \dots & y_{1n}(s) \\ \dots & \dots & \dots \\ y_{n1}(s) & \dots & y_{nn}(s) \end{bmatrix} \begin{bmatrix} v_1(s) \\ \dots \\ v_n(s) \end{bmatrix} = \begin{bmatrix} i_1(s) \\ \dots \\ i_n(s) \end{bmatrix} \quad (5)$$

where n represents the number of ports [16]. However, to simulate substrate coupling in a given circuit, a combination of the AWE macromodel and the nonlinear circuit are required, i.e. a new matrix needs to be formed for every time point in the simulation (transient simulation). As a consequence, the simulation becomes a complex task, but with present day modern matrix solvers the simulation time takes a fraction of the time taken in device simulation.

2.2.2.2 DC macromodel

In heavily doped bulk processes, Verghese et al. show in [1] that the relaxation time of the substrate, $\tau = \rho' \epsilon$, where ρ' is a constant resistivity used to describe carrier flow in the substrate and ϵ is the permittivity of the substrate, is of the order of 10^{-11} s. This means that the intrinsic capacitances can be neglected for operating frequencies up to a few GHz and switching times of the order of 0.1 ns. This then enables the substrate to be modeled as a purely resistive mesh, provided that the well capacitances, field oxide capacitances and die attach capacitances are modeled as lumped circuit elements. What is then obtained is a purely resistive macromodel that is able to simulate in DC mode, cutting simulation times down by an order of ten from the AWE macromodel, see Table 2. The DC macromodel uses mesh cells such as that shown in Figure 9a. The simulation results, presented by Verghese et al., from the AWE and DC macromodels are indistinguishable and have a maximum error of roughly 20% from device simulations, with only approximate values of bonding pad and chip-to-package capacitances [17]. This kind of resistive mesh has also been used by Panda et al. in [18].

Table 2. Run-time comparison between the device simulation program and the macromodeling techniques.

Number of mesh nodes	Device Simulation cpu time (s)	AWE Macromodel cpu time (s)	DC Macromodel cpu time (s)
2940	4375	60.6	5.5
3716	7192.8	92.3	7.2
6605	15882.2	202.2	20.3
8712	23732.2	294.3	28.3

2.2.2.3 Modified single node substrate model

In heavily-doped bulk and lightly-doped epitaxial layer processes the substrate model can be further simplified. A single node can be used for the bulk substrate connected to surface nodes as for example in Figure 10 [19].

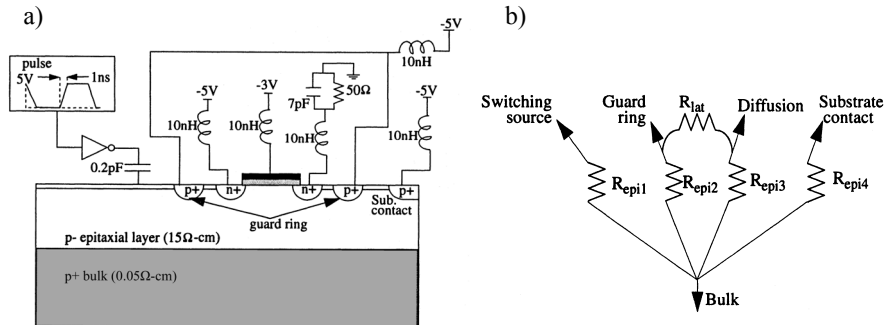


Figure 10. b) Single node model of the substrate in a).

The epitaxial resistances can be calculated as a parallel combination of component area resistance R_{AREA} and the perimeter resistance R_{PER} due to current flow:

$$R_{AREA} = \frac{\rho T}{A} \quad (6)$$

$$R_{PER} = \frac{\rho}{P} \quad (7)$$

Where ρ is the resistivity of the epi-layer, T is the effective thickness of the epi-layer, A is the active surface area and P is the perimeter of the active area. The resulting formula for the epitaxial resistances is:

$$R_{EPI} = \left(\frac{k_1 \rho T}{(L + \delta) \cdot (W + \delta)} \right) \parallel \left(\frac{k_2 \rho}{2(W + L + 2\delta)} \right) \quad (8)$$

where W and L are the width and length of the active surface area. k_1 , k_2 and δ are fitting parameters extracted from empirically measured resistances. According to Su et.al. the values $k_1 = 0.96$, $k_2 = 0.71$ and $\delta = 5.0\mu\text{m}$ would yield simulation results within 15% of measured results [14].

The model in Figure 10b has a modification from the original single node model. If the distance between two nodes is smaller than approximately four times that of the epi-layer thickness, the lateral resistance between transistors/contacts/wells becomes significant, so the lateral resistance R_{lat} is added to increase the accuracy of the single node model and is given by:

$$R_{lat} = \frac{1}{y_{g-d}} \quad (9)$$

where y_{g-d} is the conductance between the guard ring and the diffusion area in Figure 10a [1].

This substrate model has also been used on IMEC by van Heijningen et al. in [20].

2.2.2.4 Circuit level single node substrate model

A compromise of the DC macromodel and the modified single node model becomes what could be called the circuit level single node substrate model. This model has a resistance from every surface node to the single substrate node and lateral resistances between surface nodes [21]. This would result in long simulation times if lateral resistors were placed between all nodes and in order to reduce the number of resistors between surface nodes, it has been documented to use triangulation techniques to draw the resistive mesh in the lateral plane [22]. One suitable technique is a modified version of the Delaunay triangulation technique which basically starts by inserting an edge (resistance) on the shortest distance between two vertices (nodes) and continues by inserting the second shortest edge, with the premise that it does not cross any of the previous edges, etc. [23]. A small example of this technique is shown in Figure 11 where the resistance R_{a-c} is not inserted because it would cross R_{b-d} . In this simple case only one resistance is saved

for the simulation, but in the case of 900 nodes in a 30x30 mesh the total number of resistances (lateral + vertical) would reduce from $404550 + 900$ to $2700 + 900$.

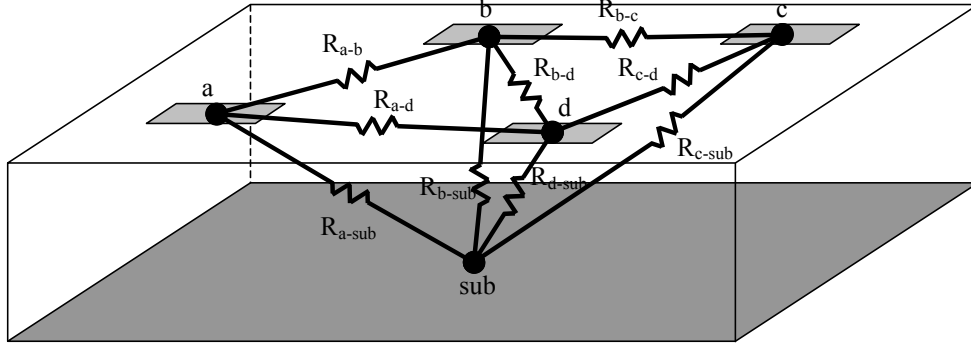


Figure 11. Circuit level single node model example where the resistance R_{a-c} has been eliminated by the modified Delaunay triangulation technique.

Trials have also been performed where capacitances have been incorporated into this model and where capacitances have been placed when well crossings occur [13]. This of course takes the simulation to a lower level and increases the simulation times.

2.2.3 Substrate noise injection modeling

There has been a great deal of previous work, performed over many years, involving the extraction of viable substrate noise injection mechanisms at both layout and circuit level. There are several injection mechanisms in substrate noise coupling that have been found and require to be considered:

Firstly there is *impact ionization*, which basically yields a current flowing out of the bulk node of the transistor and into the substrate. This current is generated by fractions of carriers in the depleted region of a saturated transistor gaining enough energy to become “hot” [24]. They then scatter and create additional electron-hole pairs. The holes generated in the NMOS transistor are then swept to the substrate, forming the current into the substrate. Impact ionization is mostly measured on the bulk node of the NMOS transistor, since the current out of the PMOS bulk node is at least one order of magnitude lower than that of the NMOS [25].

Capacitive coupling to the substrate is caused by voltage fluctuations in the source and drain of the MOS transistor which are coupled through the junction capacitances. There is also a capacitive coupling over the gate oxide via channel capacitances. Together these form a current injected into the substrate [26].

Gate induced drain leakage (GIDL) occurs when there are high fields across the gate-drain overlap region. These form a deep-depletion layer in the drain and when the voltage drop across this layer is sufficient, the valence electrons start to tunnel between bands, resulting in the creation of holes, which are swept into the substrate [27].

The hot electrons that are not subjected to impact ionization are likely to release their excess energy by emitting a photon [28]. Electron-hole pairs can then be created when the photons are reabsorbed, causing a *photon induced current (PIC)* [29].

In addition to the capacitive coupling there will also be a *diode leakage current* in the junctions of the MOSFET's source and drain, which are in actuality reverse biased diodes [26]. This current is then injected into the substrate.

From these five substrate injection mechanisms, it has been shown that the substrate currents caused by capacitive coupling and impact ionization are the dominant ones, in that order, and that capacitive coupling becomes relatively more important at high frequencies [25].

Finally, from the power distribution network, there can also be power supply noise (i.e. power bounce) and ground noise (i.e. ground bounce) directly injected into the substrate via substrate contacts. Such a noise injection mechanism has the same amplitude or even more than the capacitive-coupled injection. The problem is usually tackled with well-designed power and ground networks as well as appropriately allocated substrate contacts [1].

3 THE BENOC SIMULATION MODEL

The initial idea for the BeNoC project was to allow designers to achieve a better feel as to where problems involving noise coupling might occur at a very early stage in the design flow. As coupling problems appear to increase as new technologies and smaller devices are introduced, it will be essential to consider coupling problems when designing mixed-signal electronics, and, on occasions, even strictly digital or analog. The contribution of this project and this thesis is therefore the introduction of the simulation methods and models called BeNoC that can be used to quantify noise coupling problems in behavioral level design.

This section considers a design example using a photon counting pixel detector as a way of quantifying the problems that can be solved using the BeNoC simulation model. The model is then described in detail, including all the work involved in its development.

3.1 DEFINITION OF REQUIREMENTS

3.1.1 Design example

Sub-micron technology has enabled X-ray imaging with image sensors composed of photon-counting pixels to evolve [30]. In these image sensors, each pixel is implemented as a single channel radiation detector, which means that each detected X-ray photon in the pixel is counted. The number of counts will represent the pixel value. A count is processed such that when a photon hits the detector, the photon energy is converted into a charge pulse, i_{in} , which is integrated by the pre-amplifier, forming V_{charge} in (1) in Figure 12. This is then pulse-shaped in (2), i.e. first high-passed filtered and then low-passed filtered. The output is a semi Gaussian shaped pulse, V_{RC} in Figure 12, where the height represents the photon energy. The pulse is counted if the energy is between the two threshold levels in the window discriminator (3), i.e. implemented with two comparators. If V_{RC} does not reach the threshold th_1 and then drops below th_2 the clock generator in (4) becomes high and then low when V_{RC} exceeds th_2 on the next pulse. If th_1 is surpassed, no high transition is generated. This means that a high transition is generated by the clock generator when the photon pulse is within a certain wavelength spectra. For multiple wavelength spectra detection, one discriminator, one clock generator and one event counter are required to be designed for a particular spectra and then connected in parallel with the others. The 16-bit event counter in (5) counts the number of high transitions from the clock generator, producing a digital 16-bit value of the number of photons (i.e. luminance) that are within a particular wavelength spectra. This enables X-ray color imaging since the luminance is known for each of the wavelength (color) spectra. A significant advantage of such a photon counting image detector is that the image is directly

captured in digital form and thus no analog to digital conversion is needed during readout.

Pixel detector

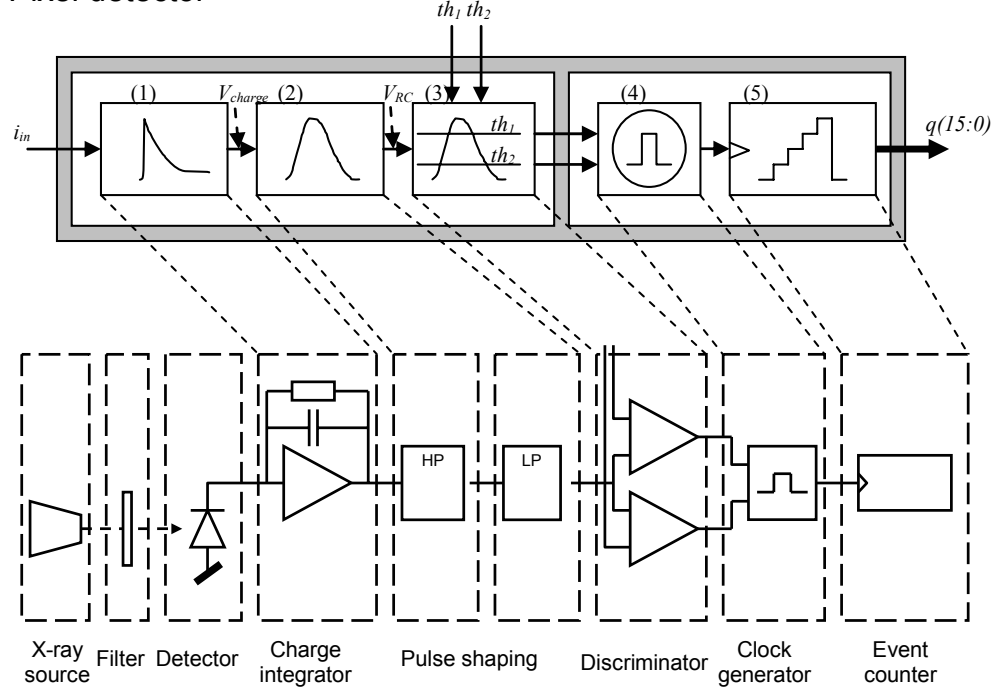


Figure 12. Behavioral mixed-signal model of the photon-counting pixel detector.

3.1.2 Design questions arising

At the initiation of the design process of the photon counting pixel detector there are many unknowns. The design of the detector surface will most likely be a mesh structure, which means that the readout electronics from the charge integrator to the event counter will lie under the detector pixels in a mesh structure. Each pixel is comprised of three to five hundred transistors, which raises the first question also discussed in [31]. Will there be a problem with tight integration of sensitive analog circuits and digital logic? In that case, should the design measure for the reduction of the noise coupling, and, if so, between what components? Since the components are so tightly integrated on a small surface, maybe the design cannot have separate power distribution networks for analog and digital components. Is this even a possibility or will the noise disrupt components in a joined power distribution network?

Many unanswerable questions exist until the design layout is ready or perhaps even until the chip is actually constructed, which means long iteration cycles and huge costs in redesign. The method here is an attempt to solve the

quantification of noise coupling problems at an early stage in a design flow and is the point where the BeNoC simulation model is of benefit.

3.2 BENOC – HOW DOES IT WORK?

This section handles the functionality of the BeNoC simulation model, starting with the proposed design flow and the overall system modeling. The models for simulating power distribution networks and substrate are described and the models for noise injection into the substrate are also discussed. Finally, a description of the proposed simulation application is provided.

3.2.1 Proposed design flow

The proposed noise coupling model is an addition to the architectural exploration stage of a top-down design flow for mixed-signal systems, as depicted in Figure 13. The noise coupling simulation starts from a behavioral model, which is extended by applying the noise coupling simulation wrapper to the behavioral model. The simulation wrappers add technology parameters, power consumption and interconnect to all functional blocks in the system.

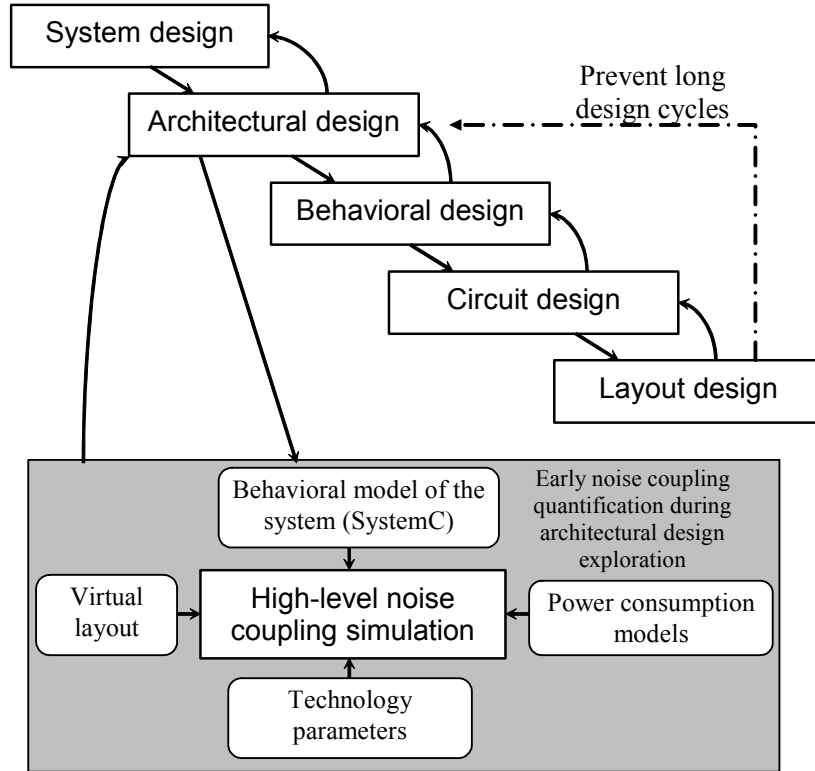


Figure 13. Proposed addition to a top-down based design flow for mixed-signal systems.

3.2.2 System modeling

The model for power distribution and substrate noise coupling is devised as an add-on wrapper that encapsulates a component module. This enables the designer to simulate noise coupling for any given module. The wrapper adds ports and a current flow in and out of both the power distribution network and substrate, which is illustrated in Figure 14 and further described in [32].

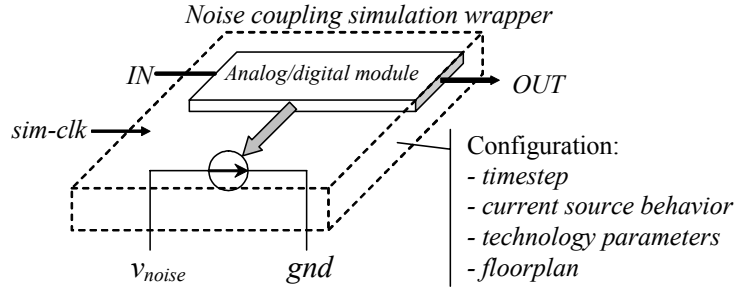


Figure 14. Wrapper model for the noise coupling simulation.

The substrate current flow consists of an injected current into the substrate that can either come from a noise injection module or recorded current values from a data file. An output current is then calculated and sent out from the wrapper. Each chosen component receives its own wrapper and all are seen as nodes in the following simulation. The application then builds up an appropriate resistive network for the substrate and an appropriate network of power lines, depending on the given technology parameters. Figure 15 depicts the proposed simulation flow.

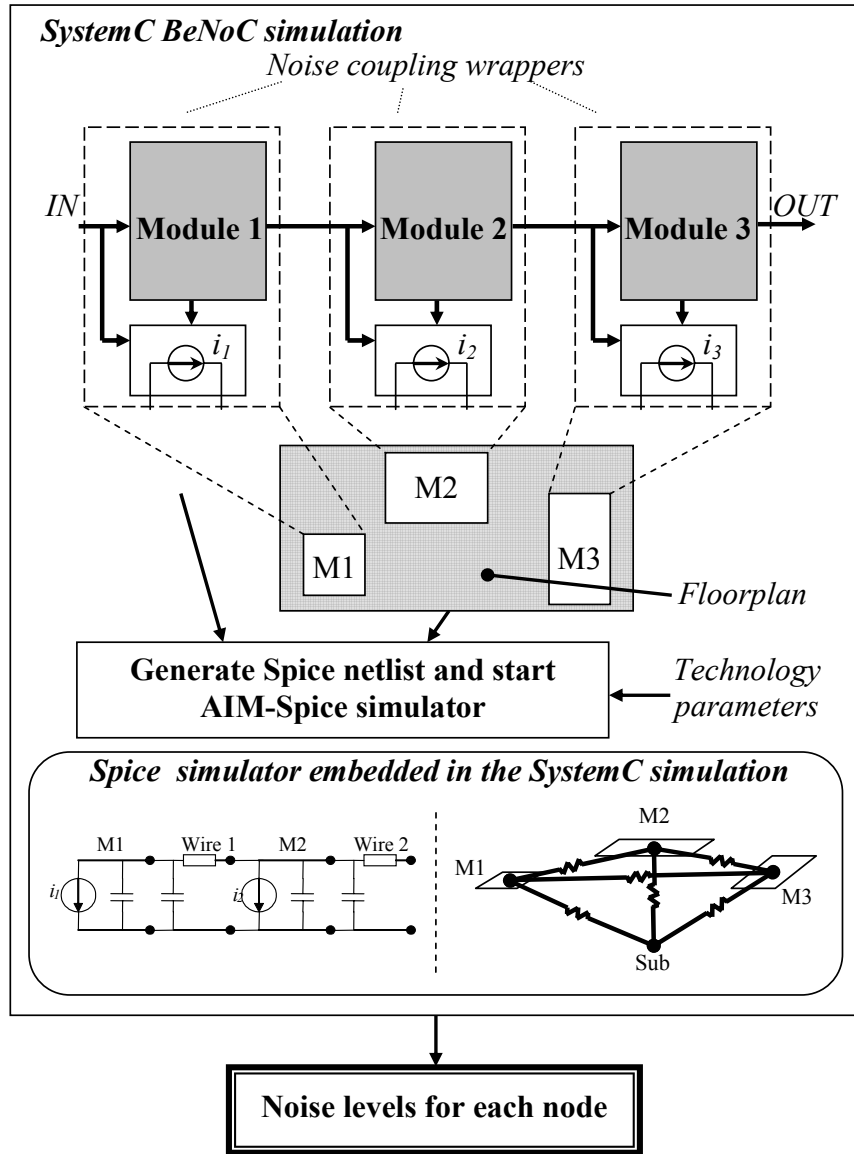


Figure 15. Simulation flow. The modules of interest are given wrappers which take the given floorplan and technology parameters, and generates an appropriate mesh that is simulated.

The modules that are interesting for noise coupling simulation are localized and simulation wrappers are added to these modules. Since wrappers can be added to both analog and digital blocks, the user is free to simulate, for example, digital noise impact on digital blocks, analog noise impact on analog blocks and digital noise impact on analog blocks. The simulation models are thus independent of the nature of the circuits, enabling noise coupling simulations in digital and analog circuits as well as in mixed-signal circuits.

3.2.3 Power distribution network modeling

The model for the power supply current in a functional block is implemented as a wrapper that adds simulation ports – simulation clock, power supply and ground. In addition, the wrapper adds a current source for the power supply. The wrapper in Figure 16 has, as an example, been placed around a 16-bit counter.

The actual implementation of the wrapper in SystemC is made as macro definitions that are called in the code of each block. The interface is added by including NC_SIM_PORTS in the code of the block, as illustrated by the counter example in Figure 16. The user configures the wrapper by defining the update period, i.e. timestep, of the simulation clock, *sim-clk*. The triggering condition of the current source is defined by adding NC_CURRENT_SOURCE in the constructor of the block with a standard SystemC sensitivity list, as shown in Figure 16. The behavior of the current source is entered as a SystemC process, which is written as a C++ method.

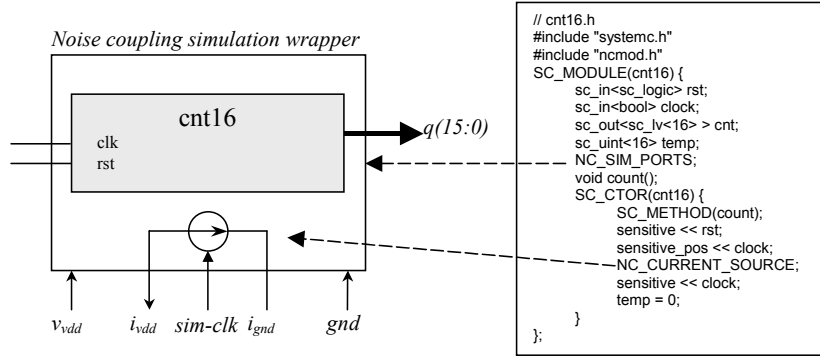


Figure 16. Noise coupling simulation wrapper.

As discussed in Section 2.1, in CMOS, long interconnects can be seen as distributed RC lines and can be accurately modeled by cascaded discrete RC-stages [8] with a particular serial resistance and a capacitance to ground. The electrical model for the wire is shown in Figure 17 and describes the a) RC-based model for wires and b) the interfaces for the system SystemC model, where i_m represents the power supply current for a functional block as described earlier and C_{comp} represents the component capacitance toward the substrate.

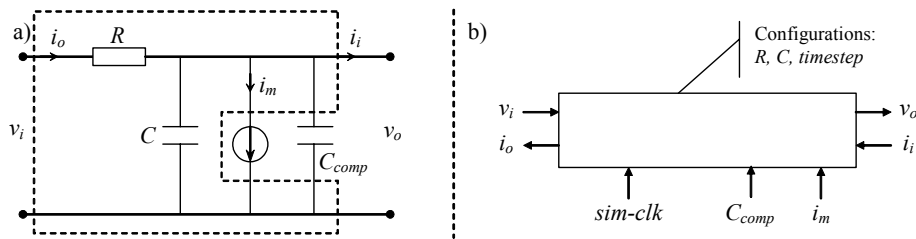


Figure 17. a) RC-based model for wires and b) the interfaces for the system SystemC model.

3.2.4 Substrate modeling

The substrate model used is a 3D single substrate node model [23]. It combines a two-contact single node configuration [33] with a lateral triangulation technique, which is a modified Delaunay triangulation [22]. In practice, every node is given one resistance toward the bulk node and resistances are also placed between nodes using a “shortest path” technique. This means that the shortest path between two nodes is given a resistance, and if the next investigated path crosses a resistance path already in existence, no resistance is placed on this new path. A modification was added to the triangulation technique to increase the accuracy of the noise coupling simulations. If four nodes are placed in a square mesh structure, i.e. with diagonals of the same length, the model sets resistances on both diagonals. An example of this modeling technique is depicted in Figure 18, where four nodes are placed on a low-doped epi, high doped bulk substrate. Notice that no resistance is placed between a and c because it would cross the shorter path between b and d.

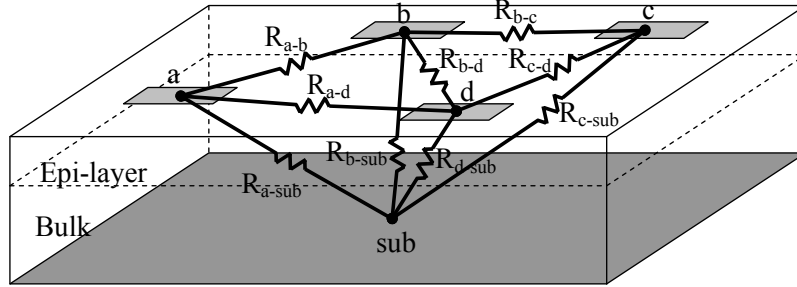


Figure 18. Example of a resistance net ready for simulation when using the 3D single substrate node model.

3.2.4.1 Verification of substrate model

Device simulations have been performed to verify the results obtained with BeNoC. In this section, the device simulations and the results are described.

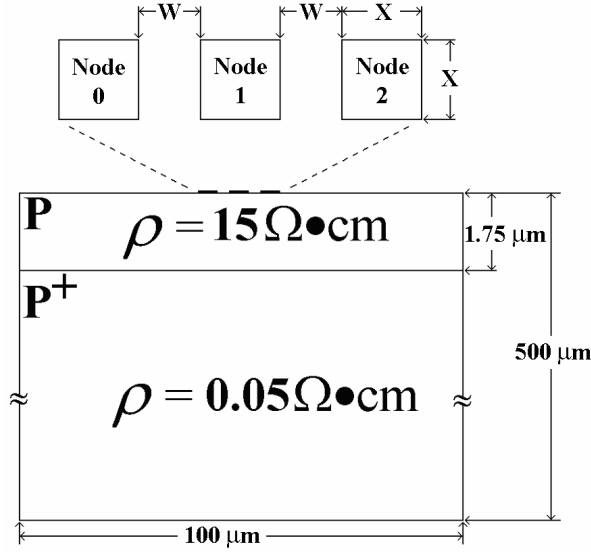


Figure 19. Substrate structure of the triple-node verification test case.

The substrate used here was heavily doped with a lightly doped epi-layer. This is usual for modern state-of-the-art CMOS technologies. The BeNoC simulation results of the SPACE generated resistor mesh representing the substrate were compared with the results using the ATLAS device simulator from Silvaco on a structure consisting of three substrate contacts (see Figure 19). Three square contacts were placed on the epi-layer surface. The simulations included injecting current into one contact and measuring the voltages on the other two. The resistance netlist of the same structure shown in Figure 19 was extracted by means of the SPACE resistance extractor. Then the resistance netlist was used in BeNoC and the same DC current sweep was implemented. The simulations were repeated for four different contact spacings. Both the results from the ATLAS simulator and the BeNoC simulator were evaluated.

The triple-node verification test case from Figure 19 was simulated in the BeNoC simulator, where each of the three nodes was encapsulated in a noise coupling wrapper. A current sweep was then injected into node 0 and the voltages from nodes 1 and 2 were plotted. This verified the functionality of the model and that the SystemC-to-AIM-Spice connection was functioning correctly. The computational simulation time for this verification test case was under one second, which matches simulation times of behavioral mixed-signal modules in SystemC [34].

The accuracy of the BeNoC model was tested against the Atlas device simulation of the same structure using the same injection current. The size variables from Figure 19 were set to $W=2\mu\text{m}$ and $X=1\mu\text{m}$. The node width W was set to reflect a modern mixed-signal design process and the node distance X was set to a small enough distance to make the direct surface coupling relevant to the

result so that part of the model is verified along with the substrate node coupling. The results are shown in Figure 20.

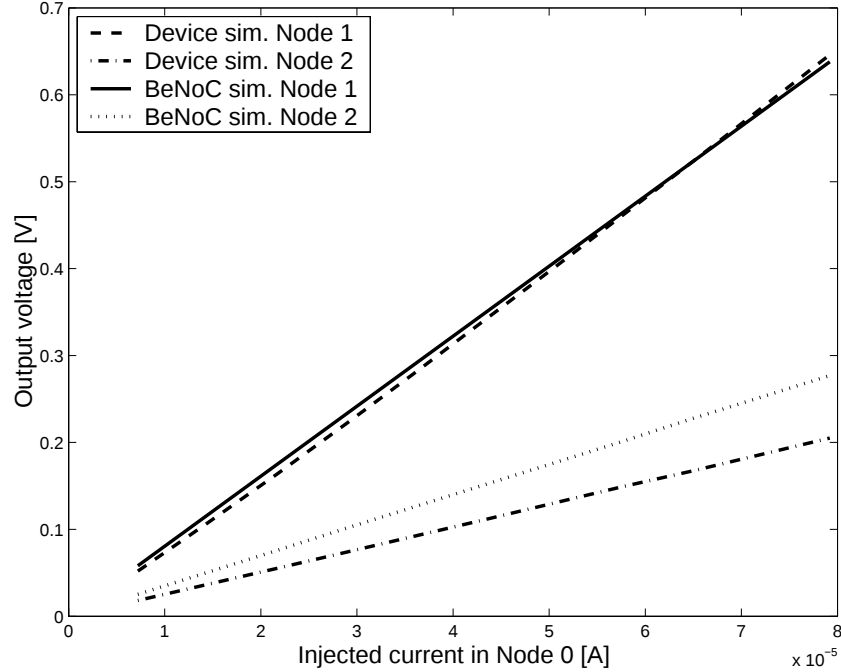


Figure 20. Output voltages for nodes 1 and 2 from Figure 5 in device simulation case and in BeNoC case.

The difference between the two simulations was then calculated as a measure of the BeNoC model accuracy against the device simulation. A selection of the results from these calculations is displayed in Table 3 where the difference error in output voltage between the models is shown for three samples of injected current values. The moderately high linear error in node 2 is partly a result of the Delaunay triangulation network reduction and partly a built-in error in the external resistance extraction models.

Table 3. Difference between the BeNoC model and device simulation.

Injected current [μ A]	Device		BeNoC		Error	
	Node 1 [V]	Node 2 [V]	Node 1 [V]	Node 2 [V]	Node 1 [V]	Node 2 [V]
14.40	0.107	0.037	0.116	0.050	8%	35%
43.20	0.340	0.111	0.348	0.151	2%	35%
79.20	0.646	0.205	0.638	0.277	1%	35%

The simulation described above was performed for four different node distances W and the tests show that the error between BeNoC and the device simulation increased when W was either very small or very large, which confirms

errors in the resistance extraction. This is an issue that needs to be addressed in future work to enhance the accuracy of the model.

3.2.5 Noise current injection models

In section 2.2.3 it is concluded that the two most significant mechanisms involved in substrate noise injection are noise through capacitive coupling and impact ionization noise. Of these two, the dominant one at high frequencies is noise through capacitive coupling. This is why the proposed current injection function represents the current leaking into the substrate due to capacitive coupling in digital CMOS transistors during switching. A behavioral noise coupling simulation needs an estimation of the power supply current i . Using this information as a starting point, the targeted model for estimating the substrate injection current for a technology $\mathbf{T}$ and a block area A can be stated as

$$i_{inj, cap}(t) = f(i(t), \mathbf{T}, A). \quad (10)$$

The switching of a CMOS circuit can approximated as

$$u(t) = \frac{1}{C_{tot}} \int_{t_0}^{t+t_0} i(t) dt \quad (11)$$

for a $0 \rightarrow 1$ transition, with the initial and end conditions

$$u(t_0) = 0, u(t_0 + t_d) = V_{dd} \quad (12)$$

and

$$u(t) = V_{dd} - \frac{1}{C_{tot}} \int_t^{t+t_d} i(t) dt \quad (13)$$

for a $1 \rightarrow 0$ transition, with the initial and end conditions

$$u(t_0) = V_{dd}, u(t_0 + t_d) = 0, \quad (14)$$

where t_d is the gate delay, t_0 the time of an input transition and V_{dd} the voltage source. From these two cases the total switched capacitance in a certain logic gate can be derived as

$$C_{tot} = \frac{1}{V_{dd}} \int_{t_0}^{t_0+t_d} i(t) dt. \quad (15)$$

Equation (14) inserted into Equation (11) results in an expression for an output node

$$u(t) = \frac{1}{\frac{1}{V_{dd}} \int_{t_0}^{t_d+t_0} i(t) dt} \int_{t_0}^{t+t_0} i(t) dt. \quad (16)$$

From [21] the noise current from capacitive coupling injected into the substrate for an inverter can be written as

$$i_{inj,cap}(t) = kC_j \frac{\partial u_{source}}{\partial t}, \quad (17)$$

where k is a constant indicating the number of transistors in the area of each block. Equations (16) and (17) are combined to give an equation for estimating the capacitive injection current

$$i_{inj,cap}(t) = \frac{kC_j}{\frac{1}{V_{dd}} \int_{t_0}^{t_d+t_0} i_{source}(t) dt} i_{source}(t). \quad (18)$$

Hence, an expression fulfilling the target function stated in equation (1) has been obtained, where the formulated parameters are given by the technology with C_j , the power supply currents with i and t_d and the number of transistors in the area with k .

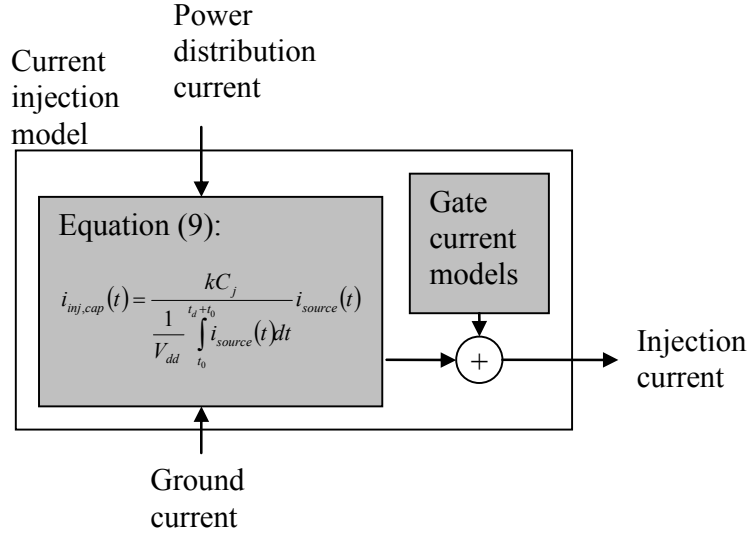


Figure 21. Schematic of the noise current injection model.

This section is concerned with the analysis of the proposed noise current injection model. The inverter is taken as an example. To improve the level of accuracy for the model described in Equation (18), it is extended using an estimating noise injection model from the gate, where there is capacitive coupling over the gate oxide and over the channel. Since the current behavior for an n-transistor and a p-transistor are different, there is one gate current estimation function for each type of transistor. They are combined to form an accurate model of the total gate current of a logic gate. In the case of an inverter, one p-transistor and one n-transistor gate current model are added together and, as shown in Figure 21, added to incoming power distribution and ground currents inserted into Equation (18).

To reduce the error in the final modeled injection current, the gate currents are modeled as differentiated voltage transitions. The error is reduced because the voltage is simpler to accurately model than the current.

The following section concerns the specific work involved in extracting the noise injection function for the inverter. From Equation (18) it can be derived that the capacitive coupled noise injection current in an inverter is the sum of the source-to-substrate junction capacitance coupled currents of the two transistors multiplied by the junction capacitance. This yields the formula

$$i_{inj,cap}(t) = C_j \frac{\partial u_{sn}(t)}{\partial t} + C_j \frac{\partial u_{sp}(t)}{\partial t} = C_j \left(\frac{\partial u_{sn}(t)}{\partial t} + \frac{\partial u_{sp}(t)}{\partial t} \right). \quad (19)$$

Briaire et al. in [25] state that the gate electrode is also a part of the capacitive coupling and is coupled to the substrate through the gate oxide and channel capacitances. This means that the gate currents multiplied by the capacitances from the gate oxide and the channel are added to Equation (19), forming a more accurate capacitive injection current

$$i_{inj,cap}(t) = C_j \left(\frac{\partial u_{sn}(t)}{\partial t} + \frac{\partial u_{sp}(t)}{\partial t} \right) + (C_{ox} + C_{ch}) \left(\frac{\partial u_{gn}(t)}{\partial t} + \frac{\partial u_{gp}(t)}{\partial t} \right). \quad (20)$$

The source currents can be input into the model as the power distribution current and the ground current. The gate currents forming $i_{g,tot}$ now remain to be modeled as each of the n and p transistor gate currents are modeled as functions

$$\frac{\partial u_{gn,p}(t)}{\partial t} = \frac{\partial}{\partial t} \begin{cases} k_1 \cdot V_{DD} \cdot \text{sinc}\left(m_1 \cdot \frac{t}{t_{sample}}\right) & \text{for } 0 \leq t < t_1, \\ k_2 \cdot V_{DD} \cdot e^{-m_2 \cdot \frac{t-t_1}{t_{sample}}} - k_2 & \text{for } t_1 \leq t \leq t_2. \end{cases} \quad (21)$$

Here, m_1 and m_2 are delay constants, and k_1 and k_2 sets the amplitude and the sign depending on what transistor (p or n) is being simulated and depending on whether the transition of the transistor is positive or negative. As discussed previously, the currents are modeled as differentials of the voltage swings to enhance the accuracy.

As an investigation regarding whether the gate current model is indeed required, a further simplification was considered for the capacitive injection current, where the gate model is completely replaced by a capacitance. This yields the equation

$$i_{inj,cap,simple}(t) \approx (C_{out+gate} + C_j) \left(\frac{\partial u_{s,tot}(t)}{\partial t} \right), \quad (22)$$

removing the necessity for Equation (21) but involving a loss in accuracy.

To ensure that the noise current injection models are valid they require to be verified, in this case against Spice simulation values. This will also reveal the level of accuracy the models deliver. The accuracy is not crucial since the models will be used at a behavioral level, but they should not differ too greatly from Spice values.

Also, the simplifications made, ignoring both the next cascaded gate and the gate currents altogether, must be assessed for validity.

3.2.5.1 Injection model simulation results

The noise injection model for the inverter example has been simulated and compared to Spice values. The logic gate in each verification case has been inserted between two logic gates of the same type to form a cascade connection. This ensures correct in- and out capacitances to and from the simulated gate. To estimate the difference between the modeled injection currents and Spice generated injection currents, spectral analyses were made for the noise current simulations. The inverter simulation for the proposed model, with and without gate current estimations, and Spice is shown in Figure 22. The spectral analyses of the three curves are shown in Figure 23.

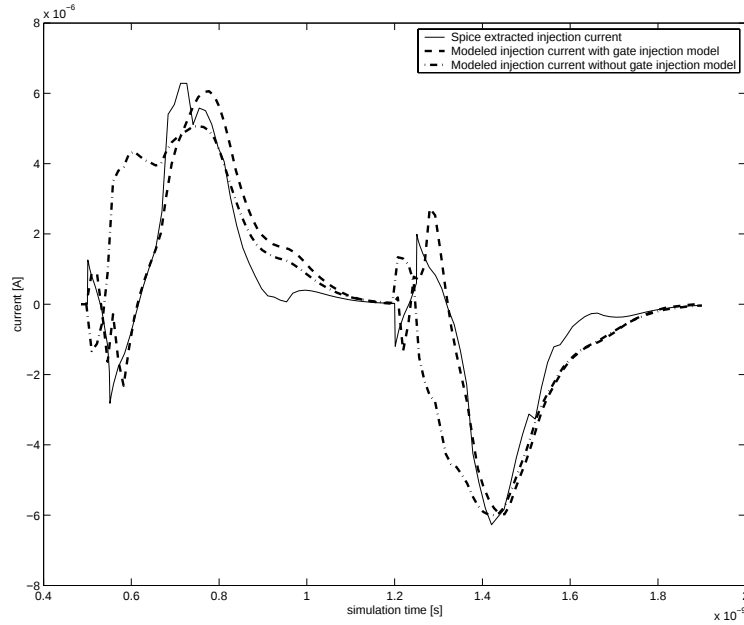


Figure 22. Transient analysis of the noise injection current of a NOT gate, modeled versus Spice.

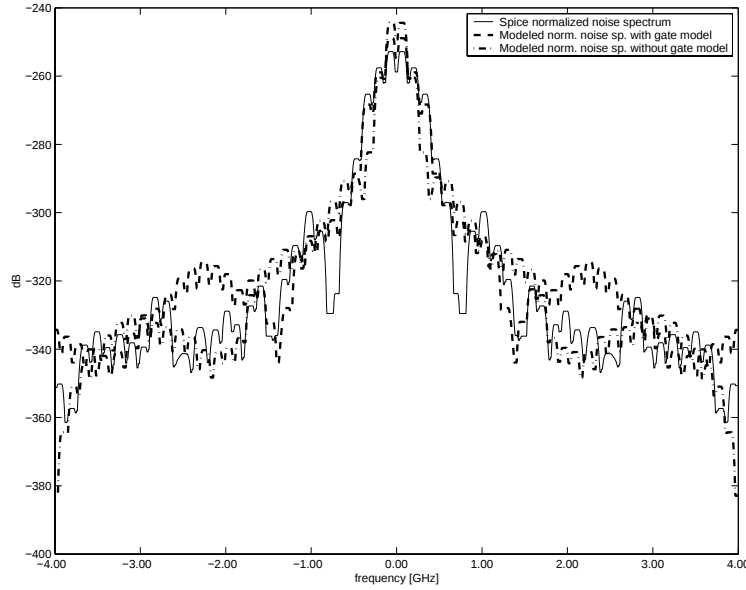


Figure 23. Spectral analysis of modeled and Spice injection current simulations from Figure 22.

In the transient analysis in Figure 22 the effects of the gate current simplification can be observed. For the model with gate current estimation, the major current spike acquires a small delay and a phantom current can also be observed at the point where the major spike is supposed to level out to zero. The further simplified model without gate current estimation has many more errors that are reflected in the low frequency part of the spectral analysis.

To further ensure the validity of the logic gate simulations, simulations were made using a different delay, which is shown in Appended paper IV.

The simulations indicate that the models with gate current estimations become more accurate with larger delays, while the model without gate current estimations has about the same level of accuracy. This is expected since the differential of the gate voltages level out with larger delays which gives smaller errors in the final injection current of the model with gate current estimations.

The levels of accuracy are promising and make the noise current injection models well suited for noise coupling simulation at the behavioral level. The further simplified model could be well suited for architectural explorations, while the gate current estimation incorporated model is suited to behavioral and circuit level in the design flow.

3.2.6 Simulation engine description

The chosen simulation engine proposed is a SystemC engine controlling an AIM-Spice engine. Since the simulations are done in SystemC, the refinement levels of the modules are up to the user's discretion, enabling substrate coupling simulation to be performed at various abstraction levels. The wrapper contains a

simulation clock that defines the accuracy of the simulation. A low timestep on the simulation clock raises the accuracy of the simulation and vice versa. An approximate floorplan of the modules is defined, this information is entered as coordinates to substrate nodes, and the model takes this into consideration when it uses the technology parameters to set up the resistive network for simulation. The resistive network is then extracted by SPACE, a layout-to-circuit extractor developed at Delft University of Technology [36]. The network is then sent to the AIM-Spice circuit simulator as a Spice netlist generated by the SystemC model. AIM-Spice simulates the netlist in parallel with the SystemC simulator and the current spread information is then sent from AIM-Spice to SystemC, which relays the information to the user. The connection between SystemC and AIM-Spice is described in further detail in the next section.

3.2.6.1 SystemC to AIM-Spice connection

The connection between the AIM-Spice circuit simulator and the SystemC behavioral simulator is implemented using parallel threads in the operating system, in which the Spice simulator is sensitive to current injection values sent from SystemC. As shown in Figure 24, the SystemC part constructs a Spice netlist that is sent to the AIM-Spice simulator, which then enters an interrupt detection mode, awaiting injection current values from SystemC.

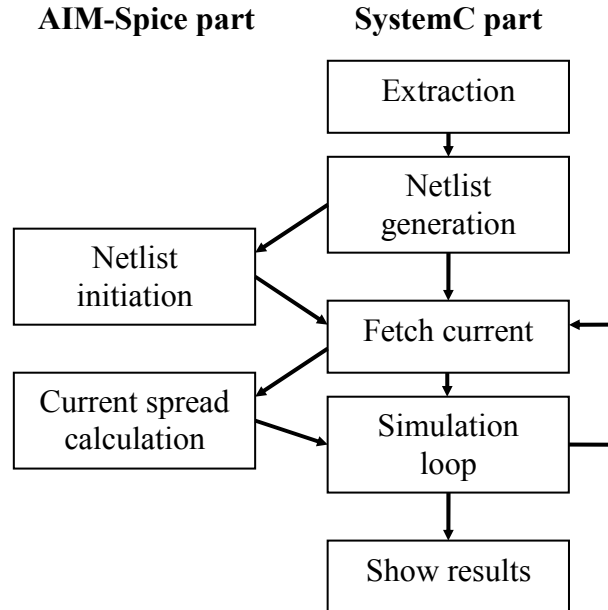


Figure 24. Connection between the SystemC part and the AIM-Spice part of the BeNoC model.

This enables SystemC to fetch current values from an injection current module while the AIM-Spice part initiates the netlist. The SystemC part then sends the fetched current value to the AIM-Spice part, which inputs the current into the

designated place in the netlist and returns the output current, from the node being watched, to the SystemC part. While the Aim-Spice part is working the SystemC part fetches the next current value from the injection current module. The simulation then continues in this manner until the simulation end time is reached and the SystemC part presents the output currents to the user. This means that the AIM-Spice simulation part runs in parallel with the SystemC simulation, thus, for modern computer architectures, speeding up the simulation time. If the user does not wish to use an injection current module, the injection current can also be collected from a data file with pre-recorded current values.

4 SUMMARY OF PUBLICATIONS

The four papers in this thesis deal with noise coupling simulation modeling including power distribution network modeling, substrate modeling and substrate noise injection modeling. In the BeNoC simulation flow in Figure 25 the content of each paper has been identified.

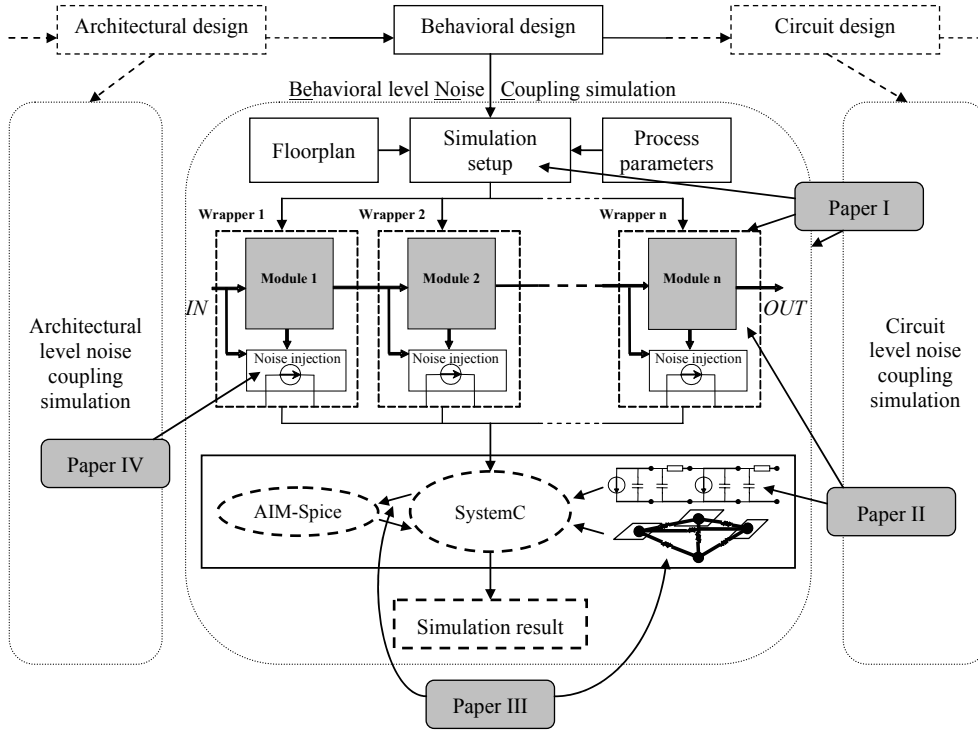


Figure 25. Identification of paper contents in the BeNoC simulation flow.

4.1 PAPER I

The concept of high-level noise coupling simulation and the first model for power distribution networks is presented. The idea of a noise coupling wrapper for each functional block is introduced. The accuracy of the model is compared to Spice simulations, yielding relative mean error estimations.

4.2 PAPER II

The place of the high-level noise coupling model in the design flow is proposed and the power distribution network model is tested in a design test case. The implementation of the model in SystemC is described and the organization of the behavioral level noise coupling simulation method is mapped. The

implemented model is tested on a pixel detector design. Accuracy and computational simulation times are compared with Spice simulations.

4.3 PAPER III

Methods and models for simulating substrate noise coupling are presented. The system overview and simulation flow are presented. A simulation link is described, connecting SystemC and AIM-Spice. The SystemC simulation models controlling AIM-Spice are verified for accuracy against device simulations.

4.4 PAPER IV

Models of noise injection currents are presented for all of the logic gates. The models are particularly developed for noise coupling simulation on the behavioral level. The model equations are derived and verified against Spice simulations.

4.5 AUTHOR'S CONTRIBUTIONS

The contribution of the author of this thesis has been essential to all the papers listed in Table 4. The exact contribution of each author is specified in the right-hand column.

Table 4. Author's contribution (M = main contributor, C = co-author).

Paper #	JL¹	TY²	BO³	KV⁴	MO⁵	PE⁶	MA⁷	Contributions
I	M	C	C		C	C	C	JL: Design of models TY: Model simulations BO: Model verification MO: Supervisor PE: Industrial contribution exploration MA: Test case provider
II	M	C	C		C	C	C	JL: Implementation of models TY: Model simulations BO: Model verification MO: Supervisor PE: Industrial contribution exploration MA: Test case provider
III	M	M		M	C			JL: Design and implementation of models TY: Model linkage programming KV: Device simulation verification MO: Supervisor
IV	M	C			C			JL: Design of models TY: Co-supervisor MO: Supervisor
1. Jan Lundgren 2. Trond Ytterdal 3. Bengt Oelmann 4. Kristian Vonbun					5. Mattias O'Nils 6. Patrik Eriksson 7. Munir Abdalla			

5 THESIS SUMMARY AND CONCLUSIONS

Methods and models for simulation of on-chip noise coupling at a behavioral level have been presented in this thesis. An introduction to the research area has been given in Section 1. A thorough review of related research in the field has been presented in Section 2. Section 3 described the work completed in developing noise coupling simulation methods and models for behavioral level simulation. Section 4 gave a short summary of the original contributions for each paper.

5.1 THE PROPOSED DESIGN FLOW

Introducing noise coupling to the behavioral level means an addition to the design work flow, where the effects of noise coupling are simulated throughout the entire design flow. This addition has been proposed to be a natural part of mixed-signal design and perhaps also for strictly digital or analog design.

5.2 SYSTEM MODELING

The model for simulating power distribution and substrate noise coupling is devised as an add-on wrapper that encapsulates a component module. The wrapper adds simulation ports and injection current models to the component being simulated. The wrappers are then connected together in a mesh to simulate the power distribution network and the substrate. The current spread is then calculated between wrappers and the resulting noise currents are presented.

5.3 POWER DISTRIBUTION NETWORK MODELING

The power distribution network lines are modeled as cascaded discrete RC-stages with a particular serial resistance and a capacitance to ground for moderate frequencies but could also be modeled as RLC-stages for higher frequencies. The power distribution model is required to deal with three different cases: (1) timestep is smaller than the RC-factor $R \cdot C$, (2) timestep and the RC-factor are of the same magnitude ($\text{timestep} \approx R \cdot C$) and (3) timestep is larger than the RC-factor. This ensures stable simulation models for all values of timestep. By using the same modeling technique, an RCL model of a wire can be built.

5.4 SUBSTRATE MODELING

The substrate model used is a 3D single substrate node model [23]. It combines a two-contact single node configuration [33] with a lateral triangulation technique, which is a modified Delaunay triangulation [22]. In practice, every node is given one resistance toward the bulk node and resistances are also placed between nodes using a “shortest path” technique.

A modification was added to the triangulation technique to increase the accuracy of the noise coupling simulations. If four nodes are placed in a square mesh structure, i.e. with diagonals of the same length, the model sets resistances on both diagonals.

The BeNoC substrate modeling technique has been verified against device simulations in the Atlas device simulator. The accuracy of the BeNoC model was tested against the Atlas device simulation of the same structure and the same injection current. The difference between the two simulations was then calculated as a measure of the BeNoC model accuracy against the device simulation.

5.5 NOISE CURRENT INJECTION MODELS

The noise injection mechanism caused by capacitive coupling has been targeted for this work and a function of this injection current has been derived. As an example, the specific injection current for an inverter has been derived and verified against Spice simulations. The noise injection model incorporates a gate current injection estimation model that reflects the contribution derived from the capacitance over the gate oxide and channel.

5.6 PROPOSED SIMULATION ENGINE

The proposed chosen simulation is a SystemC engine, which controls an AIM-Spice engine. Since the simulations are performed in SystemC, the refinement levels of the modules are up to the user's discretion, enabling substrate coupling simulation to be performed at various abstraction levels.

The connection between the AIM-Spice circuit simulator and the SystemC behavioral simulator is implemented using parallel threads in the operating system, in which the Spice simulator is sensitive to current injection values sent from SystemC.

5.7 FUTURE WORK

The future work would involve increasing the accuracy and functionality of the existing models.

- Incorporate inductances in the power distribution network model.
- Increase accuracy in the single node substrate model, reducing the linear error.

New work would incorporate bringing BeNoC together as an application.

- Implement noise current injection models in SystemC for BeNoC.
- Verify the SystemC BeNoC implementation for validity and accuracy as an application.
- Develop a floorplan design application.

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PAPER I

Behavioral Simulation of Power Line Noise Coupling in Mixed-Signal Systems using SystemC

P a p e r I

Behavioral Simulation of Power Line Noise Coupling in Mixed-Signal Systems using SystemC

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Abstract

This paper presents methods for early quantification of digital to analog noise coupling at behavioral level. The methods enable designers to both verify the behavior of their mixed-signal architecture and its sensitivity to noise coupling. The high-level noise coupling simulation models are implemented as extensions to SystemC.

1. Introduction

The integration level of electronic systems is constantly increasing, both on chip and package levels. When a complete system is integrated on a single chip or package, it will usually compromise both analog and digital functional blocks. In the integration of digital and analog circuits, potential noise coupling from the digital logic to sensitive analog nodes needs to be carefully considered. Noise generated by digital circuits is coupled over the power distribution network and through the substrate of the package or chip [1]. Quantification of the noise coupling and the degradation this causes to system performance needs to be assessed very early in the design cycle in order to avoid costly and time consuming re-design at a later stage. Accurate predictions of the noise coupling effects normally need very low-level simulations to be carried out [2][3]. Circuit level simulation however implies very long simulation times, something which quickly becomes a problem with increasing circuit and system complexity. None of the existing approaches allows the quantification of noise coupling at an architectural level [4], in a top-down design flow. The methods presented in this paper enable a designer to quantify the noise coupling effects at the early stage of architectural explorations. The noise source models for the different circuit blocks of the system can be modeled to be

data dependent, hence the noise coupling simulation will be very similar to the real system. By enabling fast evaluation of different architectures, the system designer can find analog and digital architectures with low sensitivity to interference and generating only low levels of harmful interference, respectively. Early quantification of the digital to analog noise coupling can also give valuable information to the floor planning of the chip.

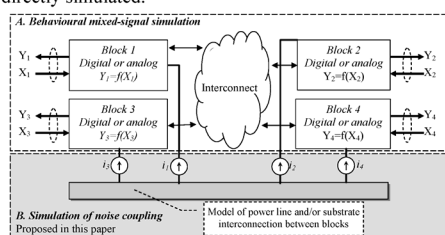
The methods for quantifying and verifying noise coupling that are described here are implemented as extensions to SystemC [5], which is a worldwide initiative to develop a system design language that is able to model hardware (both analog and digital), abstract communication and software constructs. SystemC modeling language is captured in C++ classes, which makes it an excellent platform for research since there is no overhead associated with building extension to the modeling and simulation methods in SystemC, as would be the case for a compiled approach. Since SystemC supports incremental design refinement, the model can be used on different abstraction levels, preventing long design flow iterations.

We have organized the paper as follows. Section 2 present the modeling and simulation extensions for high-level noise coupling simulation and comparison of the simulation accuracy. Finally, in Section 3, we conclude the paper.

2. High-level simulation of noise coupling

SystemC version 4.0 will support modeling and simulation of mixed-signal systems. The work to achieve this has started in both academia [6] and by the SystemC consortium [5]. The idea behind the simulation methods proposed in this paper is to extend the behavioral mixed-signal modeling and simulation methods to also include the simulation of noise coupling between analog and digital blocks, as shown in Figure 1. The simulation of the noise coupling is based on abstract models of power

In a top-down design flow supporting modeling and simulation of noise coupling, the mixed-signal behavioral models of the blocks in the system are initially developed and simulated. When these models have been developed and verified, the models for simulation of the noise coupling can be added to the simulation. The functional simulation will work exactly as in the previous case, the difference being that the simulation models for the power consumption are added to each block in the system, $(i_j - i_i)$ in Figure 1. The behavior of each current source can be individually modeled, e.g. it could be recorded from a SPICE simulation, it could include data dependency, or it could be a statistical model. Each current source is connected to the model of the power distribution network in the extended test bench, which is used for simulation of the noise coupling as shown in Figure 1. The simulation can either be used to analyze the noise at a certain point of the power distribution network or the noise voltage can be fed directly into the analog behavioral model. Thus, the noise coupling effect on the system behavior can be directly simulated.



2.1 Mixed-signal noise coupling wrapper

The actual implementation of the wrapper in SystemC is made as macro definitions that are instantiated in the code of each block. The interface is added by including *NC_SIM_PORTS* in the code of the block, as illustrated by the counter example in Figure 2. The user configures the wrapper by defining the update period, *timestep*, of the simulation clock, *sim-clk*. The triggering condition of the current source is defined by adding

[illegible]

Figure 2. Noise coupling simulation wrapper.

2.2 Modeling the power distribution network

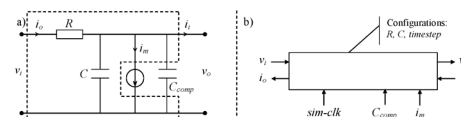


Figure 3. a) RC-based model for wires and b) the interfaces for the system SystemC model.

$$\text{Case 1: } \begin{cases} \Delta v_o = \frac{\Delta(i_m + i_i)\Delta t}{C} \cdot \gamma_1 \\ \Delta i_o = i_n + \frac{\Delta v_o}{R} \end{cases}$$

Where γ_1 and γ_2 are damping factors set to 1.0. Δt is the *timestep* of the simulation. For case 2 same equations are used but the damping factor is set to the function $\gamma_n = f_n(R, C, \Delta t)$, which is similar to the methods presented by Brambilla et al. [8]. This ensures stable simulation

models for all values of *timestep*. By using the same modeling technique, an RCL model of a wire can be built.

In Figure 4 simulation results from these three cases are shown. The simulation setup consists of three cascaded RC-stages. Current pulses on i_m , representing currents in the power supply for the blocks, are injected in stage two and three. The output voltage v_o and output current i_o of each stage are plotted. The component values are set to $\tau_{RC} = 2$ ns for all stages and the simulation time is set to 100 ns. For a *timestep* much smaller than the RC-factor (100 ps), the simulation results are very close to the results from SPICE and these cannot be distinguished from each other in the plot.

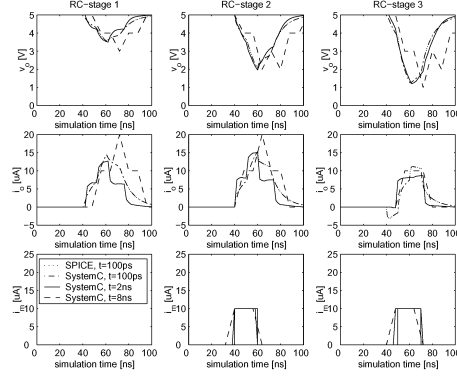


Figure 4. SystemC vs. SPICE simulation results.

For larger timesteps the accuracy will drop and, as can be expected, the error will increase in amplitude and time. For the case of a *timestep* equal to 8 ns (four times the RC-factor) this is clearly shown.

The relative mean error estimates for the three cases are made according to:

$$Rme[\%] = \frac{\sum (V_{SystemC} - V_{SPICE}) \cdot \Delta t}{\sum (V_{SPICE} \cdot \Delta t)} \cdot 100$$

The results of these error estimations are shown in Table 1. The SPICE simulation that is compared with the SystemC simulation cases has a *timestep* of 100 ps.

Table 1. The relative mean error estimations of v_o for the three cases vs. the SPICE plots.

<i>timestep</i>	RC-stage 1	RC-stage 2	RC-stage 3
100 ps	0.046 %	0.084 %	0.111 %
2 ns	1.807 %	1.945 %	2.523 %
8 ns	3.928 %	5.503 %	11.005 %

The presented model has its limitations. The actual update period in the model is $T_{update} = (2n-1) \cdot timestep$, where n is the number of RC-stages. This causes a problem for large numbers of n , since the *timestep* has to be very short, and this in turn causes long simulation times.

3. Conclusions

We have presented a simulation method for quantification of noise coupling over power distribution networks at behavioral level. The simulation model consists of two parts, a noise coupling wrapper for behavioral blocks and a noise-coupling block for interconnection. The wrapper captures the power consumption behavior of the functional block and can be captured as a data dependent current source (CS), a CS captured from SPICE data or statistical modeled CS. The interconnection block models the power distribution network and its accuracy compared to SPICE is in the range of 99.9% down to 90% depending on the update frequency of the synchronous dataflow. Both the noise-coupling wrapper and the interconnection block are implemented in SystemC as synchronous dataflow and are both compatible with the normal SystemC description style.

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PAPER II

A Power-line Noise Coupling Estimation Methodology for Architectural Exploration of Mixed-Signal Systems

P a p e r I I

A POWER-LINE NOISE COUPLING ESTIMATION METHODOLOGY FOR ARCHITECTURAL EXPLORATION OF MIXED-SIGNAL SYSTEMS

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ABSTRACT

This paper presents methods for early estimation of digital to analog noise coupling over the power distribution network in mixed-signal systems. The methods allow both behavioral verification of mixed-signal architectures and their sensitivity to noise coupling of the power distribution network. The behavioral level noise coupling simulation models are implemented as extensions to the SystemC system design language. To illustrate the effectiveness of the proposed methods, we have estimated the power distribution network noise for a photon-counting X-ray pixel array and compared this with SPICE simulations.

I. INTRODUCTION

With the new System-on-Chip (SoC) designs, the integration of digital and analog components on a single chip increases, causing undesired noise coupling effects. The currents from the switching digital logic are coupled to the sensitive analog nodes through power distribution networks and through the substrate of the chip [1]. This problem needs to be assessed as early as possible in the design flow process to avoid costly design flow iterations. Today, accurate simulations of noise coupling are only done on layout level [2][3], which gives problems with long simulation times caused by high circuit complexity. Design iterations between layout level and architectural level results in long design times. These are all factors that contribute to the final cost of the system. None of the existing models allows simulation of noise coupling at an architectural level [4] in a top-down design flow.

There are different macro models for simulating power distribution networks, two different models are currently dominating in simulation research [5]. The first is the simple RC model shown in Figure 1a, which works for $t_r > 2T_0$, where t_r is the waveform transition time of the clocked signal coupling onto the power distribution network and T_0 is the time of flight [6]. However, when t_r decreases below $2T_0$, this model have to be expanded to

include an inductance in series with the RC model. This model is shown in Figure 1b.

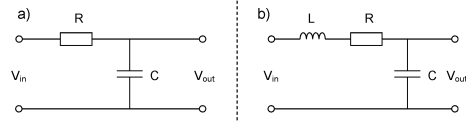


Figure 1. a) RC model for simulating power distribution networks. b) RLC model for use when $t_r < 2T_0$.

The methods presented in this paper enable a designer to quantify the noise coupling effects and explore various schemes to combat the self-generated interference during architectural design space exploration. It differentiates itself from other approaches, found in the literature, through the integration of the behavioral simulation together with a high-level model of the noise coupling. Hence, the method enables investigation of the dynamic effects the behavior has on the noise coupling at a high level, without having to design the circuits. This is achieved by combining a behavioral simulation in SystemC [7] with a high-level noise coupling simulation done offline in SPICE. The noise coupling part is added to the behavioral SystemC model by applying a wrapper to each behavioral block. The noise coupling is simulated using the behavioral model, with wrappers, together with technology parameters and a virtual layout that connects the power distribution network between the blocks. This enables the system designer to make fast simulations of different architectures and get an evaluation of the noise coupling problems in the system, enabling the designer to construct architectures with low sensitivity to noise coupling interference. This is also valuable information in the chip floor planning process. The wrapper model is a modified version of the one presented in [8], which had some limitations. When the number of simulated blocks

grew the simulation timestep had to be reduced and thereby the simulation time grew rapidly. By generating SPICE netlists and simulating the power distribution in SPICE instead of letting SystemC simulate the power distribution network, this problem was eliminated.

Next section positions the presented method in a top-down design flow. The modeling method is described in section III. Section IV demonstrates the simulation method by using the method for design space exploration of a dental photon counting X-ray pixel array. This design example is also used to compare the accuracy of the simulation results with real circuit simulations. Finally, we summarize the paper.

II. DESIGN FLOW

The proposed noise-coupling model is used during the architectural exploration phase of a top-down design flow for mixed-signal systems [4], as depicted in Figure 2. The noise coupling simulation starts from a behavioral model, which is extended by applying the noise coupling simulation wrapper to it. The simulation wrappers add technology parameters, power consumption and power supply interconnect to all functional blocks in the system. This enables early evaluation of a mixed-signal architecture's sensitivity to noise coupling over the power distribution network. Same method can also be used for finding the best floor plan. All this can be achieved without costly design iterations between architectural and layout levels.

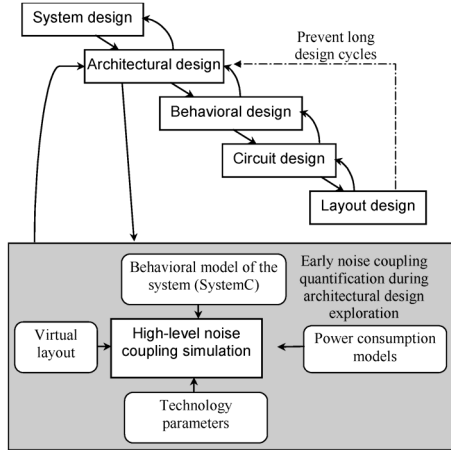


Figure 2. Proposed addition to a top-down based design flow for mixed signal systems.

III. MODELING

Modeling constructs used in the presented noise coupling method are summarized in Figure 4a. In order to simulate the noise coupling current of a functional block, a wrapper consisting of a current source and the simulation ports simulation clock, power supply and ground is added around the functional block. The wrapper is illustrated in Figure 3.

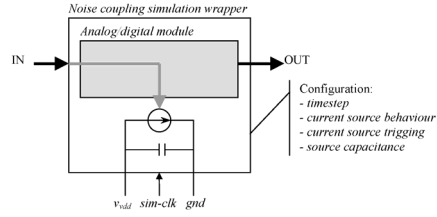


Figure 3. Mixed-signal noise coupling wrapper.

The wrapper model is implemented in SystemC as macro definitions that are added to the module of the functional block. The user adds *NC_SIM_PORTS* to the code of the block, as illustrated by the counter example in Figure 4b. The configuration of the wrapper is set by defining the update period, *timestep*, of the simulation clock, *sim-clk*. To add the triggering condition of the current source the user adds *NC_CURRENT_SOURCE* to the constructor of the block with a standard SystemC sensitivity list, as shown in Figure 4b. The behavior of the current source is entered as a SystemC process, which is written as a C++ method.

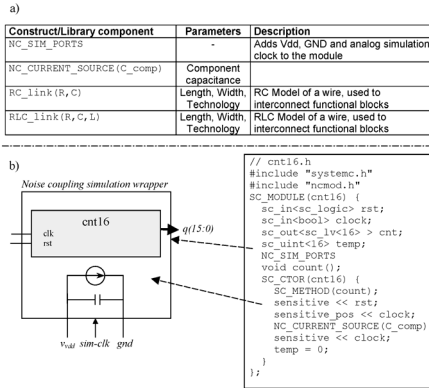


Figure 4. a) List of constructs for modeling behavioral noise coupling. b) construct applied on a 16-bit counter.

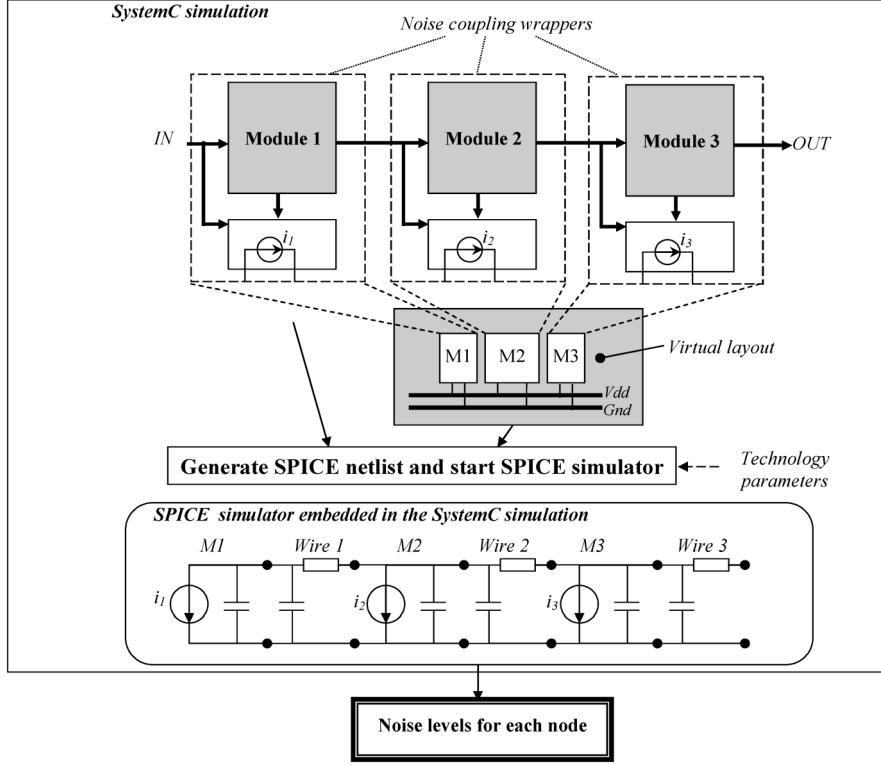


Figure 5. Organization of the behavioral noise coupling simulation method.

The noise coupling wrappers are connected by entering a virtual layout of the system, as shown in Figure 5. In the current version, the virtual layout is entered in the SystemC description. This is done by connecting the blocks with the selected wire model, listed in Figure 4a, which is completed with technology parameters. From this description a SPICE netlist is generated. This includes the power distribution network and the noise behavior of each block in the system. The noise behavior is recorded during behavioral simulation and included as piece-wise linear (PWL) current sources in the generated SPICE netlist. Currently noise coupling simulation is done offline. To enable feedback of the noise levels into the behavioral simulation, the two simulations must be done simultaneously. This integration is left for future work.

IV. ARCHITECTURAL EXPLORATION

Sub-micron technology has enabled X-ray imaging with image sensors composed of photon-counting pixels [9]. In these image sensors, each pixel is implemented as a single channel radiation detector, which means that each X-ray photon that is detected in the pixel is counted. The number of counts will represent the pixel value. A count is processed such that when a photon hits the detector, the photon energy is converted into a charge pulse, i_{ms} , which is integrated by the pre-amplifier, V_{charge} in Figure 6. This is then pulse-shaped, i.e. first high-passed filtered and then low-passed filtered, V_{CR} and V_{RC} respectively. The output is a semi Gaussian shaped pulse, V_{RC} in Figure 6, where the height represents the photon energy. The pulse is counted if the energy is between the two threshold levels in the window discriminator, i.e. implemented with two comparators. This enables X-ray color imaging and gives increased sensitivity. Another advantage with a photon counting image detector is that the image is directly

captured in digital form and thus no analog to digital conversion is needed during readout.

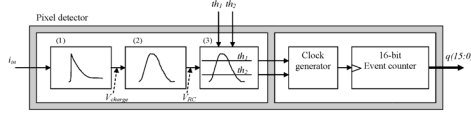


Figure 6. Behavioral mixed-signal model of the photon-counting pixel detector.

Each pixel comprises three to five hundred transistors, which accentuates the problem with tight integration of sensitive analog circuits with digital logic [10]. To quantify the noise coupling effects for the image sensor requires long design and simulation times if carried out at circuit level. We have chosen the photon counting image sensor as a test vehicle to demonstrate the effectiveness of our proposed high-level simulation methods. In the test setup we have used a small fraction of the image sensor where we simulate 16 adjacent pixels (4×4 pixels).

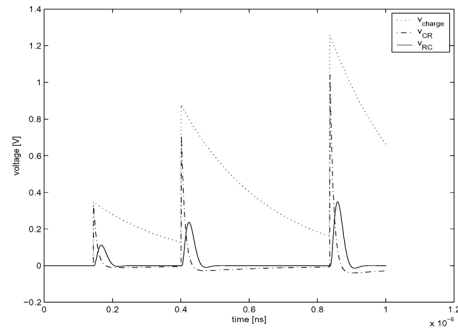


Figure 7. Behavioral model simulation plot of the analog component sub-blocks.

The behavioral model of the pixel detector is partitioned into two components, one component for analog signal processing and one component for event counting, as shown in Figure 6. The analog component comprises three sub-blocks: (1) pre-amplification V_{charge} , (2) pulse shaping (differentiation V_{CR} and N^{th} order integration V_{RC}), shown in Figure 7, and (3) window discrimination. It has three inputs: (1) i_{in} , is the charge impulse input of a certain level from the radiation detector, (2) and (3) the discrimination thresholds th_1 and th_2 . Two signals are output from the analog component, one from each level discriminator in the window discriminator. The comparator outputs are connected to a clock generator in the digital event

counting block [11], which is connected to the event counter that registers the number of detected photon events, $q(15:0)$. The two components are captured using *SC_MODULE*. The behavior of the analog module is modeled as a synchronous data-flow triggered by an analog simulation clock and the digital is modeled using standard RTL-level SystemC modeling style.

The test structure is organized as a 4×4 pixel array with a pixel size of $50 \mu m$, as depicted in Figure 8. It is simulated using both the Behavioral level Noise Coupling (BeNoC) simulation model and circuit simulation. The test case is limited to 16 pixels to enable verification with SPICE.

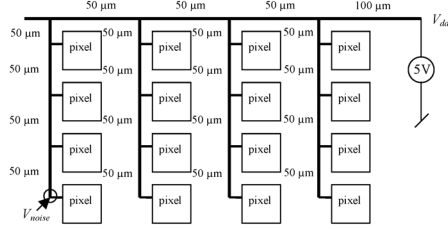


Figure 8. 4×4 array of photon counting pixels used as test vehicle for evaluation of the noise coupling simulation.

The pixels were modeled as depicted in Figure 9 with noise coupling wrappers for the digital and analog blocks.

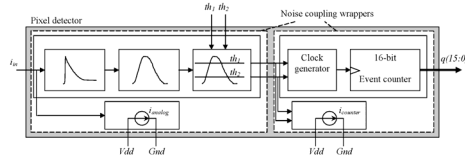


Figure 9. Behavioral mixed-signal model with power consumption wrapper.

To save area for the active pixel elements in the image sensor, we have evaluated a single power supply. This means that we have the same power supply for both the analog and the digital circuits. We have also selected power distribution network routing, as shown in Figure 8, using a fork structure, which is connected to a power supply with a $100 \mu m$ wire. Four cases are evaluated: two different power distribution network widths ($1 \mu m$, $5 \mu m$) for two different digital architectures. The first digital architecture (LFSR) is a synchronous linear feedback

shift-register and the second one is a LFSR with an asynchronous prescaler [12].

Counter	Line width	V_{noise}			Simulation time	
		Circuit	BeNoC	diff	Circuit ¹	BeNoC ¹
LFSR	1	3.1mV	3.0mV	3%	55.44	0.20+0.06
	5	0.53mV	0.51mV	4%	58.57	0.21+0.06
Prescaler	1	0.59mV	0.54mV	9%	56.46	0.19+0.06
	5	0.14mV	0.11mV	17%	56.59	0.20+0.06

Table 1. Evaluation of mixed-signal architectures using the BeNoC and comparing the simulation results with SPICE. Simulation time is measured on an ¹UltraSparc-10 300MHz (BeNoC time is divided into behavioral simulation + SPICE simulation). The test case was simulated for 2 μ s.

For the BeNoC simulation the pixels are connected using an RC wire model. In the circuit simulation only the digital part of the pixel is simulated and it uses the same R and C values as in the BeNoC simulation. Stimuli for the circuit simulation are event sequences of the two signals from the discriminators that is recorded from the behavioral SystemC simulation. Power model for the two digital architectures are captured from [12] and technology parameters that were used for these simulations:

- Wire capacitance: 0.045 fF/ μ m²
- Wire resistance: 150m Ω / $\square$.

Table 1 show that the noise coupling simulation is approximately two orders of magnitude faster, for this example, with an acceptable error for the simulation result. Although this is impressive, the main point with this approach is that the simulation can be done long before the circuits have been designed. As for most high-level design methodologies, the quality of the estimations highly affects the accuracy of the noise coupling simulation.

V. SUMMARY

In this paper we have shown that the high-level noise coupling simulation methods can be used to quantify different noise coupling parameters in a mixed-signal system. In this paper we have limited the approach to noise coupling over the power distribution network. We have demonstrated the noise coupling methods for a photon-counting X-ray image sensor (4×4 pixels) design. The results from these simulations are compared with SPICE circuit simulations of the whole pixel array. Noise coupling figures from the presented approach were obtained 100 times faster than from the full circuit simulation, without having to design the circuits.

The quantified noise coupling can be used to compare different pixel architectures, to generate constraints for analog designers, give hints on the design of the power

distribution network, and the noisy power supply can be fed directly into the behavioral model to simulate its effects on the pixel behavior. In this way, strategies for the power distribution network can be evaluated and the required constraints on the power supply rejection ratio (PSRR) can be tested and verified.

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PAPER III

Taking Mixed-Signal Substrate Noise Coupling Simulation to the Behavioral level using SystemC

P a p e r I I I

Taking Mixed-Signal Substrate Noise Coupling Simulation to the Behavioral level using SystemC

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Abstract

We present methods and models to simulate substrate noise coupling at the behavioral level. The models are implemented as a part of the SystemC based Behavioral level Noise Coupling (BeNoC) simulation application. The application is designed as a wrapper to SystemC component modules, enabling designers to simulate substrate noise coupling in their modules during the entire circuit refinement process. This is enabled through the two main contributions presented in this paper: (1) methods to connect the behavioral level with low level circuit simulations and (2) generation of a fast and accurate circuit model for substrate coupling simulations. The accuracy of the generated substrate noise coupling model is verified against device simulations. The same verification test case is used to demonstrate the connection between behavioral simulations and circuit simulations.

1. Introduction

Today’s technological advancements in mixed-signal systems are pushing for faster and faster design flow cycles, thereby increasing the demand on fast and reliable design tools, especially at the system level. In the increasing development of mixed-signal Systems-on-a-Chip (SoC), problems have surfaced in the form of noise coupling between switching digital components and sensitive analog nodes. To be able to meet these demands for faster system design cycles, the problems caused by noise coupling need to be simulated in a simple manner throughout the entire system design flow.

Two major sources of noise coupling have been detected; coupling over the power distribution network and coupling through the chip substrate [1]. By extracting the wire characteristics, noise coupling over

the power distribution network can be simulated in circuit simulators together with the circuits or as in [2] at the behavioral level. Most existing substrate noise coupling simulation techniques simulate at the layout level, where a number of simplified simulation models have been reported [3]-[6]. These models abstract the complex inner structures of the substrate using mesh cells, triangulation network reduction methods and nodal analysis. These are fairly accurate and can reflect and localize the problematic areas, but since no simulations have been done before the layout level is reached, the costs of design flow iterations are often great. Charbon et al. [7] have addressed this by enabling substrate noise coupling analysis from a gate-level netlist, which raises the abstraction and decreases the simulation time. This simulation technique, at gate-level, enables early detection of problems, which can guide the designer in the refinement process, resulting in a properly working SoC.

The methods and models presented in this paper goes one step further compared to [7], introducing substrate modeling at the behavioral level. Our approach thus enables designers to simulate substrate noise coupling through a large span of system design levels. The models are implemented as an extension to SystemC [8], allowing designers to connect the substrate noise coupling simulator to an existing SystemC component module using a wrapper technique. The models that are defined in SystemC are connected to the AIM-Spice simulator [9], which performs the substrate coupling simulations. This enables simulations of complex structures that could include for example capacitances and inductances. The AIM-Spice simulator is controlled by the SystemC models and also runs in parallel with the SystemC simulation. This optimizes the simulation time and provides reliable simulation results. The model presented in this paper is limited to noise coupling on substrates and its connection to behavioral simulations.

Noise coupling due to bond wires, leadframes and other inductive coupling sources is covered in [2].

The remaining sections of this paper are organized as follows. Section 2 describes the high-level substrate noise coupling models used in this paper. Section 3 presents the device simulation tests that was used to verify the BeNoC model. Section 4 compares the results obtained using this method with those of the device simulations. The conclusions are contained in section 5.

2. System overview

Simulating substrate noise coupling at the behavioral level calls for a reliable simulation application that uses a reduced substrate model. The accuracy of the simulations may not be central in a very abstract module and a hint as to where the problems occur may be sufficient. Of course, the simulation times are far more central at this level when the user wants to change a small detail in the module and simulate again. At the layout level, the accuracy would have a more central role in the simulations and the simulation time is not as important, since changes to the layout involves a considerable amount of time, if coupling issues have been detected. The rest of this section gives an overview of the system simulation method.

2.1. System simulation

The model for substrate noise coupling is devised as an add-on wrapper that encapsulates a component module. This enables the designer to simulate substrate coupling for any given module. The wrapper adds ports and a current flow in and out of the substrate, which is illustrated in Figure 1 and further described in [2].

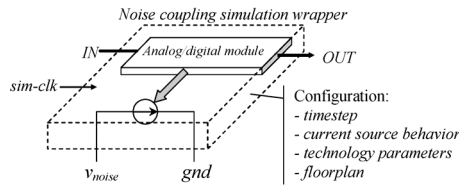


Figure 1. Wrapper model for the substrate noise coupling simulation.

The current flow consists of an injected current into the substrate that can either come from a noise

injection module or recorded current values from a data file, and an output calculated current from the wrapper. Each chosen component receives its own wrapper and they are all seen as nodes in the following simulation. The application then builds up an appropriate resistive network, depending on the given technology parameters. Figure 2 depicts the proposed simulation flow.

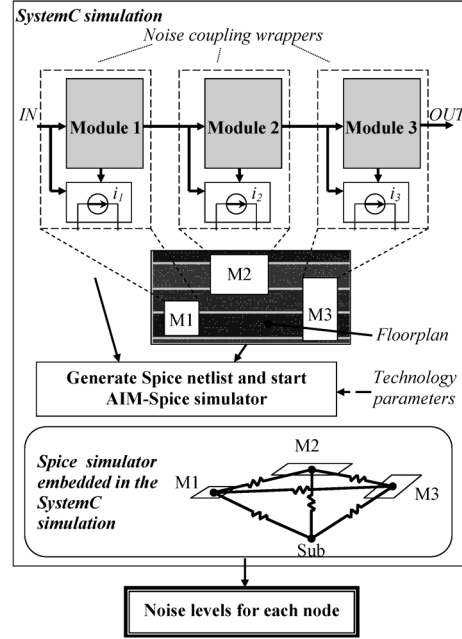


Figure 2. Simulation flow. The modules of interest are given wrappers which take the given floorplan and technology parameters, and generates an appropriate mesh that is simulated.

The modules that are interesting for substrate coupling simulation are localized and simulation wrappers are added to these modules. Since wrappers can be added to both analog and digital blocks, the user is free to simulate, for example, digital noise impact on digital blocks, analog noise impact on analog blocks and digital noise impact on analog blocks. The simulation models are thus independent of the nature of the circuits, enabling noise coupling simulations in digital and analog circuits as well as in mixed-signal circuits.

Since the simulations are done in SystemC, the refinement levels of the modules are up to the user's

discretion, enabling substrate coupling simulation to be performed at various abstraction levels. The wrapper contains a simulation clock that defines the accuracy of the simulation. A low timestep on the simulation clock raises the accuracy of the simulation and vice versa. An approximate floorplan of the modules is defined, this information is entered as coordinates to substrate nodes, and the model takes this into consideration when it uses the technology parameters to set up the resistive network for simulation. The resistive network is then extracted by SPACE, a layout-to-circuit extractor developed at Delft University of Technology [10]. The network is then sent to the AIM-Spice circuit simulator as a Spice netlist generated by the SystemC model. AIM-Spice simulates the netlist in parallel with the SystemC simulator and the current spread information is then sent from AIM-Spice to SystemC, which relays the information to the user. The connection between SystemC and AIM-Spice is described in further detail in the next section and the substrate model used is described in Section 4.

3. SystemC to AIM-Spice connection

The connection between the AIM-Spice circuit simulator and the SystemC behavioral simulator is implemented using parallel threads in the operating system, in which the Spice simulator is sensitive to current injection values sent from SystemC. As shown in Figure 3, the SystemC part constructs a Spice netlist that is sent to the AIM-Spice simulator, which goes into an interrupt detection mode, waiting for injection current values from SystemC.

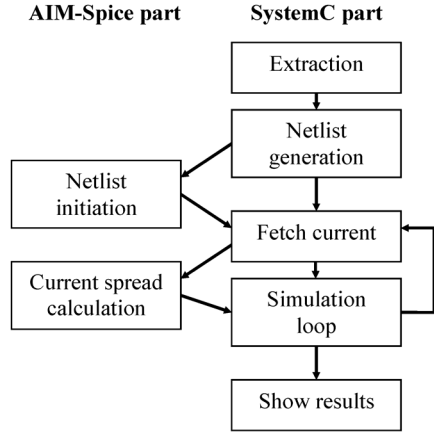


Figure 3. Connection between the SystemC part and the AIM-Spice part of the BeNoC model.

This enables SystemC to fetch current values from an injection current module while the AIM-Spice part initiates the netlist. The SystemC part then sends the fetched current value to the AIM-Spice part, which inputs the current into the designated place in the netlist and returns the output current, from the node being watched, to the SystemC part. While the AIM-Spice part is working the SystemC part fetches the next current value from the injection current module. The simulation then continues in this manner until the simulation end time is reached and the SystemC part presents the output currents to the user. This means that the AIM-Spice simulation part runs in parallel with the SystemC simulation, thus, for modern computer architectures, speeding up the simulation time. If the user does not wish to use an injection current module, the injection current can also be collected from a data file with pre-recorded current values.

4. Substrate model

The substrate model used is a 3D single substrate node model [11]. It combines a two-contact single node configuration [12] with a lateral triangulation technique, which is a modified Delaunay triangulation [13]. In practice, every node is given one resistance toward the bulk node and resistances are also placed between nodes using a “shortest path” technique. This means that the shortest path between two nodes is given a resistance, and if the next path investigated crosses an already existing resistance path, no resistance is placed on this new path. A modification was added to the triangulation technique to increase the accuracy of the noise coupling simulations. If four nodes are placed in a square mesh structure, i.e. with diagonals of the same length, the model sets resistances on both diagonals. An example of this modeling technique is depicted in Figure 4, where four nodes are put on a low-doped epi, high doped bulk substrate. Notice that no resistance is placed between a and c because it would cross the shorter path between b and d.

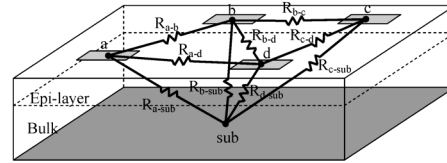


Figure 4. Example of a resistance net ready for simulation when using the 3D single substrate node model.

5. Verification

As mentioned in the introduction, device simulations have been performed to verify the results obtained with BeNoC. In this section, the device simulations are described.

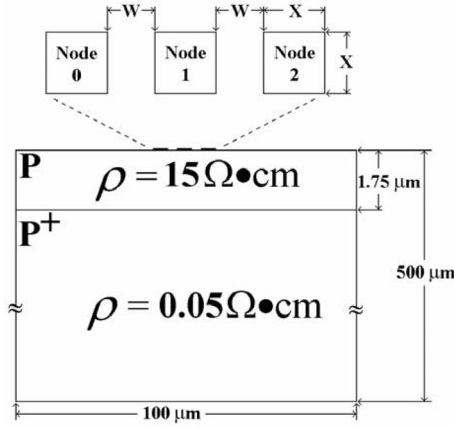


Figure 5. Substrate structure of the triple-node verification test case.

The substrate used in this work was heavily doped with a lightly doped epi-layer. This is usual for modern state-of-the-art CMOS technologies. The BeNoC simulation results of the SPACE generated resistor mesh representing the substrate were compared with the results using the ATLAS device simulator from Silvaco on a structure consisting of three substrate contacts (see Figure 5). Three square contacts were placed on the epi-layer surface. The simulations included injecting current into one contact and measuring the voltages on the other two. The resistance netlist of the same structure shown in Figure 5 was extracted by means of the SPACE resistance extractor. Then the resistance netlist was used in BeNoC and the same DC current sweep was implemented. The simulations were repeated for four different contact spacings. Both the results from the ATLAS simulator and the BeNoC simulator were evaluated.

6. Results

The triple-node verification test case from Figure 5 was simulated in the BeNoC simulator, where each of

the three nodes was encapsulated in a noise coupling wrapper. A current sweep was then injected into node 0 and the voltages from nodes 1 and 2 were plotted. This verified the functionality of the model and that the SystemC-to-AIM-Spice connection functions properly. The computational simulation time for this verification test case was under one second, which matches simulation times of behavioral mixed-signal modules in SystemC [14].

The accuracy of the BeNoC model was tested against the Atlas device simulation of the same structure and the same injection current. The size variables from Figure 5 were set to $W=2\mu\text{m}$ and $X=1\mu\text{m}$. The node width W was set to reflect a modern mixed-signal design process and the node distance X was set to a small enough distance to make the direct surface coupling relevant to the result so that part of the model is verified along with the substrate node coupling. The results are shown in Figure 6.

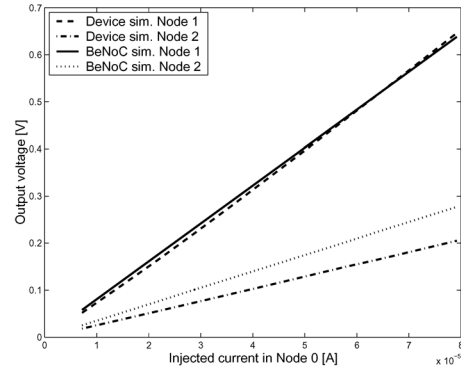


Figure 6. Output voltages for nodes 1 and 2 from Figure 5 in device simulation case and in BeNoC case.

The difference between the two simulations was then calculated as a measure of the BeNoC model accuracy against the device simulation. Some of the results of these calculations are displayed in Table 1 where the difference error in output voltage between the models is shown for three samples of injected current values. The moderately high linear error in Node 2 is partly a result of the Delaunay triangulation network reduction and partly a built-in error in the external resistance extraction models, which are targets for future work to enhance the overall simulation results.

Table 1. Difference between the BeNoC model and device simulation.

Injected current [μA]	Device		BeNoC		Error	
	Node 1 [V]	Node 2 [V]	Node 1 [V]	Node 2 [V]	Node 1 [V]	Node 2 [V]
14.40	0.107	0.037	0.116	0.050	8%	35%
43.20	0.340	0.111	0.348	0.151	2%	35%
79.20	0.646	0.205	0.638	0.277	1%	35%

The simulation described above was performed for four different node distances W and the tests show that the error between BeNoC and the device simulation increased when W was either very small or very large, which confirms errors in the resistance extraction. This is an issue that needs to be addressed in future work to enhance the accuracy of the model.

7. Conclusions

A SystemC extension has been presented that simulates substrate noise injection and coupling at the behavioral level. The SystemC model has an integrated AIM-Spice simulator, which calculates the on-chip current spread in the substrate equivalent resistive network generated by SPACE and a SystemC wrapper. To verify the accuracy of the model, device simulations have been performed on a triple-node case. The accuracy of these simulations is in the range of 1% to 35% compared to those for the device simulations, which are moderate errors in behavioral level simulations. The major source of error is identified as being in the resistance extraction, which needs to be improved. The high noise coupling simulation speed for the BeNoC model matches the behavioral SystemC simulation speed. This suggests that the presented method offers a promising method for the verification of substrate noise coupling throughout design refinements in SystemC of mixed signal systems.

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PAPER IV

Noise Injection Models for Behavioral level Noise Coupling Simulations in SystemC

P a p e r I V

Noise Injection Models for Behavioral level Noise Coupling Simulation

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ABSTRACT

In CMOS digital logic, there are two major noise sources that need to be considered. These are a circuit's power supply current and its noise current injected into the substrate of the circuit. This paper proposes a method for modeling and estimating the noise current injected into the substrate by capacitive coupling in digital circuits. The simplicity of the model and the reduction of details in the technology libraries facilitate behavioral level noise coupling simulation. The model is exemplified and evaluated for a simple NOT gate test case, for which the accuracy and simplicity of the models show great promise for simulation at the behavioral level.

Keywords

Injection models, behavioral level, noise coupling, BeNoC, SystemC.

1. INTRODUCTION

The development of mixed-signal systems and Systems on a Chip (SoC) has become a common architecture, and the future in system design is believed to be the integration of systems on a single chip. The advantages of this architecture are obvious, the systems can be made smaller, the high-inductive bond wires between chips are removed and the overall cost of systems can be reduced. However, the integration of analog and digital systems on a chip causes great problems with noise coupling, which is caused by switching currents that couples from digital logic to sensitive analog nodes [1].

The development of denser mixed-signal systems takes us to a situation where we need to worry about the on-chip noise coupling between functional blocks. These design developments are calling for new ways of simulating noise coupling since the design flow is getting faster and faster and there is virtually no room for long and costly design iterations. These iterations occur when the fabricated circuit does not work and noise coupling simulations have to be done at a layout level to localize the problematic areas on the chip. After this is done, the proper steps can be made to shield sensitive functional blocks in the design from noise coupling and then fabricate the circuit again. This costs a lot of time and money and can be avoided by getting an early indication where the problems occur. The problem thus lies in detecting if and where there might be a problem with noise coupling between analog and digital components as early as possible in the design flow.

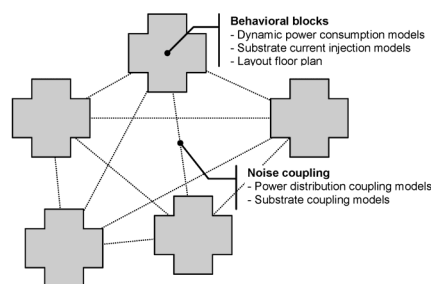


Figure 1. Schematic overview of behavioral noise coupling simulation.

The two major sources of on-chip noise coupling have been identified as being coupling over power distribution networks and coupling in the substrate [2]. To facilitate early noise coupling quantification through simulation these two sources and their coupling between blocks need to be captured. Figure 1 outlines the required models that need to be captured to enable high-level noise coupling simulation. For handling noise coupling over the power distribution network, models for dynamic power consumption of each block is needed and a model how this couples over the power distribution network [3]. The second effect, substrate noise coupling, noise coupling over the substrate has two sources of noise injection, one comes from the coupling of the power distribution network to the substrate and the other is the injection of noise currents from digital circuits [2]. Additionally, a high-level noise coupling simulation also requires a model for how the noise is distributed in the substrate.

There are a few examples, [4], [5] and [6], of high-level noise coupling simulation environments in the literature that solved the modeling problem described above in different ways. Charbon et al. [4] describe an approach for gate-level noise coupling. In this approach the substrate noise injection and dynamic power supply is characterized for each gate in a certain technology. Van Heijningen et al. also proposes a gate-level noise coupling simulation methodology, this one based on detecting switching events from VHDL. Lundgren et al. [6] presents a methodology for noise coupling simulation at behavioral level that is based on SystemC [7].

The gate-level models used in [4] and [5] are not appropriate to realize noise injection estimation in behavioral noise coupling simulation as described in [6]. In this paper we introduce a noise current injection model to behavioral level noise coupling simulation models. The idea is to only connect power distribution and ground to the injections models, which in turn estimates the current injected into the substrate and the current fed to the power distribution networks. The current injection models can then be connected to a behavioral level noise coupling model.

The paper is organized as follows; the next section describes a design case where the behavioral noise coupling simulation would be very beneficial. Section 3 describes the simulation environment that the proposed method is implemented in. Sections 4 and 5 describe the noise injection model and its application. Sections 6 and 7 present the experimental results and the drawn conclusions from these.

2. MOTIVATIONAL EXAMPLE

To see the relevance of any noise coupling simulation you need to have a design with very tightly integrated analog and digital components. An example of such a design is the photon counting pixel detector in [8]. The pixel detector is in reality used to extract x-ray pictures in "color". It is built up by a sensor chip bumped on a readout electronics chip. Now, the readout electronics needs to have highly integrated analog and digital components behind each pixel in the pixel array, where each pixel has a size of 50 μm .

The small chip area and the level of integration make substrate coupling highly relevant. The small area also makes it hard to use separate power distribution networks for analog and digital components since this would take up too much space. This fact makes power distribution noise coupling highly relevant.

3. BEHAVIORAL NC ENVIRONMENT

This section is thought to give the reader a background to the simulation application that the noise injection models are connected to.

The noise coupling application used is the Behavioral level Noise Coupling (BeNoC) simulation application developed at Mid Sweden University [9]. It is implemented in SystemC and also controls the AIM-Spice engine from SystemC [6]. The application incorporates both power distribution network noise coupling and substrate noise coupling and works as an add-on wrapper that encapsulates a component module. The wrapper adds ports and a current flow in and out of power distribution networks and substrate. The wrapper model is illustrated in Figure 2 and is further described in [10].

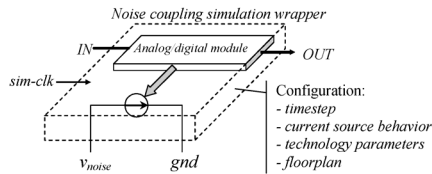


Figure 2. Wrapper model for the noise coupling simulation model BeNoC.

Each component module gets its own wrapper that, combined with a rough floorplan, generates a Spice netlist and starts the AIM-Spice simulator in parallel with the SystemC simulation. The AIM-Spice simulator then sends back the noise levels for each node simulated to the SystemC simulation part. The BeNoC simulation flow is illustrated in Figure 3 and further explained in [6].

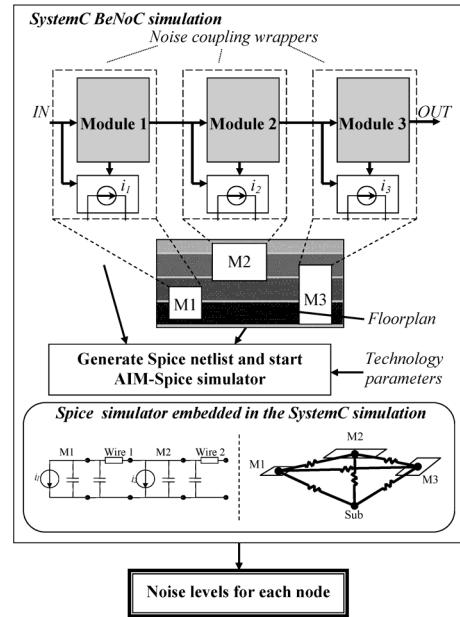


Figure 3. Behavioral level Noise Coupling (BeNoC) simulation flow.

The wrapper model needs an injection current that it sends to the substrate model and simulates the current spread in the substrate. The wrapper makes an estimate of the logic gates that is causing switching noise and makes a request to a file or module containing noise current injection values that it uses for simulation with the aid of a SystemC to AIM-Spice connection, sending values to the Spice engine which returns the current spread.

The models for noise injection will be devised as SystemC modules, one for each logic gate. The modules are connected to the incoming power distribution network and ground, and deliver injection currents when the modules are called by a noise coupling simulation wrapper. The noise injection models estimates the injection currents based on technology parameters and sends back current values to the wrapper. The wrapper is then able to simulate the current spread in the substrate and over the power distribution networks as it is designed for.

The role of the current injection model is to be an add-on to the BeNoC simulation application that makes simulation easier and

more general. An exact injection current does not need to be known by the designer anymore. The designer can focus on the functionality of the component modules.

4. NOISE INJECTION MODELING

Simulation of current injection at the behavioral level needs a reliable simulation application with an estimating current injection model. Since the simulation begins at such an early stage in the design flow, the accuracy of the model is not crucial. However, it needs to be accurate enough to enable the noise coupling application to give a pretty clear hint to where the noise coupling problems occur.

There are several injection mechanisms in substrate noise coupling that need to be considered:

First there is *impact ionization*, which basically yields a current flowing out of the bulk node of the transistor and into the substrate. This current is generated by fractions of carriers in the depleted region of a saturated transistor that gain enough energy to become “hot” [11]. They then scatter creating additional electron-hole pairs. The holes generated in the NMOS transistor are then swept to the substrate, forming the current into the substrate. Impact ionization is mostly just measured on the bulk node of the NMOS transistor, since the current out of the PMOS bulk node is at least one order of magnitude lower than that of the NMOS [12].

Capacitive coupling to the substrate is caused by voltage fluctuations in the source and drain of the MOS transistor which are coupled through the junction capacitances. There is also a capacitive coupling over the gate oxide via channel capacitances. These together form a current injected into the substrate [13].

Gate induced drain leakage (GIDL) occurs when there are high fields across the gate-drain overlap region. These form a deep-depletion layer in the drain and when the voltage drop across this layer is sufficient, the valence electrons start to tunnel between bands, resulting in the creation of holes, which are swept into the substrate [14].

The hot electrons that are not subjected to impact ionization are likely to release their excess energy by emitting a photon [15]. Electron-hole pairs can then be created when the photons are reabsorbed, causing a *photon induced current (PIC)* [16].

In addition to the capacitive coupling there will also be a *diode leakage current* in the junctions of the MOSFET’s source and drain, which are in actuality reverse biased diodes [13]. This current is then injected into the substrate.

From these five substrate injection mechanisms, it has been shown that the substrate currents caused by capacitive coupling and impact ionization are the dominant ones, in that order, and that capacitive coupling is relatively more important at high frequencies [12]. This is the motivation of targeting capacitive coupling injection in this paper.

The proposed current injection function represents the current that leaks into the substrate due to capacitive coupling in digital CMOS transistors during switching. As defined in the introduction, a behavioral noise coupling simulation needs an estimation of the power supply current i . Starting from this fact

one can state the targeted model for estimating the substrate injection current for a technology $\mathbf{T}$ and a block area A as

$$i_{inj, cap}(t) = f(i(t), \mathbf{T}, A). \quad (1)$$

The switching of a CMOS circuit can approximated as

$$u(t) = \frac{1}{C_{tot}} \int_{t_0}^{t+t_0} i(t) dt \quad (2)$$

for a 0→1 transition, with the initial and end conditions

$$u(t_0) = 0, u(t_0 + t_d) = V_{dd} \quad (3)$$

and

$$u(t) = V_{dd} - \frac{1}{C_{tot}} \int_t^{t+t_d} i(t) dt \quad (4)$$

for a 1→0 transition, with the initial and end conditions

$$u(t_0) = V_{dd}, u(t_0 + t_d) = 0. \quad (5)$$

From both cases we can derive the total switched capacitance in a certain logic gate as

$$C_{tot} = \frac{1}{V_{dd}} \int_{t_0}^{t_0+t_d} i(t) dt. \quad (6)$$

Equation (5) inserted into Equation (2) results in an expression for an output node

$$u(t) = \frac{1}{\frac{1}{V_{dd}} \int_{t_0}^{t_0+t_d} i(t) dt} \int_{t_0}^{t+t_0} i(t) dt. \quad (7)$$

From [1] the noise current from capacitive coupling injected into the substrate for an inverter can be written as

$$i_{inj, cap}(t) = kC_j \frac{\partial u_{source}}{\partial t}, \quad (8)$$

where k is a constant indicating the number of transistors in the area of each block. Equations (7) and (8) are combined to an equation for estimating the capacitive injection current

$$i_{inj, cap}(t) = \frac{kC_j}{\frac{1}{V_{dd}} \int_{t_0}^{t_0+t_d} i_{source}(t) dt} i_{source}(t). \quad (9)$$

Hence, we have an expression that fulfills the target function stated in Equation (1), where the formulated parameters are given by the technology with C_j , the power supply currents with i and t_d and the number of transistors in the area with k .

5. CASE STUDY AND ANALYSIS

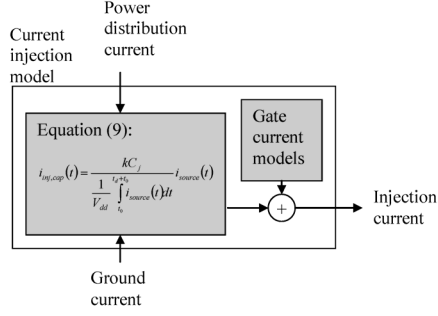


Figure 4. Schematic of the noise current injection model.

This section handles the analysis of the proposed noise current injection model. The inverter is taken as an example. To improve the level of accuracy for the model described in Equation (9), it could be extended with an estimating noise injection model from the gate, where there is capacitive coupling over the gate oxide and over the channel. Since the current behavior for an n-transistor and a p-transistor are different, there is one gate current estimation function for each type of transistor. They are combined to form an accurate model of the total gate current of a logic gate. In the case of an inverter, one p-transistor and one n-transistor gate current model are added together and, as shown in Figure 4, added to incoming power distribution and ground currents inserted into Equation (9).

To reduce the error in the final modeled injection current, the gate currents are modeled as differentiated voltage transitions. The error is reduced because the voltage is easier to model with accuracy than the current.

Now follows the work of extracting the noise injection function for the inverter, specifically. From Equation (9) it can be derived that the capacitive coupled noise injection current in an inverter is a sum of the source-to-substrate junction capacitance coupled currents of the two transistors multiplied with the junction capacitance. This yields the formula

$$i_{inj, cap}(t) = C_j \frac{\partial u_{sn}(t)}{\partial t} + C_j \frac{\partial u_{sp}(t)}{\partial t} = C_j \left(\frac{\partial u_{sn}(t)}{\partial t} + \frac{\partial u_{sp}(t)}{\partial t} \right) \quad (10)$$

Briaire et al. in [12] state that the gate electrode is also a part of the capacitive coupling and is coupled to the substrate through the gate oxide and channel capacitances. This means that the gate currents multiplied with capacitances from the gate oxide and the channel are added to Equation (10), forming the more accurate capacitive injection current

$$i_{inj, cap}(t) = C_j \left(\frac{\partial u_{sn}(t)}{\partial t} + \frac{\partial u_{sp}(t)}{\partial t} \right) + (C_{ox} + C_{ch}) \left(\frac{\partial u_{gn}(t)}{\partial t} + \frac{\partial u_{gp}(t)}{\partial t} \right) \quad (11)$$

The source currents can be input into the model as the power distribution current and the ground current. This leaves us to model the gate currents forming $i_{g, tot}$, so we model each of the n and p transistor gate currents as functions

$$\frac{\partial u_{gn, p}(t)}{\partial t} = \frac{\partial}{\partial t} \begin{cases} k_1 \cdot V_{DD} \cdot \text{sinc}(m_1 \cdot \frac{t}{t_{sample}}) & \text{for } 0 \leq t < t_1, \\ k_2 \cdot V_{DD} \cdot e^{-m_2 \cdot \frac{t-t_1}{t_{sample}}} - k_2 & \text{for } t_1 \leq t \leq t_2. \end{cases} \quad (12)$$

Here, m_1 and m_2 are delay constants depending on where in the cascade chain the inverter is, and k_1 and k_2 sets the amplitude and the sign depending on what transistor (p or n) is being simulated and depending on whether the transition of the transistor is positive or negative. As pointed out earlier, the currents are modeled as differentials of the voltage swings to enhance the accuracy.

As an investigation on whether the gate current model is needed at all, a further simplification was considered for the capacitive injection current, where the gate model is altogether replaced by a capacitance. This yields the equation

$$i_{inj, cap, simple}(t) \approx (C_{out+gate} + C_j) \left(\frac{\partial u_{s, tot}(t)}{\partial t} \right), \quad (13)$$

which excludes the need of Equation (12) but takes a loss in accuracy.

To ensure that the noise current injection models are valid they need to be verified, in this case against Spice simulation values. This will also reveal the level of accuracy the models deliver. The accuracy is not crucial since the models will be used at a behavioral level, but they should not be too far off from Spice values. Also, the simplifications made, neglecting the next cascaded gate and neglecting gate currents altogether, needs to be assessed for validity.

6. SIMULATION RESULTS

The noise injection model for the inverter example has been simulated and compared to Spice values. The logic gate in each verification case has been inserted between two logic gates of the same type to form a cascade connection. This ensures correct in- and out capacitances to and from the gate in simulation. To estimate the difference between the modeled injection currents and Spice generated injection currents, spectral analyses were made for the noise current simulations. The inverter simulation for the proposed model, with and without gate current estimations, and Spice is shown in Figure 5. The spectral analyses of the three curves are shown in Figure 6.

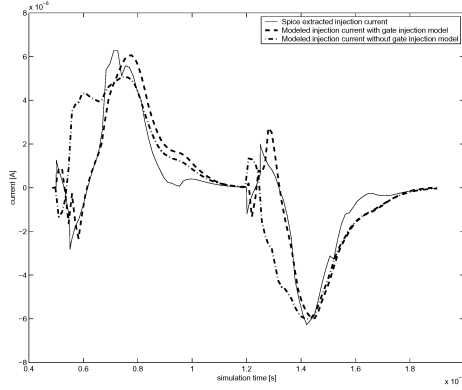


Figure 5. Transient analysis of the noise injection current of a NOT gate, modeled versus Spice.

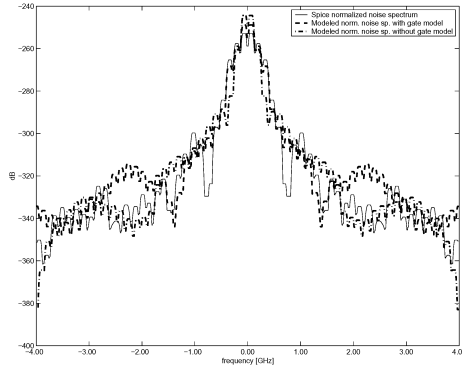


Figure 6. Spectral analysis of modeled and Spice injection current simulations from Figure 5.

In the transient analysis in Figure 5 the effects of the gate current simplification can be seen. For the model with gate current estimation, the major current spike gets a small delay and a phantom current can also be seen when the major spike is supposed to level out to zero. The further simplified model without gate current estimation has a lot more errors that are reflected in the low frequency part of the spectral analysis.

To further ensure the validity of the logic gate simulations, simulations were made with a different delay. In Figure 7 is shown a transient analysis of an inverter with a longer delay than the one in Figure 5.

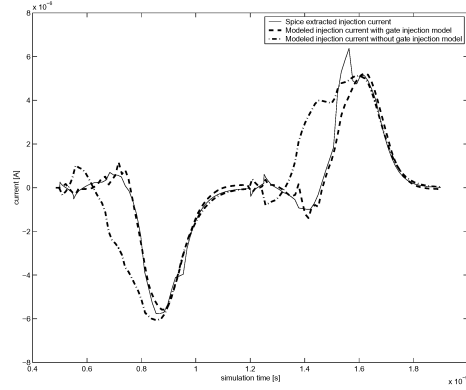


Figure 7. Transient analysis of the noise injection current of a NOT gate with longer delay than the one in Figure 5, modeled versus Spice.

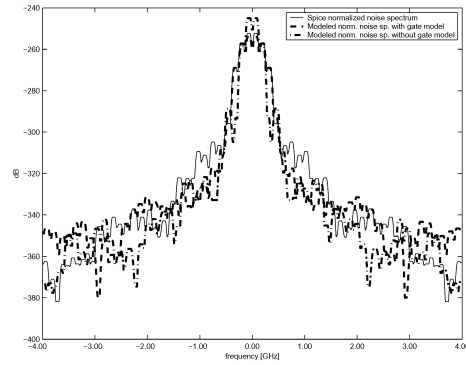


Figure 8. Spectral analysis of modeled and Spice injection current simulations from Figure 7.

The spectral analysis of the transient analysis in Figure 7 is shown in Figure 8. The simulations indicate that the models with gate current estimations get more accurate with larger delays, while the model without gate current estimations has about the same level of accuracy. This is expected since the differential of the gate voltages level out with larger delays which gives smaller errors in the final injection current of the model with gate current estimations.

The levels of accuracy show promise to make the noise current injection models well suited for noise coupling simulation at the behavioral level. The further simplified model could be well suited for architectural explorations, while the gate current estimation incorporated model is suited at behavioral and circuit level in the design flow.

7. CONCLUSIONS

A modeling technique for noise current injection suited for behavioral level noise coupling has been presented. The model has been analyzed and verified for a simple test case of an inverter. The model estimate the noise injection current from only the area, a few technology parameters and an estimate of the power supply current. The proposed modeling technique includes an injection current estimation function of the current injected due to the capacitive coupling over the gate oxide. The estimation model was compared to Spice simulations for accuracy and the accuracy indicates that the model is suited for architectural explorations in the design flow. The accuracy and simplicity of these models are very promising for the use with a behavioral level noise coupling simulation application.

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