A ZVS Flyback DC-DC Converter using Multilayered Coreless Printed-Circuit Board (PCB) Step-down Power Transformer

Hari Babu Kotte, Radhika Ambatipudi and Dr. Kent Bertilsson

***Abstract*—**The experimental and theoretical results of a ZVS (Zero Voltage Switching) isolated flyback DC-DC converter using multilayered coreless PCB step down 2:1 transformer are presented. The performance characteristics of the transformer are shown which are useful for the parameters extraction. The measured energy efficiency of the transformer is found to be more than 94% with the sinusoidal input voltage excitation. The designed flyback converter has been tested successfully upto the output power level of 10W, with a switching frequency in the range of 2.7MHz-4.3MHz. The input voltage of the converter is varied from 25V-40V DC. Frequency modulation technique is employed by maintaining constant off time to regulate the output voltage of the converter. The energy efficiency of the isolated flyback converter circuit under ZVS condition in the MHz frequency region is found to be approximately in the range of 72-84%. This paper gives the comparative results in terms of the energy efficiency of the hard switched and soft switched flyback converter in the MHz frequency region.

***Keywords*—**Coreless PCB step down transformer, DC-DC converter, Flyback, Hard Switched Converter, MHz frequency region, Multilayered PCB transformer, Zero Voltage Switching

I. Introduction

THE most essential unit required for all electronic devices is the Power Supply Unit (PSU). The requirement is to design a compact Switch Mode Power Supply (SMPS) to make it compatible with the majority of modern electronic equipment. The continuous efforts with regards to the improvement of switching devices such as MOSFETs and diodes has lead to the increased switching speeds of the power supplies. The switching devices, working at higher frequencies, causes the size of passive elements such as capacitors, inductors and transformers to be reduced and this results in the compact size, weight and the increased power density of the converter[1]. In addition, with the help of increased switching frequencies, the loop response of the power supply can be greatly enhanced. In the isolated converters such as flyback and forward, the switching frequencies are limited to less than 500 kHz because of the limitations of the existing core based transformers such as hysteresis and eddy current losses and also due to the increased switching losses of the Power MOSFET. Core based transformers have limitations such as magnetic saturation, core losses and, in addition, possess very bad high frequency characteristics because of the presence of magnetic cores [2]. In the late 1990s, research was concentrated on mitigating these limitations by using the coreless PCB transformers and their corresponding characteristics were presented in [3]. Recent investigation shows that the coreless PCB transformers can be used for signal and power transfer applications as mentioned in [4]. The transformers have however been limited to small voltage transformations as only the 1:1 transformers have shown sufficient efficiency. Here, the step-down transformer with a turn ratio of 2:1 have been developed enabling high frequency step down/up converters. The most widely used switch mode power supply topology for power applications of below 150W [5] is the flyback topology, which uses only a single magnetic element to act as a coupled inductor providing both the isolation and the energy storage. Its most attractive feature is that it requires no output inductors, whereas it is required by the remaining switching power supply topologies for filtering action. Thus, the consequent savings in both the cost and the size of the inductor forms a significant advantage in the flyback topology. The flyback converters appear in almost all modern low power equipments such as in computer monitors, laptop adapters, DVD players, set top boxes, telecom applications etc.,

In this paper, a low profile, low cost ZVS flyback power converter with a coreless step down (2:1) PCB transformer operated in MHz frequency region is presented.

II. Structure of Coreless PCB Step Down Power Transformer

A printed circuit board step down transformer is used and tested in the isolated flyback converter circuit for power transfer application. The primary and secondary windings of

Hari Babu Kotte is with the Department of Information Technology and Media, Mid Sweden University, SE-85170, Sundsvall, Sweden, (phone: +46-60148982; fax: +46-60148456; e-mail: Hari.Kotte@miun.se).

Radhika Ambatipudi is with the Mid Sweden University, Department of Information Technology and Media, SE-85170, Sundsvall, Sweden, e-mail: Radhika.Ambatipudi@miun.se).

Dr. Kent Bertilsson is with the Department of Information technology in Media, Mid Sweden University, and Sundsvall. Sweden, 85170(e-mail: Kent.Bertilsson@miun.se). He is also CEO and co-founder of SEPS Technologies AB, Storgatan 90, SE-85170, and Sundsvall, Sweden.

the transformers are manufactured as three spirals in a four layered PCB laminate. The primary windings are split into layers 1 and 3 and externally connected to layer 4 where the secondary winding is sandwiched in between the two primary windings.

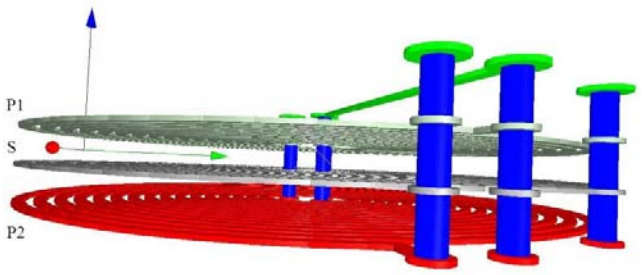


Fig.1 3D View of four layered 2:1 step down coreless PCB transformer

The PCB laminate of the transformer is FR4 material which has a breakdown voltage of 50kV/mm approximately [6]. The number of turns of the primary winding 'N_1' is 32 and for the secondary winding 'N_2' it is 16. The conductor width, separation and height are 0.6mm, 0.4mm and 70µm respectively. The outer diameter of the transformer is 36mm and the distance between the two consecutive layers of the PCB is 0.4mm.

III. Performance Characteristics of the Coreless PCB Step Down Power Transformer

In this section, the resistive, inductive and capacitive parameters of the transformer are presented. The performance characteristics such as the transfer function *H (f)* and the input impedance (Z_{in}) of the transformer with a resonant capacitor 'C_r' of 820pF at a load resistance of 50 Ohms are measured. The initial parameters such as the primary self inductance 'L_P', the secondary self inductance 'L_S' and the resistances of the windings are measured with the assistance of an HP4284A precision LCR meter at 1MHz frequency by open circuiting the opposite winding of the transformer. The preliminary primary and secondary leakage inductances of the transformers are obtained by using the Four-wire measuring method [7]. The leakage inductances of the flyback transformers, which are less than 1µH, are obtained by using the following expression

$$L_{lk} = \frac{50}{2\pi f}\frac{V_{dut}}{V_{50\Omega}} \quad (1)$$

where L_{lk} is the leakage Inductance, 'f' the excitation frequency, V_{dut}, the voltage across the device under test and $V_{50\Omega}$ is the voltage across the 50Ω resistor. The actual parameters such as the leakage-, self- and mutual-inductance of the transformers are obtained by fitting measurements of the transfer function and the input impedance into the high frequency model of the transformer shown in fig. 2. The above measured parameters are used as initial values that are

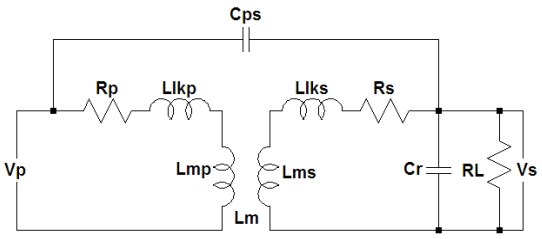


Fig.2. High frequency model of coreless PCB step down transformer

fine tuned to fit the measurement in the frequency range 1-10MHz and the final parameters are shown in table I. The measured and modelled performance characteristics of the transfer function *H (f)* and the input impedance *(Z_{in})* are shown in figs 3 and 4 respectively. The modelled performances are obtained from the high frequency equivalent model [3] with C_r of 820pF and R_L of 50Ω and are in very good agreement with the measured ones, indicating that both the model and the parameter values are correct.

TABLE I

MODELLED PARAMETERS OF THE DESIGNED STEP-DOWN TRANSFORMERS

PARAMETERS		Values
R_p(Ω)-DC	Primary winding resistance	1.10Ω
R_s(Ω)-*DC*	Secondary winding resistance	0.55Ω
L_p(µH)	Primary self inductance	17.23µH
L_s(µH)	Secondary self inductance	4.54µH
L_{lkp}(µH)	Leakage inductance of primary	0.46µH
L_{lks}(µH)	Leakage inductance of secondary	0.23µH
L_m(µH)	Mutual inductance	8.5µH
C_{ps}(pF)	Interwinding capacitance	68.0pF

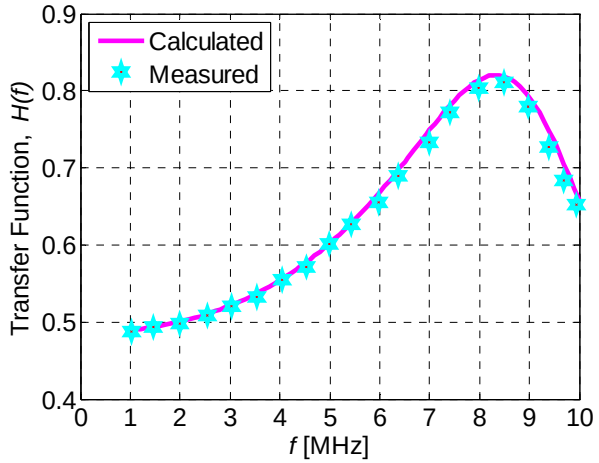


Fig. 3 Measured and modelled voltage gain of the coreless PCB step down transformer with C_r=820pF and R_L=50Ω

The intrawinding capacitances of the primary and secondary windings are very small and can be ignored in further analysis. From fig. 3 we can observe that the transfer function *H (f)* of the coreless PCB step down transformer has a resonance at a frequency just above 8MHz, where the magnitude of *H (f)* increases from 0.5 to 0.8.

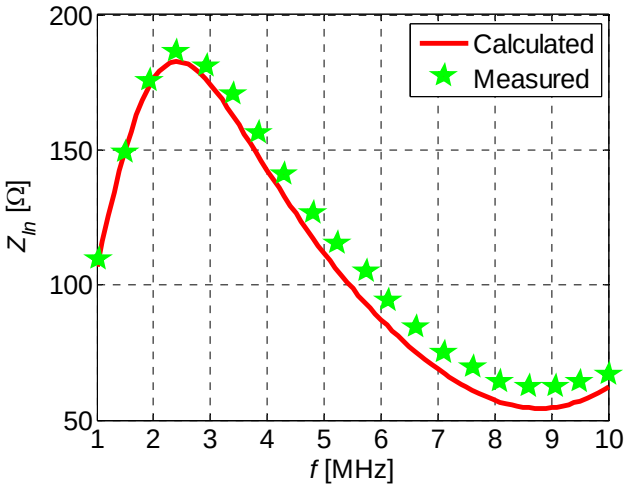


Fig. 4 Measured and modelled input impedance of the coreless PCB step down transformer with C_r=820pF and R_L=50 Ohms

The input impedance of the transformer is sufficiently high in the frequency range of 1.5-4MHz and it has a maximum of about 180Ω at a frequency of 2.4MHz.The input impedance phase angle *(φ)* of the transformer is illustrated in fig. 5 and is highly inductive in the frequency range of 1-2MHz. Hence, the optimal operating frequency region of the transformer is 1-2MHz [4] and the transformer has higher input impedance and a highly inductive nature. Above 8 MHz the transformer again becomes inductive. However, it cannot be used efficiently in that range due to the low input impedance and increased ac resistance of the windings.

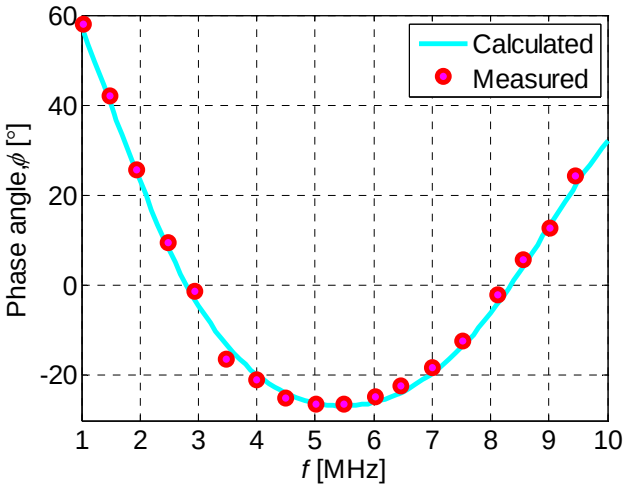


Fig.5. Measured and modelled input impedance phase angle of the coreless PCB step down transformer with Cr=820pF and R_L =50Ω

The resonant capacitor '*Cr*' across the secondary winding of the transformer as shown in fig. 2 plays an important role in these coreless PCB transformers as it provides the flexible operating frequency region. This transformer has a coupling coefficient of about 0.95.

Energy Efficiency: Since no magnetic core exists, no magnetic core losses are involved in these types of transformers. In addition, the radiation losses in these transformers are negligible compared to the conductor copper losses according to [4]. Therefore, the power loss in the primary and secondary windings of 2:1 step down transformer is given by the following equation.

$$P_{loss} = |i_p|^2 R_{ac}(p) + |i_s|^2 R_{ac}(s) \quad (2)$$

Where, i_p/i_s is the RMS current through the primary/secondary winding and R_{ac} *(p)*/R_{ac}*(s)* - Primary/secondary winding ac resistance. The input and output powers of these transformers are obtained from the following equations [3]

$$P_{in} = |V_p|^2 \, RE\left\{\frac{1}{Z_{in}}\right\} \quad (3)$$

$$P_{out} = \frac{|V_s|^2}{R_L} \quad (4)$$

And in this case, V_p is the RMS voltage across the primary winding, $Z_{in,}$ the input impedance of the transformer, V_s, the RMS voltage across the secondary winding and R_L is the Load Resistance. The measured energy efficiency of the transformer is given as

$$\eta_{meas} = \frac{P_{out}}{P_{in}} \times 100\% \quad (5)$$

The energy efficiency of the transformer is measured with a resonant capacitor of 820pF and at a load resistance of 50Ω. From fig.6 we can observe that the energy efficiency of the transformer is approximately 95% at a frequency of 2MHz.

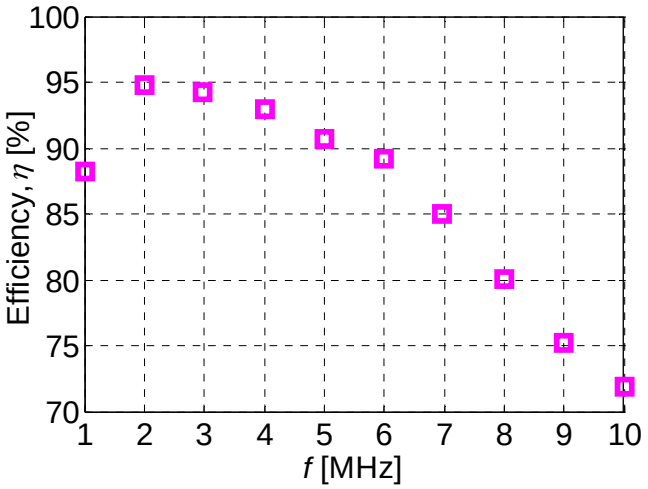


Fig. 6 Measured energy efficiency of the transformer with a resonant capacitor of 820pF and with R_L=50Ω

Since the energy efficiency of the designed coreless PCB step down power transformer is greater than 94%, it is used in the flyback converter circuit in order to evaluate the performance of the transformer in switching circuits.

IV. Zero Voltage Switching (ZVS) of the Converter

In case of hard switching converters, the rate of change of voltage (*dv/dt*) across the MOSFET and the rate of change of current (*di/dt*) flowing through the device are high and uncontrollable. The instantaneous power across the device is very high at turn-on and turn-off transition of the MOSFET which increases switching losses of converter. These results in the increased temperature of the converter, stress on the MOSFET and a higher cooling requirement. In addition, because of the high di/dt and dv/dt, there exists lot of EMI emissions from converter and reliability of the converter goes down. And also because of the increased turn-on and turn-off losses of hard switched converter the switching frequency is limited to lower frequencies and thus size of the converter increases. Passive snubbers are used in order to control high *di/dt* and *dv/dt* of the device and in this case the device losses are merely transferred to passive snubbers. This reduces the stress on the device at the cost of the energy efficiency of the converter.

There is a requirement to employ some of the soft switching techniques in order to eliminate the aforementioned limitations of hard switched converter. Therefore, in this converter one of the soft switching techniques known as zero voltage switching is employed in order to reduce switching losses of the converter. With the assistance of soft switching techniques, the devices stress can be reduced and it is possible to achieve low EMI emissions from the circuit, reduce the switching losses of the converter and there exists a possibility to improve the diode recovery. In case of ZVS, the switch is turned on when the drain source voltage across the MOSFET is zero which reduces the instantaneous power loss across the device to zero [8]. In general, ZVS can be achieved with the help of an external inductor and a capacitor which forms the resonant circuit. In case of hard switched converters, the parasitic capacitance and inductance increases the energy loss of the converter and also distracts the circuit performance. Here in soft switching converters, the unwanted parasitic capacitance and inductances prove to be advantageous in order to reach the soft switching conditions.

V. ZVS Flyback Converter Circuit with its Analytical and Experimental Results

The coreless PCB step down 2:1 power transformer is used in the flyback converter circuit as shown in fig. 7. The power MOSFET used in this circuit is ZXMN15A27K with V_{dsMax} of 150V and $R_{ds\ (on)}$ of 0.65Ω. The flyback diode of the converter is a STPS15L45CB schottky diode with a reverse blocking voltage capacity of 45V and the maximum forward average current rating of 15Amps.Here L_r and C_R form the resonant tank circuit in order to achieve ZVS condition. The resonant element L_r includes the transformer leakage inductance, parasitic wire inductances, external resonant inductor, lead inductances and C_R includes the output capacitance of the Mosfet, winding capacitances and the parasitic lead capacitances.

In case of ZVS flyback converter the characteristic impedance (Z_n), resonant frequency (f_r), normalized load resistance (r) and the voltage conversion ratio (M)[9] are given by following equations(9),(10),(11)and(12). These equations are utilized to calculate the theoretical values of the switching frequency of the flyback converter as well as the voltage stress on the mosfet in order to compare with the practical values.

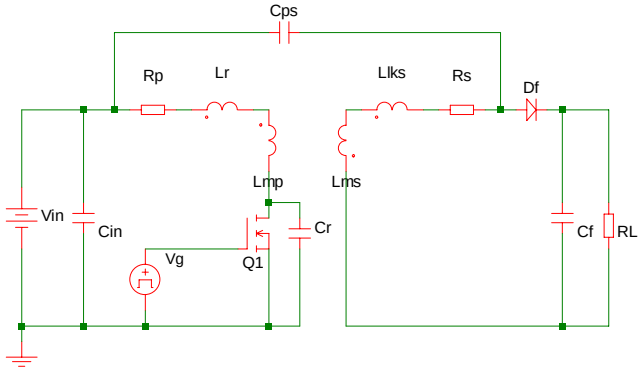


Fig. 7 ZVS flyback converter using coreless PCB step down transformer

$$Zn = \sqrt{\frac{Lr}{Cr}} \tag{6}$$

$$fr = \frac{1}{2\pi\sqrt{LrCr}} \tag{7}$$

$$r = \frac{Rl}{Zn} \tag{8}$$

$$M = \frac{Vout}{Vin} \tag{9}$$

Where,
R_l is the load resistance of the converter; V_{out}/V_{in} is the output/input voltage of the converter.
During resonant condition, the drain source voltage V_{ds} of the converter reaches the peak value and it is given as follows:

$$Vds\_\max = \mathrm{Im}\, Zn + Vin + NVout \tag{10}$$

Where '*Im*' is the magnetizing current of the transformer and '*N*' is the turns ratio of the transformer. To achieve the ZVS condition of the converter the following equation must be satisfied.

$$r \le \frac{M}{N} \tag{11}$$

The expression for the switching frequency f_{sw} of the ZVS flyback converter is given as

$$fsw = fr\left(\frac{2\pi}{(1+MN)\left[\alpha + \frac{rN}{2M} + \frac{M}{rN}(1-\cos\alpha)\right]}\right) \tag{12}$$

Where $$\alpha = \pi + \arcsin\left(\frac{rN}{M}\right) \tag{13}$$

The flyback converter was tested with the following specifications: Input supply voltage of the converter 25-40V DC with a nominal voltage of 32.5V.The output voltage of the converter is regulated at 13Volts for different input voltage conditions. The load resistance is in the range of 15-50Ω and converter has been tested within the frequency range of 2.7-4.3MHz. Here, the main switch Q1 is driven by the Mosfet driver LM5111-1M which is fed by 1.1ns resolution dsPIC microcontroller. The output capacitance of the mosfet '*Coss*' is 64.5pF at Vds=25V. The estimated total resonant capacitor 'C_R' of the circuit including the parasitic capacitance was 168pF. The leakage inductance of the transformer is 0.46µH which is a very low value to obtain the ZVS condition within the aforementioned specifications. Therefore, an external resonant inductor of 5.2µH is chosen so that the switching frequency of the converter falls within the specified range by forming a resonant tank circuit with the total resonant capacitor of 168pF.The theoretical characteristic impedance 'Z_n'(9) of the circuit is found to be 183.5Ω and the resonant frequency 'f_r'(10) of the circuit is 5.16MHz.

By varying the input voltage of the circuit at a given load of 30Ω the energy efficiency of the unregulated flyback converter under Hard Switched and ZVS condition are plotted as shown in fig.8.The energy efficiency of the converter is drastically improved by the ZVS condition when compared to hard switched condition at the same switching frequency.

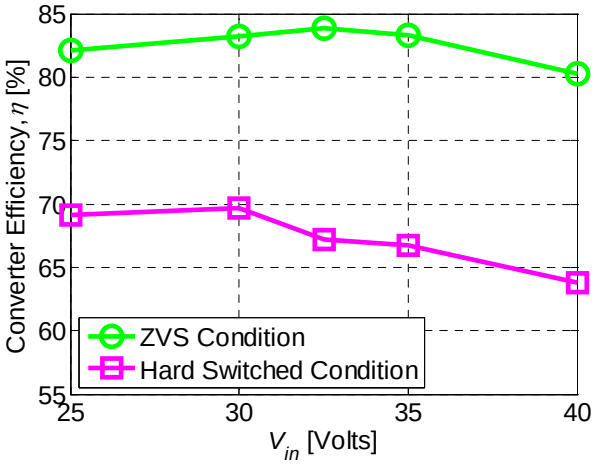


Fig.8 Measured energy efficiency of the unregulated converter under ZVS and Hard switched condition with a resistive load R_L of 30Ω.

We can observe that the efficiency of the ZVS flyback converter is maximum of 83.8% at the nominal input voltage of 32.5V whereas it is only 67% in case of hard switched converter. In both the cases, the energy efficiency is plotted at 50% duty cycle ratio. Under these conditions the theoretical (13) and practical values of the drain-source voltage of the ZVS flyback converter are determined and are illustrated as shown in fig.9.

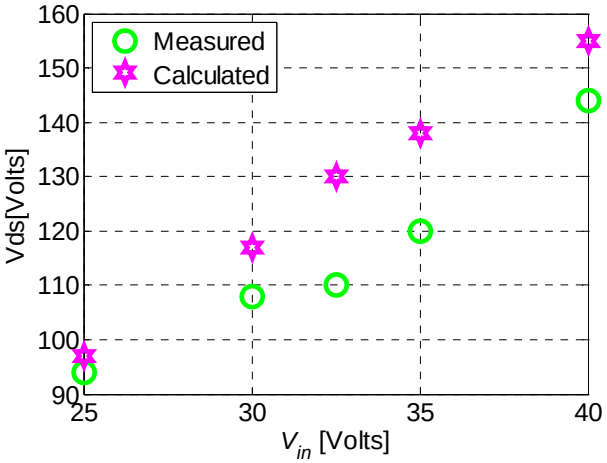


Fig. 9 Measured and Calculated Voltage stress on Mosfet under ZVS condition with a resistive load R_L of 30Ω.

The output voltage of the converter is also open loop regulated to 13Volts for different input voltage variations i.e., 25-40V with a load resistance of 30Ω. The constant off time control technique of frequency modulation is employed to regulate the output voltage. Here the output power of the converter is maintained to be 5.7Watts. The energy efficiency of the regulated converter is depicted in Fig.10. It can be observed that the energy efficiency of the converter is maximum at the nominal input voltage of 32.5V and gets reduced at lower and higher input voltages. At lower input

voltage of 25V, for maintaining the same output voltage it is required to increase the duty cycle ratio of the converter.

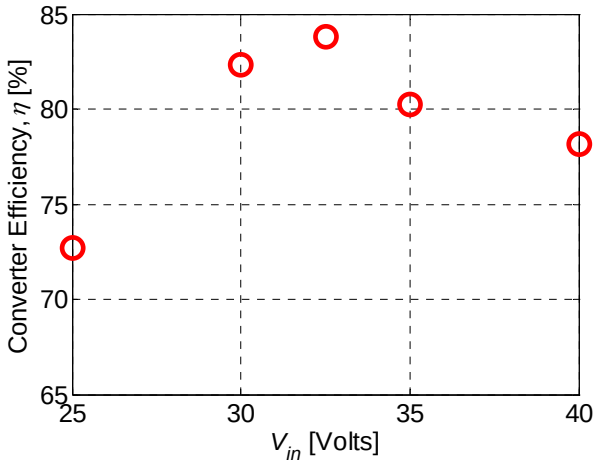


Fig. 10 Measured energy efficiency of the regulated converter with a resistive load R_L of 30Ω under ZVS condition.

This results in the increased input current of the converter which enhances the conduction losses of the Mosfet.Similarly, for maintaining the output voltage of the converter to be constant at higher input voltage of 40V, the switching frequency must be increased which increases the switching losses of the converter.The calculated and the measured switching frequency of the regulated converter are shown in fig.11. Here, as discussed earlier the measured switching frequency of the converter is minimum of about 2.8MHz at lower input voltage and maximum of 4.3MHz at higher input voltage. In all the cases, while determining the energy efficiency of the converter, no consideration is given to the gate drive power consumption.

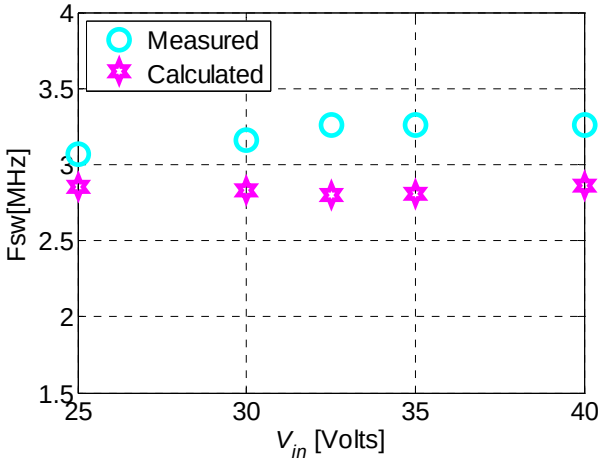


Fig.11 Measured and calculated switching frequency of the regulated converter circuit with a resistive load R_L of 30Ω under ZVS condition

The converter efficiency was measured with different load resistances ranging from 15-50Ω at a switching frequency of 3.26MHz with an input voltage of 35V shown in fig. 12. The maximum energy efficiency of the converter is observed to be approximately 84% for the load resistance of 30Ω.

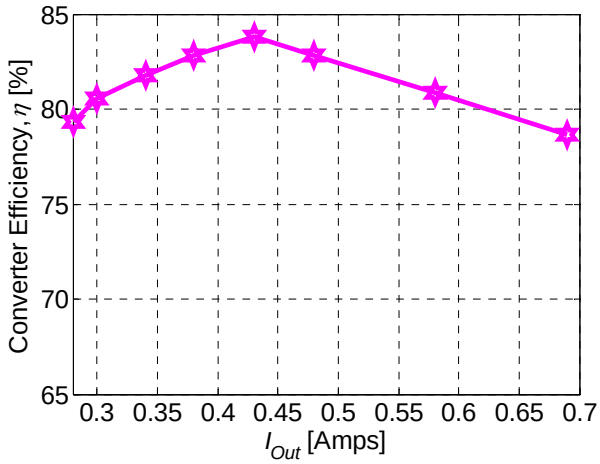


Fig.12 Measured efficiency of the flyback converter circuit with various load resistances

In this case, the output voltage of the converter obtained falls within the range of 10-14Volts at a 50% duty cycle ratio under ZVS condition. With the assistance of frequency modulation, as discussed at an earlier stage, the output voltage of the converter can be regulated.

The waveforms were captured when the converter circuit was operated at R_{L_max}=50Ω and R_{L_min}=15Ω and are illustrated in fig. 13 and fig. 14 respectively. The input voltage fed to the converter is of 35V with 50% duty cycle ratio. Fig.13 and fig.14 show the gate to source voltage (V_{gs}) applied to the switch 'Q1', drain to source voltage (V_{ds}) of the switch 'Q1' and the output voltage (V_{out}) of the converter circuit. In fig. 9 and 10 it can be observed from the drain source voltage that the ZVS condition is achieved at a frequency of about 3.26MHz.

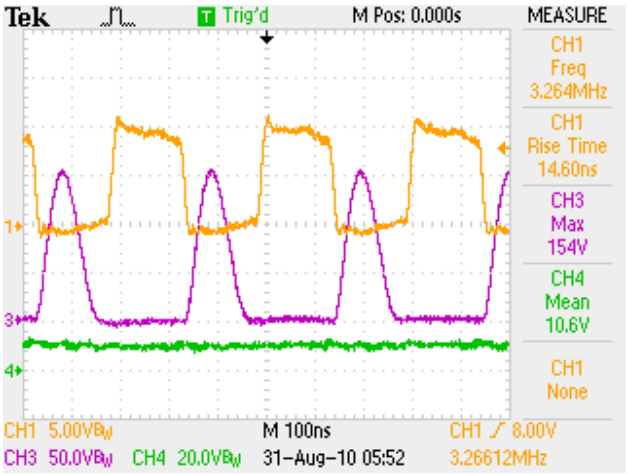


Fig. 13 Measured waveforms with R_L=15Ω. CH1 – V_{gs} (5V/div), CH3 – V_{ds} (50V/div), CH4 – V_{out} (20V/div)

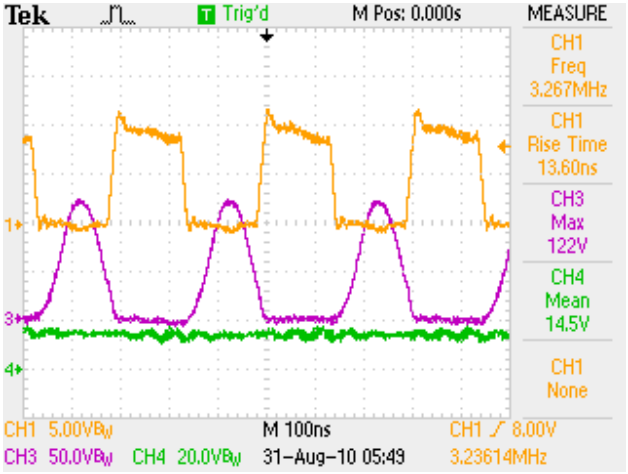


Fig. 14 Measured waveforms with R_L=50Ω. CH1 – V_{gs} (5V/div), CH3 – V_{ds} (50V/div), CH4 – V_{out} (20V/div)

The corresponding magnitude of the maximum drain source voltage is observed to be 154V and 122V respectively for minimum and maximum load s considered. It can be observed that as the load resistance is increased further beyond R_{L_max}, the circuit is losing the property of ZVS condition.

VI. Loss Estimation of the ZVS Flyback Converter

The loss estimation of the transformer in the converter has been carried at an input voltage of 40Volts with the resistive load of 30Ω by maintaining the ZVS condition of the circuit. Under these conditions the input power level of the converter is 12.32W and the corresponding output power is 10.05 W with a total power loss of 2.27W. The measured primary and secondary RMS currents of the transformer in the flyback converter are 0.364 and 0.701 amp respectively. The winding resistance of the transformer increases with frequency, starting from the DC resistance value, due to the skin effect. From the dc resistance of the transformer given in table I, the ac resistances are calculated with the following equation [10] by approximating it to circular spiral inductor.

$$R_{ac} = \frac{R_{dc} h}{\delta(1-\exp(-h/\delta))} \quad (17)$$

Where,

R_{dc} - DC resistance of the winding
h - Height of the conductor
δ - Skin depth

The calculated ac resistances of the primary/secondary windings of the transformer at that particular frequency of 3.45MHz are 2.51/1.25 Ω respectively. Therefore, the corresponding conductor losses of the transformer are obtained from (5) as 0.947W. According to antenna theory, the radiated power from the coreless transformer [3] is calculated by using the following equation.

$$P = 160\pi^6 I_o^2 \left(\frac{af_c}{c}\right)^4 \quad (18)$$

Where,
'*Io*' is the RMS current flowing through the winding, '*a*' /'f_c' is the radius/operating frequency of the transformer and 'c' is velocity of light. As mentioned above, the RMS value of the secondary current through transformer is 0.701amp and radius of the outermost turn is 18mm. The calculated radiated power for the outermost loop of the transformer is 0.138nW and the total averaged radiated power of the transformer including remaining loops is therefore negligible which shows that there are no significant EMI emissions from the transformer. The remaining losses of the converter are shared by the other components such as the ZXMN15A27K *(Q1)* and the schottky diode STPS15L45CB *(Df)*.For this particular load the temperature across the transformer and the power converter circuit excluding MOSFET driver, are measured with the assistance of an IR thermal camera and the results are depicted in fig. 15 and fig. 16 respectively.
From the temperature profiles and estimated losses of the transformer, we can say that the transformer losses are less when compared to the circuit losses of the converter.

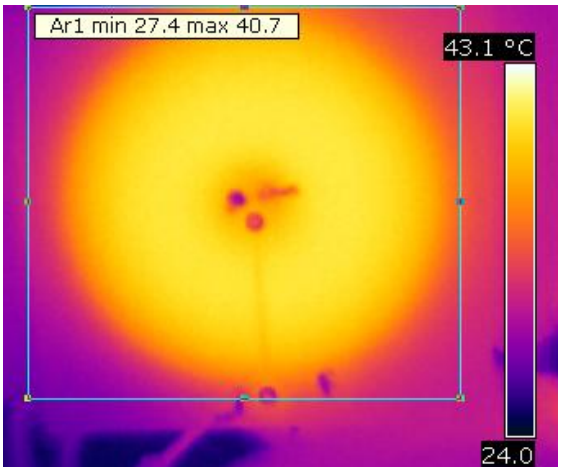


Fig.15 Measured temperature of the transformer in the flyback converter circuit

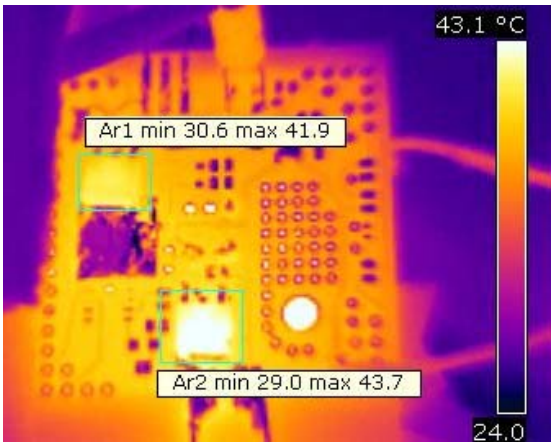


Fig.16 Measured temperature of the flyback converter circuit excluding the transformer with Ar1 - Area of the Switch ZXMN15A27K (Q1), Ar2 - Area of the schottky diode STPS15L45CB.

VII. CONCLUSIONS

A low profile, low cost ZVS flyback converter using a multilayered coreless PCB step down transformer operating in the MHz frequency range has been successfully demonstrated. This converter has been tested up to the output power level of 10W.The optimal switching frequencies of the converter in order to achieve higher efficiencies are determined analytically. The ZVS technique is incorporated into the flyback circuit in order to minimize the converter losses, EMI emissions from the circuit by reducing the di/dt and dv/dt. Under this ZVS condition for the converter circuit, the maximum energy efficiency of the converter obtained is approximately 84%. It can be concluded that there is a lot of improvement in terms of energy efficiency in ZVS converter when compared to hard switched flyback converter. The highest efficiency reported in the isolated topology operating in MHz frequency region is within the range of 70-80% in the forward converter [11] by using the two layered 14:10 transformer. In our case, by using the multilayered coreless transformer the maximum energy efficiency of the regulated converter is about 84%. This work provides a significant step in increasing the switching frequency to the MHz region with the help of multilayered step-down coreless pcb transformer for isolated DC/DC converters, enabling smaller and more compact designs to be considered in the future. The transformer technology works efficiently up to at least the tested input power level of 12.32W and here in this case the switching devices are the main limitations for further development. The power level of the design can be increased with improved thermal management. The output voltage of the converter for varied input voltage is regulated by using the constant off time frequency modulation technique. From the experimental analysis it can be concluded that a high frequency isolated switch mode power supply operating in the MHz region can be designed by using these multilayered coreless PCB step down transformers. These coreless PCB step down power transformers plays an important role where there is a tight restrictions on the height of the converter.

ACKNOWLEDGMENT

The authors would like to thank VINNOVA, The Swedish Energy Agency and European Union for their financial support.

REFERENCES

[1] Wong Fu Keung, “High Frequency transformers for switch mode power supplies’’ Griffith University, 2004
[2] Li Rulai and Zhu Yisheng “The structure and Analysis of Coreless printed Circuit Board Transformers ’’, 2003, IEEE, ISBN: 0-7803-7831-8
[3] S.C.Tang, S.Y.R .Hui and H. Chung, “Coreless Printed Circuit Board (PCB) Transformers –Fundamental characteristics and application potential ’’, ISSN 1049-3654, vol 11, No.3, December 2000
[4] Hui,S.Y.R, Tang,S.C., and Chung.H., “Coreless printed-circuit-board(PCB) transformers for signal and energy transfer ’’,Electron.Lett.,1998,34,(11),pp.1052-1054
[5] Abraham I. Pressman, ‘Switching Power Supply Design’2nd Edition, McGraw-Hill,pp.105
[6] C.F.Coombs, ‘Printed Circuits handbooks’ 5th Edition, McGraw-Hill, August 27, 2001
[7] Alex Van den Bossche and Vencislav Cekov Valchev, ‘Inductors and Transformers for Power Electronics’1st Edition, CRC Press,March24,2005
[8] Robert W .Erickson, ‘Fundamentals of Power Electronics’2nd Edition, Springer International Edition, pp.505.
[9] Wojciech A. Tabisz, Pawel M. Gradzki and Fred C.Y.Lee, “Zero-Voltage-Switched Quasi-Resonant Buck and Flyback Converters-Experimental Results at 10MHz’’ IEEE transactions on power Electronics,vol.4,No.2,April 1989.
[10] Heng-Ming Hsu, “Effective series-resistance model of spiral inductors”, Microwave and Optical technology letters, vol.46, No.2, July 20 2005.
[11] Sun-Min Hwang and Tae-Young Ahn, ‘A ZVS forward DC-DC Converter using Coreless PCB transformer and Inductor’2001.

Comparative Results of GaN and Si MOSFET in a ZVS Flyback Converter using Multilayered Coreless Printed Circuit Board Step-Down Transformer

Hari Babu Kotte* and Radhika Ambatipudi
Department of Information Technology and Media
Mid Sweden University
Holmgatan 10,Sundsvall,85170,Sweden
{Hari.Kotte & Radhika.Ambatipudi}@miun.se

Kent Bertilsson
Department of Information Technology and Media
Mid Sweden University/SEPS Technologies AB
Holmgatan 10,Sundsvall,85170,Sweden
Kent.Bertilsson@miun.se

***Abstract* - The aim of this paper is to compare two different material MOSFETs performance namely *GaN* (Gallium Nitride) and conventional *Si* (Silicon) in Zero Voltage Switching (ZVS) flyback converter circuit with Coreless PCB step down transformers. The switching frequency of the regulated converter is in the range of 3.2-5MHz. In high frequency circuits, proper selection of MOSFETs is required in order to have low gate drive power consumption so that high energy efficiency of the converter can be achieved. Even though *Si* MOSFET has already known for its popularity in low to medium power converters and high frequency applications, *GaN* MOSFET device could produce better results. This can be done by reducing the total switching loss, conduction loss because of its low $R_{ds\text{-}on}$ and gate drive power consumption of the converter as a result of low gate charge, Q_g. From the experimental results, it can be observed that *GaN* MOSFET can produce higher energy savings including gate drive power by gaining approximately 8%-10% efficiency compared to its counterpart, *Si* MOSFET in a regulated 45-15V isolated DC-DC converter.**

Index Terms –Coreless Printed Circuit Board (PCB) step down power transformer, DC-DC Converter, GaN MOSFET, MHz frequency region, ZVS flyback converter.

I. INTRODUCTION

Power Supply Unit (PSU) is the most essential unit required for all the electronic devices. There is a continuous effort in research in order to improve the power density and the energy efficiency of the Switch Mode Power Supplies (SMPS) to make them compatible with the majority of modern electronic equipment. For this, lot of progress has been made in recent years in the switching devices such as MOSFETs and diodes which resulted into the increased switching speeds of the power supplies. The converter circuit operated at higher frequencies makes it possible to reduce the size of the energy storage elements such as capacitors, inductors and transformers which in turn results in the compact size, weight, volume and the increased power density of the converter [1]. By employing the traditional *Si* MOSFET, the switching losses of the converter gets increased in MHz frequency region of 1-5MHz range. The gate charge, Q_g of the *Si* MOSFET at its respective operating voltage is high which increases the gate drive power consumption. Then the overall energy efficiency of the converter with the traditional *Si* MOSFET goes down. Therefore, in order to overcome the drawbacks of the traditional *Si* MOSFET at higher switching frequencies, there is a tremendous research going on in order to introduce the new materials and structures of the semiconductor devices. In this process a new material *GaN* with the lateral structure having the better switching characteristics, high conductivity [2] is introduced. *GaN* material possesses high critical electric field of 3.3MV/cm [3] which is much higher than for *Si* material whose electric field is just 0.3MV/cm [4]. This property enables GaN device to withstand higher drain source voltage with low effect on its on state resistance, R_{ds_on}

In this paper, recently introduced commercially available *GaN* MOSFET is evaluated at MHz frequency region in ZVS flyback converter by using the multilayered coreless printed circuit board transformers. The comparative results of the converter with *GaN* and traditional *Si* MOSFET are presented under different conditions.

II. CORELESS PCB STEP DOWN POWER TRANSFORMER

As the core based transformers cannot be utilized in the high frequency converters operating in 1-5MHz because of the increased core losses, multilayered coreless PCB transformers for step down applications were designed. The designed 2:1 step down power transformer operated in MHz frequency region is employed in the ZVS flyback converter circuit. These transformers are highly energy efficient and can be utilized in the power transfer applications as quoted in [5]. According to antenna theory, this transformer is not considered as a good antenna/receiver and hence the radiated power emitted from these transformers is negligible [6]. The structure of this transformer is in such a way that the primary and secondary windings of the transformer are manufactured as three spirals in a four layered FR4 PCB laminate. Here, primary windings are in the layers 1 and 3 and are externally connected with the help of 4th layer where the secondary winding is in between two primary windings [5]. The number of turns of the primary winding 'N_1' is 32 and for the secondary winding 'N_2' it is 16.

978-1-4244-9162-9/10/$26.00 ©2010 IEEE

The modeled parameters such as self/leakage inductance of the primary/secondary winding of the transformer [5], [7] are 17.23μH/0.46μH and 4.54μH/0.23μH respectively. Also, the primary/secondary winding resistance of the transformer is 1.1Ω/0.55Ω and has an interwinding capacitance of 68pF.

III. Comparison of GaN and Si MOSFET Parameters

In the current ZVS flyback converter the two MOSFETs considered are of *GaN* (EPC1012) and *Si* (IRFR220PBF) with V_{dsMax} of 200V. The physical dimensions of these devices are illustrated in Fig. 1 and their packages are of Land Grid Array (LGA) and DPAK respectively.

Fig.1 Size comparison of 200V *Si* (DPAK) –left and *GaN* (LGA) - right enhancement mode MOSFET

The continuous drain current I_d of *GaN* and *Si* at ambient temperature is 3A and 4.8A respectively. The on-state resistance R_{ds_on} of *GaN* is 100mΩ where as it is 800mΩ for the *Si* MOSFET in their respective V_{gs} and I_d conditions. The total gate charge 'Q_g' is 1.9nC and 14nC for the *GaN* and *Si* MOSFET at V_{gs} of 5Volts and 10Volts respectively and their corresponding typical reverse recovery charge are Zero and 0.91nC. The low on-state resistance of *GaN* is obtained because of the high electron mobility and the low temperature co-efficient. The lateral device structure and majority carrier diode of *GaN* also resulted in low gate charge and zero reverse recovery charge for the *GaN* MOSFET [8]. These features of *GaN* MOSFET provide the scope to operate them at higher switching frequencies which is highly desirable in high speed SMPS. The reverse transfer capacitance of *GaN* MOSFET is only 7.5pF where as it is 30pF for the *Si* MOSFET. The low transfer capacitance of *GaN* enables it to have fast voltage switching capability compared to *Si* MOSFET due to the reduced Miller effect. In the current high frequency switching converter application it is important to choose a proper MOSFET in order to reduce the system losses. Since, there exists a trade-off between the on-state resistance (R_{ds_on}) and the gate charge (Q_g) of the MOSFET a parameter known as Figure of Merit (FOM) [9] is helpful in order to choose a low loss switching device for the high speed converter. FOM of the *GaN* and *Si* MOSFET can be calculated by using the following equation (1)

$$FOM(Vgs,Vds) = Rds\_on(Vgs,Vds) \times Qg(Vgs;Vds) \quad (1)$$

FOM of *GaN* device is approximately 1.33 which is much lower than FOM of the *Si* MOSFET which is of about 31.3. These are calculated at their corresponding optimal operating regions.

IV. Experimental results

The ZVS flyback converter with *GaN* and *Si* MOSFET was tested with the following specifications: Input supply voltage range of the converter is 30-60V DC with a nominal voltage of 45V. The output voltage of the converter in both the cases is regulated to 15V for input voltage and load changes. The load resistance considered is in the range of 30-60Ω and converter has been tested within the frequency range of 3.2-5MHz. Here, both the MOSFETs are driven by the MOSFET driver LM5111-1M which is fed by 1.04ns resolution dsPIC33fj06GS502 microcontroller. In both the cases, the total resonant capacitor 'C_r' of the circuit including the drain source capacitance of the MOSFET and parasitic capacitance was estimated and found to be approximately 80pF. Here, the leakage inductance of the transformer is 0.46μH which is not sufficient to operate the converter in ZVS region. Hence, an external resonant inductor of 5.2μH is included in series with the leakage inductance and therefore the operating frequency of the converter is within desired range by forming a resonant tank circuit with the total resonant capacitor of 80pF. The characteristic impedance (2) and the resonant frequency (3) of the circuit are calculated [7], [10] as follows:

$$Zn = \sqrt{\frac{Lr}{Cr}} \quad (2)$$

$$fr = \frac{1}{2\pi\sqrt{LrCr}} \quad (3)$$

Where,

L_r – total resonant inductor including L_{lkp}
Cr – total resonant capacitor

The calculated characteristic impedance 'Z_n' of the circuit is found to be 284Ω and the resonant frequency 'f_r' of the circuit is 8MHz.

The measured energy efficiency of the unregulated converter with *GaN* and *Si* MOSFETs with the variation of input voltage is illustrated in Fig 2. Here, the duty cycle ratio considered is of 50% and the converter is operated in ZVS condition with load resistance of 30Ω.

From Fig.2 it can be observed that the maximum energy efficiency of the converter including gate drive power consumption with *GaN* MOSFET is 82.5% and with *Si* MOSFET it is 74.2% at the nominal input voltage of 45V. The output power level of the converter at the maximum input voltage of 60V in both the cases is approximately 12Watts.

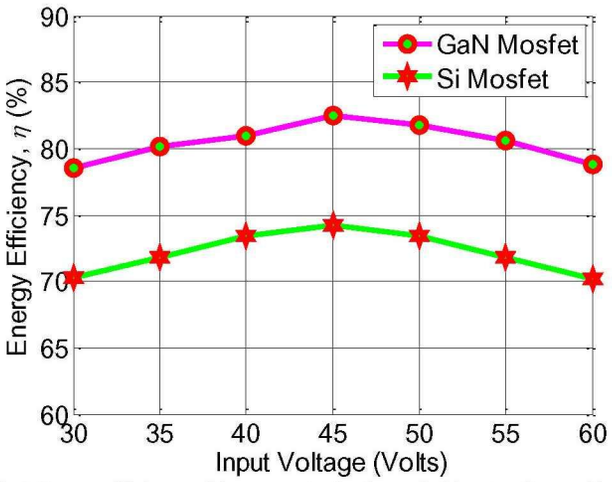


Fig.2 Energy efficiency of the converter for the varied input voltage with GaN and Si MOSFETs

The energy efficiency of the regulated converter with respect to input voltage variation is depicted in Fig 3. The output voltage of the converter is regulated to 15Volts within ± 1% change for input voltage variations i.e., 30-60V with a load resistance of 30Ω. In order to regulate the output voltage, the constant off time control technique of frequency modulation [7] is employed. The energy efficiency of the converter is higher with *GaN* when compared to *Si* MOSFET. While considering the efficiency of the converter, gate drive power consumption is taken into account. Here, the theoretical power consumed by the MOSFET driver [11] is given as

$$Pgate = Vg \times fsw \times Qg \tag{4}$$

Where,

V_g - Gate voltage
f_{sw} - Switching Frequency of the MOSFET
Q_g - Total gate charge of the MOSFET

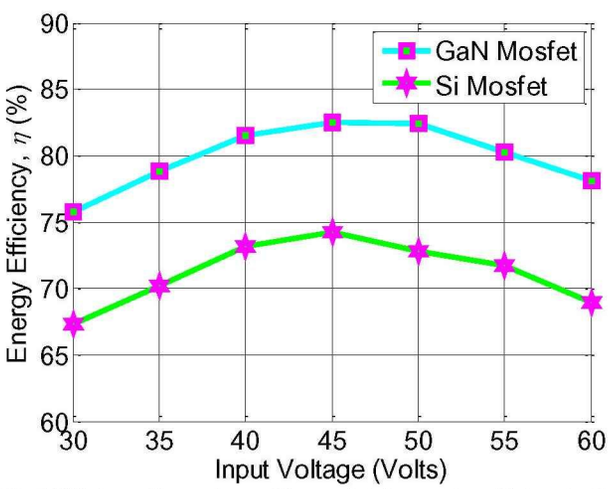


Fig.3 Efficiency Comparison of the regulated converter with input voltage variation

While determining the gate drive power with *GaN* and *Si* MOSFET, the theoretical and practical power consumed by the driver is given as in Table I. In this case, the gate drive power is determined at the worst case i.e., at maximum switching frequency of the converter at 5MHz and at an input voltage of the converter of 60Volts.

TABLE I
GATE DRIVE POWER CONSUMPTION OF CONVERTER WITH TWO MOSFETS

Device	Theoretical and Practical gate drive power consumption				
	V_{gs}(V)	Q_g(nC)	f_{sw}(MHz)	P_{gate}(Watts) Theoretical	P_{gate}(Watts) Practical
GaN	5	1.9	5	0.04	0.05
Si	10	14	5	0.50	0.58

From Table I it is evident that the gate drive power consumption of the converter with *GaN* MOSFET is very low when compared with *Si* MOSFET at their respective optimal operating regions. This gate drive power consumption difference has an impact on the energy efficiency of the converter apart from the conduction and switching losses of the MOSFET which can be observed in the Fig.3. The conduction (static) losses are higher in the converter with *Si* MOSFET because its R_{ds_on} is almost 8 times higher when compared to *GaN* MOSFET. We can observe that the maximum energy efficiency is observed at nominal voltage and it gets reduced at lower input voltages because of increased conduction losses and at higher input voltages because of increased switching losses [10].

The energy efficiency of the converter is also measured while the load resistance is varied from 30-60Ω and it is illustrated in Fig. 4. Here, the input voltage considered is of 45V and the output voltage is regulated to 15Volts with ± 1% tolerance band. In both the cases, the converter is operated in ZVS condition and it ceases to follow this condition as the load resistance increases.

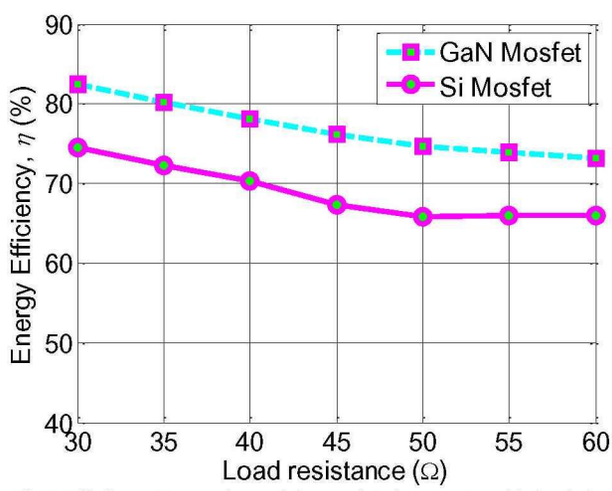


Fig.4 Efficiency Comparison of the regulated converter with load change

At the light load condition i.e., with R_L of 60Ω, the waveforms were captured for the converter circuit with GaN MOSFET and shown in Fig. 5.

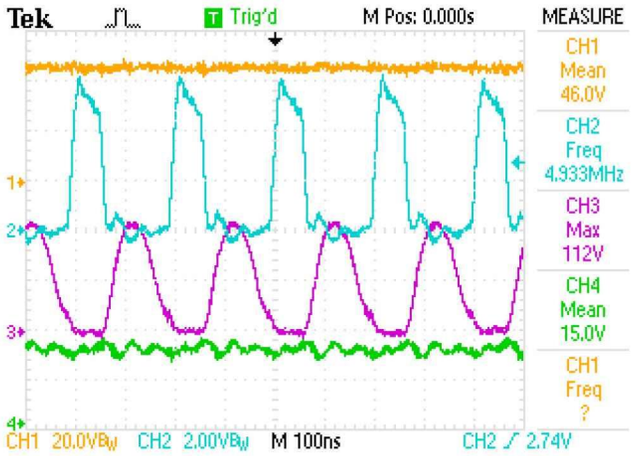


Fig.5 Measured waveforms with R_L=60Ω. CH1 – V_{in_nom} (20V/div), CH2 – V_{gs} (2V/div), CH3 – V_{ds} (50V/div), CH4 – V_{out} (15V/div)

Fig.5 shows the nominal input voltage V_{in_nom} fed to the converter, gate to source voltage V_{gs}, drain source voltage V_{ds} of the MOSFET and the output voltage V_{out} of the converter. In this case it can be observed that the converter has lost ZVS condition.

The *GaN* MOSFET utilized in this converter costs about 2.62$/unit whereas for *Si* MOSFET it is about 0.95$/unit. But these exceptional features such as low switching loss, conduction loss and low gate drive power consumption can be only obtained by utilizing *GaN* MOSFET together with Coreless PCB step down/up power transformers which is beneficial for the future generation ultra low profile converters.

CONCLUSIONS

A comparative result of ZVS flyback converter with *GaN* and *Si* MOSFETs operating in MHz frequency region (3-5MHz) by using coreless PCB step-down power transformers has been successfully demonstrated. FOM is calculated for both the *GaN* and *Si* devices. It is found that FOM of *GaN* MOSFET is very low compared to *Si* MOSFET. For the same output power the energy efficiency of the converter with *GaN* MOSFET is 8-10% higher than the *Si* MOSFET. In case of the converter with *GaN* MOSFET, the gate drive power consumption is approximately reduced by 10 times when compared to the converter with *Si* MOSFET at an operating switching frequency of 5MHz. Also because of the low R_{ds_on} of the *GaN* MOSFET the conduction losses of the converter with *GaN* is lower compared to its counterpart *Si* MOSFET. From FOM point of view and from the experimental analysis it can be concluded that *GaN* device is a better choice in high frequency SMPS. The combination of coreless PCB step-down power transformers and the *GaN* switching devices provides the scope for the stringent height and low profile dc-dc converters because of their operating capability in MHz frequency region.

ACKNOWLEDGMENT

The authors would like to thank Mid Sweden University, VINNOVA, The Swedish Energy Agency, County Administrative Board in Västernorrland and European Union for their financial support.

REFERENCES

[1] Wong Fu Keung, "High Frequency transformers for switch mode power supplies" Griffith University, 2004
[2] Efficient Power Conversion, *Fundamentals of GaN power transistors*, Application note, 2009.
[3] Tatsuya TANABE, Shin HASHIMOTO, Yusuke YOSHIZUMI and Mokoto KIYAMA, 'High-quality GaN Epitaxial Layers on GaN substrates for Power Devices', Electronics.
[4] K.Ikeda, H. Umezawa and S. Shikata,'Edge termination techniques for p-type diamond Schottky barrier diodes', Diamond & Related Materials No.17,2008, pp.809–812
[5] Radhika Ambatipudi, Hari Babu Kotte and Kent Bertilsson, "Coreless Printed Circuit Board (PCB) Step-down Transformers for DC-DC Converter Applications," *International Conference on Electrical Machines and Power Electronics*, Issue 71, ISSN: 1307-6892, pp. 370-379, October 2010.www.waset.org.
[6] S.C.Tang, S.Y.R.Hui, and H. Chung, "Coreless Printed Circuit Board (PCB) Transformers –Fundamental characteristics and Application potential'', IEEE Circuits and Systems Newsletter, Vol. 11, No. 3, Third Quarter 2000, pp.1, pp.3-15 and pp.47.
[7] HariBabu Kotte, Radhika Ambatipudi and Kent Bertilsson, ''A ZVS Flyback DC-DC Converter using Multilayered Coreless Printed-Circuit Board (PCB) Step-down Power Transformer," *International Conference on Electrical Machines and Power Electronics*, Issue 71, ISSN: 1307-6892, pp. 80-88, October 2010.www.waset.org.
[8] Efficient Power Conversion, EPC1012 Datasheet.
[9] Infineon Technologies, *How to Compare the Figure of Merit (FOM) of MOSFETs*, Application note, June 2003.
[10] Wojciech A. Tabisz, Pawel M. Gradzki and Fred C.Y.Lee, "Zero-Voltage-Switched Quasi-Resonant Buck and Flyback Converters-Experimental Results at 10MHz'' IEEE transactions on power Electronics,vol.4,No.2,April 1989.
[11] National Semiconductor, LM5111 Dual 5A Compound Gate Driver, Datasheet.

8th International Conference on Power Electronics - ECCE Asia
May 30-June 3, 2011, The Shilla Jeju, Korea

High Speed Cascode Flyback Converter Using Multilayered Coreless Printed Circuit Board (PCB) Step-Down Power Transformer

Hari Babu Kotte[1], Radhika Ambatipudi[1], and Kent Bertilsson[1, 2]
[1] Department of Information Technology and Media, Holmgatan 10, Sundsvall, Sweden, SE-85170
[2] SEPS Technologies AB, Storgatan 90, Sweden, SE-85170
hari.kotte@miun.se

***Abstract*-- In this paper, design and analysis of the high speed isolated cascode flyback converter using multilayered coreless PCB step down power transformer is presented. The converter is tested for the input voltage variation of 60-120V with a nominal DC input voltage of 90V. The designed converter was simulated and tested successfully up to the output power level of 30W within the switching frequency range of 2.6-3.7MHz. The cascode flyback converter is compared with the single switch flyback converter in terms of operating frequency, gate drive power consumption, conduction losses and stresses on MOSFETs. The maximum energy efficiency of the cascode converter is approximately 81% with a significant improvement of about 3-4% compared to single switch flyback converter. The gate drive power consumption which is more dominant compared to conduction losses of the cascode converter using *GaN* MOSFET is found to be negligible compared to single switch flyback converter.**

***Index Terms*-- Cascode flyback DC-DC converter, Multilayered coreless PCB transformer, Gate drive power consumption, MHz frequency operation.**

I. INTRODUCTION

As the high frequency operation is associated with energy storage elements, operating the converters in high frequency region reduces the size of magnetic components [1] such as transformers, inductors and capacitors. The most common semiconductor device utilized for high frequency converters is the power MOSFET instead of power BJT [2], [3]. Since, power MOSFETs are the majority carrier devices compared to their counterparts BJTs these are considered as faster, rugged and possesses higher current gain. Also MOSFETs contains the higher input impedance which makes it possible to design a simple gate drive circuitry. On the other hand, as the switching frequency is increased, the switching losses of semiconductor devices in converter circuit such as MOSFETs, diodes and the gate drive power consumption which is functional dependent on frequency increases. In core based transformers the hysteresis and eddy current losses which also depends on frequency gets increased. Even though the core materials are available upto few hundreds of kHz to MHz, the core losses combined with the winding losses makes them to utilize these transformers for lower operating frequencies in switch mode power supplies (SMPS). Hence in order to meet these challenges, lot of research is progressing in both semi conductor and magnetic areas. The recent investigation on the multilayered coreless printed circuit board step-down 2:1 transformers provides the way to use them for power transfer applications in MHz frequency region [4]. Also in semi conductor devices area, due to the theoretical limitations of *Si* material [5], new materials such as GaN and *SiC* which provides excellent high frequency switching behavior, high thermal performance characteristics are introduced. According to [6], among these two materials *GaN* provides the higher performance characteristics compared to SiC material. These improvements in magnetics and with latest semi conductor *GaN* MOSFETs, it is possible to design the low profile, high speed and high power density SMPS.

Flyback topology is the most widely used SMPS topology in most of the AC-DC and DC-DC converter applications for power ratings of below 150W [7] because it requires only a single magnetic element i.e., coupled inductor. This serves the purpose of isolation, step-up/step-down conversions as well as acts an energy storage element. The attractive feature of this topology is that it does not require any output inductors as any other topology demands. In AC-DC and DC-DC Converters such as laptop adapters and telecom applications, high voltage power MOSFETs of 500-1000V consists of high gate charge. While operating these transistors at higher frequencies the power required to turn on the MOSFETs gets increased which leads to high gate drive power consumption. This has a significant effect under light load and low power conditions. As per figure of merit discussed in [8], there exists a tradeoff between the gate charge 'Q_g' and the on-state resistance 'R_{ds_on}' of MOSFET. If a high voltage MOSFET which consists of low 'Q_g' is selected it consists of higher 'R_{ds_on}' which leads to conduction losses of MOSFET. Therefore, in order to reduce the on-state resistance of these MOSFETs, the die area must be increased which in turn reduces the switching speed of MOSFET. Paralleling of MOSFETs is also one of the solutions for reducing the conduction losses however it also suffers from the same disadvantage of low switching speeds of converter.

Therefore, in this paper a low profile, high speed cascode flyback power converter using multilayered

978-1-61284-957-7/11/$26.00 ©2011 IEEE

coreless PCB step-down power transformer is reported. The significance of gate drive power in cascode flyback converter over the increased conduction loss, energy efficiency, switching speed compared to its counterpart single switch flyback converter is discussed.

II. Multilayered Coreless PCB Step-Down Power Transformer

Recent research [9], [10] proves that the multilayered 2:1 coreless PCB step-down power transformers are highly energy efficient of about 90-97% in MHz frequency region and can be used for DC-DC converter applications. Since, this provided the scope for increasing step-down ratio of transformer, a further step-down ratio transformer of approximately 8:1 which is of primary-secondary-secondary-primary (PSSP) structure for SMPS application was designed on a four layered FR4 laminate. The breakdown strength of PCB laminate used to design coreless PCB transformer is 50kV/mm [11]. The two secondaries of transformer are connected in parallel and are sandwiched in between the two primaries which are connected in series for optimal design. The windings are spiral in shape in order to reduce the interwinding capacitance of the transformer and also to increase the amount of inductance compared to other structures [12]. Here, the number of turns of primary/secondary in each layer is 24/6 with a primary/secondary DC resistance R_p/R_s of transformer as 2.71/0.08Ω. The electrical parameters of transformer such as self/leakage inductance of primary and secondary are 29.38µH/1.9µH and 0.548µH/0.038µH respectively which are obtained by following the procedure described in [4]. The interwinding capacitance of transformer is 125pF and the intrawinding/self capacitances of these transformers are considered as almost negligible. The achieved coupling coefficient 'K' by using the following equations is 0.93.

$$K = \frac{Lm}{\sqrt{Lp \cdot Ls}} \tag{1}$$

$$Lm = \sqrt{Lmp \cdot Lms} \tag{2}$$

L_m Mutual inductance
L_p/L_s Primary/secondary self inductance

The prototype of the designed multilayered coreless PCB step-down transformer is shown in fig.1.

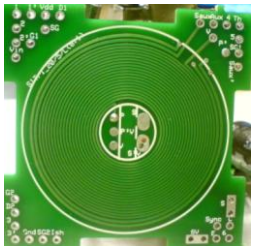


Fig. 1: Multilayered coreless PCB step-down 8:1 transformer

This transformer was integrated into the cascode and single switch flyback converter and the performance of converter circuit was evaluated.

III. Operating Principle of Cascode Flyback Converter

The cascode converter using multilayered coreless PCB step-down power transformer is shown in fig. 2. In case of cascode flyback converter, a low voltage (LV) MOSFET 'Q_1' having low gate charge 'Q_g' is connected in series with the high voltage (HV) MOSFET 'Q_2'.

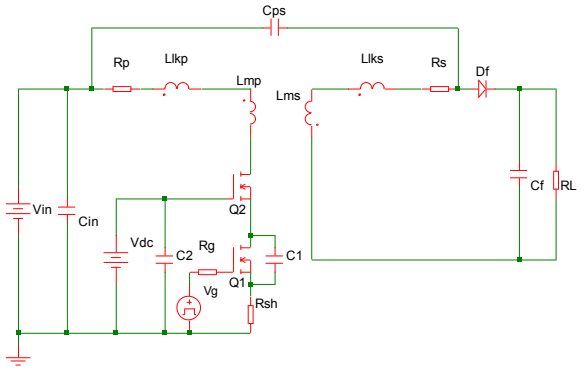


Fig. 2: Cascode flyback converter using multilayered coreless PCB step down transformer

In this case, the LV MOSFET 'Q_1' is driven directly from the MOSFET gate driver. A capacitor 'C_1' is placed across the drain source of LV MOSFET 'Q_1' in order to limit the drain-source voltage of LV MOSFET 'Q_1' within its maximum drain-source breakdown voltage 'V_{ds_max}'. This also ensures the gate- source voltage of HV MOSFET 'Q_2' within its gate-source voltage limits. A reservoir capacitor 'C_2' is placed across the gate of the HV MOSFET 'Q_2' and it is charged with the external DC source.

The operation of cascode converter [13] using two MOSFETs can be explained in different modes as follows.

Mode (i)-(V_{gs1}>V_{th1} & V_{gs2}>V_{th2}): When the gate - source voltage of LV MOSFET 'Q_1' ie., V_{gs1} is greater than its gate threshold voltage, V_{th1}, the MOSFET 'Q_1' fully enhances and it gets turned ON. As soon as the LV MOSFET 'Q_1' turns ON, due to the voltage across the reservoir capacitor 'C_2', which falls across the gate-source of HV MOSFET 'Q_2', it gets turned ON. At this instant of time, the cascode converter gets into the conduction state and hence the current starts flowing through the primary winding of flyback transformer and the two switches (Q_1 and Q_2). In this state, the voltage drop across both MOSFETs is equal to their on-state voltage drops. Here, the flyback diode 'D_f' is in reverse biased condition and hence the filter capacitor, 'C_f' supplies the load current.

Mode (ii)-(V_{gs1}<V_{th1}): When the gate-source voltage 'V_{gs1}' is less than its gate threshold voltage 'V_{th1}',

MOSFET 'Q_1' gets into turned OFF condition. Since, the voltage across MOSFET 'Q_2' is constant, when the MOSFET 'Q_1' is OFF, the current takes the path through the parallel capacitor across 'Q_1' i.e., C_1 and the gate - source capacitance of HV MOSFET 'Q_2'. Now the drain-source voltage 'V_{ds1}' across LV MOSFET starts to increase. At this instant of time, the potential of source terminal of HV MOSFET 'Q_2' starts to build up.

Mode (iii)-($V_{gs2}<V_{th2}$): As the potential of source terminal of HV MOSFET 'Q_2' builds up, the gate-source voltage 'V_{gs2}' of HV MOSFET gets reduced and when it reaches its gate threshold voltage 'V_{th2}', the HV MOSFET 'Q_2' gets turned OFF. At this instant, the drain-source voltage 'V_{ds2}' of HV MOSFET 'Q_2' raises. Under this condition, the current in both the switches now tries to flow in the drain-source capacitance of HV MOSFET 'Q_2', the drain-source capacitance of LV MOSFET 'Q_1', its parallel capacitor 'C_1' and into the reservoir capacitor 'C_2'. To a small extent this current also flows into its miller capacitance.

Mode (iii)-($V_{gs1}<V_{th1}$ & $V_{gs2}<V_{th2}$): When gate-source voltage of both switches 'Q_1' and 'Q_2' are less than their corresponding gate threshold voltages, the switches comes into the turn OFF condition. In this case, the flyback diode 'D_f' comes into the ON state and the stored energy in the secondary winding is fed to the load resistance, R_L.

The gate-source and drain-source voltage of HV and LV MOSFETs in different modes of operation conditions is illustrated in fig. 3.

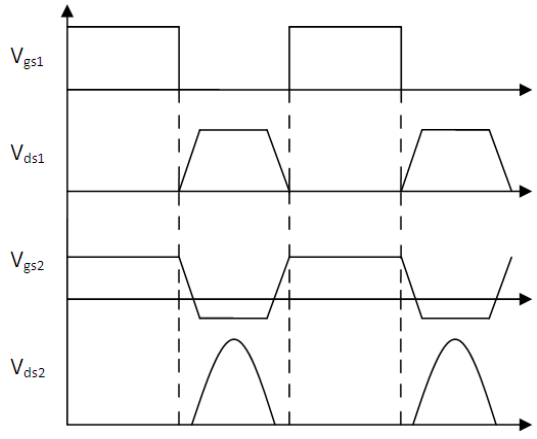


Fig. 3: Gate and drain voltages across two switches (Q_1 and Q_2) of cascode converter

Because of the low gate charge of LV MOSFET, 'Q_1', the gate drive power consumption due to 'Q_1' is considered to be negligible.

The DC current flowing into the gate of the HV MOSFET 'Q_2' is also negligible because of equalization of the amount of charge entering and leaving the capacitor 'C_2' [14] during turn ON/OFF process. The whole gate charge is thus charging/discharging the external capacitor and hence not wasted. In this way the drive power required to switch the HV MOSFET is almost zero and that of the LV MOSFET is negligible.

IV. Experimental Results

The cascode flyback converter and single switch flyback converter were initially simulated by using SIMetrix simulation software. Soft switching techniques enable the high frequency operation, high energy efficiency, compact and light weight converters, [15]-[17]. Therefore both the cascode and single switch flyback converters were maintained to operate under zero voltage switching (ZVS) conditions. Based upon the analysis and simulation results the prototype was designed and then tested with following conditions: The input voltage to converter is varied from 60-120V with a dc nominal voltage of 90V.The full load resistance of the converter is of 10Ω with the switching frequency range of 2.6-3.7MHz. Here, MOSFET is driven with the help of LM5111-1M MOSFET gate driver whose rise/fall times are of about 14 ns/12 ns for 2 nF load. In cascode flyback converter, the LV MOSFETs 'Q_1'considered are 1) *Si* MOSFET- ZXMN15A27K and 2) *GaN* MOSFET – EPC1013 and the HV MOSFET 'Q_2' considered is *Si* MOSFET STP3NK60ZFP whose characteristics are listed in Table I. The secondary side diode considered is of *Si* schottky SR1660 whose reverse blocking voltage capacity is of 60V and with forward current rating of 16Amp.

TABLE I
MOSFETS AND CORRESPONDING PARAMETERS

S.No	MOSFET(Material)	V_{ds_max} (V)	I_d (A)	R_{ds_on} (Ω)	Q_g (nC)	C_{oss} (pF)
1	ZXMN15A27K (Si)	150	2.4	0.65	6.6	64.5
2	EPC1013 (GaN)	150	3.0	0.1	1.7	85
3	STP3NK60ZFP (Si)	600	2.4	3.3	11.8	43

In case of flyback converter the *Si* HV MOSFET STP3NK60ZFP is considered for comparison with the cascode flyback converter. The following tests were carried out by using the multilayered coreless PCB step-down transformers and the three cases are as follows.

Case (i): Cascode converter with 'Q_1' as Si LV MOSFET: ZXMN15A27K and 'Q_2' as Si HV MOSFET: STP3NK60ZFP

Case (ii): Cascode converter with 'Q_1' as GaN LV MOSFET: EPC1013 and 'Q_2' as Si HV MOSFET: STP3NK60ZFP

Case (iii): Flyback converter with 'Q_1' as Si HV MOSFET: STP3NK60ZFP

In the first two cases, the HV MOSFET 'Q_2'is driven with a supply voltage of 12V dc with a charging capacitor of 10μF.The simulated and measured energy efficiency of the converter in all the three cases is illustrated in fig. 4

including gate drive power consumption at 50% duty cycle ratio.

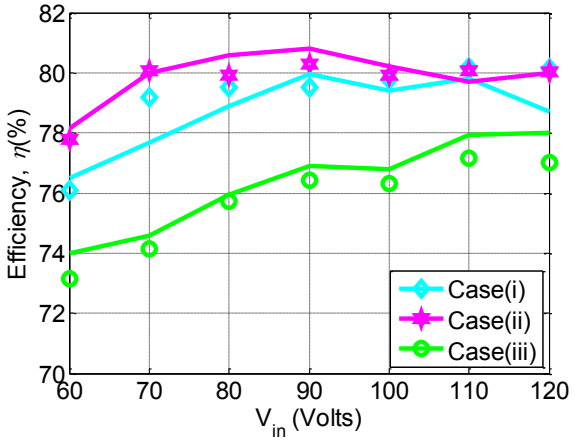


Fig. 4: Simulated (Solid) and Measured (Symbol) Energy efficiency of the converters for input voltage variation with R_L=10Ω

This figure shows that the simulated and measured energy efficiency of converters is in good agreement with each other. From fig. 4 it can be observed that the maximum energy efficiency of the converter is achieved in case of cascode converter with *GaN* MOSFET followed by the cascode converter with *Si* MOSFET. At nominal input voltage of 90V, the energy efficiency of the cascode converter with GaN/Si MOSFETs is 80.4%/79.5% respectively and for the single switch flyback converter it is only 76.4% because of the improved gate drive power consumption and also due to the fast rise and fall times of the LV MOSFET 'Q_l' in cascode flyback converter. From fig. 4 we can observe that the energy efficiency of single switch flyback converter is drastically reduced compared to cascode converter particularly at lower input voltages because of the influence of gate drive power. The measured gate drive power consumption in case (i) is 0.28Watts, in case (ii) is 0.05Watts and in case (iii) it is 0.6Watts. This shows that the gate drive power consumption in cascode flyback converter using *GaN* MOSFET is negligible because of low 'Q_g'.

In cascode converter due to two series connected MOSFETs, the static/conduction loss gets increased which is dependent on R_{ds_on} of MOSFETs. Therefore, the conduction losses of the MOSFETs in single switch flyback converter and cascode converter were measured at a given power with nominal input voltage. The measured conduction loss in case (i) is 0.133 Watts, in case (ii) it is 0.118 Watts whereas in case (iii) it is only 0.115 Watts. From the measured gate drive power consumption and conduction losses in all the three cases, it can be observed that the gate drive power consumption is a dominant factor compared to conduction losses of MOSFETs. Even though the low R_{ds_on} MOSFET is placed in single switch flyback converter, the gate charge of the MOSFET gets increased according to figure of merit (3) for the given power application [8],[18] which increases the gate drive power consumption with lower conduction losses. The figure of merit of MOSFETs can be given as follows.

$$FOM(Vgs,Vds) = Rds\_on(Vgs,Vds)\cdot Qg(Vgs;Vds) \qquad (3)$$

Therefore, the gate drive power which is a function of frequency finds its advantages in high frequency SMPS with cascode topology particularly in low power and light load conditions compared to single switch flyback converter. In the cases (i) and (ii), at higher input voltages there exists no significant improvement in terms of energy efficiency. However, at lower input voltages the energy efficiency in case (ii) is increased because of gate drive power consumption as discussed earlier. Also in terms of size there exists a significant improvement in case (ii) compared to case (i) where ZXMN15A27K is of DPAK and EPC1013 is land grid array (LGA 1.7x0.9mm) package. The GaN MOSFET utilized in cascode converter costs about 2.42$/unit whereas for ZXMN15A27K is about 0.57$/unit. But these exceptional features such as low conduction loss and low gate drive power consumption can be only obtained by utilizing *GaN* MOSFET together with coreless PCB step down power transformers which is beneficial for the future generation ultra low profile converters. The maximum switching frequency of the cascode converter at V_{in} of 120V with GaN/Si as LV MOSFETs was found to be 3.65/3.64MHz respectively whereas in case of single switch flyback converter it is 2.88MHz only. This represents that higher switching speeds are possible with the cascode converter compared to single switch flyback converter.

The maximum load power attained in all the three cases is approximately 30Watts and load power profile with respect to input voltage variation is illustrated in fig. 5.

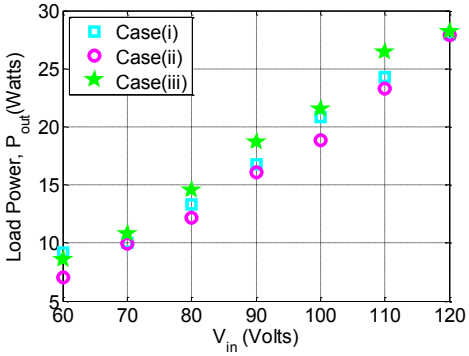


Fig. 5: Measured load power of the converters for input voltage variation with R_L=10Ω

Fig. 5 shows that all measurements and comparisons were made at approximately same power levels in all the three cases for varied input voltage. At nominal input voltage, output voltage of the converter in all cases is approximately 13V and this can be regulated to 12V for wide input voltage & load variation using constant off time frequency modulation technique discussed in [9].
At an input voltage of 70V, the simulated waveforms of cascode flyback converter with *Si* MOSFET at a load resistance of 10Ω i.e., case (i) are illustrated in fig. 6.

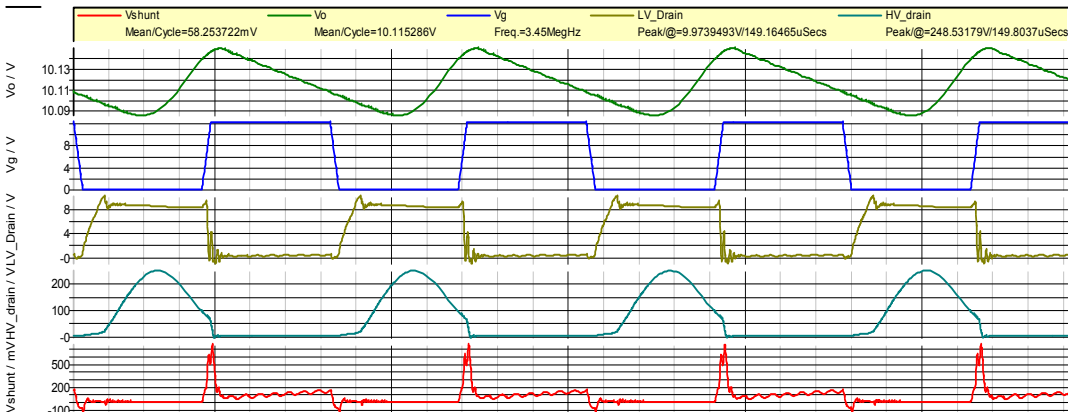


Fig. 6: Simulated waveforms of Cascode converter, case (i) with R_L=10Ω, *top-bottom-Output Voltage (V_o), Gate voltage (V_g), Drain Voltage of 'Q1' (V_{dsmax_Q1}), Drain Voltage of 'Q2' ($V_{dsmax-Q2}$), Shunt voltage (V_{shunt})*

The figure shows the output voltage of converter (V_o), gate-source voltage fed to LV MOSFET Q_1 (V_g), drain-source voltages V_{ds_max} of both MOSFETS Q_1 & Q_2 and the voltage across shunt resistor R_{sh} i.e., V_{sh}.

Under the same conditions, measured waveforms were captured from oscilloscope and are shown in fig. 7.

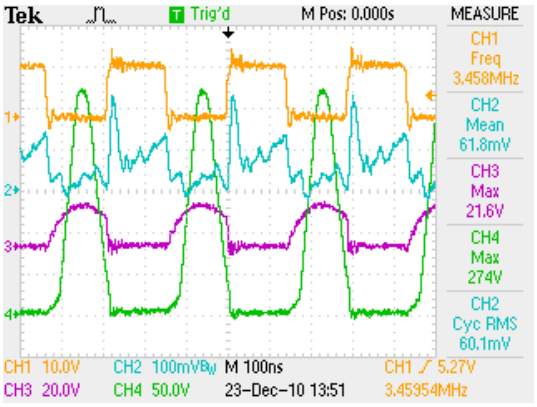


Fig. 7: Measured waveforms with R_L=10Ω. CH1 – V_{gs} (10V/div), CH2- V_{sh} (100mV/div), CH3 – (Q1) V_{ds} (20V/div), CH4 – (Q2) V_{ds} (50V/div)

In fig. 7, CH1-CH4 shows the gate to source voltage (V_{gs}) applied to the LV switch 'Q_1', voltage across shunt resistor 'R_{sh}'of 0.33Ω, drain to source voltage (V_{ds}) of LV switch 'Q_1' and drain to source voltage (V_{ds}) of HV switch 'Q_2'of the converter circuit. It can be observed from fig. 7, that the MOSFETs are almost operated in ZVS conditions.

The stress on high side MOSFETs in cascode converter and the single switch converter with the input voltage variation are depicted in fig. 8. From fig. 7 and fig. 8, at an input voltage of 70V the stress on HV MOSFET is reduced by approximately 22V in cascode converter compared to single switch flyback converter. In addition to the above mentioned advantages of high speed cascode converter, the stress on the HV MOSFET 'Q_2' gets reduced compared to single switch flyback converter and hence the reliability of converter gets increased.

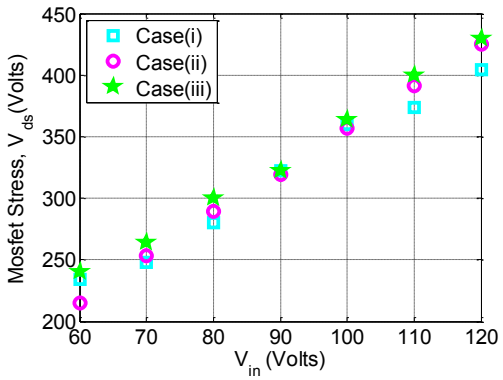


Fig. 8: Measured drain-source voltage of the HV MOSFETs with the input voltage variation

V. LOSS ESTIMATION OF CASCODE CONVERTER

The loss estimation was made for case (i) under following conditions. At the nominal input voltage of 90V, with a load resistance of 10Ω the input/output power of converter is 21.1/16.8Watts respectively which leaves the total loss of about 4.3Watts. At this instant, the switching frequency of the converter is 3.45MHz.

A) Transformer Losses: The measured mean/RMS currents flowing through the primary are 0.235/0.252 Amps. The RMS current flowing through the secondary winding of flyback transformer is 1.7Amps. The calculated AC resistances of the primary/secondary obtained as mentioned in [4] are 9.77Ω/0.310Ω and the copper losses of the transformer which can be given by the following equation (4) are 0.62/0.89Watt respectively.

$$P_{loss} = \left(i_p^2 \cdot R_{ac}(p) + i_s^2 \cdot R_{ac}(s)\right) \quad (4)$$

Where,
i_p/i_s- RMS currents through primary/secondary winding
$R_{ac}(p)$ / $R_{ac}(s)$ - Primary/secondary winding ac resistance

B) MOSFET Losses: A MOSFET loss consists of both conduction and switching losses [19]. The average conduction losses i.e., static losses [20] of LV/HV MOSFET whose R_{ds_on} is 0.65/3.3 are 0.017/0.088Watts respectively which can be obtained as follows.

$$Pc\_avg = \mathrm{Im}ean^2 \cdot Rds\_on \cdot D \qquad (5)$$

Where,
I_{mean} – mean current flowing through the switch
R_{ds_on} – on state resistance of MOSFET
D – Duty cycle ratio

MOSFET switching loss consists of both turn-on and turn-off losses [21]. Since, converter was not operated fully under ZVS conditions, it experiences some of the turn on losses which can be obtained as follows.

$$Pswitching = \frac{1}{2}\left(Tsw\_on + Tsw\_off\right) \cdot Vds \cdot Id \cdot fsw \qquad (6)$$

Where,
T_{sw_on} – turn-on switch transition time
T_{sw_off} – turn-off switch transition time
V_{ds} – drain source voltage
I_d – current though MOSFET
f_{sw} – switching frequency

Under the above mentioned conditions, the estimated turn-on losses of LV/HV MOSFET are 0.439/0.604Watts.

Here, since the drain-source voltage of MOSFETs is almost zero at the instant when the switch is turned off, the turn-off losses are considered as negligible.

C) MOSFET driver loss: Theoretically, the power consumption of MOSFET driver [22] can be given as follows

$$Pgate = Vg \cdot fsw \cdot Qg \qquad (7)$$

Where,
V_g - Gate voltage
f_{sw} - Switching frequency of MOSFET
Q_g - Total gate charge of MOSFET

The calculated/measured MOSFET driver loss is found to be 0.27/0.28Watts.

D) Diode Losses: The flyback diode conduction loss [20] obtained by using equation (8) loss is 0.388Watts.

$$Pdiode = Vf \cdot ID\_avg \cdot (1 - D) \qquad (8)$$

Where,
V_f - Diode forward voltage drop
I_{D_avg} - average current flowing through flyback diode

E) Miscellaneous losses: It consists of 'C_{oss}' loss and switching losses of secondary rectifier diode and remaining circuit losses.

In general, the loss across the output capacitance 'C_{oss}' is given as follows.

$$P\cos s = \frac{1}{2} \cdot Coss \cdot Vds^2 \cdot fsw \qquad (9)$$

These computed losses are illustrated as a pie diagram in fig. (9). The losses are represented in anti clockwise direction starting from the transformer losses which is designated as 'T_r_Loss' in fig. 9.

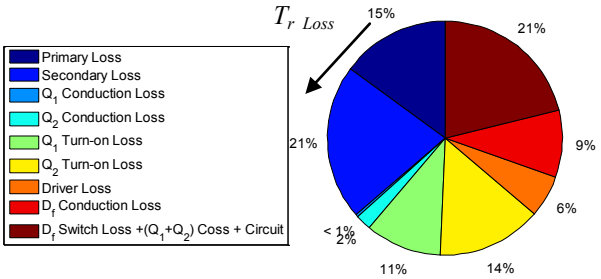


Fig. 9: Loss estimation of cascode converter –Case (i)

Under these conditions, the temperature of cascode converter circuit including coreless PCB transformer, LV/HV MOSFETs, flyback diode MOSFET driver, are measured with the assistance of IR thermal imaging camera. This thermal profile of above mentioned devices in the cascode converter is depicted in fig. 10.

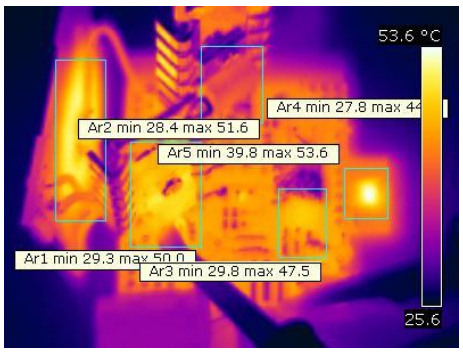


Fig. 10: Ar1 - Area of the Switch STP3NK60ZFP (Q2), Ar2 - Area of the Transformer, Ar3 - Area of the Switch ZXMN15A27K (Q1), Ar4 - Area of the schottky diode SR1660, Ar5 – MOSFET Driver LM5111

The loss contributed by the multilayered coreless PCB transformer is around 36% out of the total loss. With the proper design of this coreless PCB transformer i.e., by reducing the primary and secondary resistances, also by maintaining exact ZVS conditions a highly energy efficient, low profile cascode flyback converter can be achieved.

VI. Conclusion

A low profile cascode flyback converter with multilayered coreless PCB step down power transformer for an output power level of upto 30Watts operating in

2.6-3.7MHz was presented. Since the HV MOSFET and the LV *GaN* MOSFET in the cascode converter needs negligible power, the gate drive power consumption is approximately reduced by 12 times compared to single switch flyback converter for the same output power level. The conduction losses increment in the cascode converter with the advanced switches like *GaN* MOSFET is negligible. Also the stress of the HV MOSFET can be shared by the LV MOSFET in case of cascode converter compared to single switch flyback converter which increases its reliability. Apart from these advantages, with the help of cascode converter higher switching speeds of converter are possible compared to single switch flyback converter. The energy efficiency of the cascode converter including gate drive power was improved by 3-4% compared to single switch flyback converter and the maximum energy efficiency of the cascode converter is approximately 81%. Since, at low power conditions the energy efficiency with cascode converter is greatly increased compared to single switch flyback converter it can be concluded that there will be a great improvement in the power consumption under no-load and light load conditions. From the loss estimation, it can be concluded that by reducing the dc resistance of the transformer, and also by operating the converter in perfect ZVS conditions the energy efficiency of cascode flyback converter in MHz can be further improved.

ACKNOWLEDGMENT

The authors would like to thank Mid Sweden University, VINNOVA, The Swedish Energy Agency, County Administrative Board in Västernorrland and European Union for their financial support.

REFERENCES

[1] Wong, Fu Keung, "High Frequency transformers for switch mode power supplies", Griffith University, 2004.

[2] B.N.Shashikala, B.S.Nagabhushana, S.K.Shastry, "Modeling and Performance Evaluation of Wide Bandgap Semiconductor devices for High Power Applications", Journal of recent advances in Networking, VLSI and Signal Processing, pp.327-335, ISSN: 1790-5227, ISBN: 978-960-474-162-5.

[3] Alex Lidow, "Can Gallium Nitride Replace Silicon?" Power Electronics Europe, Issue 2, 2010.

[4] Radhika Ambatipudi, Hari Babu Kotte and Kent Bertilsson, "Coreless Printed Circuit Board (PCB) Step-down Transformers for DC-DC Converter Applications," Proceedings of World Academy of Science, Engineering and Technology, Vol.70, pp 380-389, ISSN: 1307-6892, October 2010, Paris.

[5] Khan, M.A.; Simin, G.; Pytel, S.G.; Monti, A.; Santi, E.; Hudgins, J.L.; , "New Developments in Gallium Nitride and the Impact on Power Electronics," *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, vol., no., pp.15-26, 16-16 June 2005.

[6] Sam Devis, "Enhancement Mode Gallium Nitride MOSFET delivers impressive Performance", Power Electronics, March 1, 2010.

[7] Abraham I. Pressman, 'Switching Power Supply Design'2nd Edition, McGraw-Hill, pp.105

[8] Infineon Technologies, *How to Compare the Figure of Merit (FOM) of MOSFETs*, Application note, June 2003.

[9] Hari Babu Kotte, Radhika Ambatipudi and Kent Bertilsson, "A ZVS Flyback DC-DC Converter Using Multilayered Coreless Printed-Circuit Board (PCB) Step-down Power Transformer," Proceedings of World Academy of Science, Engineering and Technology, Vol.70, pp 148-155, ISSN: 1307-6892, October 2010, Paris.

[10] S.C.Tang, S.Y.R .Hui and H. Chung, "Coreless Printed Circuit Board (PCB) Transformers –Fundamental characteristics and application potential", IEEE Circuits and Systems Newsletter, Vol. 11, No. 3, 3rd Quarter 2000, p.1, pp.3-15 & p.47.

[11] C.F.Coombs, 'Printed Circuits handbooks' 5th Edition, McGraw-Hill, August 27, 2001

[12] K. Kawabe, H.Koyama and K. Shirae, "Planar Inductor", IEEE Transactions on Magnetics, Vol.Mag-20, No.5, Pages 1804- 1806, September 1984.

[13] Ernest H.Wittenbreder, "Cascode MOSFET Cascode Switches for Power Converters", US6, 483,369 B1, November 19, 2002.

[14] Carl.K.Sawtell, Paolo Menegoli, "Cascode Switch Power Supply," US7, 345,894 B2, March 18, 2008.

[15] Buonomo, S.; Musumeci, S.; Pagano, R.; Porto, C.; Raciti, A.; Scollo, R.; , "Driving a New Monolithic Cascode Device in a DC–DC Converter Application," *Industrial Electronics, IEEE Transactions on* , vol.55, no.6, pp.2439-2449, June 2008

[16] R. J. Wai, L. W. Liu, and R. Y. Duan, "High-efficiency voltage-clamped DC–DC converter with reduced reverse-recovery current and switch voltage stress," IEEE Trans. Ind. Electron., vol. 53, no. 1, pp. 272–280,Feb. 2006.

[17] S. Musumeci, R. Pagano, A. Raciti, S. Buonomo, V. Enea, G. Gullotta, and C. Ronsisvalle, "A new monolithic power actuator devoted to high voltage and high frequency applications," in Proc. 16th Int. Symp. Power Semi cond. Devices ICs, Kitakyushu, Japan, 2004, pp. 445–448.

[18] Hari Babu Kotte, Radhika Ambatipudi and Kent Bertilsson,"Comparative Results of GaN and Si MOSFET in a ZVS Flyback Converter Using Multilayered Coreless Printed Circuit Board Step Down Transformer," Proceedings of 2010 3rd International Conference on Power Electronics and Intelligent Transportation System (PEITS 2010)", November 20-21, 2010, Shenzhen, China.

[19] Robert W .Erickson, 'Fundamentals of Power Electronics'2nd Edition, Springer International Edition, pp.92-97

[20] Marty Brown,"Power Sources and Supplies, World Class Designs", Third edition, Newnes press, ISBN: 978-0-7506-8626-6, 2007, pp.257.

[21] Z.J. Shen, Y. Xiong, X. Cheng, Y. Fu and P. Kumar, "Power MOSFET Switching Loss Analysis: A New Insight", *in Proc. IEEE IAS Meeting*, Tampa, FL, Oct.2006, pp. 1438-1442.

[22] National Semiconductor, LM5111 Dual 5A Compound Gate Driver, Datasheet.

8th International Conference on Power Electronics - ECCE Asia
May 30-June 3, 2011, The Shilla Jeju, Korea

High Frequency Half-Bridge Converter using Multilayered Coreless Printed Circuit Board Step-Down Power Transformer

A. Majid, H.B.Kotte, J.Saleem, R.Ambatipudi, S.Haller, K.Bertilsson
Electronics Design Division Mid Sweden University Sundsvall, Sweden
abdul.majid@miun.se

***Abstract*-- This paper introduces high frequency half bridge DC-DC converter, using multilayered coreless Printed Circuit Board (PCB) step down power transformer. The converter is simulated and then implemented on a PCB. Complementary Pulse Width Modulated (PWM) signals are generated to turn on high and low side Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) alternately by a micro-controller. The isolated gate drive signals are provided to the high side MOSFET by using high frequency coreless PCB isolation transformer. We tested the converter for switching frequency range of 2 to 3 MHz, and for maximum input voltage up-to 170 V. The maximum output power achieved is 40 W and the maximum energy efficiency is approximately 82 %.**

***Index Terms*—Printed Circuit Board, Pulse Width Modulation , Switch Mode Power Supplies.**

I. INTRODUCTION

New devices and topologies are always the pushing power in the development of power electronics. Switch Mode Power Supplies (SMPS) are used for DC-DC power conversion and it is desirable to reduce the size of the SMPS by increasing the switching frequency of the converter circuit used in the power supply. The main objective of this trend is to increase the power density by decreasing the size of the passive components such as inductors, capacitors and transformer and to improve the dynamic performance [1]. This results in compact power converter and enhanced loop response of the power supply [2]. With the fabrication of high frequency and efficient power electronic devices and also with the design of high frequency multilayered PCB power transformers, it has become possible to design high frequency and power efficient isolated converters. Multilayered PCB step down transformers are highly energy efficient and can be used in SMPS for power transfer applications in MHz frequency range. Recent research reveals that high frequency and high energy efficiency of the step down transformers is possible [3]. At high frequencies, the switching losses increase and limit the performance, especially at high voltages. To overcome this problem, often different soft switching techniques are used. To achieve super efficient power conversion, at higher voltages and higher frequencies, more research is needed.

Half bridge converter circuits can be used in various applications such as power supplies and motor drive. Although, the structure of the half bridge circuit is complicated because isolated gate drive signals are required for high side MOSFET but there are certain advantages to use this topology in DC-DC converter circuits. The advantage of half bridge is that the effective duty cycle, as seen by input and output filter, is twice that of individual switch duty cycle. Also, the effective frequency is twice that of the individual switch frequencies. Both high efficiency and high power density are achievable with half bridge converter topology [4].This paper presents a half bridge converter using multilayered PCB transformers.

II. DESCRIPTION AND EXPERIMENTAL RESULTS OF THE CIRCUIT

In this section the detailed description of the high frequency half bridge converter circuit is presented and the experimental results are shown.

The half bridge converter circuit was simulated and all parameters were optimized. The maximum energy efficiency of the converter was computed by variation of the circuit parameters. At best achieved conditions 85 percent energy efficiency was achieved in simulations. The circuit diagram of the Half Bridge converter is shown in Fig.1.

The actual circuit was implemented on a PCB. We used microcontroller to generate PWM signals that were fed to a MOSFET driver. After passing through the driver, the signals were fed to the gate of the lower MOSFET. Although there are some MOSFET drivers available with switching frequency up-to 1MHz and high side voltage up-to 125V [5] but there is no high side MOSFET driver available in the frequency range greater than 1 MHz and high side voltage range greater than 125V. To circumvent this problem, a multilayered coreless PCB isolation transformer [6] is used to transmit gate drive signals from input to isolated output. By using this gate drive transformer, a low power consumption passive gate drive circuitry [7] was built up and utilized to drive the high side MOSFET. Here, a zener diode was used to limit the gate-source voltage below 12 V.

CoolMOS SPU02N60S5 Power MOSFETs were used in the design. These devices offer significant advantages at high power levels. They can be operated with the lowest control power, the cheapest drive circuitry and the highest switching frequencies. They are ideal for applications like highly efficient power supplies and low power application like battery charger, line adapter and auxiliary supplies [8].

978-1-61284-957-7/11/$26.00

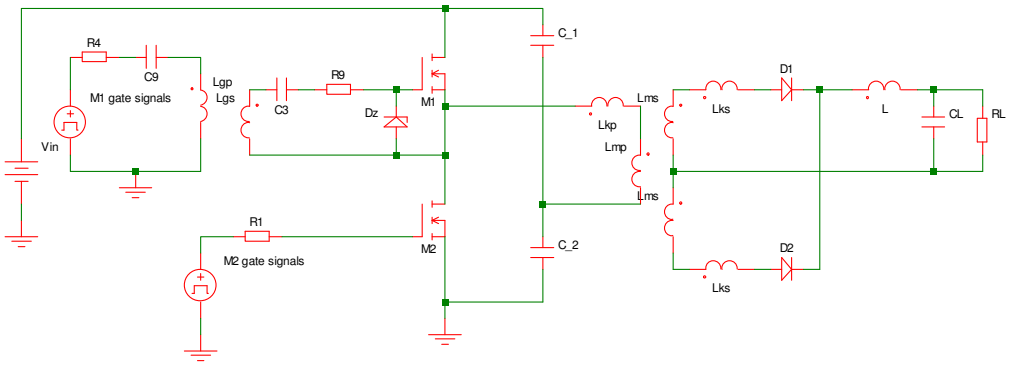


Figure 1. Circuit diagram of half bridge converter circuit

Since, the converter is designed to operate in MHz frequency range, traditional core based transformer cannot be used in high frequency converters. This is because in core based transformers, the core losses become dominant when the switching frequency of the converter is increased. Coreless PCB transformers can be used in signal and power transfer applications, in high frequency converters, because they do not have core and there are no core losses [9].

The 4:1 coreless PCB center-tapped power transformer designed for half bridge converter can be operated in the frequency range of 1 to 6 MHz. The transformer is designed in four layers of PCB and it has two primary windings in the first and the fourth layer while two secondary windings in second and third layer. With this structure better coupling between primary and secondary windings is achieved. The primary windings are connected in series and the secondary windings are connected in parallel to achieve the desired inductance. The number of turns in primary winding are 24 and in secondary winding are 6. The electrical parameters of the transformer were measured using RLC meter at 1 MHz. The self/leakage inductances of the primary/secondary winding are 7.73µH/1.38µH and 2.33µH/0.417µH respectively, whereas the primary/secondary winding ac resistance of the transformer is 2.2Ω/0.7Ω, with an inter-winding capacitance of approximately 50pF. The 4:1 multi-layer coreless PCB power transformer and gate drive transformer used in the circuit are shown in Fig. 2.

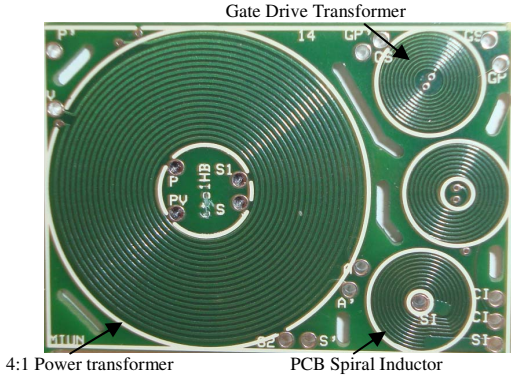


Figure 2. Transformers used in the converter circuit

The measured energy efficiency of this step down power transformer for load resistance of 10 Ω and sinusoidal excitation up to the output power level of approximately 17 W is illustrated in Fig. 3.

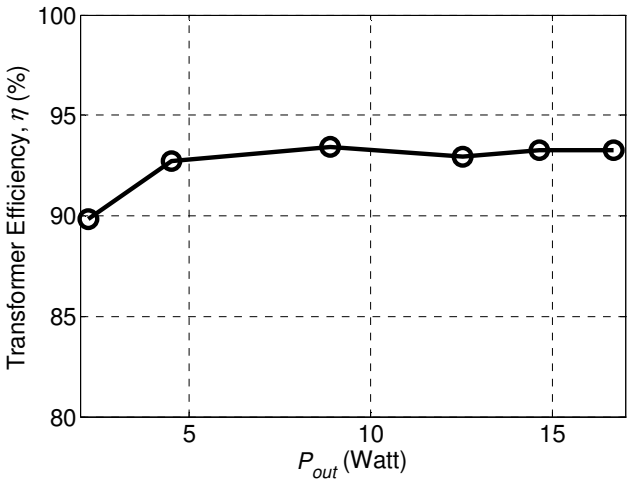


Figure 3. Energy efficiency of power transformers used in the converter circuit

On secondary side, the SR 1660 Schottky barrier rectifier diode was used. It has maximum average forward rectified current capability of 16A and maximum DC blocking voltage of 60V. The coreless PCB spiral inductor of 300nH and the output filter capacitor of 10uF were used for the removal of ripples to get the DC output voltage.

The prototype of the designed half bridge converter with integrated multi-layer coreless PCB transformer is shown in Fig. 4. Complementary gate signals, with 30% duty cycle, are applied to both MOSFETs. The gate signals for both high and low side MOSFETS are shown in Fig. 5. The Drain-Source voltages of both MOSFETs are shown in Fig. 6.

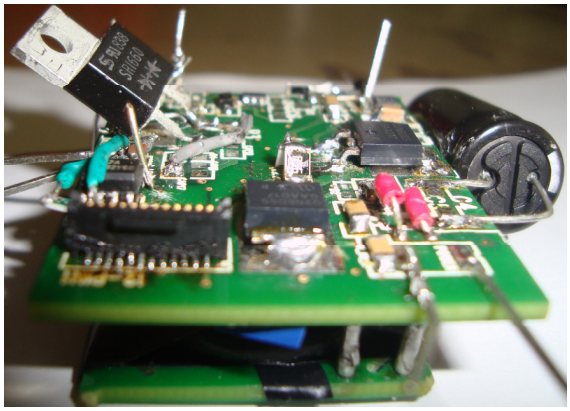


Figure 4. Prototype of Half Bridge converter circuit

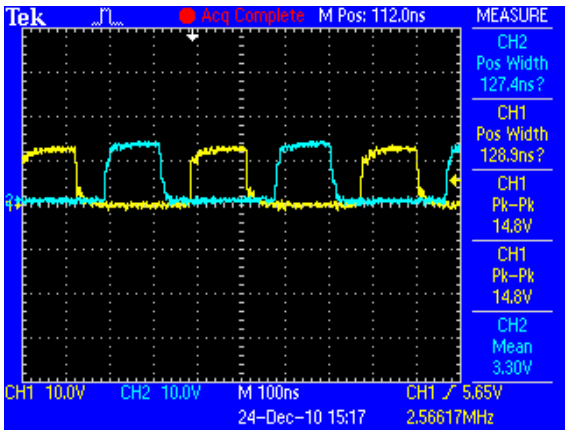


Figure 5. Gate signals for High and Low side MOSFETS

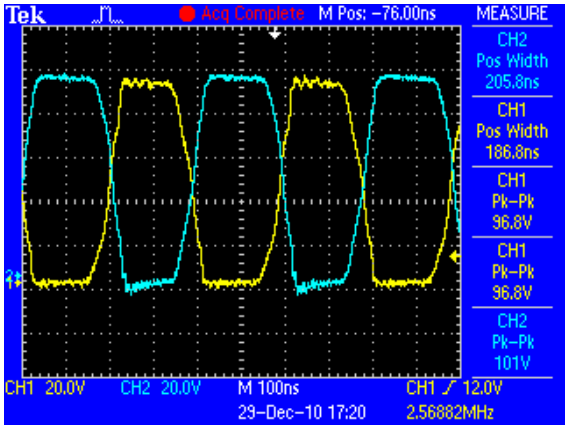


Figure 6. Drain-Source voltages of High and Low side MOSFETS

The energy efficiency of the unregulated half bridge converter circuit was computed for the input DC voltage of up-to 170 V and switching frequency in the range of 2 to 3 MHz, with the load resistances of 10 Ω, 20 Ω and 40 Ω. When computing the efficiency, the power dissipation of the gate drive circuit was not included.

It was observed that by increasing the input voltage of the converter, at load resistors 10 Ω, 20 Ω and 40 Ω and switching frequency of 2.5MHz, the energy efficiency of the unregulated half bridge converter varies. With 10 Ω load resistor and 170 V input voltage, the output voltage of the converter is 20 V and output power was 40 W.

The maximum energy efficiency of the converter for input voltage of 16 V with duty cycle of 30% and load resistor of 20Ω was achieved. Under these conditions, the output voltage of converter was 20 V and output power was 22.9 W. The efficiency values, with the variation of input voltage, and load resistor values of 10 Ω, 20 Ω and 40 Ω are plotted Fig. 7.

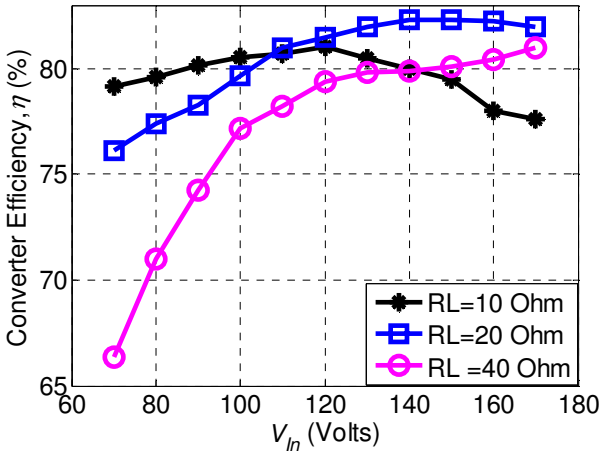


Figure 7. Energy Efficiency with variation in input voltage variation for RL =10Ω, 20Ω and 40Ω

Theoretically, each MOSFET should have maximum of 50% duty cycle but due to the rise/fall times they are switched below 50 % duty cycle. By keeping the switching frequency, input voltage and load resistance constant, it was observed that the efficiency of the converter varies by variation in the duty cycle of the switching PWM signals. The maximum value of the energy efficiency was achieved at 30 % duty cycle. The variation of energy efficiency with the variations in the duty cycle is shown in Fig. 8.

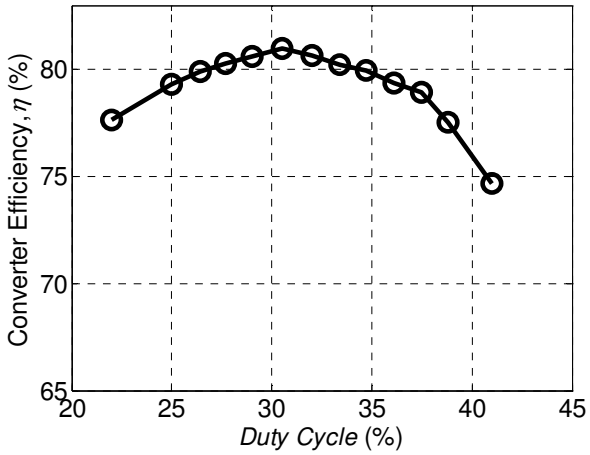


Figure 8. Energy efficiency with the variation of duty cycle

The energy efficiency of the converter also varies with the variation in the switching frequency. While keeping the input voltage, duty cycle and load resistance constant, the variation of energy efficiency with the variation in the switching frequency was computed.

The variation in the energy efficiency as a function of frequency is shown in Fig. 9. It was observed that as the switching frequency of MOSFETs was increased beyond 2.7MHz, the efficiency of the converter was reduced due to increased switching losses of power MOSFETs, gate drivers and Schottky diodes.

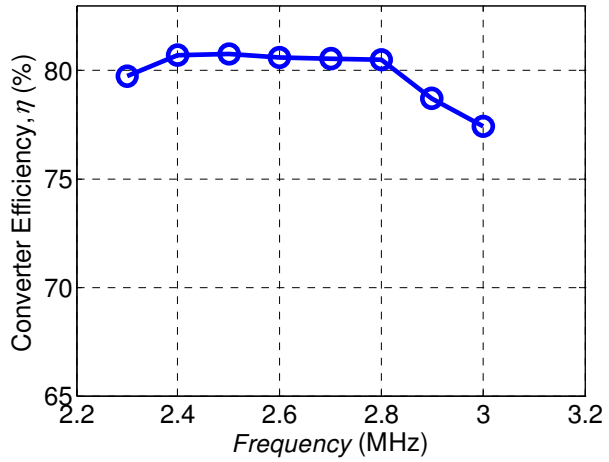


Figure 9. Energy efficiency with the variation of switching frequency

III. ESTIMATION OF LOSSES IN THE CONVERTER CIRCUIT

The losses in the converter were estimated with input voltage of 120 V and the load resistance of 10Ω. The input power of the converter was 27 W while, output power was 22 W. The power loss of the converter was 5 W. It is understood that as the switching frequency increases, the switching loss and gate loss increase [1]. These losses in the converter are shared by MOSFETs, gate driver, transformer and rectifier diode.

Power dissipation in the gate drive can be calculated according to equation 1 [10].

$$P_{driver} = V_G \times Q_G \times f_{sw} \quad (1)$$

Where *fsw* is the switching frequency, V_G is the gate voltage and Q_G is gate charge of the MOSFET.
SPU02N60S5 has gate charge specified as 12 nC for V_G = 12 V. The power dissipation in the driver, due to charging and discharging of MOSFET gate capacitances, at switching frequency of 2.5 MHz, is 0.39 W. If both channels of the LM5111 are operating at equal frequency, with equivalent loads, the total losses will be twice of this value, which is 0.78 W. The power dissipation of the microcontroller is 0.33 W. Hence, approximately 1 W power is dissipated in the gate drive circuit.
The MOSFETs are the prominent sources of loss within the converter. There are two categories of losses in MOSFETs i.e. the conduction loss and switching loss. Since in our design the MOSFETs are operated in saturation region the conduction loss is less as compared to switching loss. The switching loss occurs when the MOSFETs are in transition state and are more complicated to analyze as compared to conduction loss. The temperature profile of MOSFETs measured with IR thermal camera is given in the Fig. 10.

Figure 10. Temperature profile of MOSFET

The output rectifier also contributes to the losses of the converter. Although the schottky diodes have lowest forward voltage drop but compared to normal P-N junction diode its forward voltage increases more quickly with higher current. Analysis of switching loss of rectifier diode is complicated. Thermal profile of SR-1660 schottky diode is shown in Fig. 11.

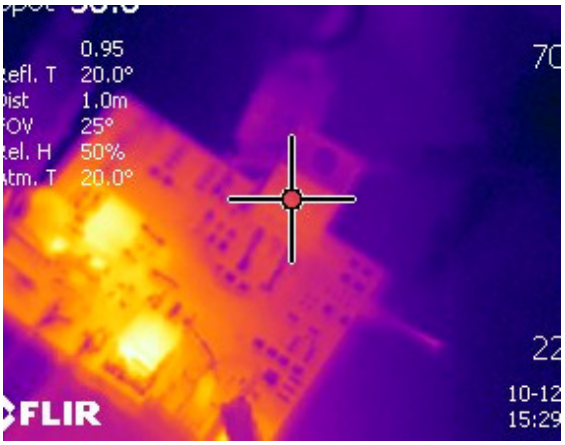


Figure 11. Temperature profile of Rectifier diode

Power loss in the transformer is computed according to equation 2 [2].

$$P_{loss} = |i_p|^2 R_{AC}(p) + |i_s|^2 R_{AC}(s) \quad (2)$$

Where R_{AC} *(p)* and R_{AC} *(s)* are AC resistance of the primary and secondary winding respectively and i_p and i_s is RMS current through primary and secondary winding respectively. At 2.5MHz, R_{AC} (p) and R_{AC}(s) of the transformer were calculated as mentioned in [10] and are given as 2.68Ω and 0.82Ω respectively. i_p and i_s were estimated to be 0.42A and 0.7A respectively. The power loss of transformer is estimated to be approximately 1.5W. The temperature profile of transformer is given in Fig. 12.

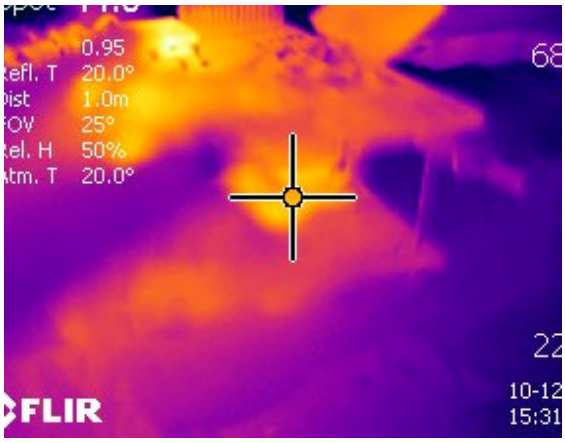


Figure 12. Temperature of transformer

By analyzing temperature profile, it can be inferred that the MOSFETs losses are dominant while transformer losses are less as compared to other circuit components.

IV. CONCLUSION

Compact, low cost and high density half bridge DC-DC converter was successfully designed and tested by implementation of the circuit on a printed circuit board. The converter was operated in MHz frequency region and maximum output power upto 40 W. The maximum energy of unregulated converter was approximately 82 %. The maximum energy efficiency as a function of input voltage, duty cycle and switching frequency was computed. Multilayered coreless PCB transformers used in the converter circuit have shown major contribution in the energy efficiency and compactness of the size. This research work is revolutionary step in the design of half bridge DC-DC converter, operating in MHz frequency region, using coreless PCB transformers. It is concluded that it is possible to design very small and compact switch mode power supplies in the future when better switching devices and techniques are developed.

REFERENCES

[1] Eberle, W.; Zhiliang Zhang; Yan-Fei Liu; Sen, P.C.; , "A Current Source Gate Driver Achieving Switching Loss Savings and Gate Energy Recovery at 1-MHz,"*Power Electronics, IEEE Transactions on* , vol.23, no.2, pp.678-691, March 2008.

[2] Hari Babu Kotte, Radhika Ambatipudi and Kent Bertilsson, "A ZVS Flyback DC-DC Converter Using Multilayered Coreless Printed-Circuit Board (PCB) Step-down Power Transformer," *Proceedings of World Academy of Science, Engineering and Technology,* Vol.70, pp 148-155, ISSN: 1307-6892, October 2010, Paris.

[3] Radhika Ambatipudi, Hari Babu Kotte and Kent Bertilsson, "Coreless Printed Circuit Board (PCB) Step-down Transformers for DC-DC Converter Applications," *Proceedings of World Academy of Science, Engineering and Technology,* Vol.70, pp 380-389, ISSN: 1307-6892, October 2010, Paris.

[4] Bob Bell, "Half-bridge topology finds high density power converter apps", http://www.powerdesignindia.co.in/STATIC/PDF/200810/PDIOL_2008OCT24_PMNG_TA_03.pdf?SOURCES=DOWNLOAD (last accessed December 22, 2010)

[5] MAXIM 125V/3A, High-Speed Half-Bridge MOSFET Drivers, "http://datasheets.maxim-ic.com/en/ds/MAX15018-MAX15019.pdf", (last accessed December 29, 2010)

[6] Radhika Ambatipudi, "Multilayered Coreless Printed Circuit Board (PCB) Step-down Transformers for High Frequency Switch Mode Power Supplies (SMPS)", *Licentiate Thesis 61, Mid Sweden University*, ISSN: 1652-8948, ISBN: 978-91-86694-40-1.

[7] Hari Babu Kotte, "High Speed (MHz) Switch Mode Power Supplies(SMPS) using Multilayered Coreless PCB Transformer technology Passive gate drive circuit using Coreless Printed Circuit Board (PCB) Signal Transformer", Licentiate Thesis 62, Mid Sweden University, ISSN: 1652-8948, ISBN: 978-91-86694-41-8.

[8] L. Lorenz, G. Deboy, A. Knapp and M. März, "COOLMOS™ - a new milestone in high voltage Power MOS", *Siemens AG, Semiconductor Division,* Balanstr. 73, 81541 Munich, Germany.

[9] Radhika Ambatipudi, Hari Babu Kotte and Kent Bertilsson,"Comparison of Two Layered and Three Layered Coreless Printed Circuit Board (PCB) Step-Down Transformers", Proceedings of *The 3rd International Conference on Power Electronics and Intelligent Transportation System* (PEITS 2010), November 20-21, Shenzhen , China.

[10] LM5111 Dual 5A Compound Gate Driver by National semiconductors Data sheet

High-Speed (MHz) Series Resonant Converter (SRC) Using Multilayered Coreless Printed Circuit Board (PCB) Step-Down Power Transformer

Hari Babu Kotte, *Member, IEEE*, Radhika Ambatipudi, *Member, IEEE*, and Kent Bertilsson

***Abstract*—In this paper, design and analysis of an isolated low-profile, series resonant converter (SRC) using multilayered coreless printed circuit board (PCB) power transformer was presented. For obtaining the stringent height switch mode power supplies, a multilayered coreless PCB power transformer of approximately 4:1 turn's ratio was designed in a four-layered PCB laminate that can be operated in megahertz switching frequency. The outermost radius of the transformer is 10 mm with achieved power density of 16 W/cm^2. The energy efficiency of the power transformer is found to be in the range of 87–96% with the output power level of 0.1–50 W operated at a frequency of 2.6 MHz. This designed step-down transformer was utilized in the SRC and evaluated. The supply voltage of the converter is varied from 60–120 V_{DC} with a nominal input voltage of 90 V and has been tested up to the power level of 34.5 W. The energy efficiency of the converter under zero-voltage switching condition is found to be in the range of 80–86.5% with the switching frequency range of 2.4–2.75 MHz. By using a constant off-time frequency modulation technique, the converter was regulated to 20 V_{DC} for different load conditions. Thermal profile with converter loss at nominal voltage is presented.**

***Index Terms*—DC–DC power converters, high-frequency magnetics, megahertz frequency, transformers.**

I. Introduction

LOTS OF research is progressing in the semiconductor and magnetic fields in order to meet the ever increasing demand for the low-profile, low-power, high-power density and highly energy efficient converters for portable appliances. Current switching frequencies of the commercially available isolated power converters are typically in the range of 100–500 kHz. Operating the converters from several hundred kilohertz to megahertz leads to a low-profile and high-power density converter with the reduction of passive elements size such as inductors, transformers, and energy storage capacitors [1]–[4]. However, the increased switching frequencies of a converter impose challenges such as core losses of core-based transformers/inductors, skin and proximity effects due to the induced eddy currents in the windings, dielectric losses [5], switching losses of power devices, and the increased gate drive power consumption of the converter that are frequency dependent and hence cannot be ignored. In order to eliminate the core losses that are predominant in a high-frequency region, development in magnetic field shows that the air core, i.e., coreless printed circuit board (PCB) planar transformers can be a potent alternative to the existing core-based transformers in several megahertz switching frequencies for low-medium power applications. In the earlier research, it has been demonstrated that these coreless PCB transformers can be used as an isolation transformer for both signal and power transfer applications in the power range of 0.5–100 W with higher energy efficiencies in a megahertz switching frequency region [6]–[8]. Even though there exists no magnetic core, the skin and proximity effects of the conductors play a dominant role at higher operating frequencies. Therefore, the recent study on the winding strategies, i.e., by introducing an optimum hollow factor [9] in the circular spiral inductor shows that the losses of the windings at higher operating frequencies can be reduced along with the improvement of the quality factor. Apart from this, different winding strategies were also investigated [1] to reduce the parasitic capacitances of multilayered coreless PCB inductor in order to operate in a wide operating frequency region.

Since most of the switch mode power supplies (SMPS) applications such as laptop adapters, LCD monitors, etc., demand step-down conversion ratios, the research has been also focused on the design, analysis, and application potential of multilayered coreless PCB step-down transformers. In previous works [10], [11], the authors have demonstrated that various multilayered coreless PCB step-down transformers of different turn's ratio evaluated for sinusoidal/square wave excitation are highly energy efficient in the megahertz frequency region. Therefore, these multilayered coreless PCB step-down power transformers were utilized in various single-ended topologies such as flyback, cascode flyback converters [12]–[14] to achieve low-profile converters. However, when these converters are operated in the megahertz switching frequency region, it is recommended to implement the soft-switching techniques such as zero-voltage switching (ZVS)/zero-current switching (ZCS) to reduce the switching losses, which in turn increases the stresses of the MOSFETs and conduction losses [15]. Since for the given power transfer application at a given switching frequency, the size of the power transformer in double-ended topologies compared to single-ended ones can be reduced [16], [17] because of the full utilization of the transformer. Due to this reason, the double-ended topologies such as half-bridge, full-bridge, and push–pull are becoming more popular in modern days for

Manuscript received February 8, 2012; revised April 24, 2012; accepted June 24, 2012. Date of current version October 12, 2012. Recommended for publication by Associate Editor R.-L. Lin.

The authors are with the Department of Information Technology and Media, Mid Sweden University, Sundsvall SE-85170, Sweden (e-mail: Hari.Kotte@miun.se).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2012.2208123

low-medium power applications especially in telecom and automotive industries [17]. Also, the copper losses of the transformer can be reduced in double-ended topologies compared to single-ended converters due to the reduction of the transformer size. For operating the converters in the megahertz frequency region, resonant converters such as series resonant, parallel resonant, series–parallel, and *LLC* resonant converters are suitable where the switching losses of the converter at the switch transitions can be decreased dramatically. In these resonant converters, since the switch currents/voltages are processed in sinusoidal manner, the losses at the transitions and electromagnetic interference (EMI) emissions of the converter get reduced [18]. This also results in the high-frequency operation of the converter possessing low MOSFET stress without sacrificing the energy efficiency. Series resonant converters (SRCs) operated above resonant frequency have many advantages such as inherent short-circuit protection, ZVS conditions, reduced harmonics, utilization of transformer leakage inductance, [19], etc.

In this regard, a multilayered coreless PCB step-down center-tapped power transformer of approximately 4:1 turn's ratio with the dimensions of 20 mm $\times$ 20 mm $\times$ 1.48 mm operating in the megahertz frequency region was designed and evaluated. Here, for driving the high-side MOSFET of the SRC, a multilayered coreless PCB signal transformer of 1:1 turn's ratio was also designed and assessed. Even though the SRC has the disadvantage of uncontrollability of the output voltage at light load conditions [19], due to its numerous advantages as discussed earlier, in this paper the design, analysis with simulation and experimental results of the SRC using multilayered coreless PCB signal and power transformer were presented.

II. Multilayered Coreless PCB Power and Signal Transformers

A. Design Methodology of Multilayered Coreless PCB Power Transformer

One of the limiting factors for operating isolated converter topologies in the megahertz switching frequency region is core losses of transformer that are frequency dependent [20]. Therefore, in order to operate the converter in a high-frequency region, a multilayered center-tapped coreless PCB step-down power transformer was designed. Since in case of coreless PCB transformers, the total self-inductance is dependent on the geometrical parameters of the primary/secondary windings, it is required to choose these parameters in an optimal manner in order to design an efficient transformer. For a given power transfer application, based upon the topology, specified input/output voltages and frequency "*f*" of operation, the inductance and the turn's ratio required for the transformer can be obtained. The coreless PCB transformer operation is based on the resonance phenomena between leakage inductance and the external resonant capacitor. Therefore, by assuming a leakage inductance of about 10% of its self-inductance, based upon the required operating frequency of the transformer, a resonant capacitor is selected. Here, for the power transfer application of 50 W, the estimated primary inductance of the transformer is found to be approximately in the range of 6–8 μH in the operating frequency of 2–4 MHz with the transformer turn's ratio of 4:1. A hollow winding factor that is defined as the ratio of inner radius "$R_{\rm in}$" to that of the outermost radius "$R_{\rm out}$" [9] is considered as 0.45, in order to increase the quality factor "*Q*" and hence to reduce the dc resistance of the transformer. Here, the inner radius of the transformer is considered as 4.5 mm that results in the outermost radius of approximately 10 mm. For increasing the effect of hollow factor, the width "w" of the winding should be considered as at least ten times of the skin depth corresponding to the operating frequency [9] of transformer. Here, it is approximately 8–10 times its skin depth corresponding to the operating frequency region of 2–4 MHz by also taking into the consideration of current carrying capability of the conductors. In order to increase the amount of inductance for the given radius, the separation between tracks "*s*" should be as close as possible within the manufacturing capability. Here, in this case, it was considered as half of the width of the trace width "*w*." This gives a larger amount of inductance with high-quality factor and low ac resistance. To meet the isolation requirements between primary and secondary windings of the transformer, the PCB laminate thickness "*t*" of about 0.4 mm is considered. Transformer's PCB laminate is FR4 material whose breakdown voltage is of 50 kV/mm approximately [21]. The height of the conductor is considered as 70 μm for all the windings of the transformer. This can be reduced to decrease the ac resistance of transformer with the expense of increased dc resistance. In order to attain the desired amount of primary/secondary inductances of transformer by using the aforementioned geometrical parameters, the calculations were done by using the Hurley and Duffy method [22].

B. Geometrical and Electrical Parameters of Designed Multilayered Coreless PCB Power Transformer

The cross-sectional view and 3-D view of the designed coreless PCB power transformer are shown in Fig. 1(a) and (b), respectively. The transformer has two primaries on the first and fourth layers, whereas its secondary windings are sandwiched in between the two primaries in order to ensure better coupling between the windings. The number of turns "*N*" in each layer of the four-layered PCB is 12 with a track width "w"/separation "*s*" of 0.34/0.17 mm, respectively. The height of copper track "*h*" is 70 μm, and the thickness of the PCB substrate "*t*" is 0.4 mm resulting in the total height of the transformer "*T*" as 1.48 mm.

The two primaries of first and fourth layer are connected in series and hence the total number of primary turns is 24. Since it is required to carry larger amount of currents on the secondary side compared to primary, two windings are paralleled on the secondary side that leads to six number of turns resulting a 12:6:6:12 primary–secondary–secondary–primary (PSSP) structured multilayered coreless PCB center-tapped power transformer.

In the series resonant converter, the leakage inductance of transformer plays a dominant role in determining the resonant frequency of the circuit. So, it is highly beneficial if the sufficient leakage inductance is attained by the designed transformer itself so that the size of the external inductor can be reduced or in some

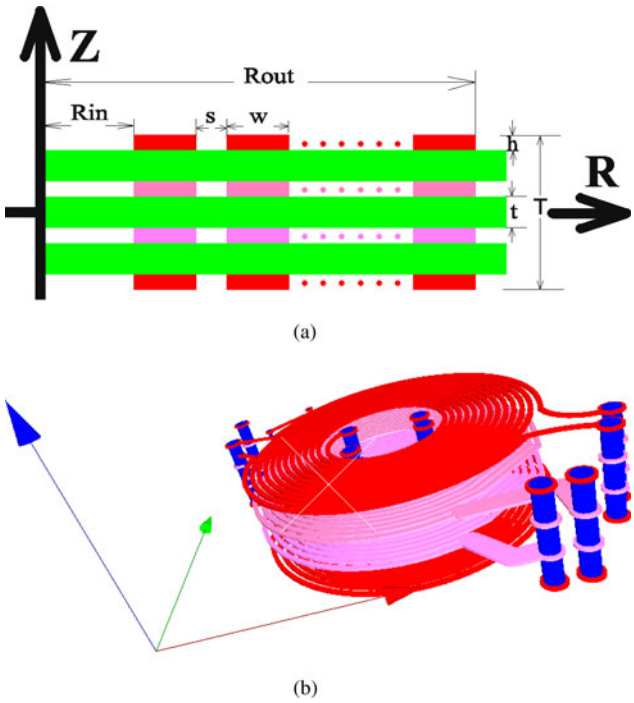


Fig. 1. (a) Cross-sectional view of multilayered coreless PCB power transformer in *R–Z* plane. (b) Three-dimensional view of the multilayered coreless PCB power transformer of PSSP structure.

cases it can be avoided. Therefore, in terms of leakage inductance point of view, among the various structure of transformers such as PSSP, secondary–primary–primary–secondary (SPPS), and primary–secondary–primary–secondary (PSPS) [23], [24] it is better to use the transformer of either PSSP or SPPS structure compared to PSPS. Also in case of interleaved structure, i.e., PSPS, the isolation requirement is higher between the layer stack up, whereas for the other structures such as PSSP and SPPS, the distance between the two adjacent intrawinding layers can be reduced. In coreless PCB transformer where copper losses are dominant, it is recommended to have lower ac resistance in order to reduce the losses in the transformer and thereby in converter circuit. Hence, PSSP structure that attains lower resistance compared to SPPS was taken into consideration compared to other structures for designing the high-frequency multilayered coreless PCB step-down power transformer.

The electrical parameters of the designed coreless PCB transformer are measured by using the precision *RLC* meter HP 4284A at 1 MHz. The measured self-inductances "L_p/L_s" of the primary/secondary windings are obtained by open circuiting the opposite winding of the transformer and are recorded as 7.89 and 0.64 μH, respectively. Since the leakage inductances "L_{lkp}/L_{lks}" play a prominent role in the resonant converter circuits, it is important to measure the leakage inductance precisely. Therefore, the primary/secondary leakage inductances are obtained by solder shorting the opposite winding of the transformer and corresponding values for the designed transformer are 1.95/0.16 μH. All the interconnections while taking the measurements were minimized in order to achieve exact electrical parameters. The turn's ratio "n" of the designed transformer obtained from measured self-inductances of primary/secondary is 3.51 that can be obtained as follows:

$$n = \sqrt{\frac{Lp}{Ls}}. \tag{1}$$

The interwinding capacitance "C_{ps}" between the primary and each secondary winding of transformer is found to be 30 pF and the intrawinding/self-capacitance "C_{pp}/C_{ss}" is found to be negligible. The calculated coupling coefficient (K) obtained from the measured parameters of the transformer is 0.75. The measured dc resistance of the primary/secondary winding of the transformer per layer using Agilent 34405A digital multimeter is 0.52/0.10 Ω, respectively. Due to the eddy current phenomena, the winding losses get increased as the frequency increases causing both the skin and proximity effects. Since, it is a four-layered PCB power transformer, proximity losses are dominant compared to the losses incurred by the skin effect. Hence, it is necessary to estimate the ac resistance of primary/secondary windings of transformer in the desired operating frequency region. The ac resistance of the transformer in "m^{th}" layer can be obtained by using the following expression [25], [26]:

$$R_{\text{ac},m} = R_{\text{dc},m} \cdot \frac{\xi}{2}\left[\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi} + (2m-1)^2 \cdot \frac{\sinh\xi - \sin\xi}{\cosh\xi + \cos\xi}\right] \tag{2}$$

where

ξ $= h/\delta$;
$R_{\text{dc},m}$ dc resistance of the winding in the corresponding layer;
h height of conductor;
δ skin depth in a conductor;
m number of layers in a winding section where MMF reaches from 0 to maximum value.

In the previous expression, the first term represents skin effect whereas the second term describes the proximity effect. In this transformer, where the structure is of PSSP, "m" tends to unity whereas for the other noninterleaved transformer windings it is greater than unity [26]. The calculated ac resistance of both primary/secondary windings of transformer using the aforementioned expression is illustrated in Fig. 2.

C. Performance Characteristics of Designed Multilayered Coreless PCB Power Transformer

The deterministic features of operating frequency of transformers such as transfer function *H(f)* that is defined as the ratio of the magnitude of secondary voltage V_{sec} to that of the primary voltage V_{pri} of transformer, input impedance Z_{in} [10], [27] were measured with the help of RF power amplifier, BBM0A3FKO by giving sinusoidal excitation. The load resistance R_L is of 10 Ω and a resonant capacitor C_{res} of 6.8 nF is connected across the secondary terminals of transformer. These characteristics along with measured energy efficiency of the transformer are plotted in Fig. 3. The maximum gain frequency of transformer from the transfer function *H(f)* plot under loaded conditions in Fig. 3 is found to be 8 MHz, whereas the maximum impedance

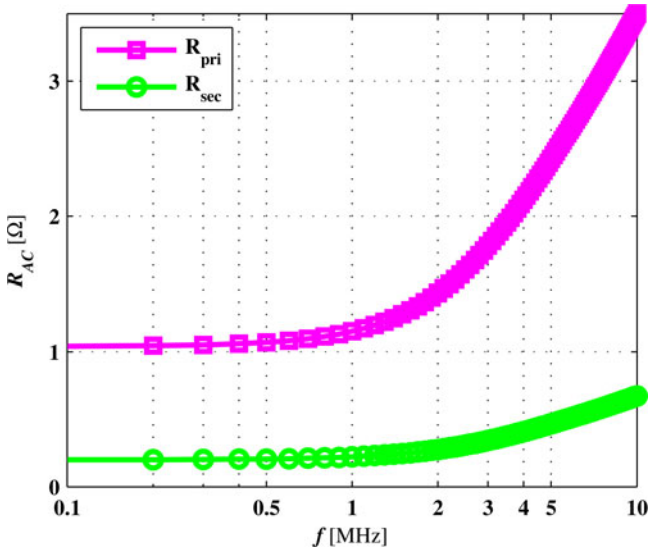


Fig. 2. Calculated ac resistance of primary/secondary windings of the multilayered coreless PCB step-down power transformer.

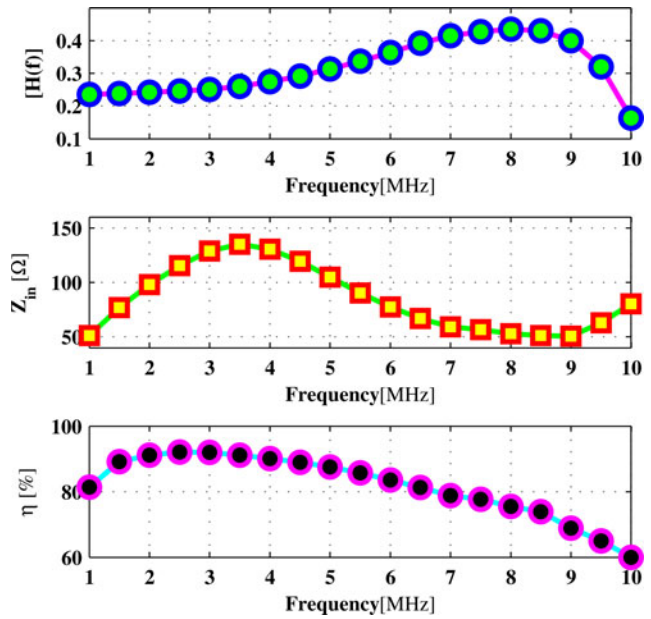


Fig. 3. Measured transfer function "*H (f)*," input impedance "$Z_{\rm in}$" and efficiency "η" at R_L of 10 Ω, with $C_{\rm res}$ of 6.8 nF.

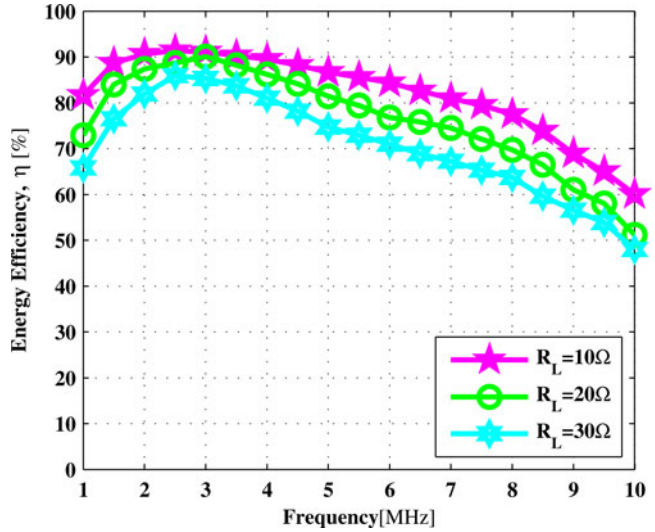


Fig. 4. Measured energy efficiency of coreless PCB step-down power transformer for different loads, with $C_{\rm res} = 6.8$ nF.

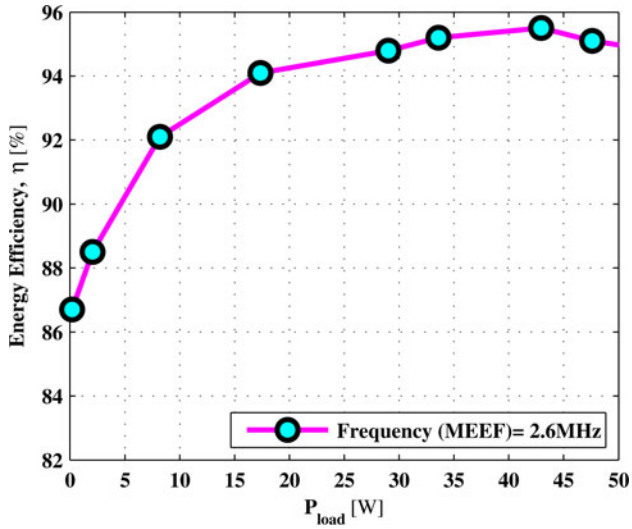


Fig. 5. Measured energy efficiency of coreless PCB step-down power transformer at R_L of 10 Ω, with $C_{\rm res} = 6.8$ nF at a frequency (MEEF) of 2.6 MHz.

frequency (MIF) is 3.5 MHz with an input impedance of 135 Ω approximately. As mentioned in [27] and [28] for power transfer application, the maximum energy efficiency frequency (MEEF) of the transformer is less than the MIF. In this case, MEEF of the transformer is found to be 2.6 MHz with an energy efficiency of 92% approximately. At the MEEF, the input voltage fed to the primary winding of transformer is 45 $V_{\rm rms}$, and then the secondary voltage is found to be 10.5 $V_{\rm rms}$ at a load resistance of 10 Ω resulting in the output power of 10.5 W. The measured energy efficiency of transformer is illustrated in Fig. 4 under different loaded conditions with a resonant capacitor of 6.8 nF. It can be observed from Fig. 4 that the energy efficiency of transformer is maximum for all the loads at MEEF of transformer as discussed earlier. Since the transformer is utilized for power transfer application, the energy efficiency of transformer as a function of the load power is required. Therefore, the power test of transformer is reported at MEEF in the output power range of 0.1–50 W with sinusoidal excitation. The energy efficiency of transformer with respect to output power level for the optimal load condition of 10 Ω is illustrated in Fig. 5. From Fig. 5, it can be observed that energy efficiency of the transformer is in the range of 87%–96% for the load power range of 0.1–50 W at a frequency of 2.6 MHz. Under these conditions, the maximum power density of transformer is reported to be 16 W/cm^2. The primary/secondary voltage and current waveforms of transformer at 2.6 MHz with a load power of 20 W are depicted in Fig. 6. The waveforms are captured with the help of Tektronix TPS2024 four-channel isolated oscilloscope

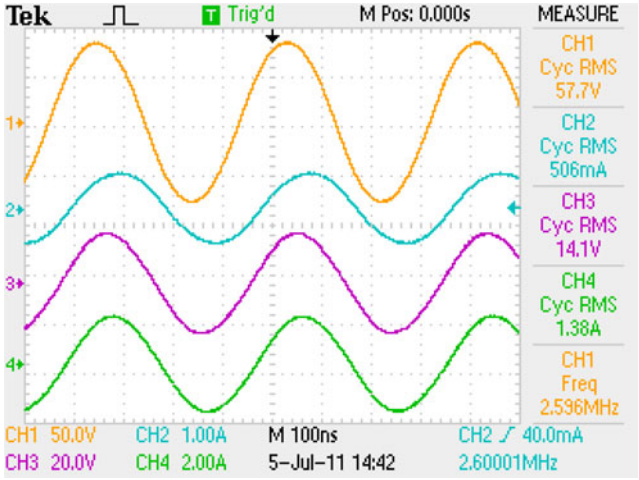


Fig. 6. Measured waveforms of transformer with $C_{\rm res}$ = 6.8 nF and R_L = 10 Ω. CH1—$V_{\rm pri}$ (50 V/div), CH2—$I_{\rm pri}$ (1 A/div), CH3—$V_{\rm sec}$ (20 V/div), CH4—$I_{\rm sec}$ (2 A/div).

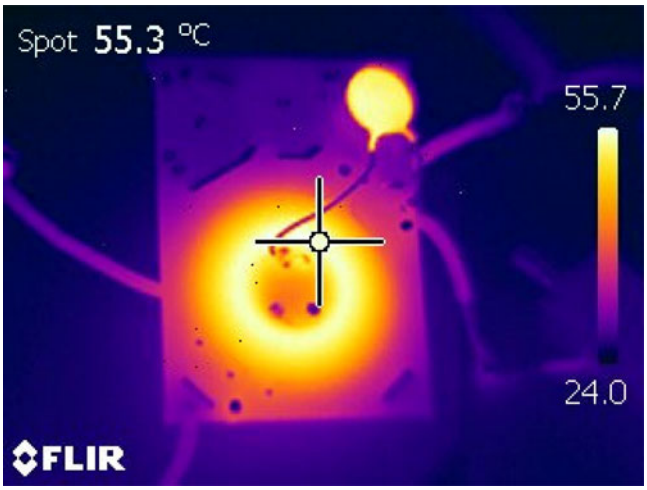


Fig. 7. Thermal profile of coreless PCB power transformer with $C_{\rm res}$ = 6.8 nF, operating frequency of 2.6 MHz with a load power of 20 W and ambient temperature of 25 °C.

whose bandwidth is 200 MHz. The primary/secondary voltages are measured using voltage probes P5120/P2220, respectively, whereas the currents flowing in transformer are obtained using Tektronix ac current probes CT2. The corresponding thermal profile of transformer at a power level of approximately 20 W was recorded with IR thermal imaging camera and shown in Fig. 7. The temperature of transformer at this power level is found to be 55.3 °C with an ambient temperature of 25 °C.

Since the operating frequency of transformer can be varied with the help of external resonant capacitor "$C_{\rm res}$," the effect of resonant capacitors on transformer was determined.

The measured energy efficiency of transformer by varying the resonant capacitors at an optimal load resistance of 10 Ω is illustrated in Fig. 8. It can be observed that MEEF of transformer is moved toward lower operating frequencies by increasing the value of external resonant capacitor. Since the power transformer possesses the desired conditions for power transfer application, the transformer was utilized in the SRC and evaluated.

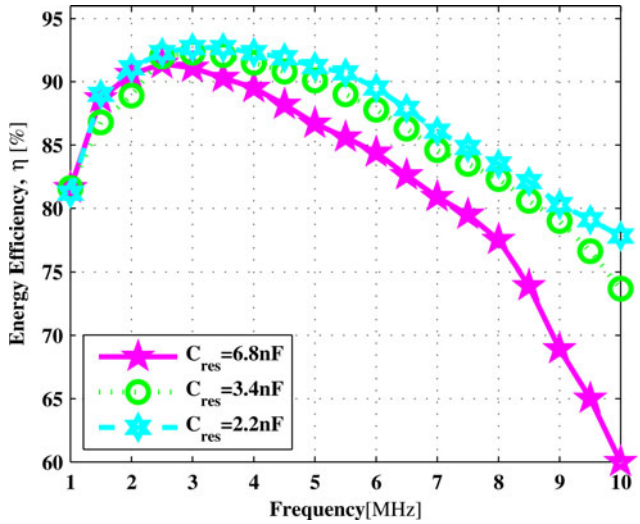


Fig. 8. Measured energy efficiency of coreless PCB step-down power transformer for various resonant capacitors at R_L of 10 Ω.

D. Signal Transformer

Converter circuit topology plays an important role particularly while utilizing the coreless PCB transformer for power transfer applications in terms of radiated emissions [29] because of the absence of magnetic core. If the transformer is utilized in single-ended topologies such as flyback, forward, etc., since the current waveforms are nonsinusoidal in nature, the amount of radiated emissions from the coreless PCB transformers are high compared to double-ended topologies. In addition to this as discussed earlier, for the given power transfer application, size of the transformer gets reduced in the double-ended converter that leads to maximum utilization of the transformer compared to single-ended topologies. Based upon the previous conclusions, a double-ended series resonant converter topology was chosen for characterizing the designed multilayered coreless PCB step-down transformer for power transfer applications.

For driving the high-side MOSFET in the SRC, a high-side MOSFET driver capable of operating in the megahertz frequency region and at high input voltages is required. However, there exists no commercially available MOSFET gate driver according to author's knowledge exceeding the input voltage of 125 V and 1-MHz switching frequency [30]. Therefore, it is required to design a gate drive circuitry capable of driving the high-side MOSFET at higher switching frequencies with galvanic isolation. In this regard, a transformer was designed in a multilayered PCB in order to reduce area of the transformer, resistance of the winding for the same amount of inductance compared to two-layered transformer and also for reduction of radiated EMI [11], [29]. A four-layered signal transformer of 1:1 turn's ratio where two primaries/secondaries are connected in series was designed. The prototype along with the dimensions of signal transformer and power transformer is illustrated in Fig. 9(a) and (b), respectively.

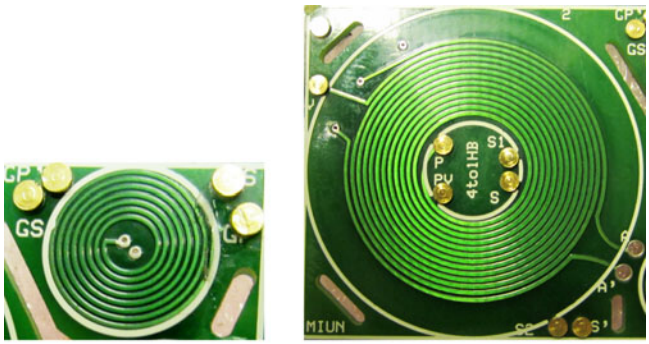


Fig. 9. (a) Coreless PCB signal transformer (8.75 mm × 8.75 mm × 1.48 mm) and (b) power transformer (20 mm × 20 mm × 1.48 mm).

For signal transfer applications, it is desirable to operate the coreless PCB transformers at the "MIF" [31] in order to minimize the gate drive power consumption of the circuit. Therefore, for a given application, the desired inductance of the transformer is determined by knowing the input capacitance of the MOSFET that acts as resonant capacitor, for achieving MIF in the operating frequency region of the converter. From the initial estimations by knowing the peak input voltage of the transformer "$V_{\rm peak}$," Frequency of operation "*f*," MOSFET input capacitance that determines the peak current "$I_{\rm peak}$" the required amount of primary inductance of the gate drive transformer was determined. In order to operate the gate drive circuit in the frequency range of 2–4 MHz, for the MOSFET load capacitances of 100–1000 pF, ideally it is required to have the transformer primary inductance in the range of 1.5–3 μH.

The geometrical parameters of signal transformer such as width "*w*"/separation "*s*" of the winding are 0.22/0.18 mm, respectively. The number of turns of the primary/secondary is 16 with an outermost radius of 4.4 mm. The electrical parameters of the designed signal transformer measured at 1 MHz such as self-/leakage inductance of primary/secondary are 1.01/0.26 and 1.28/0.33 μH, respectively. Since the designed transformer possesses lower inductance compared to the estimated inductance as discussed earlier, and also in order to reduce the magnetizing current through the transformer and hence the gate drive power consumption, high-frequency NiZn ferrite plates whose radius is of 5 mm with the thickness of approximately 1.5 mm were utilized. The electrical parameters of the designed signal transformer along with ferrite plates measured at 1 MHz such as self-/leakage inductance of primary/secondary are 1.95/0.45 and 1.85/0.44 μH, respectively, which are measured as discussed in the previous section. The interwinding capacitance of transformer is 11 pF with the coupling coefficient of 0.76. The dc resistance of primary/secondary winding is 0.64 Ω. Since the MOSFET load is a parallel combination of resistance and capacitance, a load consisting of 100 Ω and 1000 pF is connected across the secondary winding of the transformer. With the sinusoidal excitation, the performance characteristics of signal transformer such as transfer function *H(f)*, $Z_{\rm in}$, and energy efficiency are illustrated in Fig. 10.

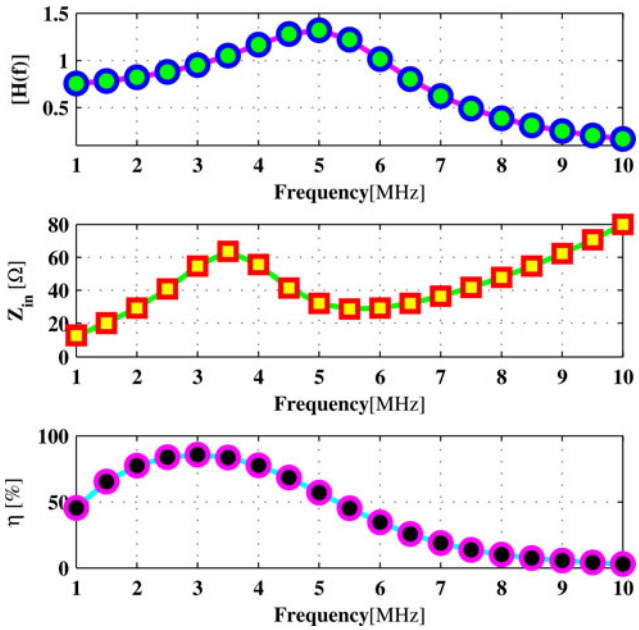


Fig. 10. Measured transfer function "*H(f)*," input impedance "$Z_{\rm in}$" and efficiency "η" of signal transformer at R_L of 100 Ω, with $C_{\rm res}$ of 1000 pF.

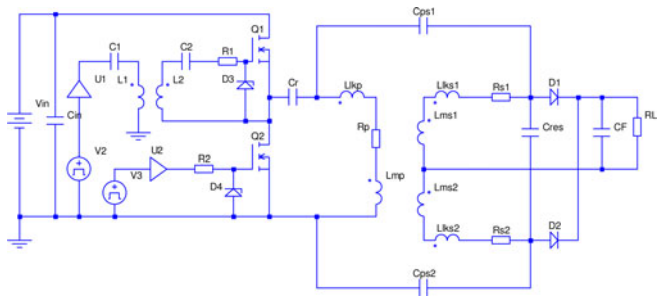


Fig. 11. Schematic diagram of the SRC using multilayered coreless PCB signal and power transformers.

The characteristics from Fig. 10 illustrate that the transfer function/voltage gain of the transformer is high with sufficient input impedance and energy efficiency within the wide frequency range of 1–4 MHz. Hence, this transformer was utilized in the gate drive circuitry of the SRC for driving high-side MOSFET in the megahertz switching frequency region and evaluated.

III. SRC

An SRC is considered by connecting the resonant elements such as L_r and C_r in series with that of the load as illustrated in Fig. 11.

The resonant element "L_r" can be obtained from measured primary and secondary leakage inductances and turn's ratio of transformer by using (3) and it is of 3.94 μH

$$L_r = L_{lkp} + n^2 L_{lks}. \tag{3}$$

A series resonant capacitor "C_r" of 1.36 nF is utilized in the SRC and therefore resonant frequency of the converter is

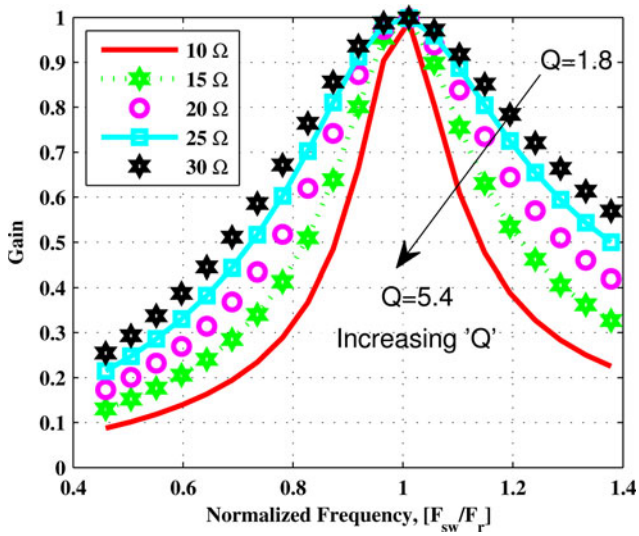


Fig. 12. DC gain characteristics and quality factor "Q" of the SRC using multilayered coreless PCB power transformer.

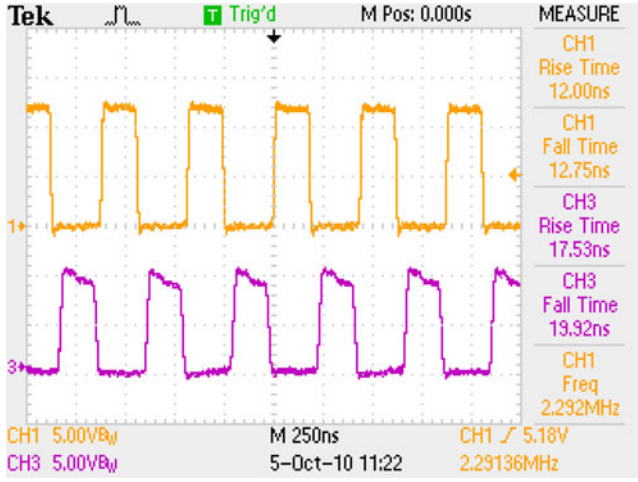


Fig. 13. Measured gate drive signals of low side "Q_2"—CH1 and high-side "Q_1"—CH3 power MOSFETs.

2.17 MHz that is obtained as follows:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}. \tag{4}$$

The characteristic impedance "$Z_{\rm ch}$" of the circuit is given as

$$Z_{\rm ch} = \sqrt{\frac{L_r}{C_r}}. \tag{5}$$

The quality factor "Q" of the SRC is obtained from the characteristic impedance "$Z_{\rm ch}$" and load resistance "R_L"

$$Q = \frac{Z_{\rm ch}}{R_L}. \tag{6}$$

Since for MOSFETs, ZVS is preferred compared to ZCS [32] the optimal operating condition of the SRC is obtained above resonant frequency "f_r" of tank circuit. Therefore, the switching frequency of the converter should be greater than 2.17 MHz. In this region, the converter is ensured to be operated in ZVS conditions and hence the turn-on losses in switching devices get minimized that increases the overall energy efficiency of the converter. The dc gain characteristics from [33] of the SRC for load variation of 10–30 Ω are illustrated in Fig. 12. Here, below "f_r," the converter is said to be operated in ZCS whereas above "f_r" it operates in ZVS condition.

It can be observed that the dc gain of SRC is always less than unity as the resonant tank elements, and load forms voltage divider circuit. The dc gain is observed to be maximum at resonant frequency "f_r."

IV. Converter Prototype With Simulation and Experimental Results

In order to achieve lower leakage inductance in the conventional transformer, generally the interleaved structure (PSPS) is employed compared to other structures. However, if the conventional transformer has to be utilized for the resonant converter circuits, in order to achieve the desired leakage inductances, it is required to either introduce the air gap in the transformer or to utilize the external resonant inductor to operate it in the high-frequency region. By introducing the air gap, there exist several challenges to be faced in conventional transformers such as the nonuniform current distribution in the windings, lower magnetizing inductance, etc., with which the energy efficiency of the transformer and hence the converter gets reduced at higher operating frequencies [34], [35]. On the other hand, if the external inductor has to be utilized, the power density and the energy efficiency of the converter get reduced. Due to the aforementioned drawbacks in the conventional transformer, especially in high-frequency dc–dc converter applications, the multilayered coreless PCB step-down power transformers can be utilized. Therefore, the high-frequency dc–dc SRC with the multilayered coreless PCB power and signal transformers was tested and evaluated in this section in the megahertz frequency region. The high-side and low-side MOSFETs "Q_1" and "Q_2" selected according to specifications in converter circuit are ZXMN15A27K whose breakdown voltage is $V_{\rm dsMax}$ of 150 V and $R_{\rm ds(on)}$ of 0.65 Ω. The required gate drive signals are provided by using 1.04-ns resolution dsPIC microcontroller strengthened by the MOSFET driver LM5111. Here, the low-side MOSFET "Q_2" was directly driven from one of the MOSFET driver outputs using a gate resistance "R_2." The other output of MOSFET gate driver is given to the primary side of signal transformer as shown in Fig. 11 and the secondary side signal is level shifted by using a series capacitor "C_2" and a zener diode "D_3." This signal is fed to high-side MOSFET "Q_1" and both these low-side CH1 and high-side signals CH3 at a switching frequency of approximately 2.3 MHz with corresponding rise and fall times are depicted in Fig. 13. Here, the resistor "R_1" is placed in series with that of the capacitor "C_2" for limiting the current through the zener diode "D_3." In order to prevent the short through currents in MOSEFTs of the converter, a dead time of 34 ns is provided in between high-side and low-side MOSFETs.

The rectifier diodes "D_1" and "D_2" utilized on secondary side of the converter are SR1660 Schottky diodes whose reverse

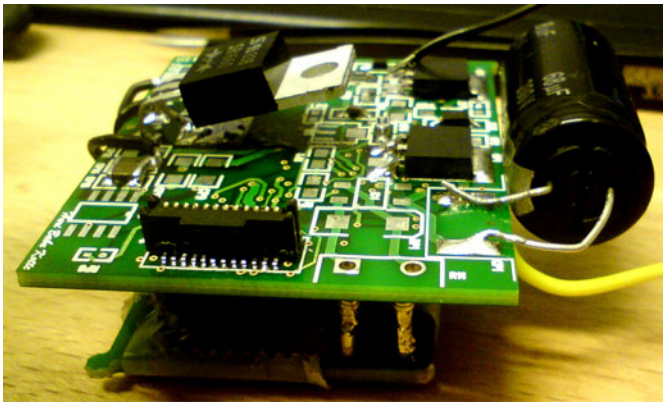


Fig. 14. Prototype of the SRC (45 mm × 35 mm) including coreless PCB transformers.

blocking voltage is 60 V with maximum average forward current rating of 16 A. The series resonant capacitor "C_r" placed in the converter is of 1.36 nF whose voltage rating is of 200 V with $\pm 5\%$ capacitance tolerance. The SRC prototype including controller and transformers is illustrated in Fig. 14. Here, controller and converter parts are on either side of PCB and coreless PCB power and gate drive transformers are connected by using interface pins.

The converter was operated with following specifications: dc input voltage range of 60–120 V with $V_{\rm nominal}$ of 90 V, with the load variation of 10–30 Ω in steps of 5 Ω. A resonant capacitor "$C_{\rm res}$" of 240 pF is connected across secondary winding of transformer in order to bring MEEF in the range of 2–3 MHz in the SRC. The choice of the resonant capacitor to improve the energy efficiency of transformer was such that the resonant frequency of the converter circuit is unchanged. Here, the external resonant capacitor "$C_{\rm res}$" and the interwinding capacitance "$C_{\rm ps1}$" of transformer together referred to the primary side [27] is given by (7) and it is 33.0 pF that is negligible and hence do not affect the characteristics of SRC

$$C_{\rm res'} = \left(\frac{1}{n^2}\right) \cdot 2 \cdot C_{\rm res} + \left(\frac{1-n}{n^2}\right) \cdot C_{\rm ps1}. \qquad (7)$$

Therefore, with the help of external resonant capacitor "$C_{\rm res}$," the energy efficiency of the converter was improved by 1–2% compared to without any external secondary resonant capacitor and maintained high in this frequency region without changing the characteristics of the SRC. The converter was initially simulated using SiMetrix software by modeling high-frequency SRC for the aforementioned conditions.

The measured energy efficiency of the unregulated converter for different load conditions in terms of input voltage variation with a duty cycle ratio of 82% is illustrated in Fig. 15. From this figure, it can be observed that the energy efficiency of the converter is approximately 86.2% where the input/output voltage of the converter is 120/20.13 V at a switching frequency of 2.63 MHz.

The energy efficiency of the converter is obtained maximum at the full load of 15 Ω and it is decreasing in nature for varied load resistances. The input and output power level of the converter

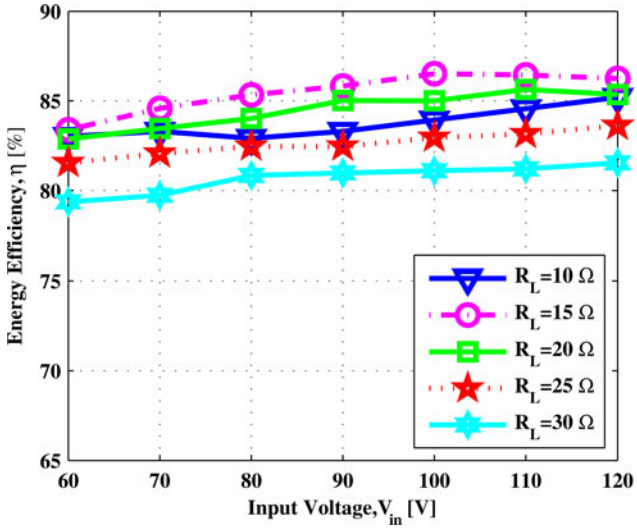


Fig. 15. Measured energy efficiency of the SRC for varied input voltage "$V_{\rm in}$," with different load conditions.

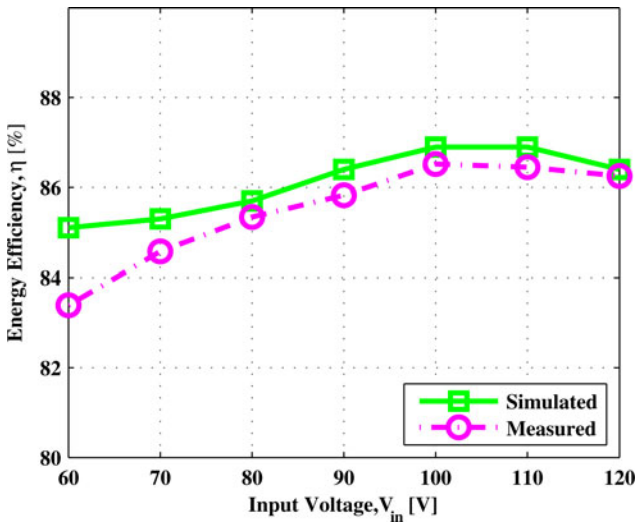


Fig. 16. Simulated and measured energy efficiency of the SRC for $R_L = 15\ \Omega$.

under these conditions is approximately 31.3/27 W, respectively. The tested maximum output power of the converter at 10-Ω load resistance is 34.5 W with input/output voltages of 120/18.6 V and the achieved energy efficiency under these conditions is reported to be 85.2%.

At an optimal load resistance "R_L" of 15 Ω, the simulated and measured energy efficiency of the converter is illustrated in Fig. 16. From this figure, it can be observed that the simulated and measured energy efficiency of the converter is in good agreement with each other. The simulated and measured waveforms for the nominal input, $V_{\rm nominal}$ of 90 V are illustrated in Figs. 17 and 18, respectively. Figs. 17 and 18 show the gate to source voltage fed to low-side MOSFET $V_{\rm gs}$, drain to source voltage of low-side MOSFET $V_{\rm ds}$, primary voltage $V_{\rm pri}$ and current $I_{\rm pri}$ fed to transformer. Here, the SRC is operated under ZVS conditions at a switching frequency of 2.63 MHz that can be observed from drain to source voltage of the converter in

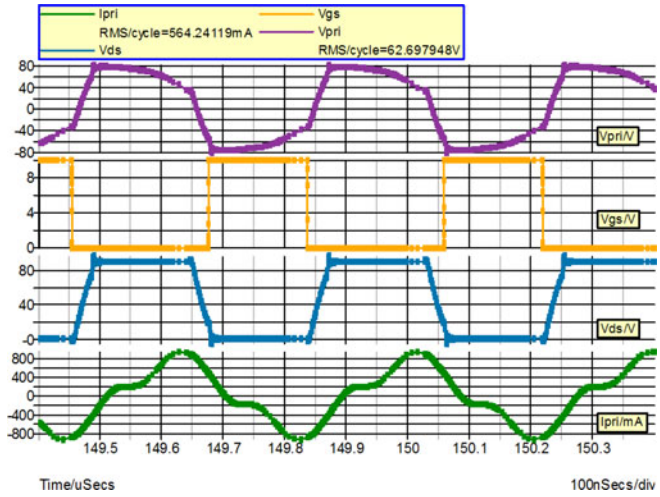


Fig. 17. Simulated waveforms of SRC for V_{nominal} and $R_L = 15\ \Omega$.

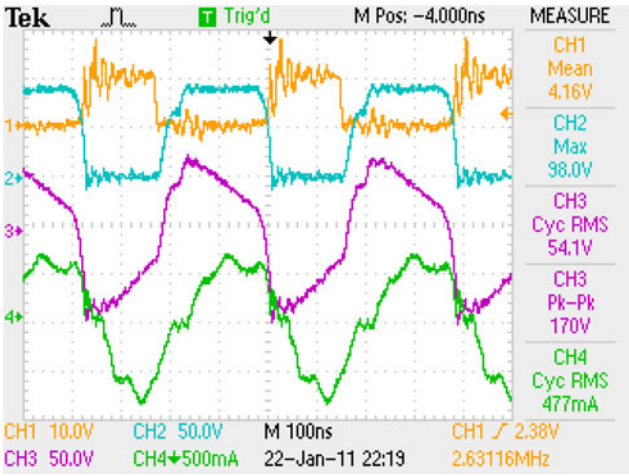


Fig. 18. Measured waveforms with $R_L = 15\ \Omega$. CH1—V_{gs} (10 V/div), CH2—V_{ds} (50 V/div), CH3—V_{pri} (50 V/div), CH4—I_{pri} (500 mA/div).

Fig. 18. The maximum drain–source voltage of the MOSFET at this condition is 98 V. The corresponding captured waveforms of the primary and half of the secondary winding voltages and currents of the transformer are illustrated in Fig. 19.

A. Loss Estimation of the Series Resonant Converter

At nominal input voltage V_{nominal} of 90 V, the losses of the converter were estimated and determined the contribution of the losses by the elements of the circuit approximately. The measured input/output powers of the converter are 16.74/14.36 W, respectively, at the nominal input voltage of 90 V. The energy efficiency of the converter is approximately 86% with a resistive load of 15 Ω. The total power loss of the converter is 2.38 W. The major losses in the converter are contributed by coreless PCB transformer, MOSFETs, and rectifier diodes of the circuit. The measured rms currents of primary/half of the secondary winding of transformer are 0.47/0.67 A, respectively. From the calculated ac resistance of power transformer shown in Fig. 2, at a particular switching frequency of the converter,

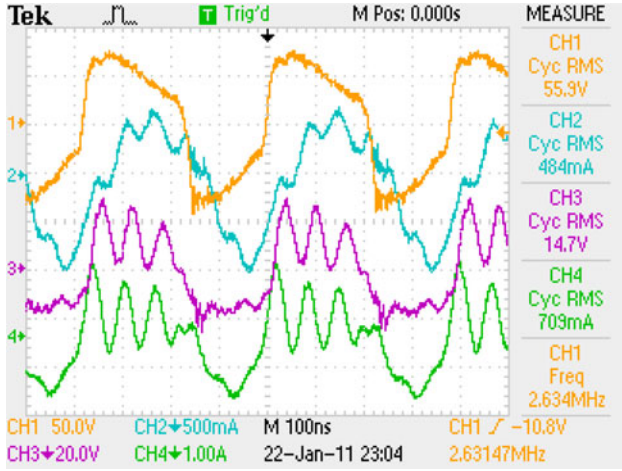


Fig. 19. Measured waveforms with $R_L = 15\ \Omega$, CH1—V_{pri} (50 V/div), CH2—I_{pri} (500 mA/div), CH3—V_{sec} (20 V/div), CH4—I_{sec} (1 A/div).

i.e., at 2.63 MHz, the primary/secondary copper losses of transformer are estimated. The total winding losses of transformer is found to be approximately 1 W. The measured current flowing through resistive load "I_{load}" is 0.98 A and the forward voltage drop "V_f" of each diode corresponding to load current is 0.45 V. Therefore, the conduction loss of diodes is computed from (8) and it is 0.36 W for two diodes

$$P_{\text{conduction\_diode}} = V_f \cdot I_{\text{load}} \cdot D. \tag{8}$$

Since the MOSFETs consist of both conduction and switching losses [36], it is important to estimate these losses in the converter particularly when operated at higher switching frequencies. In this converter, each switch conducts with duty cycle ratio "D" of 41%. The measured average current "I_{avg}" flowing through the MOSFET is 0.19 A with an on-state resistance "$R_{\text{ds-on}}$" of each MOSFET as 0.65 Ω. Therefore, the total conduction loss of two MOSFETs obtained by using the following equation is 19.2 mW:

$$P_{\text{conduction}} = I_{\text{avg}}^2 \cdot R_{\text{ds-on}} \cdot D. \tag{9}$$

The switching losses of the MOSFETs [37] can be computed as follows:

$$P_{\text{switching}} = \frac{1}{2}\left(T_{\text{sw\_on}} + T_{\text{sw\_off}}\right) \cdot V_{\text{ds}} \cdot I_d \cdot f_{\text{sw}} \tag{10}$$

where

$T_{\text{sw\_on}}$ turn-on switch transition time;
$T_{\text{sw\_off}}$ turn-off switch transition time;
V_{ds} drain–source voltage;
I_d current through MOSFET;
f_{sw} switching frequency.

Since the converter is operated in ZVS conditions, the turn-on losses of MOSFET are negligible. Therefore, the measured switching loss, i.e., turn-off loss of high-/low-side MOSFETs are 0.4/0.43 W, respectively. The left over losses are contributed by the series resonant capacitor "C_r" because of its equivalent series resistance and by remaining circuit elements. These losses are represented as bar graph and depicted in Fig. 20.

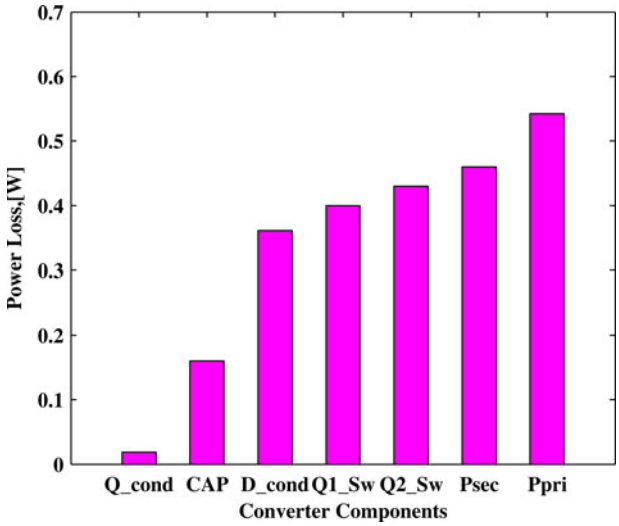


Fig. 20. Loss estimation of the SRC for V_{nominal} with $R_L = 15\,\Omega$.

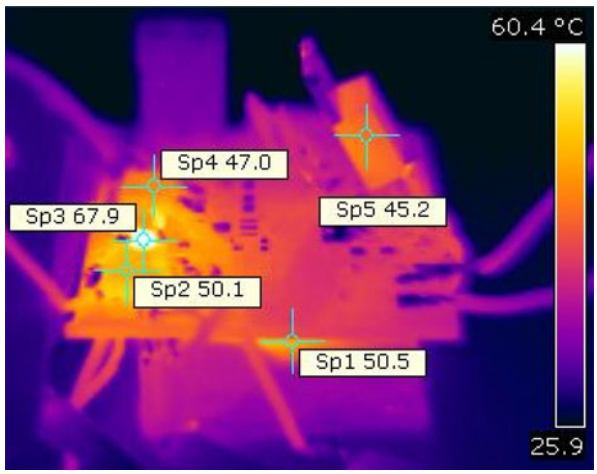


Fig. 21. Measured temperature of the SRC including the transformer with Sp1—spot temperature of transformer, Sp2—spot temperature of low side MOSFET (Q_2), Sp3—spot temperature of series resonant capacitor (C_r), Sp4—spot temperature of high-side MOSFET (Q_1), Sp5—spot temperature of diode rectifier ($D_1 + D_2$).

From Fig. 20, it can be observed that the transformer contributes approximately 42% of the converter losses. Further, the energy efficiency of the converter can be improved by optimizing the transformer design, by employing latest GaN MOSFETs that give promising results at higher switching frequencies [38], as well as with synchronous rectification on the secondary side of the converter.

Under the same operating conditions of V_{nominal} and load resistance of 15 Ω, the temperature of the converter including transformer are recorded using IR thermal imaging camera and thermal profile of the converter is illustrated in Fig. 21.

The input voltage of the converter is maintained constant at $V_{\mathrm{in\_max}}$ of 120 V and load resistance "R_L" of the converter is varied from 15 to 30 Ω. The energy efficiency of the regulated converter is depicted in Fig. 22. Here, the output voltage of the converter is regulated to 20 V with ±2% tolerance by using a constant off-time frequency modulation technique.

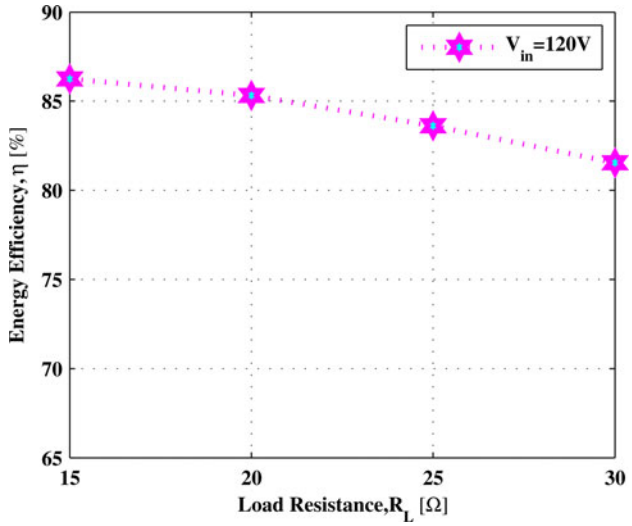


Fig. 22. Energy efficiency of the regulated converter with different load conditions for a constant input voltage.

V. Conclusion

An ultralow profile, low-cost SRC using the multilayered coreless PCB step-down, center-tapped power transformer along with the signal transformer is fabricated in a PCB of 45 mm × 35 mm area. The design method for the multilayered coreless PCB step-down transformer for the given power transfer application was proposed. The power transformer tested for sinusoidal excitations was found to be highly energy efficient in the megahertz frequency region with the tested power density of 16 W/cm^2. The designed multilayered signal transformer was proven to be successful for driving the high-side power MOSFET in the megahertz switching frequency region. The converter was operated above resonant frequency to achieve ZVS conditions in order to reduce the turn-on loss, EMI emissions from the converter. The demonstrated converter was tested up to the output power level of 34.5 W with the maximum energy efficiency of 86.5%. This study provides a considerable step by employing the switching frequencies of megahertz in isolated dc/dc converters using multilayered coreless PCB signal and step-down power transformers. This enables smaller and more compact design of SMPS in near future. From loss estimation, the losses of converter elements are determined and with further improvement of the transformer design and with synchronous rectification and latest GaN MOSFETs that give promising results at higher switching frequencies, the energy efficiency of the converter can be improved.

References

[1] C. K. Lee, Y. P. Su, and S. Y. R. Hui, "Printed spiral winding inductor with wide frequency bandwidth," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2936–2945, Oct. 2011.

[2] J. S. Glaser and J. M. Rivas, "A 500 W push-pull dc-dc power converter with a 30 MHz switching frequency," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 21–25, 2010, pp. 654–661.

[3] C. Quinn, K. Rinne, T. O'Donnell, M. Duffy, and C. O. Mathuna, "A review of planar magnetic techniques and technologies," in *Proc. 16th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2001, vol. 2, pp. 1175–1183.

[4] Y. Katayama, S. Sugahara, H. Nakazawa, and M. Edo, "High-power-density MHz-switching monolithic DC-DC converter with thin-film inductor," in *Proc. IEEE 31st Annu. Power Electron. Spec. Conf.*, vol. 3, pp. 1485–1490.

[5] R. Ambatipudi, H. B. Kotte, and K. Bertilsson, "Effect of dielectric material on the performance of printed circuit board power transformers in MHz frequency region," in *Proc. Coil Winding, Insulation Electr. Manuf. Int. Conf. Exhib.*, Berlin, Germany, Jun. 26–28, 2012.

[6] S. C. Tang, S. Y. Hui, and H. S.-H. Chung, "A low-profile low-power converter with coreless PCB isolation transformer," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 311–315, May 2001.

[7] S. C. Tang, S. Y. R. Hui, and H. S.-H. Chung, "A low-profile power converter using printed-circuit board (PCB) power transformer with ferrite polymer composite," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 493–498, Jul. 2001.

[8] S. C. Tang, S. Y. R. Hui, and H. S. Chung, "A low-profile wide-band three-port isolation amplifier with coreless printed-circuit-board (PCB) transformers," *IEEE Trans. Ind. Electron.*, vol. 48, no. 6, pp. 1180–1187, Dec. 2001.

[9] Y. Su, X. Liu, C. K. Lee, and S. Y. Hui, "On the relationship of quality factor and hollow winding structure of coreless printed spiral winding (CPSW) inductor," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3050–3056, Jun. 2012.

[10] R. Ambatipudi, H. B. Kotte, and K. Bertilsson, "Coreless printed circuit board (PCB) step-down transformers for DC-DC converter applications," in *Proc. World Acad. Sci., Eng. Technol.*, Paris, France, Oct. 2010, vol. 70, pp. 380–389.

[11] R. Ambatipudi, H. B. Kotte, and K. Bertilsson, "Comparison of two layered and three layered coreless printed circuit board (PCB) step-down transformers," in *Proc. 3rd Int. Conf. Power Electron. Intell. Transportation Syst.*, Shenzhen, China, Nov. 20–21, 2010, pp. 314–317.

[12] H. B. Kotte, R. Ambatipudi, and K. Bertilsson, "A ZVS flyback DC-DC converter using multilayered coreless printed-circuit board (PCB) step-down power transformer," in *Proc. World Acad. Sci., Eng. Technol.*, Paris, France, Oct. 2010, vol. 70, pp. 148–155.

[13] H. B. Kotte, R. Ambatipudi, and K. Bertilsson, "Comparative results of GaN and Si MOSFET in a ZVS flyback converter using multilayered coreless PCB step down transformer," in *Proc. 3rd Int. Conf. Power Electron. Intell. Transportation Syst.*, Shenzhen, China, Nov. 20–21, 2010, pp. 318–321.

[14] H. B. Kotte, R. Ambatipudi, and K. Bertilsson, "High speed cascode flyback converter using multilayered coreless printed circuit board (PCB) step-down power transformer," in *Proc. IEEE 8th Int. Conf. Power Electron. and ECCE Asia*, May 30–Jun. 3, 2011, pp. 1856–1862.

[15] B.-R. Lin, J.-Y. Dong, and J.-J. Chen, "Analysis and implementation of a ZVS/ZCS DC–DC switching converter with voltage step-up," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2962–2971, Jul. 2011.

[16] A. K. Hari, "Voltage-mode push-pull converters deserve a second look," *Power Electron. Technol.*, pp. 14–19, Mar. 2009. Available: http://powerelectronics.com/power_semiconductors/Feature2_0309.pdf.

[17] Bob Bell (2006), "Half-bridge topology finds high-density power converter apps," Design Article, National Semiconductor, Santa Clara, CA, [Online]. Available: www.eetimes.com

[18] S. Valtchev, B. V. Borges, and J. B. Klaassens, "Series resonant converter applied to contactless energy transmission," in *Proc. 3rd Conf. Telecommun.*, 2001, pp. 474–478.

[19] L. Rossetto and G. Spiazzi, "Series resonant converter with wide load range," in *Proc. IEEE 33rd IAS Annu. Meeting Ind. Appl. Conf.*, Oct. 12–15, 1998, vol. 2, pp. 1326–1331.

[20] F. K. Wong, "High frequency transformers for switching mode power supplies," Ph.D. dissertation, Griffith Univ., Brisbane, Australia, Mar. 2004.

[21] C. F. Coombs, *Printed Circuits Handbook*, 5th ed. New York: McGraw-Hill, Aug. 27, 2011.

[22] W. G. Hurley and M. C. Duffy, "Calculation of self and mutual impedances in planar magnetic structures," *IEEE Trans. Magn.*, vol. 31, no. 4, pp. 2416–2422, Jul. 1995.

[23] N. Dai, A. W. Lofti, C. Skutt, W. Tabisz, and F. C. Lee, "A comparative study of high-frequency, low-profile planar transformer technologies," in *Proc. 9th Annu. Appl. Power Electron. Conf. Expo.*, Feb. 13–17, 1994, vol. 1, pp. 226–232.

[24] N. Dai and F. C. Lee, "High-frequency eddy-current effects in low-profile transformer windings," in *Proc. 28th Annu. IEEE Power Electron. Spec. Conf.*, Jun. 22–27, 1997, vol. 1, pp. 641–647.

[25] J. A. Ferreira, "Improved analytical modeling of conductive losses in magnetic components," *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 127–131, Jan. 1994.

[26] Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen, "Optimal Design and tradeoff analysis of planar transformer in high-power DC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2800–2810, Jul. 2012.

[27] S. C. Tang, S. Y. Hui, and H. S.-H. Chung, "Coreless planar printed-circuit-board (PCB) transformers-a fundamental concept for signal and energy transfer," *IEEE Trans. Power Electron.*, vol. 15, no. 5, pp. 931–941, Sep. 2000.

[28] R. Ambatipudi, "Multilayered coreless printed circuit board (PCB) step-down transformers for high frequency switch mode power supplies (SMPS)," Licentiate Thesis 61, Mid Sweden Univ., Sundsvall, Sweden, 2011.

[29] R. Ambatipudi, H. B. Kotte, and K. Bertilsson, "Radiated emissions of multilayered coreless printed circuit board step-down power transformers in switch mode power supplies," in *Proc. IEEE 8th Int. Conf. Power Electron. and ECCE Asia* , May 30–Jun. 3, 2011, pp. 960–965.

[30] Maxim MAXIM 125 V/3 A, High-Speed Half-Bridge MOSFET Drivers, [Online]. Available: http://datasheets.maxim-ic.com/en/ds/MAX15018-MAX15019.pdf

[31] S. Y. Hui, S. C. Tang, and H. S.-H. Chung, "Optimal operation of coreless PCB transformer-isolated gate drive circuits with wide switching frequency range," *IEEE Trans. Power Electron.*, vol. 14, no. 3, pp. 506–514, May 1999.

[32] B. Yang, "Topology investigation of front end DC/DC converter for distributed power system," Ph.D. thesis, Virginia Polytechnic Inst. and State Univ., Blacksburg, ch. 4, p. 98, 2003.

[33] M. S. J. Asghar, *Power Electronics*, 3rd ed. Englewood Cliffs, NJ: Prentice-Hall, 2006.

[34] D. Fu, "Topology investigation and system optimization of resonant converters," PhD dissertation, Virginia Polytechnic Inst. and State Univ., Blacksburg, Feb. 2010, ch. 1, pp. 43–44.

[35] E.-S. Kim, H.-K. Song, J.-H. Kim, H.-K. Lee, and Y.-H. Kim, "Efficiency characteristics of a half-bridge series resonant converter for the contactless power supply," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 24–28, 2008, pp. 1555–1561.

[36] R. W. Erickson, *Fundamentals of Power Electronics*, 2nd ed. New York: Springer, 2001, pp. 92–97.

[37] Z. John Shen, Y. Xiong, X. Cheng, Y. Fu, and P. Kumar, "Power MOSFET switching loss analysis: A new insight," in *Proc. IEEE 41st IAS Annu. Meeting Conf. Rec. Ind. Appl. Conf.*, Oct. 8–12, 2006, vol. 3, pp. 1438–1442.

[38] H. B. Kotte, R. Ambatipudi, and K. Bertilsson, "A ZVS half bridge DC-DC converter in MHz frequency region using novel hybrid power transformer," in *Proc. PCIM Europe Power Conversion Intell. Motion Conf.*, Nuremberg, Germany, May 2012, pp. 399–406.

Hari Babu Kotte (M'12) was born in Ongole, Andhra Pradesh, India, in 1979. He received the B.Tech. degree in electrical and electronics engineering, in 2001, and the M.Tech. degree in information technology in power engineering, in 2004, both from Jawaharlal Nehru Technological University, Hyderabad, India. He received the M.Sc. and Licentiate (M.Phil.) degrees in electrical engineering from the Department of Information Technology and Media, Mid Sweden University, Sundsvall, Sweden, in 2007 and 2011, respectively, where he is currently working toward the Ph.D. degree in the field of high-speed (megahertz) switch mode power supplies.

He had a teaching experience of about four years (from 2001 to 2005) for undergraduate students covering various electrical engineering subjects in JB Institute of Engineering and Technology and CVR College of Engineering, Hyderabad, India. He had around 15 international publications and one text book on *Power Electronics* (Chennai, India: SciTech Publications, 2005) for undergraduate students. His main research interests are power semiconductor devices, high-speed power conversion, resonant converter topologies, and computer-aided analysis by simulations and design.

Dr. Babu is also one of the three winners of International Young Engineer Award in the Power Conversion and Intelligent Motion Conference held in Nuremberg, Germany, 2012 sponsored by ECPE, Infineon, and Mitsubishi Electric.

Radhika Ambatipudi (M'12) was born in Nandipadu, Andhra Pradesh, India, in 1982. She received the B.Tech. degree in electrical and electronics engineering from Jawaharlal Nehru Technological University, Hyderabad, India, in 2004, and the M.Sc. and Licentiate (M.Phil.) degrees in electrical engineering from the Department of Information Technology and Media, Mid Sweden University, Sundsvall, Sweden, in 2007 and 2011, respectively, where she is currently working toward the Ph.D. degree in the field of high-frequency magnetics.

From July 2004 to August 2005, she was an Assistant Professor in CVR Engineering College, Hyderabad, India. She has published around 15 international papers covering the topics high-frequency transformers, converters, and EMI issues. Her main research interests are printed planar power and signal transformers for switch mode power supplies, high-frequency power conversion, and computer-aided analysis by simulations and design.

Kent Bertilsson was born in Sundsvall, Sweden, in 1973. He received the M.Sc. degree in electronics from Mid Sweden University, Sundsvall, in 1999, and the Ph.D. degree from Royal Institute of Technology, Stockholm, Sweden, in 2005, in the field of device design and optimization of silicon carbide devices.

Since 2005, he has been leading the research in power electronics at Mid Sweden University mainly in fields such as high-frequency power converters and welding applications as an Associate Professor (2011). In 2009, he cofounded SEPS Technologies AB, Sundsvall, commercializing the development of high-frequency power transformers and converters designed in Mid Sweden University and where he is currently the CEO. He has published more than 50 papers in international journal and conferences in the fields of semiconductor device simulations, silicon carbide devices, detectors and power electronics.

A 45W LLC Resonant Converter in MHz Frequency Region for Laptop Adapter Application using GaN HEMTs

Hari Babu Kotte*, Radhika Ambatipudi and Kent Bertilsson
Department of Information Technology and Media, Mid Sweden University, Holmgatan 10, Sundsvall, Sweden, 85170.
Hari.Kotte@miun.se, +46–723622781

Abstract

The authors report the feasibility of low profile, high power density and energy efficient isolated DC/DC converter in 3 – 4 MHz frequency region corresponding to low line input voltage of 90 – 110 V_{ac} suitable for 45W laptop adapter application. Using novel planar power transformer and GaN HEMTs, the simulation and experimental results of LLC resonant converter for DC input voltage range of 127 – 155V_{dc} with a regulated output voltage of 22V_{dc} was presented. The maximum energy efficiency of converter at the full load condition is reported to be approximately 91%, whereas light load efficiency was improved by using pulse skip modulation (PSM) technique.

1. Introduction

With the ever increasing demand for low profile, high power density converters for the portable appliances such as palm top computers, laptop adapters and iPads, it is required to increase the switching frequency of converters. However, due to increased switching frequencies there exist several challenges in terms of magnetic devices, switching losses/gate drive power consumption in converter along with the EMI issues. On the other hand by increasing switching frequency of converters, there exists a huge reduction in passive element size such as transformers/inductors and EMI filters [1], [2] and also fast dynamic response can be achieved. Due to the theoretical limitations on the existing 'Si' devices in MHz frequency region of operation, advanced semiconductor devices such as GaN HEMTs were introduced in to the market which makes it feasible to operate the converters in MHz frequency region [3], [4] and [5]. In order to reduce the switching losses and EMI emissions from the converter, usually soft switching techniques such as zero voltage switching (ZVS) / zero current switching (ZCS) are employed in the switching converter topologies. Also, the soft switching topologies such as LLC resonant converters are gaining importance for high frequency applications to reduce switching losses and EMI in the converters. The current switching frequency of the AC/DC converters has been limited to 132 kHz due to several factors such as EMI issues, magnetic elements, high frequency high side gate drive circuitry etc., However, in this paper an attempt has been made to realize the feasibility of the high frequency isolated AC/DC converter with the following specifications of input voltage 90 - 110V_{ac}, output voltage 22V_{dc} with ±5% tolerance, load power of 45W in the switching frequency range of 3 – 4MHz. In this regard, an integrated planar power transformer suitable for operating in the MHz frequency region was designed by considering the above mentioned specifications and thereby the simulation and experimental results of the LLC resonant converter in MHz frequency region has been presented.

2. Design of high frequency transformer

Since, one of the limitations for operating the converter in MHz frequency region is the core and copper losses of the transformer, a novel high frequency planar power transformer suitable for the given application has been designed. The center tapped planar power transformer was designed on a six layered PCB where a single turn auxiliary winding is on the top layer and the remaining layers are distributed for primary and secondary windings forming a primary-secondary-secondary-primary (PSSP) structure. The thickness of PCB is of 1.82mm

with a separation of 0.4mm between primary and secondary windings in order to meet the isolation requirements. Each layer of transformer consists of 4 number of turns with track width/separation of 0.42/0.18mm respectively. For a given power transfer application, the primaries of two layers are connected in series resulting in 8 number of turns to achieve the desired amount of inductance. Here, on the secondary side of the transformer, two conductors out of four are paralleled in each layer of secondary winding leading to 2 number of turns/layer resulting in 4:1:1 center tapped power transformer. The prototype of the designed integrated planar power transformer is illustrated in fig.1. In order to avoid the external inductor requirement in an LLC resonant converter operation, an air gap is introduced at the center post so that the desired ratio of magnetizing inductance to that of the resonant inductance can be maintained.

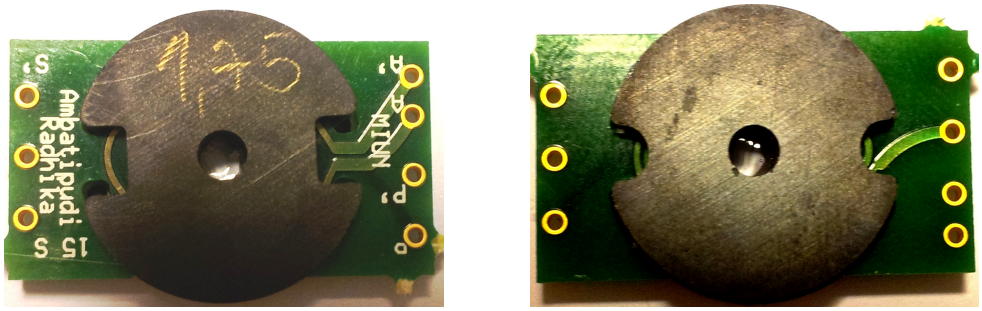


Fig.1. TOP and BOTTOM view of integrated planar power transformer (22x18x5) in mm

The electrical parameters of the transformer measured at 3MHz using sine phase impedance analyzer are listed in table.1. The designed transformer possesses the coupling coefficient of 0.96.

Table.1. Measured electrical parameters of the planar transformer at 3MHz

Parameters	$R_p[\Omega]$	$R_s[\Omega]$	$L_p[\mu H]$	$L_s[\mu H]$	$L_{lk}[\mu H]$	$L_m[\mu H]$	C_{ps} [pF]	K
Values	0.68	0.1	4.8	0.327	0.400	4.4	22.2	0.96

The measured primary and secondary winding AC resistance of the transformer using sine phase impedance analyzer in the frequency range of 1 – 5 MHz is as shown in fig.2. From fig.2, we can observe that the AC winding resistance is increasing in nature due to both skin and proximity effects.

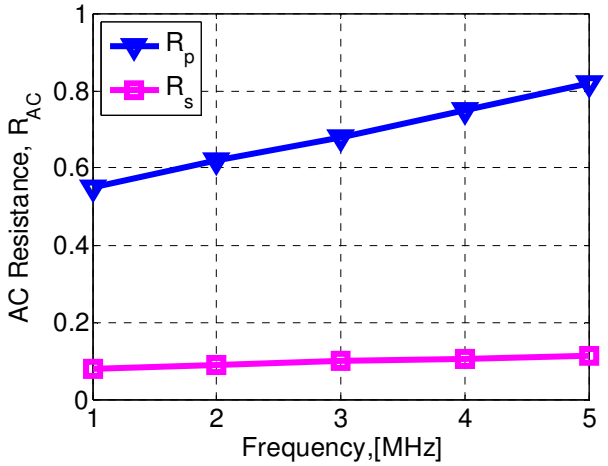


Fig.2. Primary/secondary AC winding resistances of integrated planar power transformer

3. LLC resonant converter with designed high frequency transformer

For the given specifications, the DC gain characteristics of the LLC resonant converter for quality factors corresponding to full load and light load conditions are illustrated in fig.3 since it is necessary to understand the operation of the converter. In LLC resonant converter, in order to reduce the magnetizing current, the ratio of magnetizing inductance 'L_m' to resonant inductance 'L_r' i.e., 'm' is considered as large [6]. Therefore, here with the help of an air gap without any external inductor, 'm' is considered as 11 where 'L_m/L_r' are 4.4/0.4µH respectively.

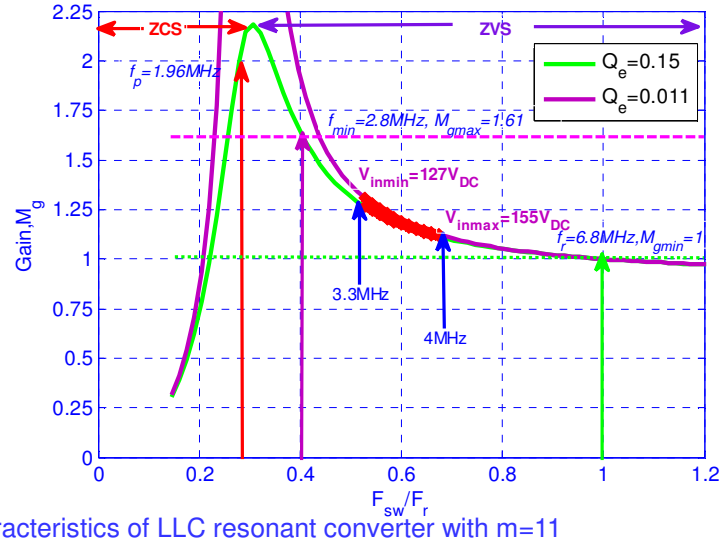


Fig.3. DC gain characteristics of LLC resonant converter with m=11

The frequency of the series resonant circuit (L_r and C_r) 'f_r' is obtained as 6.8MHz by considering an external series capacitor of 1.36nF. The frequency corresponding to all the resonant elements ie., (L_m+L_r+C_r) 'f_p' is 1.96MHz whereas the calculated minimum 'f_{min}' and maximum 'f_{max}' switching frequency of converter corresponding to given specifications resulted in 2.8/6.8MHz respectively. The frequencies 'f_p', 'f_r' and the quality factor 'Q_e' in the figure are obtained as follows

$$f_p = \frac{1}{2\pi\sqrt{(L_m + L_r)C_r}} \tag{1}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2}$$

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e} \tag{3}$$

$$R_e = \frac{8n^2}{\pi^2} R_L \tag{4}$$

Where,
n – Effective turn's ratio obtained from measured self inductances
R_L – Load resistance (Ω)
However, the converter has been operated in the frequency range of 3.3MHz to 4MHz which is within the maximum and minimum gain/frequency limits as shown in fig.3 for achieving the output voltage within the tolerance band of ±5%. From fig.3, it can also be observed that it is possible to obtain the regulated output voltage for the wide input voltage range.

3.1. Simulation and experimental results of LLC resonant converter

The schematic diagram of the LLC resonant converter circuit with the high frequency model of integrated planar power transformer is shown in fig.4.

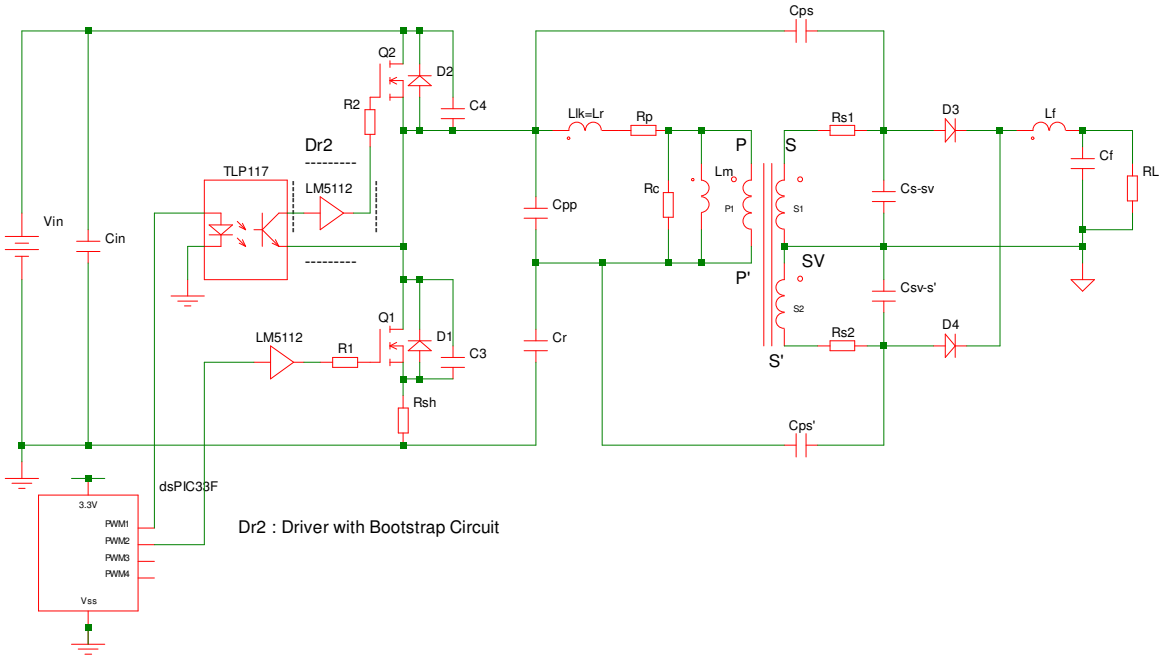


Fig.4.Schematic diagram of LLC resonant converter with high frequency model of planar transformer

The designed center tapped integrated planar power transformer having a turn's ratio of 4:1:1 is placed in the LLC resonant converter and evaluated. Since, '*GaN*' HEMTs pos sesses better high frequency switching characteristics compared to it's counterpart '*Si*' MOSFET as discussed earlier, EPC 2012 GaN HEMTs from the efficient power conversion have been selected as both low side 'Q_1' and high side 'Q_2' switches of LLC resonant converter according to the converter specifications. These HEMTs posseses the breakdown voltage 'V_{ds_max}' of 200V with continuous drain current 'I_d' of 3A and '$R_{ds\text{-}on}$' of 100mΩ. The typical gate charge 'Q_g' and output capacitance 'C_{oss}' of this device under specified conditions are 1.5nC and 73pF respectively. The gate drive signals for these HEMTs are provided by using 16 bit digital signal controller (dsPIC33f16gs502). It consists of high speed PWM module with 1.04ns resolution for frequency, duty cycle, dead time and phase shift which is advantageous for high frequency SMPS. The gate driver for driving the HEMTs of LLC resonant converter is of LM5112 with typical rise/fall times of 14/12ns respectively for a 2nF load with the peak current capability of 7A. Here, the low side switch 'Q_1' was directly fed from the driver LM5112 with an external series gate resistance 'R_1' of 10Ω. Since, there exists no commercially available high side gate drivers for voltages greater than 105V and the frequencies greater than 1MHz, a high speed digital optocoupler 'TLP117' with a propagation delay of maximum 20ns is used. It provides the isolation between the signal from the PWM channel of the controller and the gate driver of the MOSFET and thereby the isolated strengthened signal is fed to the high side switch 'Q_2'. The minimum isolation voltage of the selected optocoupler is approximately 3.7kVrms. The series resonant capacitor 'C_r' placed in the converter is of C0G ceramic capacitor whose value is 1.36 nF (±5% tolerance) with a voltage rating of 200V. The diodes 'D_3' and 'D_4' utilized on secondary side of the LLC resonant converter are SR1660 schottky diodes whose reverse blocking voltage is of 60V with maximum average forward current rating of 16A. Initially the LLC resonant converter is simulated using Simetrix software by considering the high frequency model of the integrated planar power transformer and the spice model of the GaN HEMTs and the schottky diode rectifier.

The simulated waveforms of the converter for the minimum input voltage of 127V_{dc} and at a full load power of 45W are depicted in fig.5. The switching frequency of the converter under these conditions is considered as 3.3MHz. From top to bottom, the figure shows the gate/drain signals of low/high side HEMTs, voltage across the primary winding of transformer 'V_{pri}', voltage across the series capacitor 'V_{cap}', output voltage/current of the converter 'V_{out}'/'I_{out}' and the current flowing through the primary winding of the transformer 'I_{pri}'.

From fig.5, with the considered circuit parameters, it can be observed that both the switches are operating in zero voltage switching (ZVS) condition leading to lower switching losses of the converter. Under the same conditions, the measured waveforms of the converter are illustrated in fig.6. The figure shows the gate signal of the low side switch (yellow), drain signal of the low side switch (blue) and the voltage across the series capacitor (green). It can be observed from the figure, that the low side GaN HEMT is operating in the ZVS condition. The converter has been simulated from full load to 10% of the full load for the input voltage of 127V_{dc} and the energy efficiency is recorded. Similarly, the measurements have been taken for the converter circuit under the same operating conditions with the help of Agilent 6811B AC power source/analyzer. The corresponding simulated and measured energy efficiency of the converter as a function of load power is illustrated in fig.7.

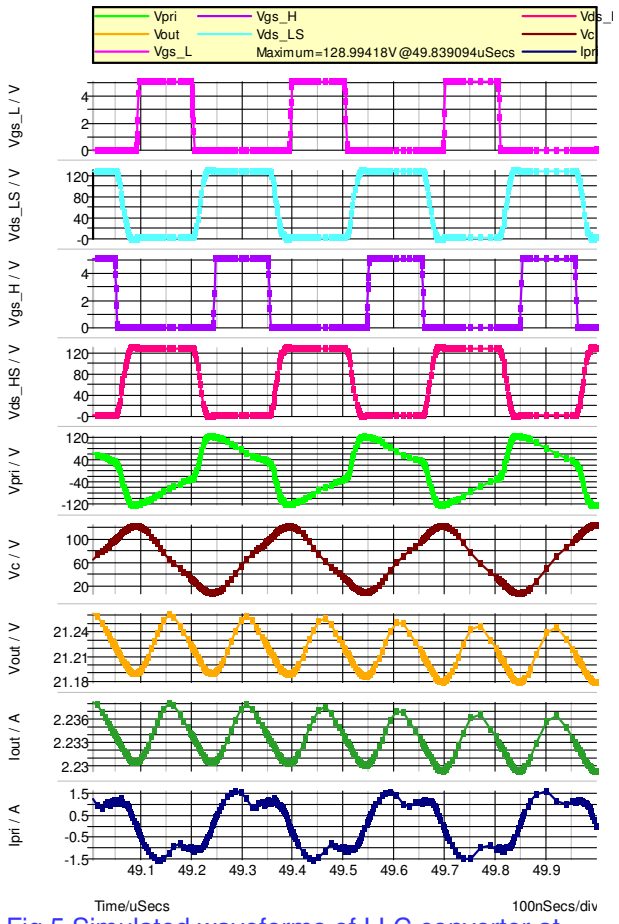


Fig.5.Simulated waveforms of LLC converter at R_L=11Ω and at a frequency of 3.3MHz

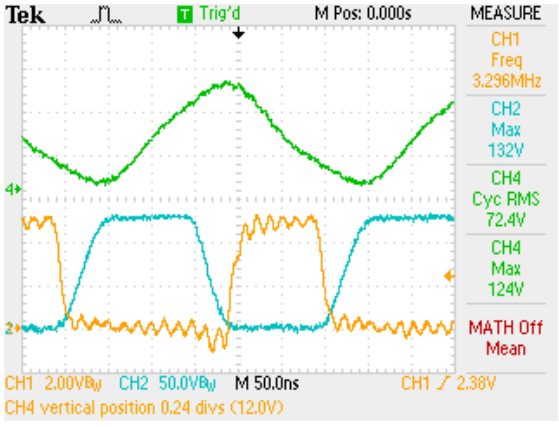


Fig.6. Measured switching waveforms of regulated LLC resonant converter

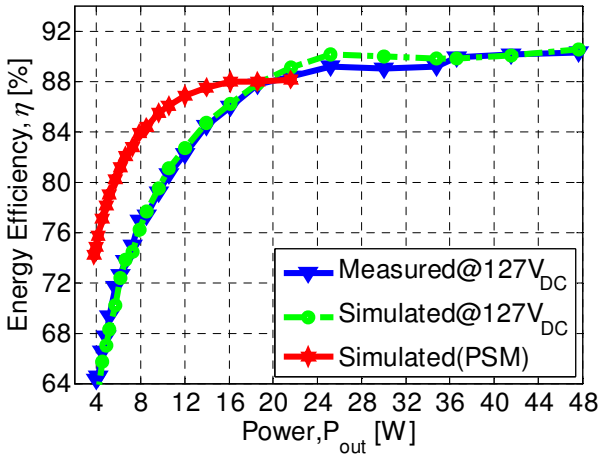


Fig.7.Measured/simulated efficiency of regulated LLC resonant converter as a function of load power

The measured energy efficiency of the converter under the full load condition is 90.48% with the input/output power levels of 49.7/44.97W respectively. Here, the measured regulated

output voltage of the converter is 22.11V_{dc}. It can be observed from fig.7, that the simulated and measured energy efficiency are in good agreement with each other. The measured energy efficiency of the converter with the 10% load condition is 64.26%. Since, under the light load conditions, the energy efficiency gets degraded due to the increased switching losses, conduction losses and other circuit losses, efficiency of LLC resonant converter is improved with the help of Pulse Skip Modulation (PSM). The simulated energy efficiency of the converter with PSM is also illustrated in the same fig.7 for comparison. With this technique, the energy efficiency of the converter is improved by around 10% under the light load condition.
The measured energy efficiency of the AC/DC converter for an input voltage of 90V_{ac} together with the measured DC-DC converter efficiency as a function of load power is depicted in fig.8. It can be observed that approximately 1% efficiency is lost due to the diode bridge rectifier compared to the DC-DC converter efficiency under the full load condition. Here, the output voltage of the converter is regulated to 22V_{dc} within ±5% tolerance band.
The measured energy efficiency of regulated converter with input voltage variation from 127V_{dc} – 155V_{dc} using constant off time frequency modulation is shown in fig.9. It can be observed from the figure, for the considered input voltage variation, the switching frequency of the converter is varied from 3.3MHz to 3.96MHz which is within the limits calculated from the DC gain characteristics shown in fig.3. The maximum energy efficiency of 90.56% of the converter is obtained at the input voltage of 139V_{dc}. When the input voltage is increased beyond the nominal voltage of 141V_{dc}, the converter efficiency is decreasing in nature due to

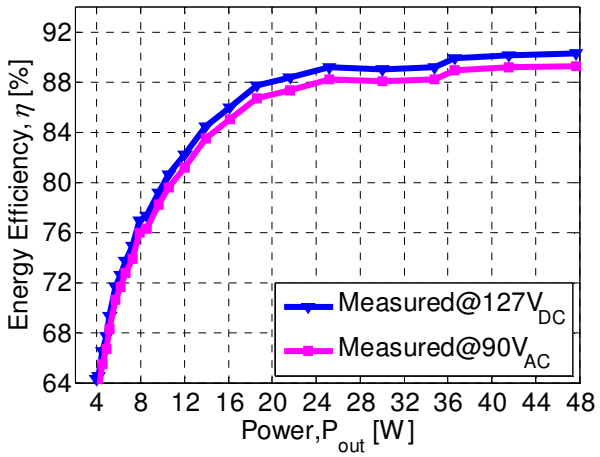


Fig.8.Measured efficiency of regulated AC/DC and DC/DC LLC resonant converter as a function of load power

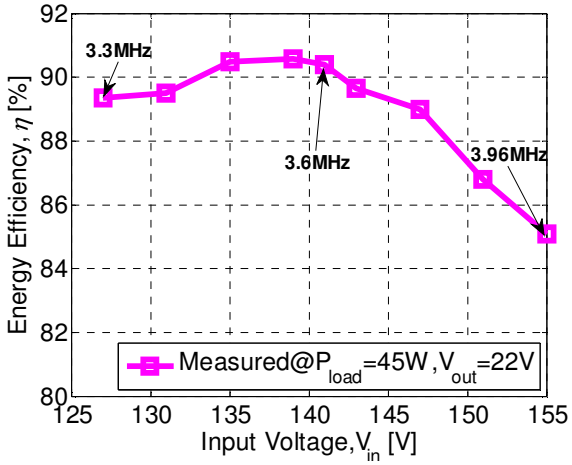


Fig.9.Measured energy efficiency of regulated LLC resonant converter as a function of input voltage

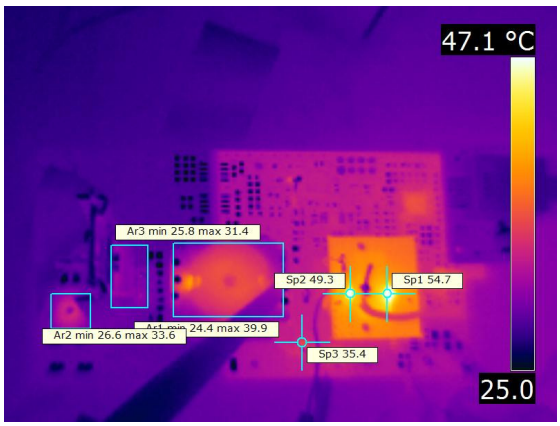


Fig.10. Thermal profile of LLC DC-DC converter at f_{sw} of 3.3MHz and P_{load} of 45W at V_{in}^{min} of 127V_{DC} at an ambient of 25°C

the distortion in the high side gate signal, which can be increased by improving the gate drive circuitry.

The thermal profile of the LLC DC-DC resonant converter at a full load condition with minimum input voltage of $127V_{dc}$ including high side and low side HEMTs (Sp1 and Sp2), series capacitor (Sp3), integrated planar power transformer (Ar1),filter inductor (Ar2) and schottky diode (Ar3) is shown in fig.10 with an ambient temperature of 25°C.

4. Conclusion

An energy efficient LLC resonant DC/DC converter for the input voltage range of 127 - $155V_{dc}$ with an output voltage of $22V_{dc}$ in the switching frequency range of 3 - 4MHz using GaN HEMTs has been demonstrated. The peak energy efficiency of the LLC resonant converter is reported to be approximately 91% at the load power of 45W. With these results of DC/DC converter, an energy efficient low profile AC/DC converter circuit in MHz frequency region for the low line input voltage of 90 - $110V_{ac}$ (due to the limitation of high speed high voltage GaN HEMT) with 50/60Hz supply frequency can be realized. The energy efficiency of the converter with the bridge rectifier is found to be reduced by approximately 1% than that of the achieved energy efficiency of the DC/DC converter at the minimum input voltage. From this, we can conclude that the low profile energy efficient AC/DC converter operating in MHz switching frequency region can be realized in near future for laptop adapter application with the help of GaN HEMTs and the high frequency energy efficient planar power transformers.

5. Literature

[1] Z. Pavlovic, J.A. Oliver, P. Alou, O. Garcia, R. Prieto, J.A. Cobos “Multiple-output Class E Isolated dc-dc Converter” IEEE ECCE Conf.2010, pp.3313-3318.

[2] Matsuura, K.; Yanagi, H.; Tomioka, S.; Ninomiya, T.;, "Power-density development of a 5MHz-switching DC-DC converter," *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE* , vol., no., pp.2326-2332, 5-9 Feb. 2012

[3] Sam Devis, ‘Enhancement Mode Gallium Nitride MOSFET Delivers impressive Performance‘, www.powerelectronics.com, March 1, 2010.

[4] Michael de Rooij, Johan Strydom, ‘eGaN® FET-Silicon Shoot-Out Vol. 9: Wireless Power Converters’, www.powerelectronics.com, June 27, 2012

[5] Kotte, Hari Babu; Ambatipudi, Radhika; Bertilsson, Kent; “A ZVS Half Bridge DC-DC Converter in MHz Frequency Region Using Novel Hybrid Power Transformer”, Proceedings of *PCIM Europe Power Conversion Intelligent Motion Conference, Nuremberg, Germany, May 2012,* pp.399 – 406, ISBN : 978-3-8007-3431-3

[6] Hang-Seok Choi, “Half-bridge LLC resonant converter design using FSFR-series Fairchild Power Switch,” Fairchild Semiconductor, Application Note AB-4151, 2007, pp.1 – 17.

High Performance Planar Power Transformer with High Power Density in MHz Frequency Region for Next Generation Switch Mode Power Supplies

Radhika Ambatipudi*, *Student Member*, *IEEE*
Department of Information Technology and Media
Mid Sweden University
Sundsvall, Sweden
Radhika.Ambatipudi@miun.se

Hari Babu Kotte and Kent Bertilsson
Department of Information Technology and Media
Mid Sweden University
Sundsvall, Sweden
{Hari.Kotte, Kent.Bertilsson}@miun.se

***Abstract*—The authors report the utilization of the core based transformer for power transfer applications with high power density and high energy efficiency in the MHz frequency region. A custom made POT core center tapped transformer of 4:1:1 turn's ratio using novel winding strategy with the core diameter of 16mm is designed and evaluated. The designed transformer has been characterized using sinusoidal excitation for a given output power in the frequency range of 1 – 10MHz and determined the operating frequency region of the transformer. The power tests of the transformer has been carried out up to the power level of 62W at an operating frequency of 6.78MHz with a peak energy efficiency of 98.5% resulting in the record power density of ~1100W/in^3. The designed transformer has been characterized using class E isolated DC-DC converter topology at an output power of approximately 18W. The simulated energy efficiency of the converter is 88.5% under the full load condition. This work provides the significant step for the development of next generation high power density isolated converters (both AC/DC and DC/DC) in MHz frequency region.**

I. INTRODUCTION

The trend towards the low profile, high power density and highly energy efficient converters for portable appliances such as laptop adapters, iPads, mobile chargers, LCD monitors etc., is pushing the switching frequency of converters from several hundred kHz to MHz. In this regard, tremendous progress is achieved in semiconductor field such as introduction of wide band gap material devices in to the market such as SiC and GaN MOSFETs. GaN devices possesses several advantages compared to their 'Si' counterparts such as low switching/conduction losses and gate drive power consumption, capable to withstand high break down voltages in small die area [1] and can be switched effectively in MHz frequency region [2], [3]. Apart from the high frequency switching devices, in order to achieve high power density converters, it is required to possesses the highly energy efficient, high power density transformers/inductors preferably integrated power transformers suitable for operating in the high frequency region. However, with respect to magnetic point of view, increasing the switching frequency of converter results in increased core and copper losses in the windings, unbalanced magnetic flux distribution, dielectric losses [4], etc., Therefore, it is required to design an optimal transformer for the given power transfer application by minimizing the core and copper losses in order to realize the high power density converters. Lot of research is progressing in order to improve the performance of transformer such as introduction of hollow winding factor [5], [6] different winding strategies [7] in order to reduce the copper losses and stray capacitances respectively. For high frequency operation of transformers, it is also required to investigate suitable magnetic [2] and dielectric materials [8] for the given power transfer applications and frequency range. In [9], it has been reported that the hybrid core power transformer which can be operated in 3 – 5MHz region for a power transfer application of 50W has the power density of 47W/cm^3 with the transformer peak energy efficiency of 98%. In this paper, an attempt has been made to custom design the core in order to increase the power density and operating frequency of transformer preferably in 5 – 10 MHz which can be suitable for power transfer applications is designed and investigated.

II. HIGH FREQUENCY PLANAR POWER TRANSFORMER

From magnetic point of view, the operating frequency of the converters is in few hundreds of kHz, due to the nonexistence of the low profile, highly energy efficient and high power density planar power transformers. In this regard, an attempt has been made to design a highly energy efficient planar transformer suitable for power transfer applications in MHz frequency region.

A. Magnetic materials

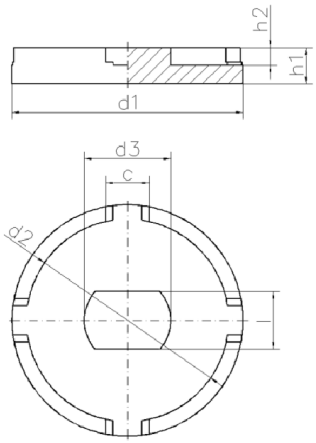
Regarding magnetic materials, MnZn and NiZn ferrite cores possess the desirable characteristics to operate them in the MHz frequency region compared to other existing materials. However, MnZn (3F35, 3F4, 3F45, 3F5) core material possesses minimal amount of core loss in the frequency

978-1-4673-4355-8/13/$31.00 ©2013 IEEE

region of 1-4MHz compared to NiZn core material and when the frequency of operation is greater than 4MHz, NiZn ferrite core exhibit low magnetic losses [2]. Hence, in this regard high frequency NiZn (4F1) material which is optimized for the frequency range of 4 – 10MHz has been considered for designing the planar power transformer. The initial permeability and the resistivity of the considered material are of 80 and $10^5\Omega$m respectively whereas the curie temperature is $\geq 260^oC$.

B. Shape of the core

In order to meet the stringent EMC requirements in MHz frequency region, POT core is considered as it possesses excellent shielding characteristics compared to other cores. Further these cores are suitable for the high frequency DC-DC converters up to the power levels of 125W [10]. In order to increase the power density of the transformer, the custom made POT core has been designed which is shown in fig.1.



All dimensions 'mm'

d_1 = 16.0
d_2 = 14.0
d_3 = 6.0
l = 4.0
h_1 = 2.5
h_2 = 1.2
c = 3.0

Fig.1 Dimensions (in mm) of the custom made POT core design

The overall diameter/height of the designed POT core half is 16/2.5 mm respectively. The effective length/area of cross section (l_e/A_e) of the core is 15.3mm and 30.3mm^2 respectively resulting in the core volume (V_e) of 464mm^3.

C. Transformer windings

The primary/secondary windings of the transformer along with the auxiliary winding were designed on the six layered printed circuit board. The printed circuit board considered is of FR4 laminate whose dielectric strength is 50kV/mm [11].
The shape of the winding is considered as circular spiral in order to obtain the higher amount of inductance and lower interwinding capacitance for achieving the high bandwidth of the transformer. PSSP structure of transformer provides the benefit of meeting isolation requirements without having the penalty of increasing distance between the layers, compared to that of the interleaved structure PSPS which is highly beneficial for the stringent height applications [6]. Therefore, here the PSSP structure of the transformer is considered. The 3D view of the transformer is illustrated in fig.2. The primary/secondary number of turns on each layer of PCB is 4, while single turn auxiliary winding is placed on the top layer of PCB. The primaries of the second and sixth layer are connected in series resulting in total number of turns as 8.

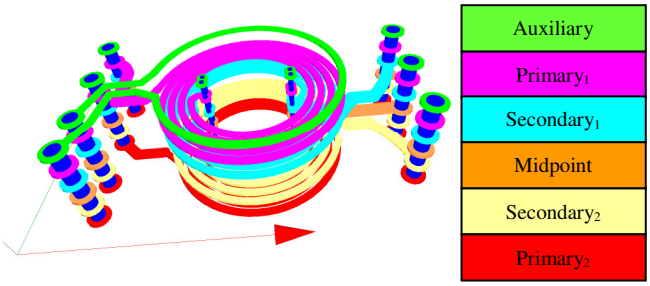


Fig.2 3D view of the planar power transformer

Two turns of each secondary winding are connected in parallel in order to carry large amount of secondary currents compared to that of the primary, forming a 4:1:1 center tapped transformer. Here, the windings are paralleled in a layer instead of a single solid wide conductor due to the increased rate of rise of eddy current phenomena in MHz frequency region resulting in the increased leakage inductance/AC resistance of the transformer [12]. The width/separation of the primary/secondary winding is considered as 0.43/0.19mm respectively according to design rules specified in [6]. The height of the copper track in all the layers of transformer is considered as 70µm. The distance between various layers of the PCB ie., auxiliary-primary$_1$-secondary$_1$-midpoint-secondary$_2$-primary$_2$ is 0.2-0.4-0.2-0.2-0.4 resulting in the total thickness of transformer as 1.82mm.The inner radius/outermost radius of the designed transformer windings is 3.7/6mm respectively. The prototype of the designed planar power transformer is illustrated in fig.3.

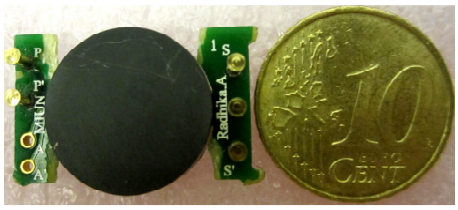


Fig. 3 Prototype of planar POT Core power transformer (20x16x5mm)

The electrical parameters such as primary/secondary resistances 'R_p/R_s', self 'L_p/L_s', leakage 'L_{lk}' and mutual inductances 'L_m' along with the interwinding capacitance 'C_{ps}' of the custom designed planar power transformer are measured using sine phase impedance analyzer at 5MHz and is given in table.1.

TABLE I. MEASURED ELECTRICAL PARAMETERS @ 5MHZ

Parameters	Electrical parameters							
	R_p	R_s	L_p	L_s	L_m	C_{ps}	K	L_{lk}
Values	1.05	0.12	6.79	0.42	1.66	18.5	0.98	0.21

Where
R_p/R_s - primary/secondary resistances in Ω

L_p/L_s - primary/secondary self inductances in µH
C_{ps} - interwinding capacitance (C_{ps}) in pF

From the measured parameters, the coupling coefficient '*K*' and the turn's ratio '*n*' of the transformer were computed. The intrawinding/self capacitance of the designed transformer is very small and hence can be ignored. The DC resistance of primary/secondary windings of transformer measured using agilent 34405A digital multimeter is 0.23/0.08Ω respectively. Due to skin and proximity effects, the AC resistance of the multilayer transformer increases as the frequency of operation is increased. Therefore, the measured AC resistance of the primary/secondary windings of the transformer in the frequency range of 1 – 10MHz using sine phase impedance analyzer is depicted in fig.4. The measured AC resistance of primary/secondary windings of the transformer at a frequency of 6.78MHz is 1.16/0.11Ω respectively. The experimental results of the designed transformer are discussed in the coming sections.

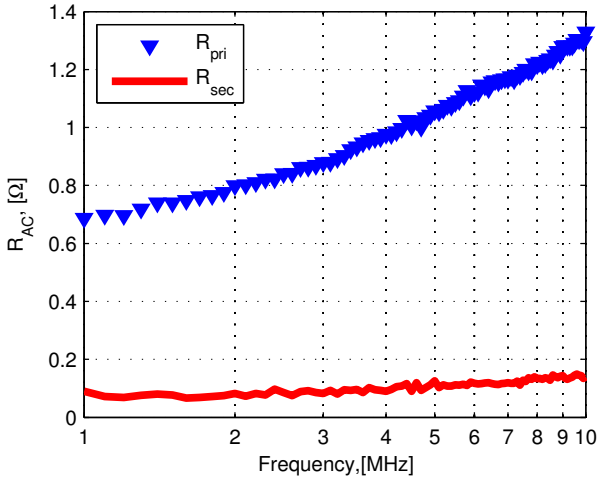


Fig. 4 Measured AC resistance of primary/secondary windings of planar power transformer

III. EXPERIMENTAL RESULTS OF PLANAR POWER TRANSFORMER

In order to determine the performance of designed planar POT core power transformer, the experiments were carried out with the sinusoidal excitations in the frequency range of 1 – 10MHz. For the entire frequency range, the load power 'P_{out}' of the transformer is maintained to be constant of 10W, at a load resistance of 10Ω. The measured energy efficiency along with the transformer temperatures is illustrated in fig.5. The efficiency of the transformer is found to be in the range of 82 – 98.5% and the peak energy efficiency of 98.5% is observed to be at the frequency of 8.5MHz. Under these conditions, the temperature of the transformer is also recorded for the entire frequency region.

From fig.5, it can be observed that the energy efficiency of transformer at lower operating frequencies is reduced due to the increased core losses (NiZn ferrite material) of the transformer as discussed earlier. Since, the transformer's energy efficiency is found to be greater than 96% in the frequency range of 5 – 10 MHz; it has been characterized at a

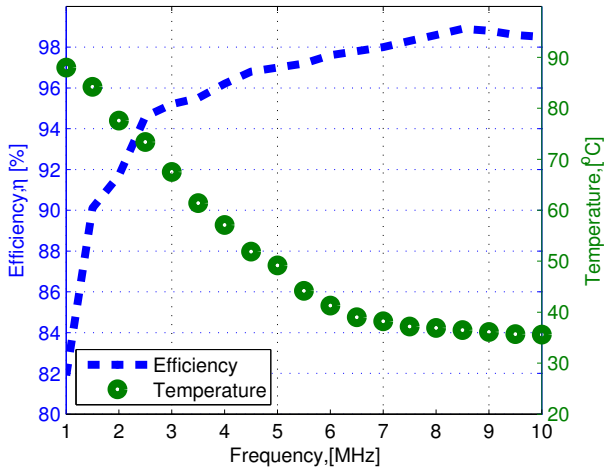


Fig. 5 Measured Energy efficiency and transformer temperature at R_L=10Ω, P_{out}=10W

frequency of 6.78MHz up to load power of approximately 62W. The experiments were carried with the help of radio frequency power amplifier BBM0A3FKO whose load power capacity is of 100W. The measured energy efficiency as a function of load power is illustrated in fig.6. With the total transformer core volume of 0.0566 in^3, the power density of the transformer at the maximum tested output power of 62W is ~1100W/in^3.

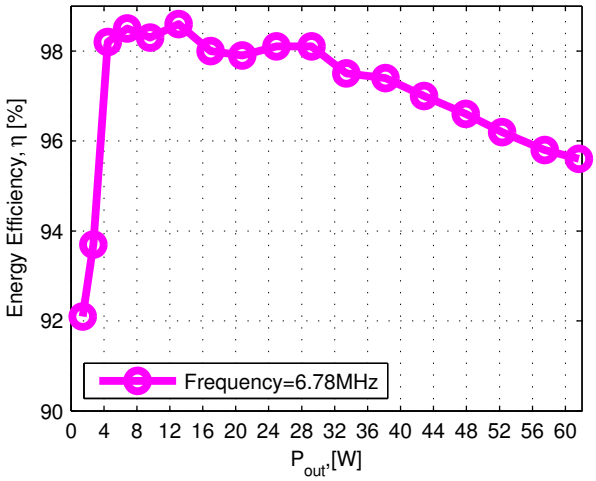


Fig. 6 Measured energy efficiency of power transformer as a function of load power at a frequency of 6.78MHz

The measured primary/secondary voltage/current waveforms of transformer are illustrated in fig.7. With the input voltage of 106V (RMS) across the primary winding, at a frequency of 6.78MHz, and when the secondary winding is loaded with the resistor of 10Ω, the obtained secondary voltage is found to be 24.8V(RMS) as shown in fig.7. Under these conditions, the output power is found to be 58W approximately with the energy efficiency of ~96%.

The corresponding thermal profile of power transformer recorded with FLIR IR thermal imaging camera is depicted in fig. 8. The recorded temperature of the transformer at an

ambient temperature of 25°C is found to be 79.7°C with a power loss of 2.52W.

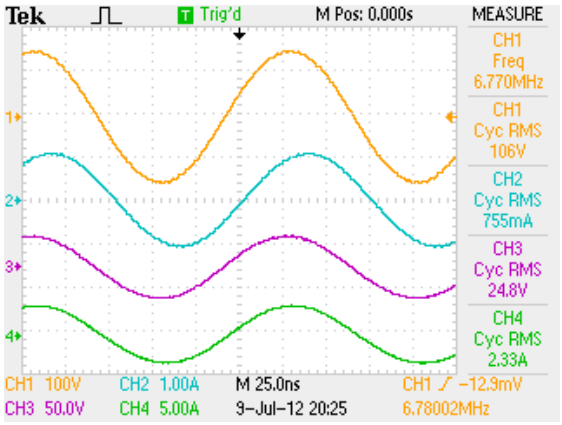


Fig. 7 Measured waveforms of transformer at R_L=10Ω and at a frequency of 6.78MHz. CH1 – V_{pri} (100V/div), CH2 – I_{pri} (1A/div), CH3 – V_{sec} (50V/div), CH4 – I_{sec} (5A/div)

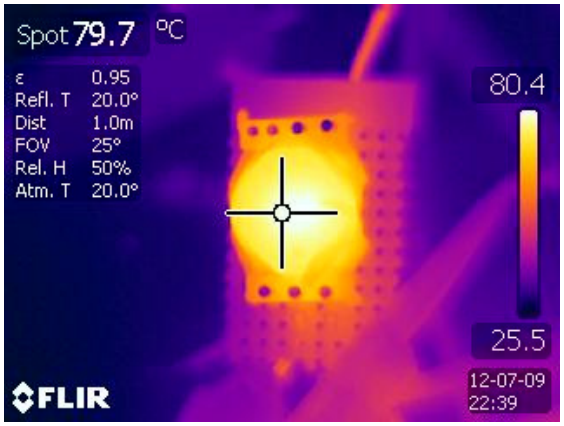


Fig. 8 Thermal profile of power transformer at a frequency of 6.78MHz, P_{out} of 58W and at an ambient temperature of 25°C.

By knowing the primary/secondary resistances of transformer at the operating frequency and the currents flowing through the transformer, the copper losses were approximately estimated and found to be 1.25W. The remaining loss of 1.27W is contributed by the core of the transformer at this operating frequency.

IV. Application Potential of the Designed High Frequency Planar Power Transformer

The high frequency model of the designed planar power transformer has been placed in class E isolated converter topology and evaluated its performance by using SiMetrix simulation software.

Class E isolated DC-DC Converter: Here, isolated class E converter topology is considered since it exhibits several advantages in high frequency operation. The advantages are zero turn on losses resulting in high energy efficiency of converter, the utilization of the output capacitance for achieving ZVS condition of the MOSFET [13]. For class E isolated converter topology, by following the design guidelines specified in [13], [14], the converter was designed for the following specifications. Nominal DC input voltage: V_{nom} of 60V_{dc}, Output voltage: V_{out} of 15V_{dc}, Switching frequency: f_{sw} of 5MHz, Load power: P_{out} of 16W

The schematic diagram of the class E isolated DC-DC converter using the high frequency model of the designed transformer is illustrated in fig.9. For the aforementioned design specifications, the calculated series inductance 'L_s' is of 15.5µH. The calculated series/parallel capacitances 'C_s/C_p' are 69.2/63pF respectively. Here the output capacitance of the MOSFET 'C_{oss}' alone itself is 63pF. Hence, no external parallel capacitor has been added. The full load resistance of the converter is considered as 14.06Ω. Here the quality factor 'Q' and the duty ratio 'D' of the transistor are considered as 5 and 0.5 respectively. The primary/secondary AC resistances of the transformer at the corresponding switching frequency of 5MHz are considered in the high frequency model of the transformer.

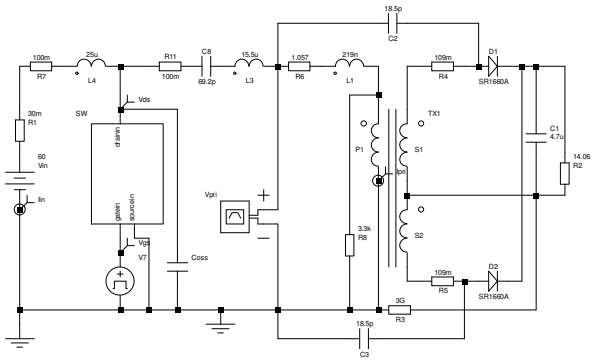


Fig. 9 Schematic diagram of the Class E isolated DC-DC converter operated at 5MHz using high frequency model of power transformer

The switching waveforms of the class E isolated DC-DC converter for the considered design specifications are depicted in fig.10.

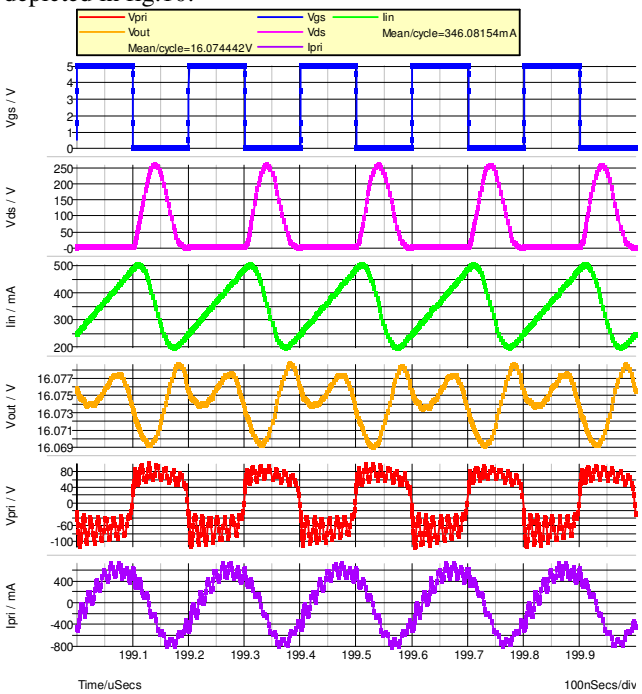


Fig. 10 Switching waveforms of the Class E isolated DC-DC converter at 5MHz using designed high frequency power transformer

From top to bottom, fig.10 illustrates the gate source/drain voltage 'V_{gs}/V_{ds}' of the MOSFET, input mean current 'I_{in}', output voltage 'V_{out}', and then followed by primary voltage/current of the transformer 'V_{pri}'/ 'I_{pri}'. Under these conditions, the input power/output power 'P_{in}/P_{out}' of the converter is 20.76/18.37W respectively resulting in the energy efficiency of 88.5%.

V. CONCLUSION

A highly energy efficient custom made POT core transformer suitable for power transfer applications in the frequency range of 5 – 10MHz has been designed and evaluated. The design guidelines of the transformer along with the dimensions of the custom made POT core have been presented. The energy efficiency of the transformer for the given power level of 10W is found to be greater than 97% in the frequency region of 5 – 10MHz. From the thermal profile of the transformer at a load power of 10W, it can be concluded that the designed core can be utilized for the frequency range of 5 – 10MHz. The maximum tested power density of the designed transformer is reported to be approximately 1100W/in^3 with the tested power level of 62W at an operating frequency of 6.78MHz. From the evaluation of the transformer in the class E isolated DC-DC converter, it can be concluded that the highly energy efficient low profile isolated converters in MHz frequency can be realized. In near future, ultra flat low profile isolated power converters can be designed with the help of this highly energy efficient, high power density transformer along with the commercially available GaN MOSFETs.

ACKNOWLEDGMENT

The authors would like to thank European Union, Vinnova and Swedish Energy Agency.

REFERENCES

[1] Sam Devis, 'Enhancement Mode Gallium Nitride MOSFET Delivers impressive Performance', www.powerelectronics.com, March 1, 2010.

[2] Matsuura, K.; Yanagi, H.; Tomioka, S.; Ninomiya, T.;, "Power-density development of a 5MHz-switching DC-DC converter," *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE* , vol., no., pp.2326-2332, 5-9 Feb. 2012.

[3] Michael de Rooij, Johan Strydom, 'eGaN® FET-Silicon Shoot-Out Vol. 9: Wireless Power Converters', www.powerelectronics.com, June 27, 2012.

[4] Wong Fu Keung, "High Frequency transformers for switch mode powersupplies'' Griffith University, 2004

[5] Yipeng Su; Xun Liu; Chi Kwan Lee; Hui, S.Y.; , "On the Relationship of Quality Factor and Hollow Winding Structure of Coreless Printed Spiral Winding (CPSW) Inductor," *Power Electronics, IEEE Transactions on* , vol.27, no.6, pp.3050-3056, June 2012.

[6] Kotte, H.B.; Ambatipudi, R.; Bertilsson, K.; , "High-Speed (MHz) Series Resonant Converter (SRC) Using Multilayered Coreless Printed Circuit Board (PCB) Step-Down Power Transformer," *Power Electronics, IEEE Transactions on* , vol.28, no.3, pp.1253-1264, March 2013.

[7] Chi Kwan Lee; Su, Y.P.; Hui, S.Y.R.; , "Printed Spiral Winding Inductor With Wide Frequency Bandwidth," *Power Electronics, IEEE Transactions on* , vol.26, no.10, pp.2936-2945, Oct. 2011.

[8] Ambatipudi, R.; Kotte, H.B.; Bertilsson, K.; ,, "Effect of Dielectric Material on the Performance of Coreless Printed Circuit Board (PCB) Step-down Power Transformers in MHz Frequency Region", *Proceedings of INDUCTICA 2012 Coil Winding, Insulation and Electrical Manufacturing International Conference and Exhibition (CWIEME)*, Berlin, Germany 26 – 28, June 2012.

[9] Kotte, Hari Babu; Ambatipudi, Radhika; Bertilsson, Kent; , "A ZVS Half Bridge DC-DC Converter in MHz Frequency Region Using Novel Hybrid Power Transformer", Proceedings of *PCIM Europe Power Conversion Intelligent Motion Conference, Nuremberg, Germany, May 2012,* pp.399 – 406, ISBN : 978-3-8007-3431-3.

[10] Dr. Marian K.Kazimierczuk, High Frequency Magnetic Components, John Wiley & Sons, 2009.

[11] C.F.Coombs, "Printed Circuits handbooks" 5th Edition, McGraw-Hill,August 27,2001.

[12] Ambatipudi, R.; Kotte, H.B.; Bertilsson, K.; ,, "Analysis of Solid and Parallel Winding Structures in MHz Planar Transformers Suitable for Switch Mode Power Supplies", Submitted for Journal of Power Electronics (JPE), South Korea (under revision)

[13] Kazimierczuk, M.K.; Bui, X.T.; , "Class-E DC/DC converters with a capacitive impedance inverter," *Industrial Electronics, IEEE Transactions on* , vol.36, no.3, pp.425-433, Aug 1989.

[14] Kazimierczuk, M.; Puczko, K.; , "Exact analysis of class E tuned power amplifier at any Q and switch duty cycle," *Circuits and Systems, IEEE Transactions on* , vol.34, no.2, pp. 149- 159, Feb 1987.