Study of High Level Synthesis Tool Generated RTL vs Designer Written RTL for Vision Functions

Abstract

Field Programmable Gate Arrays (FPGAs) are attracting number of applications that have real-time and high performance requirements. The data dominated embedded vision systems applications are specially attracting the parallel computing architecture of FPGA for exploiting the parallelism in front end imaging data. The motivation is that FPGAs offer high performance and low latency as compared to microprocessor based software platforms i.e., microcontrollers and Graphical Processor Units (GPUs).
However, development time on FPGAs is greater as compared to software platform. Traditionally, FPGAs are configured by hardware engineers at Register transfer level (RTL) languages; these manual designs require significant time and efforts. Also efficient designing at Register transfer level requires significant specialized knowledge. There's more need then requirement to increase the abstraction level from structural design to behavioural design to attain quick and efficient use of reconfigurable features of an FPGA. High Level Synthesis (HLS) tools are attracting the industrial and academic communities for investigation the aforementioned problem. However, Register Transfer Level (RTL) generated from HLS is not resource optimized. The software imaging libraries that are used by HLS tool provide frame based processing which is bottleneck for achieving high performance.
In this work, main focus was to perform a comparative study of resource utilization in terms of logics and memory, and power consumption of HLS generated RTL and designer written RTL. In addition to this, frame and pixel based processing feature and interfacing challenges between HLS generated RTL and designer written RTL are investigated. Xilinx Vivado HLS (High level synthesis) tool is used to generate RTL for image processing operations using Xilinx HLS video library and openCV.
The study of explored imaging functions reveal that currently available HLS tool can generate RTL that has resource utilization difference with a factor of approximately 10.5 for Look up Tables (LUTs), 14 for Registers, 2.3 for External IOBs and 50% percent difference for Block RAMs, as compared to designer written RTL. The difference in power consumption was measured to be 400mW. The generated RTL supports pixel level processing which is important for high performance systems. However, interfacing the generated RTL with designer written RTL is a challenge because of non-existence of common standard.

Keywords:
Image processing using FPGA, Xilinx Vivado HLS, High Level Synthesis (HLS), OpenCV, Register Transfer Level (RTL).

Date and Place:
Tisdag, 23 December 2014, klockan 10:00 to 111:00 i sal S113, Mittuniversitetet Sundsvall, Sweden.