Energy Efficient and Programmable Architecture for Wireless Vision Sensor Node

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PhD Thesis presentation

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PHD THESIS ERRATA

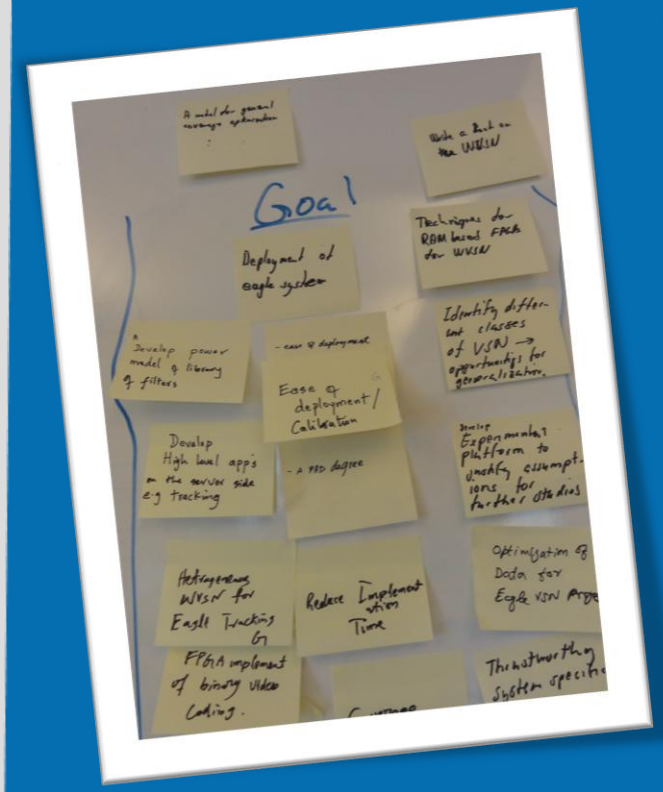
- On page 6, the correct sentence is FLASH based FPGA offers **lower** operating frequency.
- On page 52, Figure 4-8 needs to be replaced with **Fig.10** of paper IV.
- On page 74, StrategyA3 output data is **421** bytes and for StrategyA4 the output data is **411** bytes.
- On page 91, the timing is **235** msec instead of 215 msec.
- On page 91-92, the supply voltage is **3.6** instead of 3.5.
- On page 102, paper **VII** and **VIII** paper numbering should be interchanged.

Vision

My vision is to conduct qualitative research in the field of Wireless Vision Sensor Networks.

Mission

Developing low energy and programmable wireless Vision Sensor Nodes (VSN).



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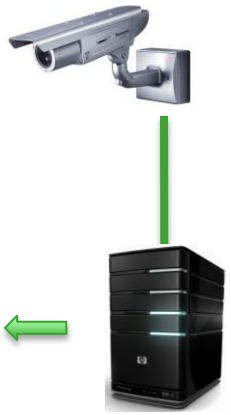
OUTLINE

- Introduction
- Challenges
- Architectures analysis
- Data reduction techniques
- VSN with SRAM based FPGA
- Conclusion

INTRODUCTION

- Camera theory research in 5th century.
- Camera technology started in 20th century.
- Use of camera for surveillance started in 1942.



Surveillance

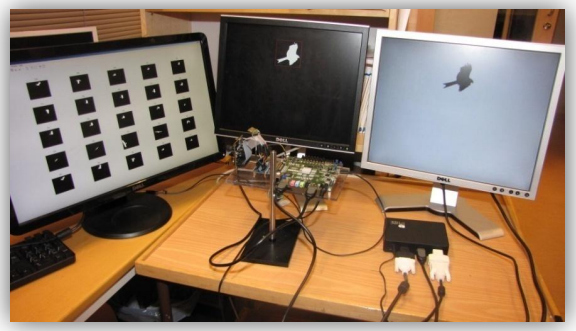
Machine vision

TOWARDS AUTOMATION

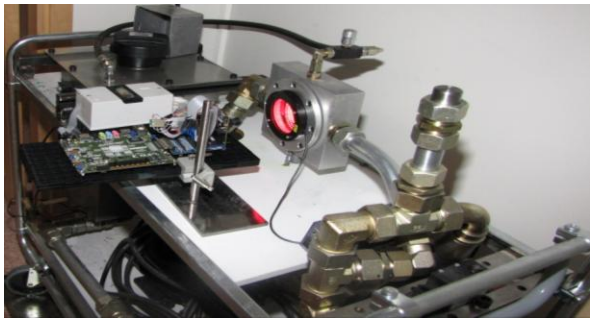
Surveillance

Machine Inspection

Automated Surveillance

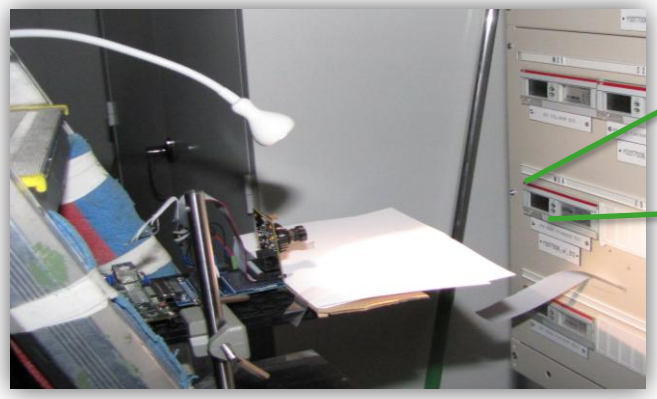


Automated Machine inspection



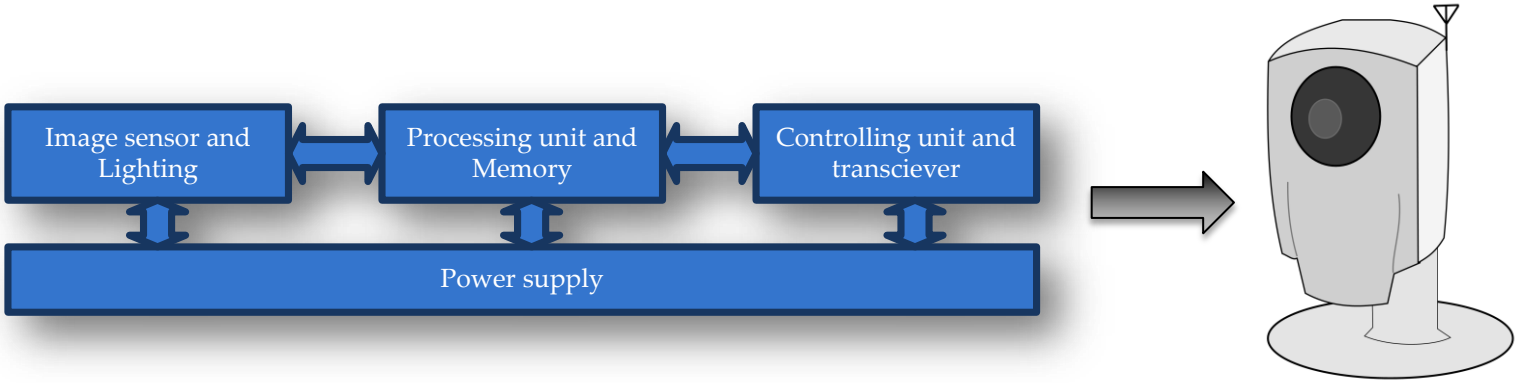
CAMERA FOR INTERNET OF THINGS

- Remote meter reading



SMART CAMERA

- The technological development have enabled camera to integrate different components.



COMMERCIAL SMART CAMERAS

NI1722

A20

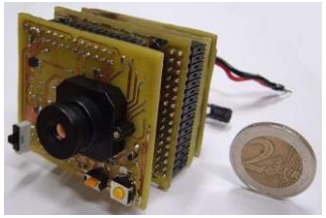
GT300

Manufacturer	Product	Processor	Power	FPS
Texus Instruments	NI 1722	400 MHz Freescale PowerPC	11 W	60
Datalogic,	A20 series	1,334 MIPS	12 W	60
Matrox imaging	GT300	1.6 GHz processor	10 W	110

SMART CAMERAS BY RESEARCH GROUPS

Firefly

MeshEye

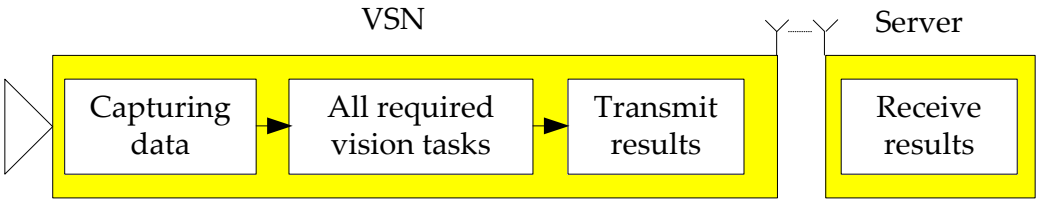


MireEye

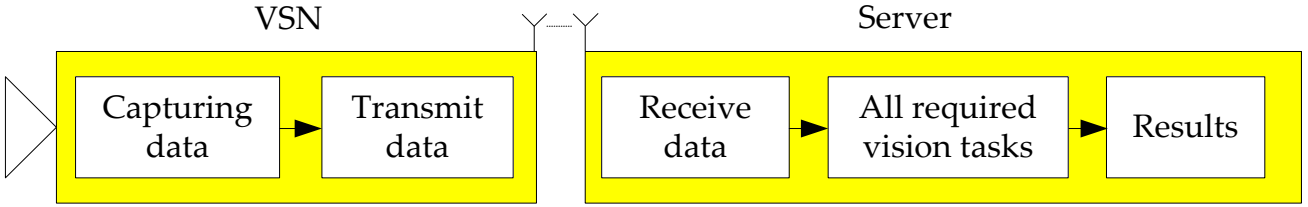
VSN	Processing platforms	Power	FPS	Applications
Firefly Mosaic	ARM7TDMI (32-bit), TMEL Atmega1281,	572.3 mW	5.2	Assisted living
MeshEye	AT91SAM7S (32-bit)	290 mW	10	Surveillance
MircreEye	ATMEL FPSLIC SoC (FPGA plus microcontroller)	500 mW	15	People detection
Binary Sensor	Flash-based FPGA, IGLOO M1-AGL600	231 mW	5	People counting

EXISTING APPROACHES

- Generally researchers employ two approaches.
  - Capture and process locally and transmit final results.

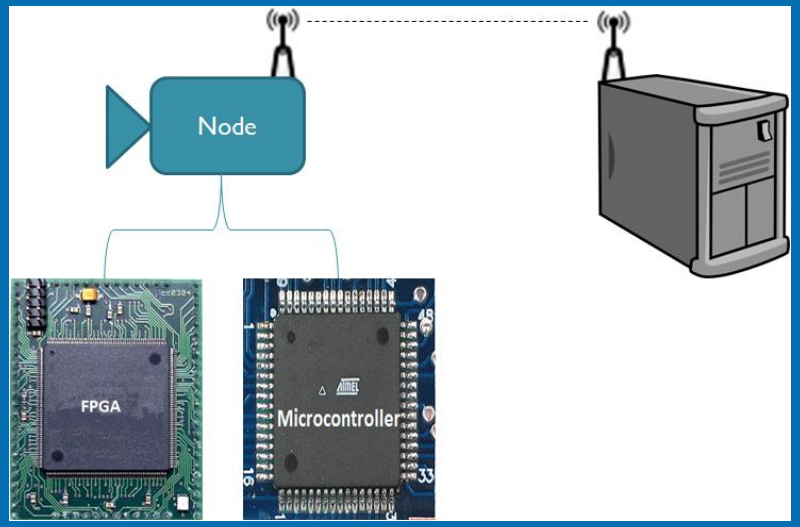


  - Capture and transmit to server for processing.



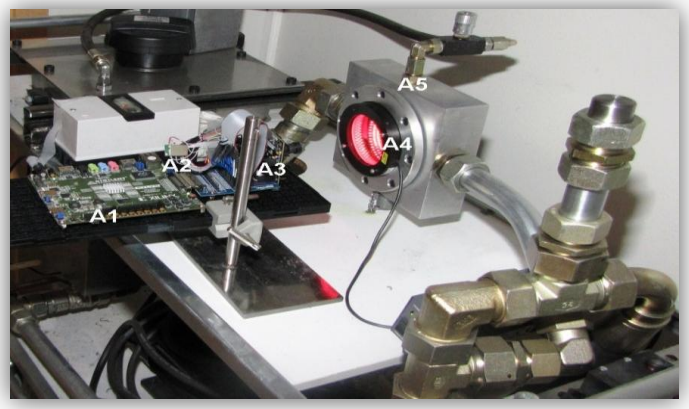
VSN ARCHITECTURES ANALYSIS

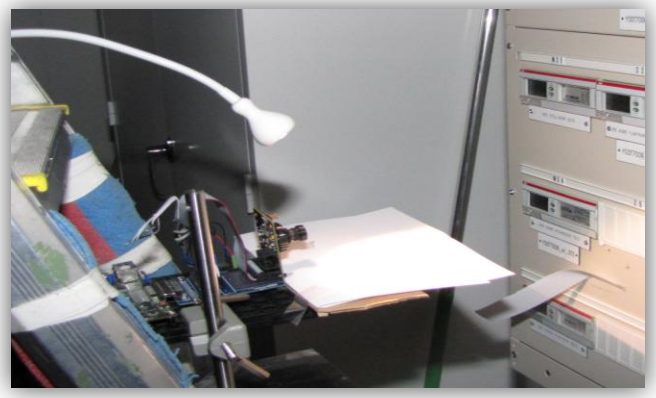
- Partitioning processing load among
  - Software
  - Hardware
  - Server.

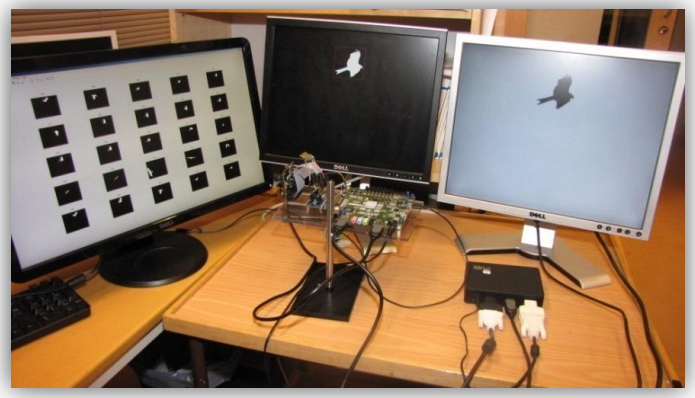


TEST CASES

- Particle detection
- Bird detection
- People counting
- Remote meter reading







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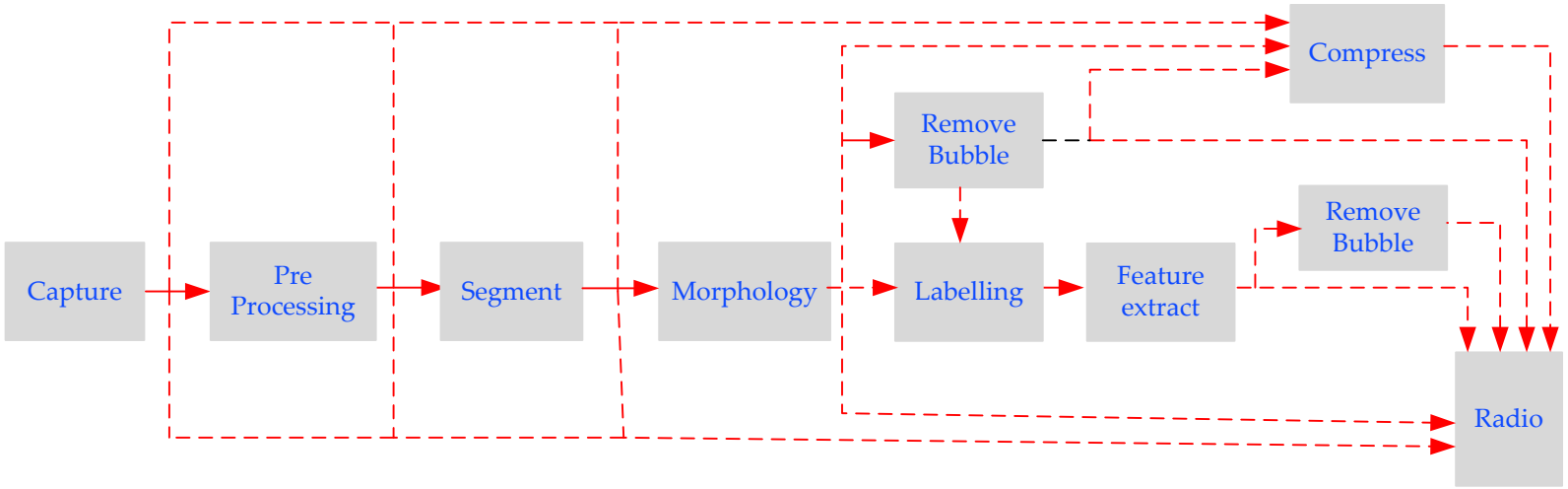
ALGORITHM FLOW



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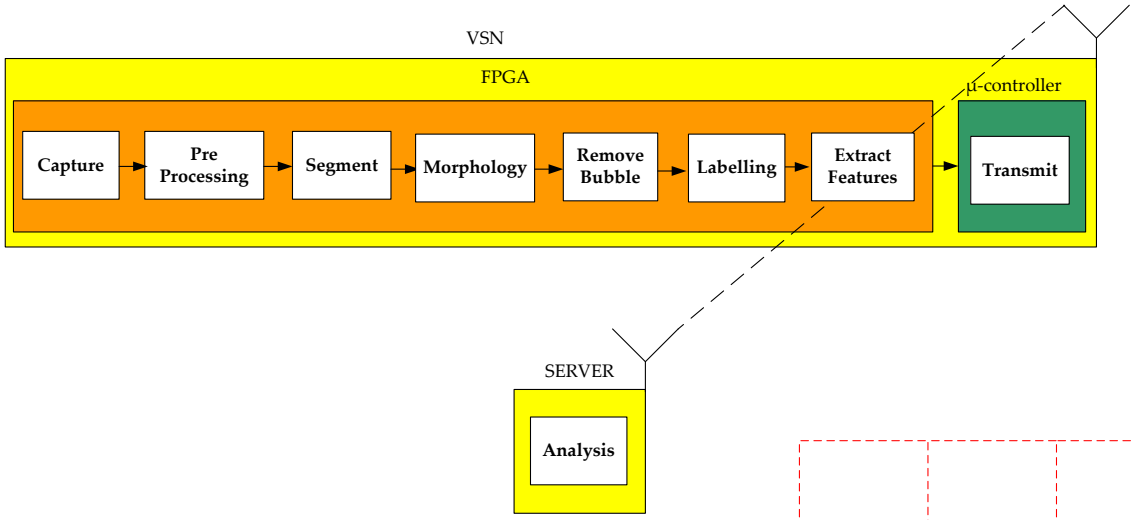
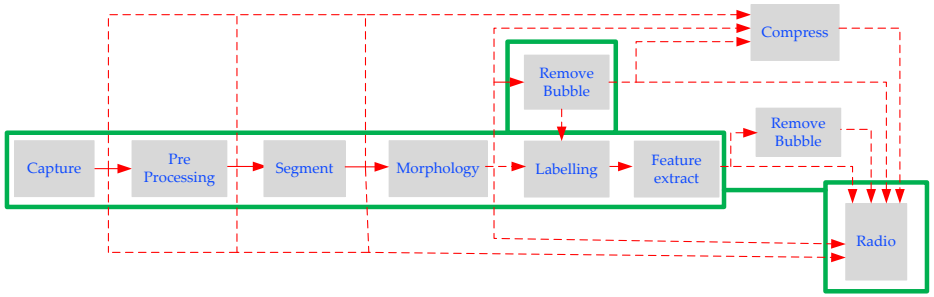
STRATEGY16

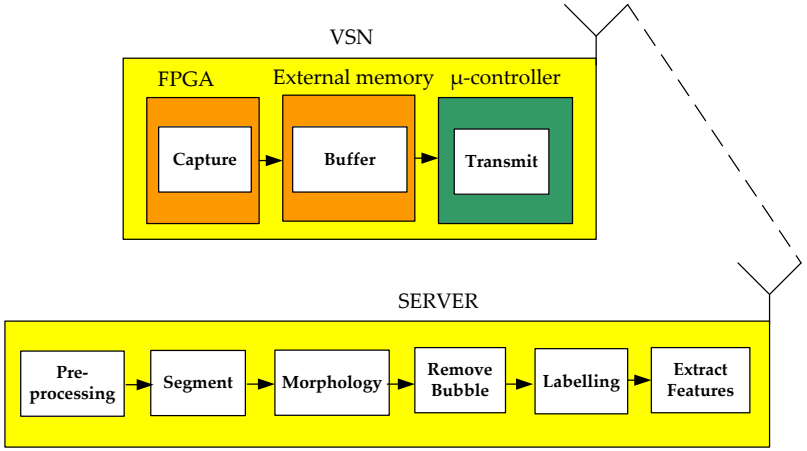
- Data sent is approx. 114 Bytes

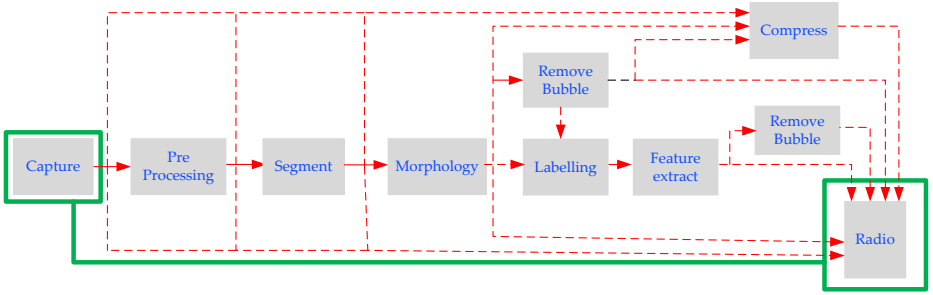




STRATEGY36

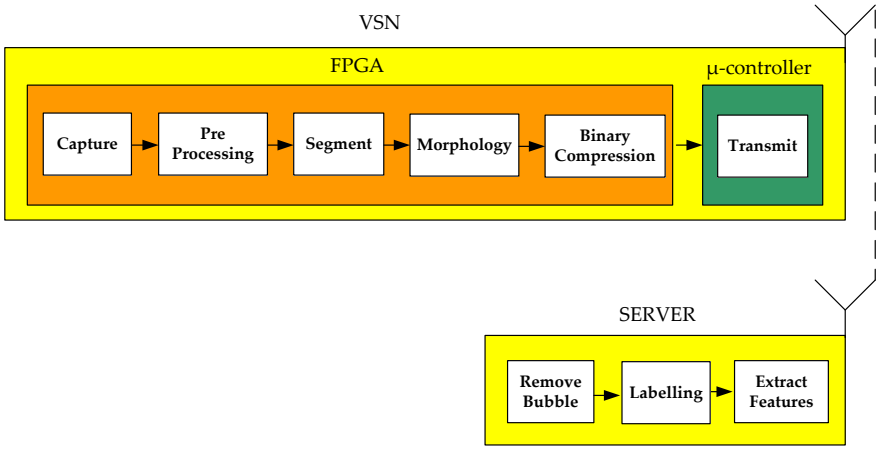
- Data sent is approx. 250KB

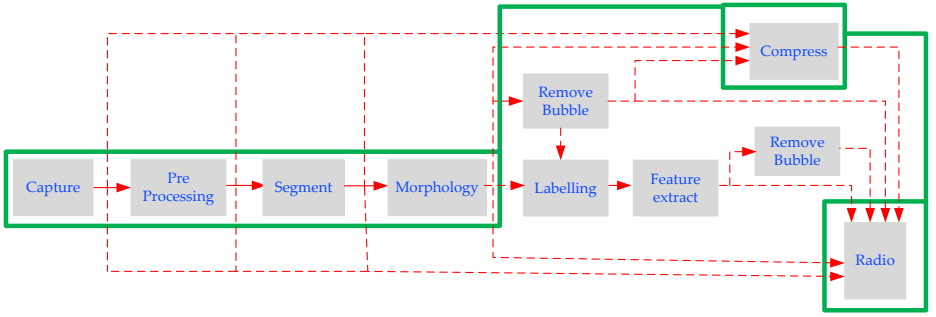




STRATEGY13

- Data sent is approx. 500 Bytes





LIFETIME WITH SIMULATED POWER

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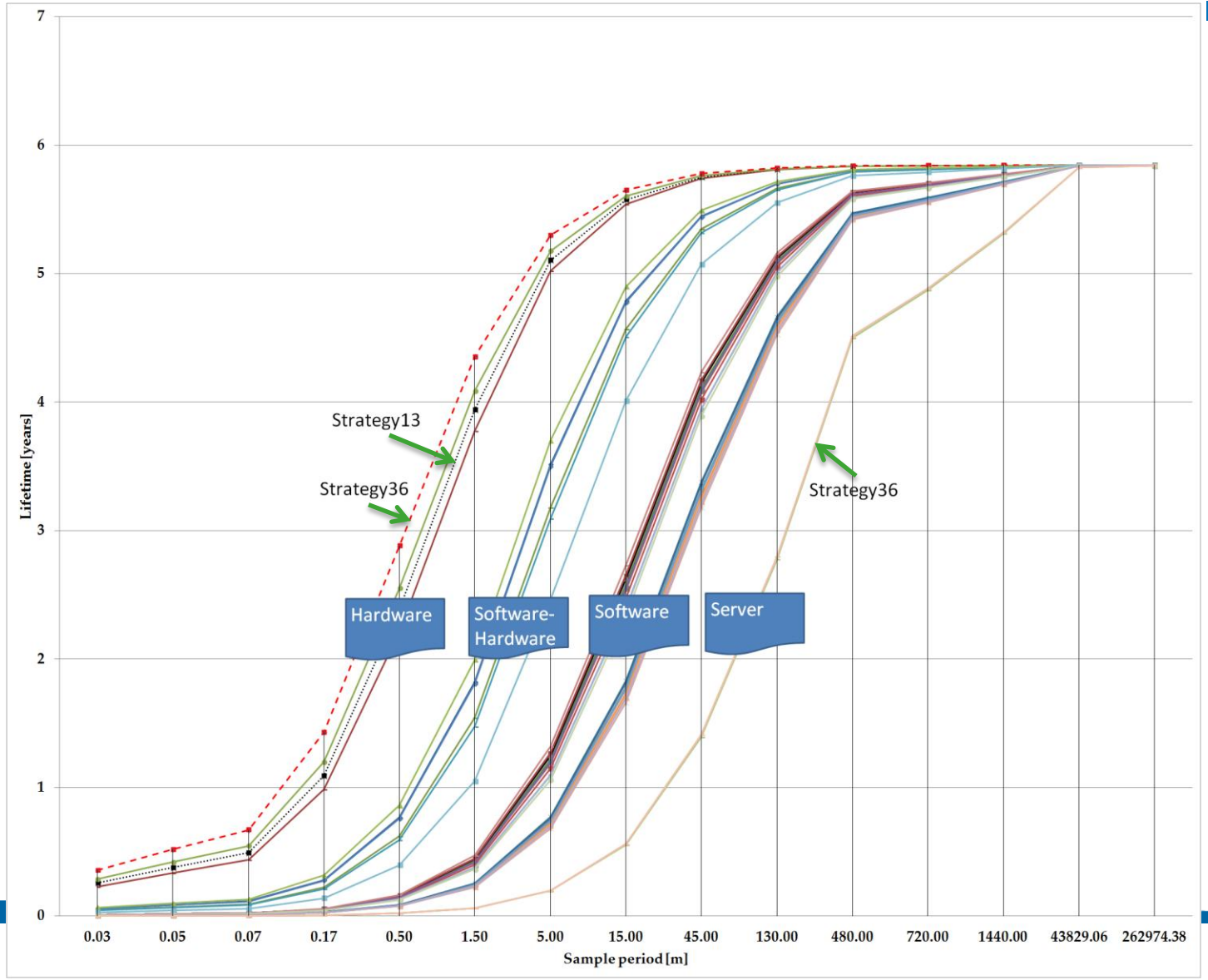

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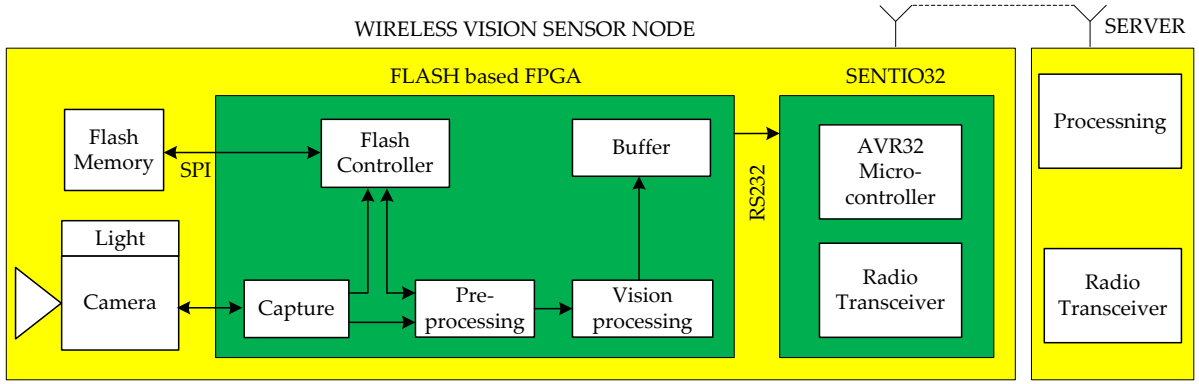
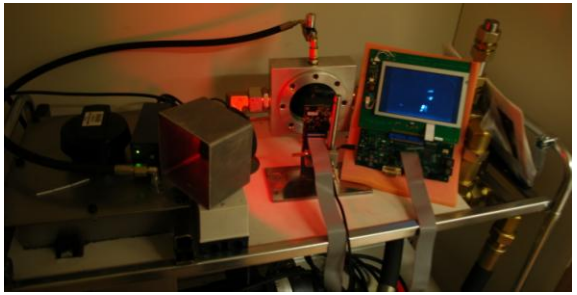
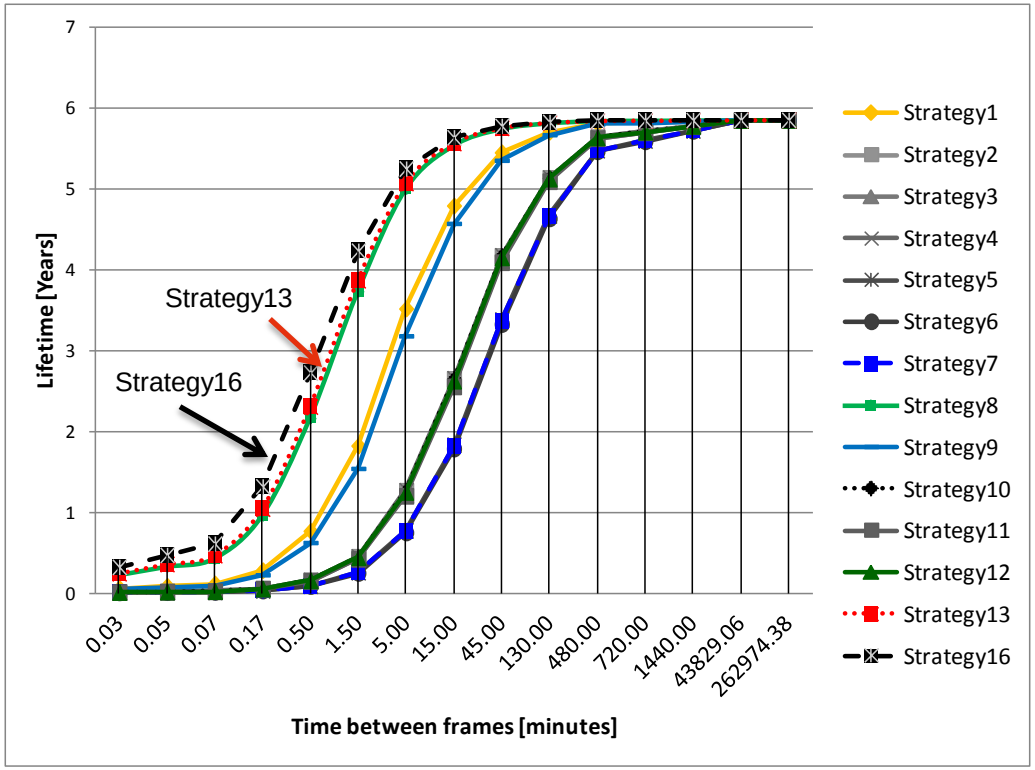
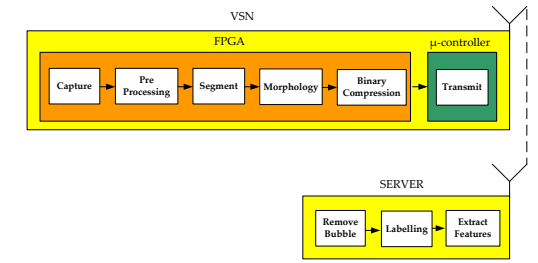
FLASH BASED VSN IMPLEMENTATION



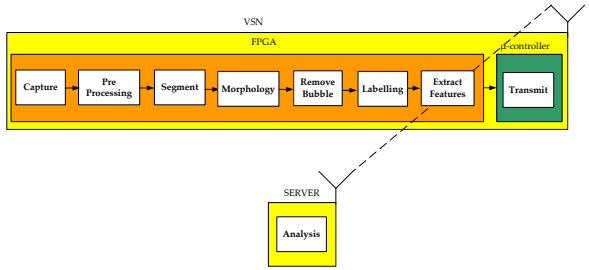


LIFETIME WITH MEASURED POWER



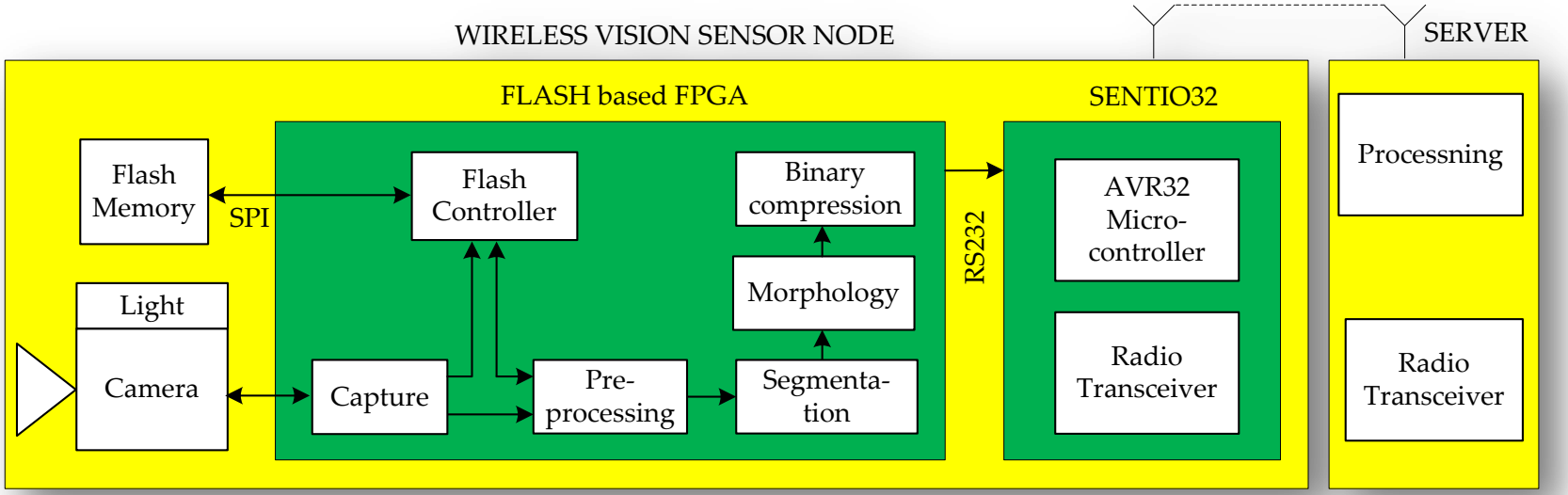


Strategy13

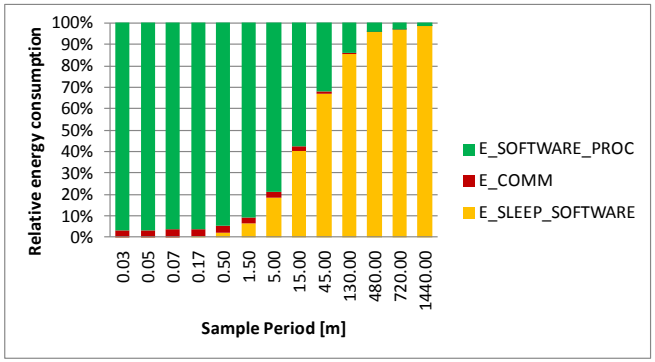


Strategy16

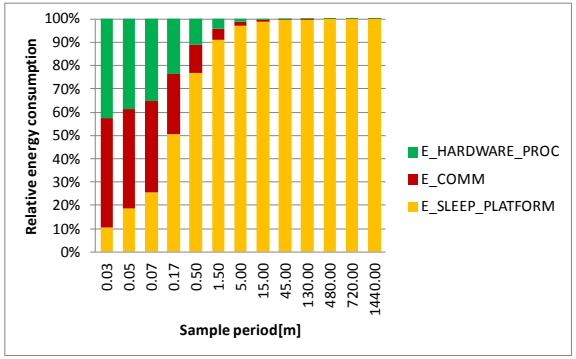
FLASH BASED VSN ARCHITECTURE



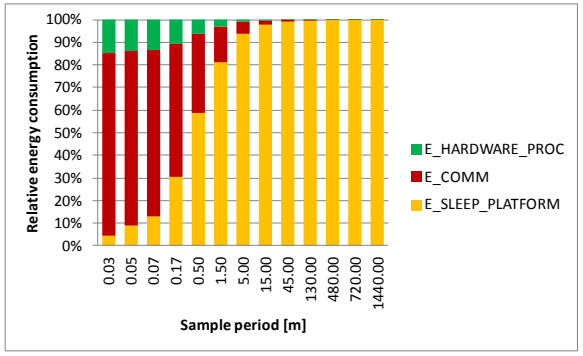
ENERGY CONTRIBUTION VSN



All required vision tasks on software (Strategy34)



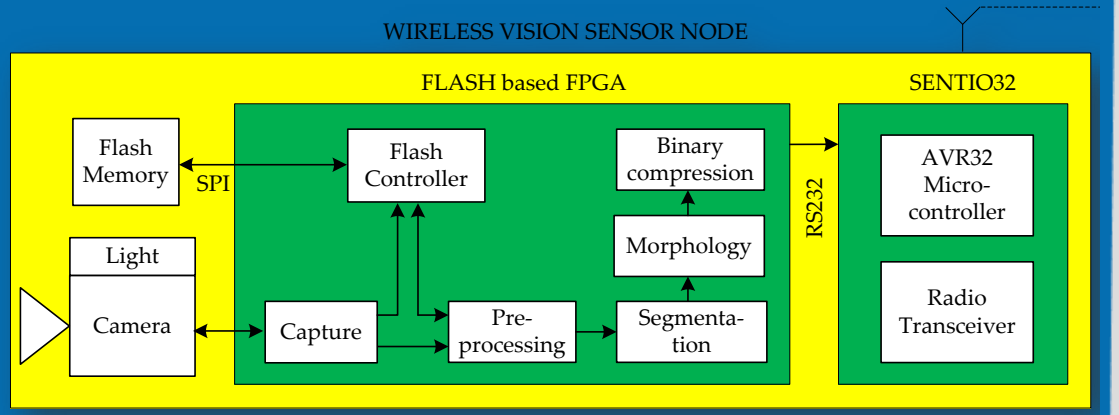
All required vision tasks on hardware (Strategy16)



Front end tasks and binary compression on hardware (Strategy13)

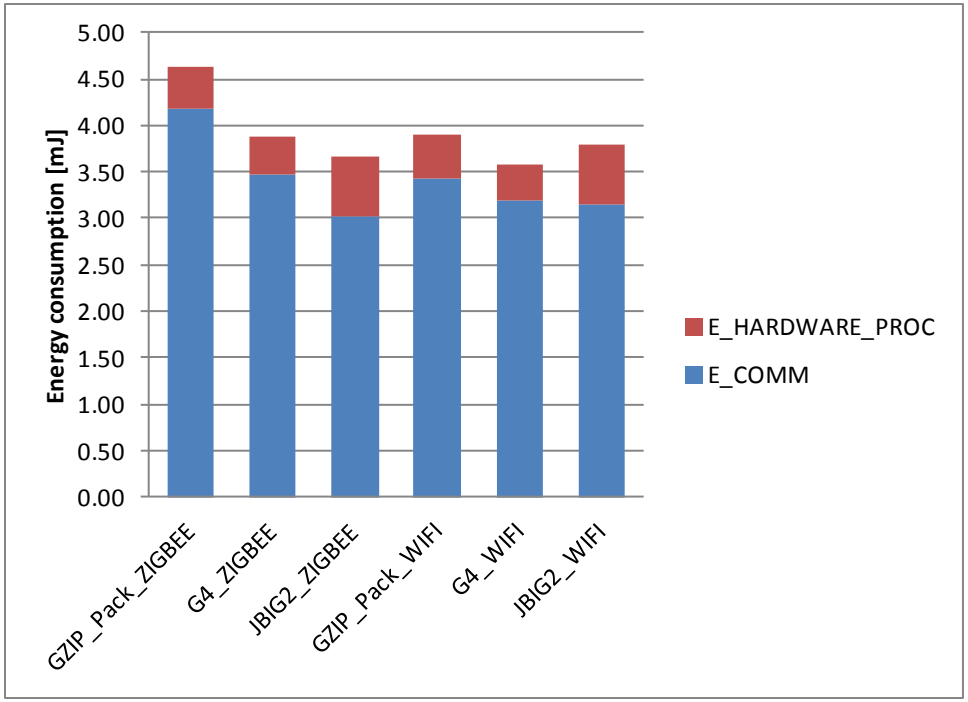
DATA REDUCTION

- Bi-level image coding
- Bi-level video coding



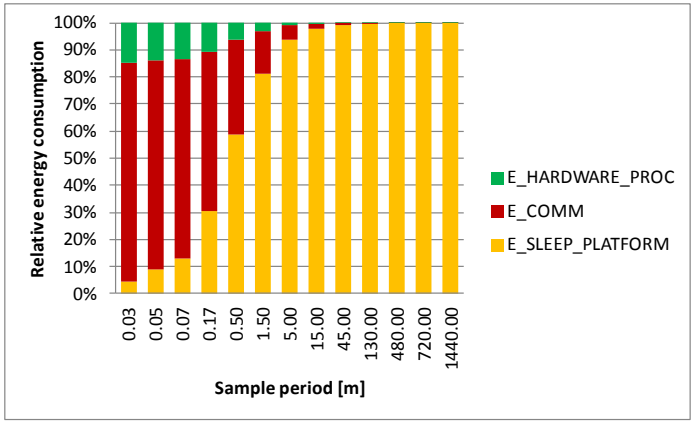
BI-LEVEL IMAGE CODING

- Investigated compression schemes
  - G4
  - G3
  - JBIG2
  - Rectangular
  - GZIP
  - GZIP_pack
  - and JPEG_LS



NEED FOR BI-LEVEL VIDEO CODING

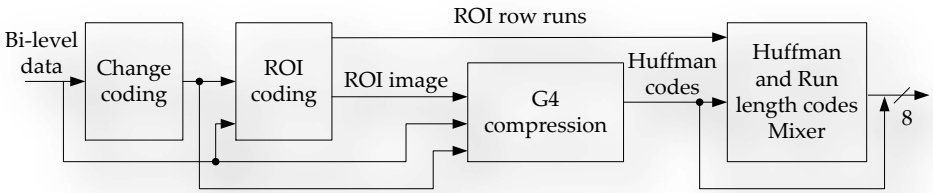
- Data reduction beyond limit of simple image coding.
- Bi-level video codec is required but not available.
- Coding complexity needs to be reduced.

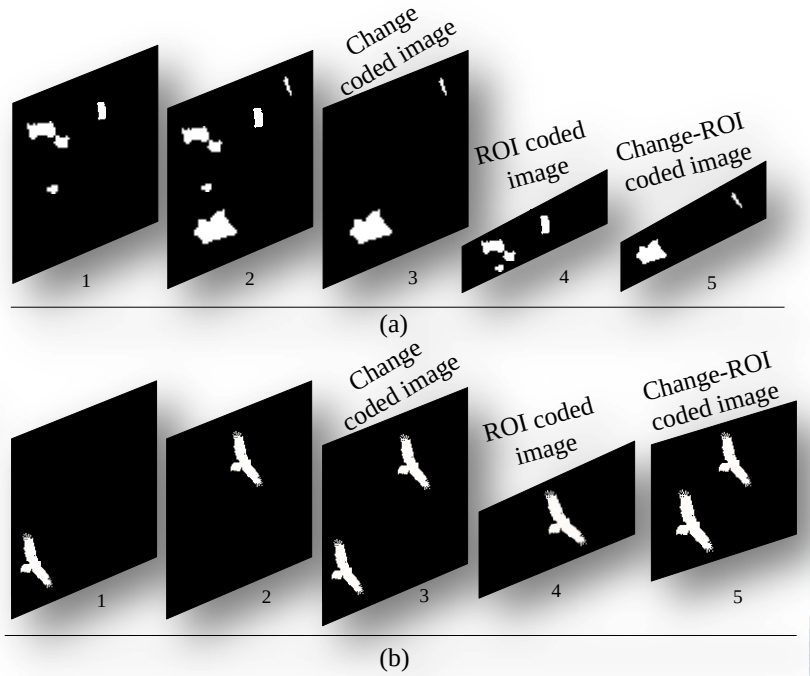


Strategy13

BI-LEVEL VIDEO CODEC

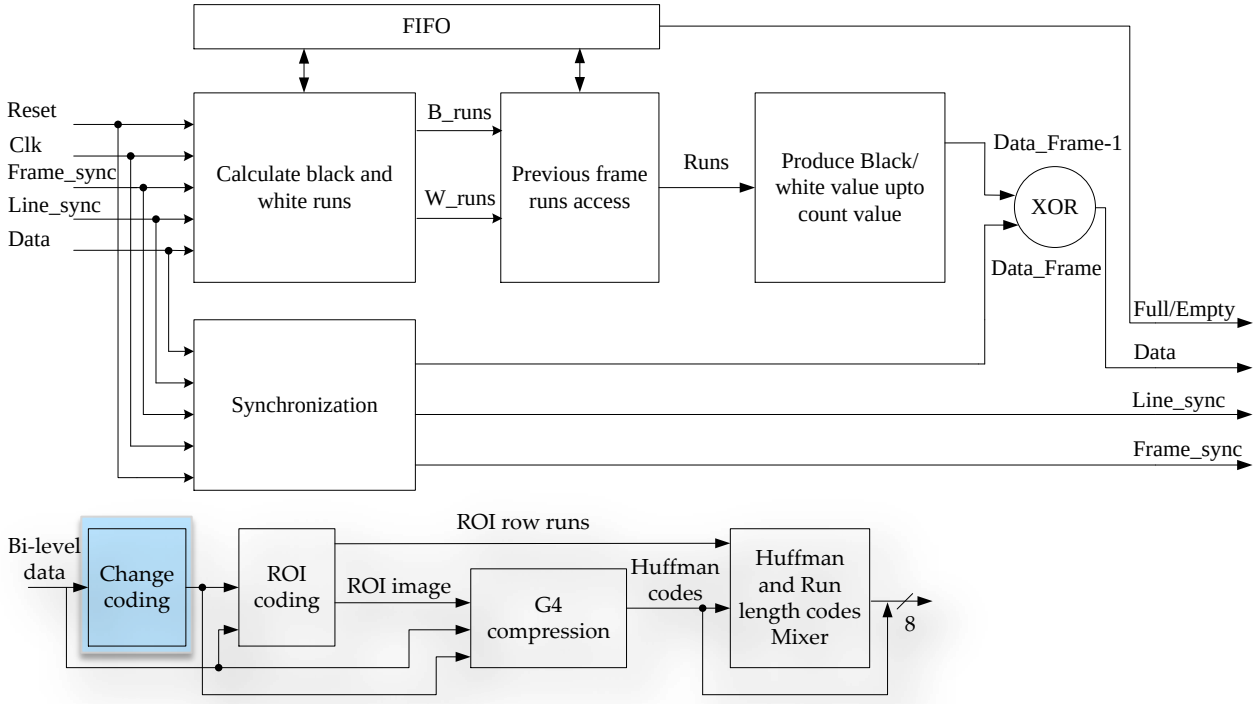
- Bi-Level video codec functionality
  - Image coding
  - Change coding
  - ROI coding
  - Change-ROI coding





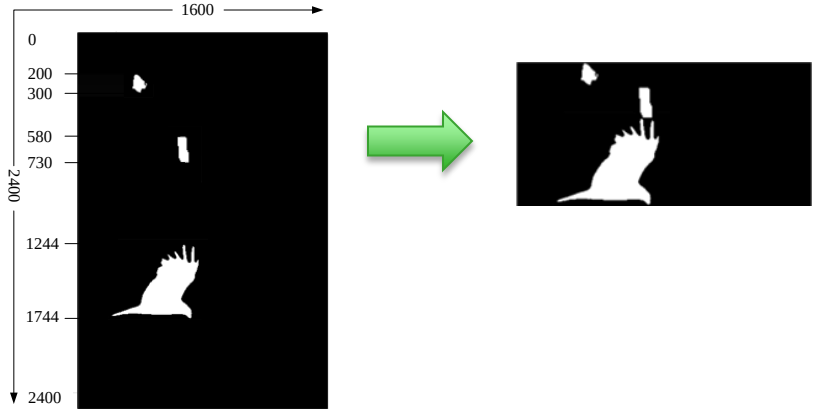
CHANGE CODING

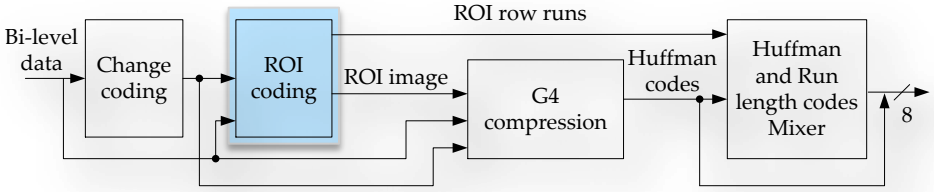
- Only changes are coded.



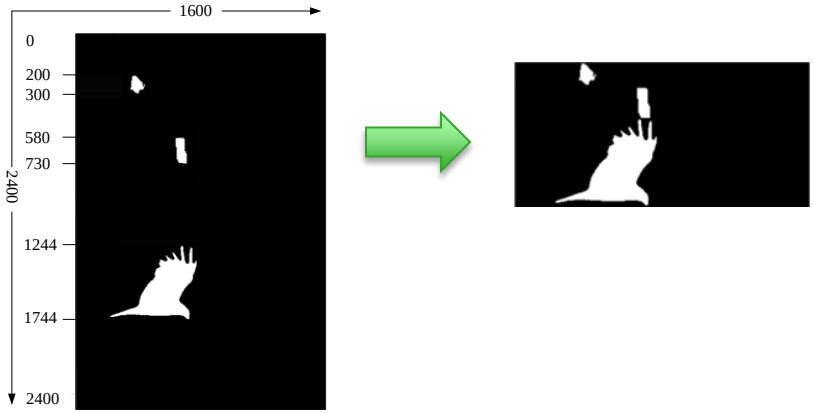
ROI CODING

- Area of image with objects is coded.





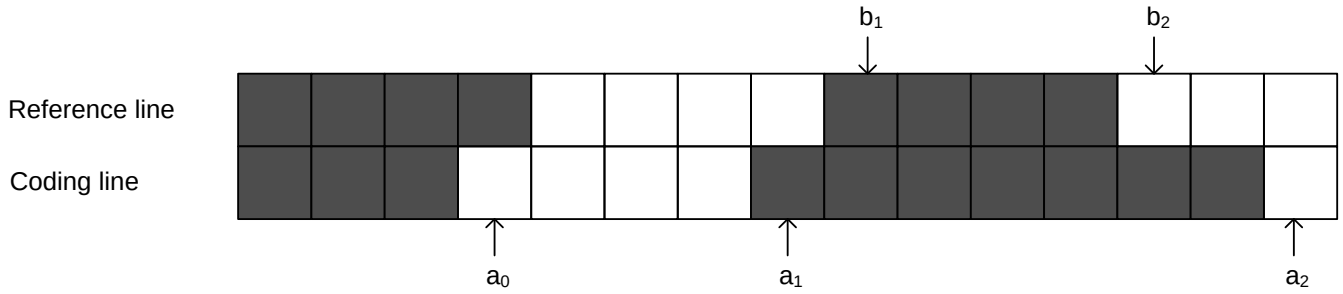
ROI CODING

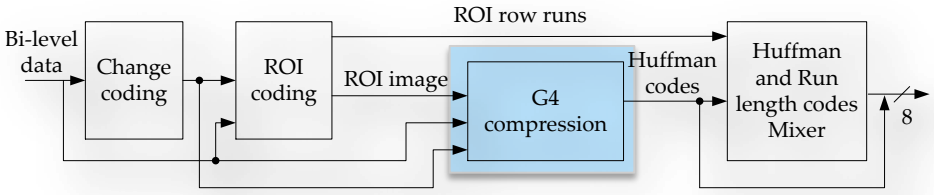


Runs	Symbols colour	Run length coding (8 bits)	Run length coding (9 bits)
200	Black	200,0*	200,0*
100	White	100	100
280	Black	0,25	280
656	Black	0,0,146	0,145

G4 COMPRESSION

- G4 used 2-Dimensional line by line coding.
- In this, the position of changing picture elements rather than alternating black and white runs are calculated.





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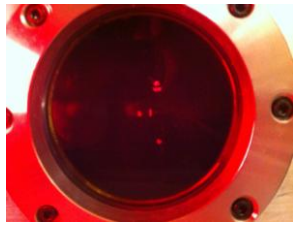
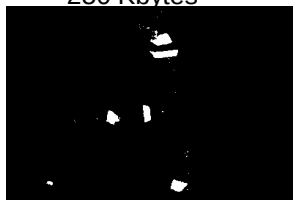
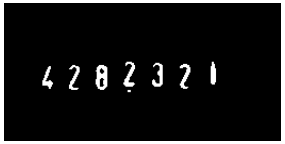
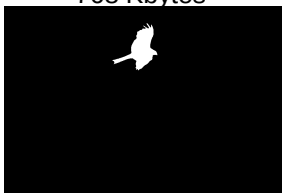
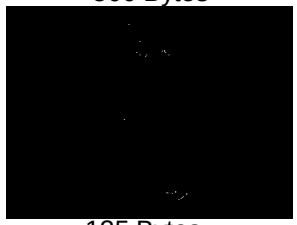
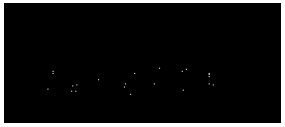
	Particle detection	Meter reading	Bird detection	People counting
Input Images	 250 Kbytes	 250 Kbytes	 768 Kbytes	 200 Kbytes
Image coding	 500 Bytes	 585 Bytes	 411 Bytes	 2060 Bytes
Change coding	 125 Bytes	 150 Bytes	 667 Bytes	 2552 Bytes
ROI coding	 223 Bytes	 203 Bytes	 249 Bytes	 1716 Bytes
Change-ROI coding	 33 Bytes	 65 Bytes	 517 Bytes	 2605 Bytes

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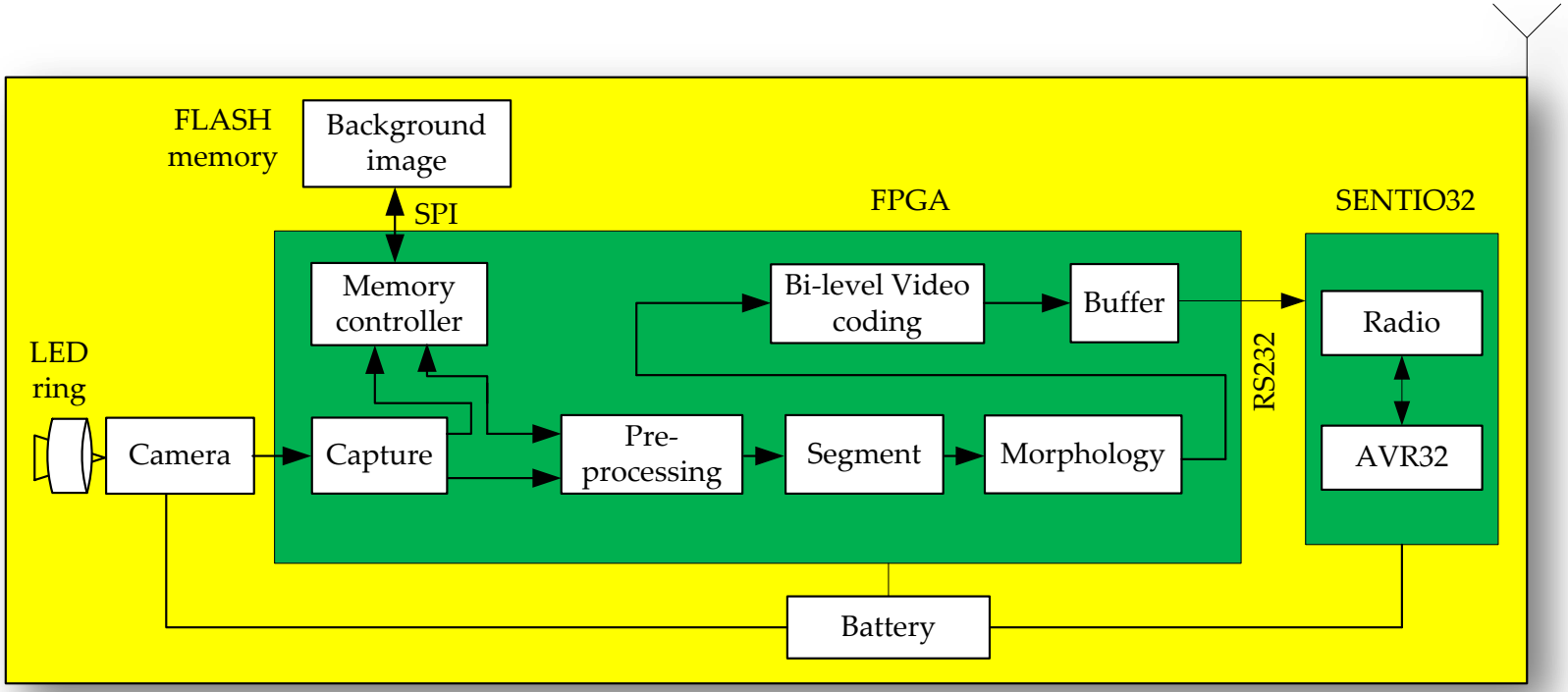
VSN WITH BI-LEVEL VIDEO CODEC



COMPARISON OF SYSTEMS

- Reduced energy consumption of 1.5 to 376 times.
- Reduced output data by a factor of approximately 3 to 246.

Applications	Systems	E_Proc (mJ)	E_Comm (mJ)	Avg. Output data (bytes)	Bits/ pixel	Max. Freq. (FPS)
Particle detection	Published [8]	0.63	3.52	500	0.016	60
	Proposed	2.04	0.38	33	0.001	100
Meter reading	Published [2]	430.3	207.9	6912	0.500	0.04
	Published_scaled [2]	515.3	478.3	16000	0.500	0.03
	Proposed	2.04	0.60	65	0.002	100
Bird detection	Conventional	6.03	4.9	703	0.007	33
	Proposed	5.76	1.83	249	0.003	33
People counting	Published [3]	0.004	4.29	2048	2.000	15
	Published_scaled [3]	0.08	27.06	51200	2.000	5
	Proposed	1.57	11.6	1715	0.067	18

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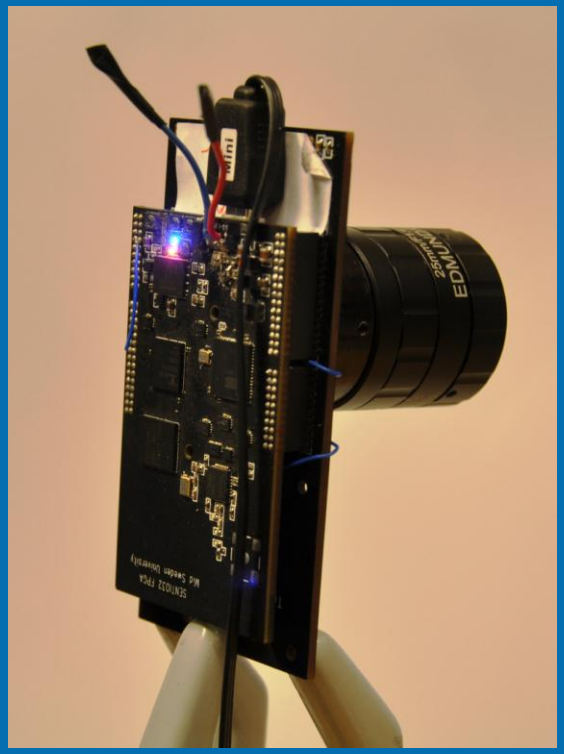
FPGA BASED VSN: SENTIOF-CAM

- SRAM based FPGA for duty cycling
- Low complexity background subtraction



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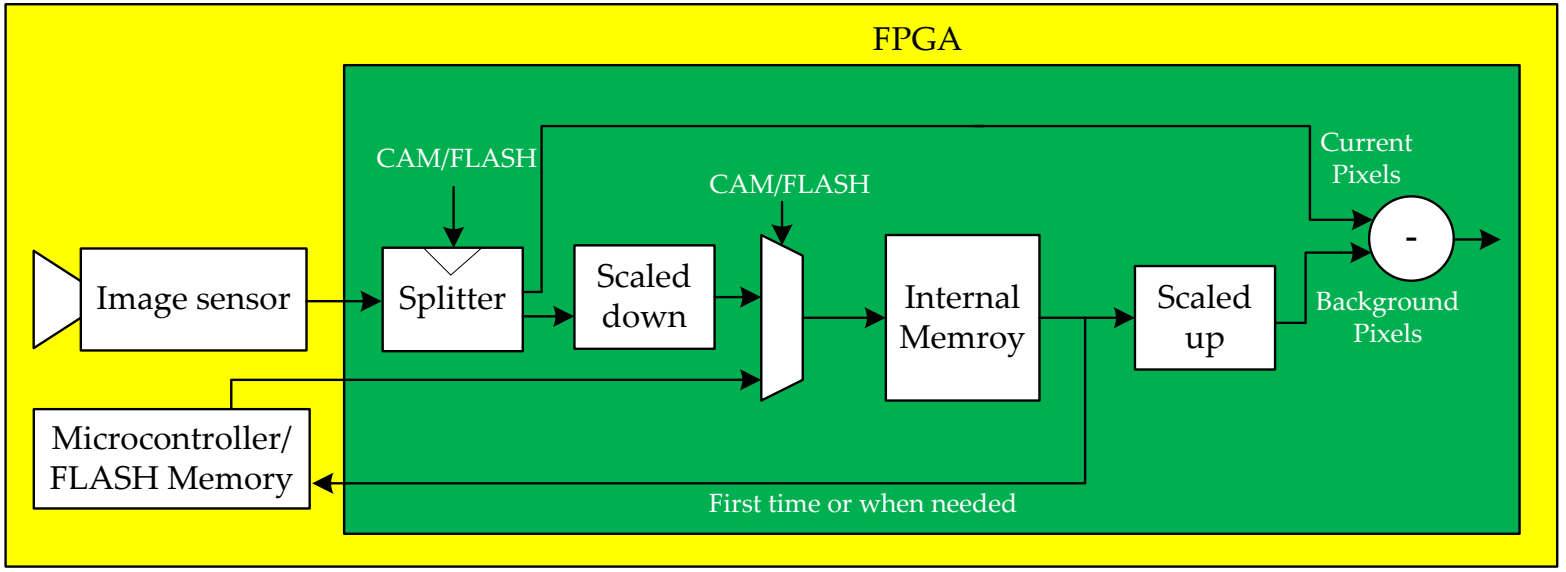
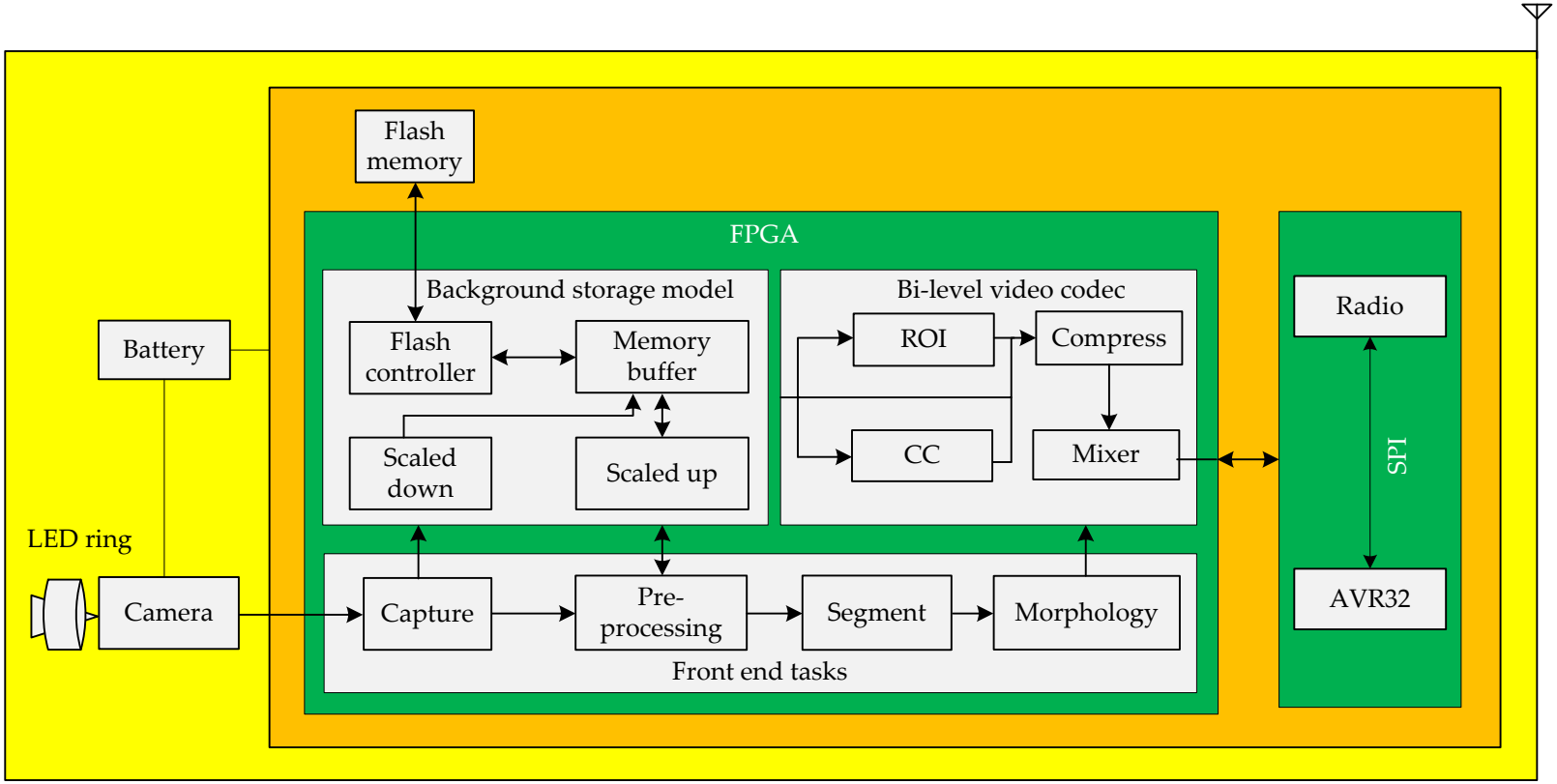
LOW COMPLEXITY BACKGROUND

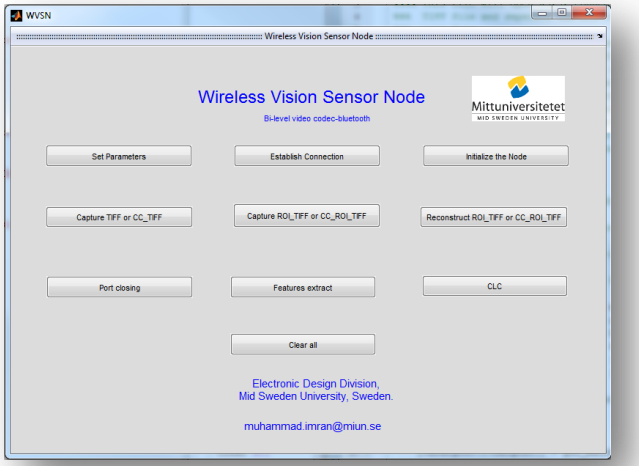


VSN ARCHITECTURE

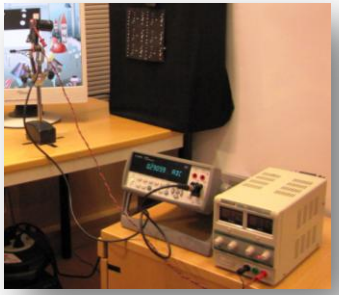


SETUP: SENTIOF-CAM

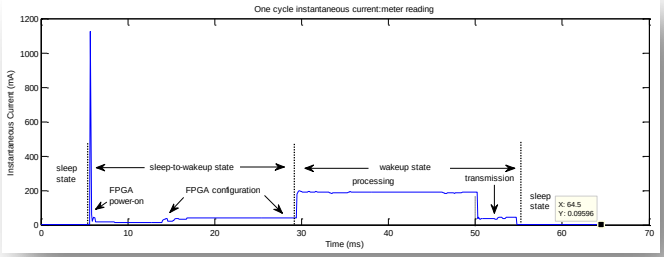
SENTIO32 SENTIOF-CAM GUI and received data FOV



GUI

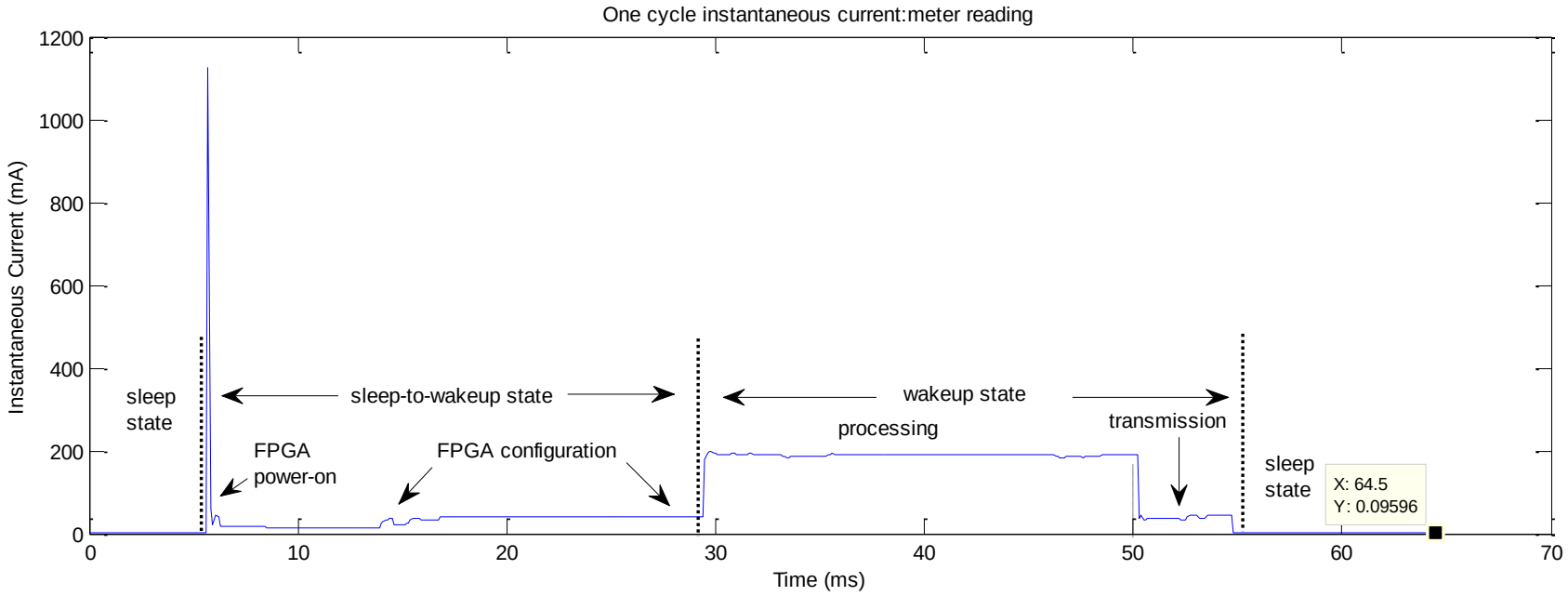


Measurement setup



Instantaneous current for a duty cycle

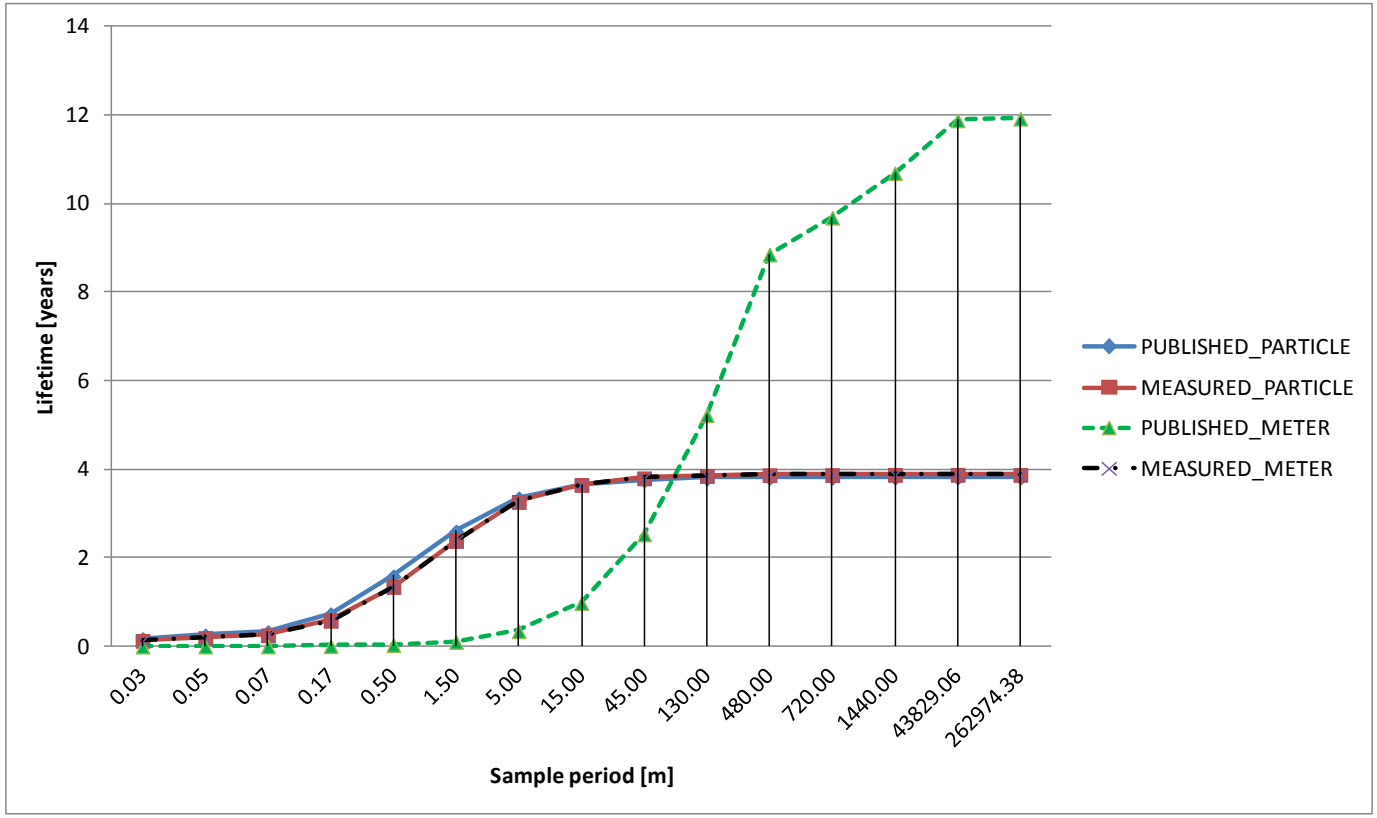
CURRENT MEASUREMENT FOR DUTY CYCLE



POWER AND TIME OF DIFFERENT PROCESSES

Applications	Config. time (ms)	Config. power (W)	Proc. time (ms)	Proc. power (W)	Comm. Time (ms)	Comm. power (W)	Total energy (mJ)
Particle detection	23.6	0.12	21	0.67	3.2	0.13	17.2
Meter reading	23.6	0.12	21	0.67	4.3	0.13	17.4

LIFETIME


14
12
10
8
6
4
2
0
Lifetime [years]
0.03
0.05
0.07
0.17
0.50
1.50
5.00
15.00
45.00
130.00
480.00
720.00
1440.00
43829.06
262974.38
Sample period [m]
PUBLISHED_PARTICLE
MEASURED_PARTICLE
PUBLISHED_METER
MEASURED_METER

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CONCLUSION

- An energy efficient and programmable VSN is developed and implemented.
  - Low complexity
  - Generic architecture
- To reduce communication energy on hardware implemented VSN, a bi-level video coding is developed and implemented.
- A VSN with proposed Bi-level video coding reduced energy consumption by a factor of 1.5 to 376.
- A VSN with SRAM based FPGA has been evaluated for duty cycle applications.
  - Depending on application a lifetime of 3.2 years with 37 kJ energy (AA).

FUTURE WORK

- This study can be extended for applications which require greyscale or colour data for classification.
- Bi-level video coding which handle movement of objects.
- A taxonomy which has been proposed can be improved by making it more exhaustive.
- Wireless smart camera technology can be integrated for Internet of things.

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THANKS!

- Prof. Mattias O'Nils
- Najeem Lawal
- Prof. Bernhard Rinner
- Committee members
- All audience

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