Calculating Power consumption using XPower Analyzer with VCD file from Modelsim and ISiM

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Xilinx Power Analyzer (XPA) does an analysis on real design data. Use XPA after design implementation in ISE, using the NCD file output from Place & Route (PAR). XPA now features a vectorless estimation algorithm; a way of assigning activity rates to nodes even if these activity rates are not defined in the design file or specified in any other way. However, we recommend using simulation activity files (SAIF or VCD) from simulation for accurate power analysis. We recommend always using the latest version of ISE to get the latest version of XPA, which contains the latest characterization data for power analysis.

XPA is used for design power optimization. At the point in your design phase when XPA is used, your ISE project should have successfully completed Place & Route (PAR) and generated an NCD output file

1. In the Processes tab, right-click **XPower Analyzer**.
2. Select **Process Properties**.
3. In the XPower Analyzer Properties dialog box, specify the files.

In the standalone tool, you will have the option to include these files when you load the design. Specify the files to include in the Open Design dialog box.
The files you can specify to add information to your analysis are:

- **NCD** - Output file from PAR that is required by XPA for power analysis.
- **Settings file** - Optional file. The Settings file contains application settings and node activity rates saved from an XPower Analyzer session. Any manual changes (edits) you have made in the XPA window can be saved to a settings file. The settings file (in XML format) can then be used to load any relevant design information from a previous XPA session into a later session.
- **PCF** - Optional file. The PCF (Physical Constraints File) contains constraint information to help determine clock frequencies. All clock information from the UCF (User Constraints File) are reported in the PCF, so if the design is well constrained loading the PCF is important for accurate power results.

- **VCD or SAIF file** - Optional file. These simulation activity files include specific switching information (toggle rates, signal rates, and frequency information) that will give the most accurate power estimation. Note that XPA might not always be able to match all of your design nets with nets in the simulation file so you may have to enter some switching information manually. It is important to make sure you look at what design information was pulled in and what (if any) design information was not pulled in. In the Console window take note of any warning messages, since they may indicate that design information was not pulled into XPA.

All other files are generated when design has completed Plaxe and Route (PAR).

VCD file Genereation

The recommended XPower flow uses a VCD file generated from post PAR simulation. To generate a VCD file, you must have a Xilinx supported simulator. See the *Synthesis and Simulation Design Guide* for more information.
XPower supports the following simulators:
• ISE Simulator (ISM)
• ModelSim
• Cadence Verilog XL
• Cadence NC-Verilog
• Cadence NC-VHDL
• Cadence NC-SIM
• Synopsys VCS
• Synopsys Scirocco
XPower uses the VCD file to set toggle rates and frequencies of all the signals in the design.
Manually set the following:
• Voltage (if different from the recommended databook values)
• Ambient temperature (default = 25 degrees C)
• Output loading (capacitance and current due to resistive elements)
For the first XPower run, voltage and ambient temperature can be applied from the PCF, provided temperature and voltage constraints have been set.
Xilinx recommends creating a settings file (XML). A settings file saves time if the design is reloaded into XPower. All settings (voltage, temperature, frequencies, and output loading) are stored in the settings file. See the "-wx (Write XML File)" section of this chapter for more information.

VCD file Generation using Modelsim

For VHDL simulations, the commands to generate a VCD file must be entered interactively, or contained in a do file.

```
vcd file my_design.vcd
vcd add testbench/uut/*
```

This technique will work for both VHDL and Verilog in ModelSim.

Note: When creating a VCD file using the NC simulator, the command must include the -f switch.

The above lines generate a VCD file called my_design.vcd. The entity name of our testbench is testbench and the instance name of the unit under test is uut.

Or the most simple way could be typing this in the Transcript window of Modelsim

```
vcd file my_design.vcd
vcd add *  // This command adds the specified objects to a VCD file [5].
```

vcd flush // This command flushes the contents of the VCD file buffer to the specified VCD file [5].

VCD file Generation using ISiM

```
vcd dumpfile file_name.vcd
vcd dumpvars -m UUT -l 0
run 30 ms
vcd dumpflush
```

in my case, file_name is *vcd_capture_module* UUT is *sim_3x3_08bits.*

Explanation of above commands

-m <*module_name*> dumps the module of that name

-l

0 - Level 0 causes a dump of all variables in the specified module and in all module instances below the specified module. The argument 0 applies only to subsequent arguments which specify module instances, and no to individual variables.
1 -Level 1 dumps all variable within the module specified by -m; it does not dump variables in any of the modules instantiated by the module specified by -m.

Dumpflush
Empties the operating system's VCD file buffer to ensure that all the data in that buffer is stored in the VCD file. After executing, dump process resumes as before so no value changes are lost. Invokes Verilog $dumpflush directive.

XPower Analyser Steps

Step 1

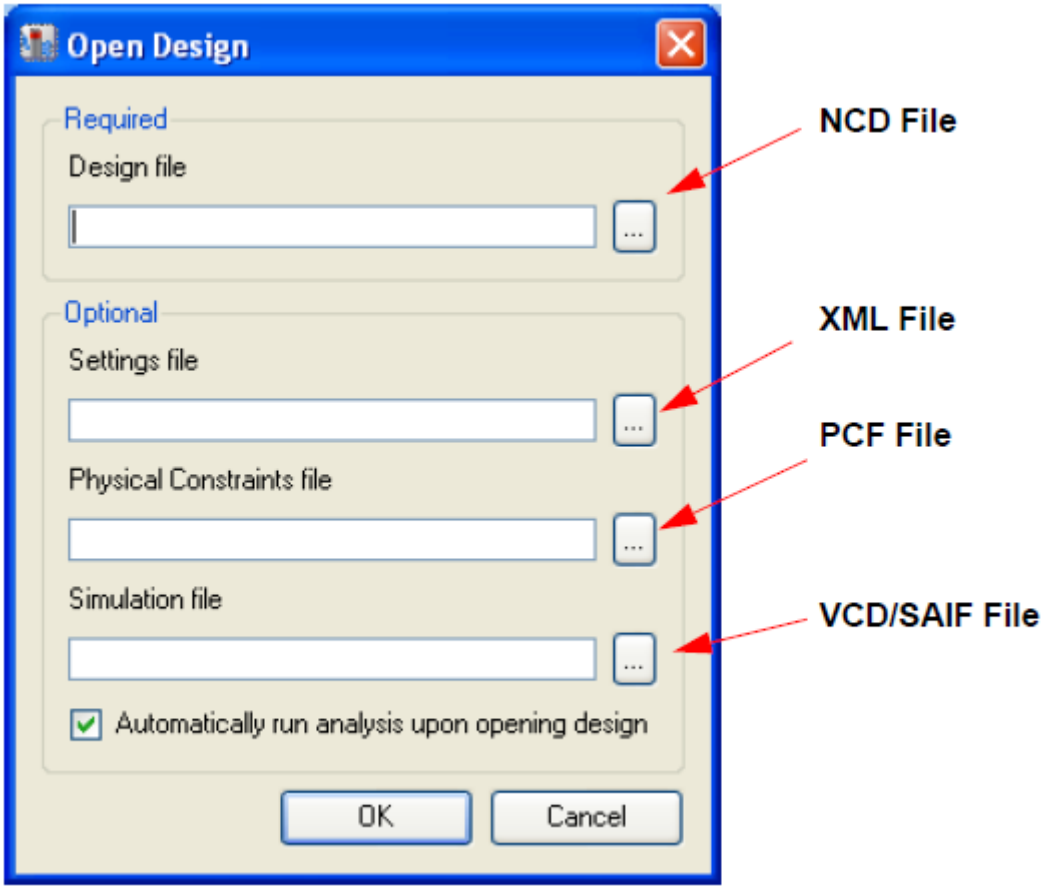
Open XPA

In ISE, in the Processes tab, double-click the **XPower Analyzer** process, located under **Place & Route**.

Step 2

In XPA, open the design files in this way:

1. Select **File > Open Design**.



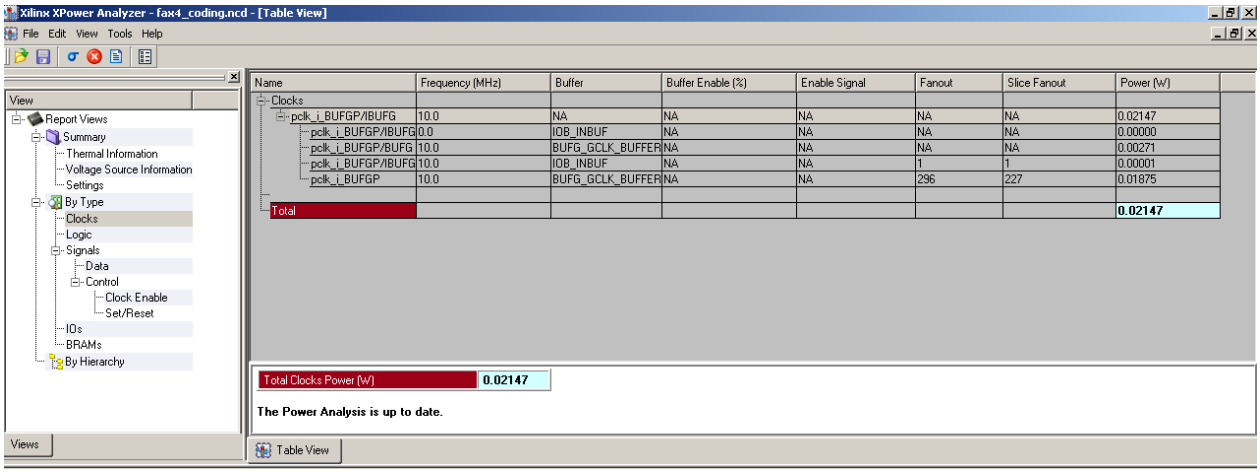
Step 3

Give all the path of all files

Step 4

For a design in which no VCD or SAIF stimulus file is available yet, you can use the **Settings** view to enter estimated activity rates for all different design elements. The vectorless analysis engine will then propagate these settings to your design.
Note that activity rates from the **Settings** view are used by XPA as initial inputs for the vertorless propagation engine. If you want to set the **By Type** entries (for example, the enable rate for BRAMs or the toggle rate for DSPs)

In the **Clocks** view (under **By Type**), make sure all clock frequencies have been correctly extracted from the Physical Constraints File (PCF). If the clocks in your design were properly constrained in the UCF (User Constraints File) before implementation then frequencies should be correctly extracted from the PCF (Physical Constraints File) in XPA.



When you make any changes in the setting , update these changes by clicking on Tools-> update power analysis

References

[1]. *Development System Reference Guide*, Xilinx

[2]. *Xilinx Power Tools Tutorial*, Xilinux.

[3]. http://www.xilinx.com/itp/xilinx5/help/xpower/html/p_procedures/other/p_create_sim_files_vhdl.htm

[4]. http://bwrc.eecs.berkeley.edu/classes/cs152/projects/lab5.htm

[5]. http://www.microsemi.com/document-portal/doc_view/134097-modelsim-command-reference-manual-v10-3a

Note:

This document is just for having quick references to these tutorials.

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