Interfacing Thermal and Visual Camera with FPGA based Nexus4 Board

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This is a reference document for interfacing tamarisk 320 thermal camera with Nexus4 FPGA based board by using PMOD pins. Tamarisk 320 camera comes with two options, feature board and without feature board. The camera without feature board (base configuration) offers digital output in the form of 8-bit or 14-bit parallel digital video, 8-bit, 14-bit camera link video and shutter control though 60-pin connector. This configuration requires user to develop an interface board because the 60 –pins are not easily accessible. The interface board, developed by one of my colleague Matthias Kramer at Mid Sweden University is shown in Figure 1.

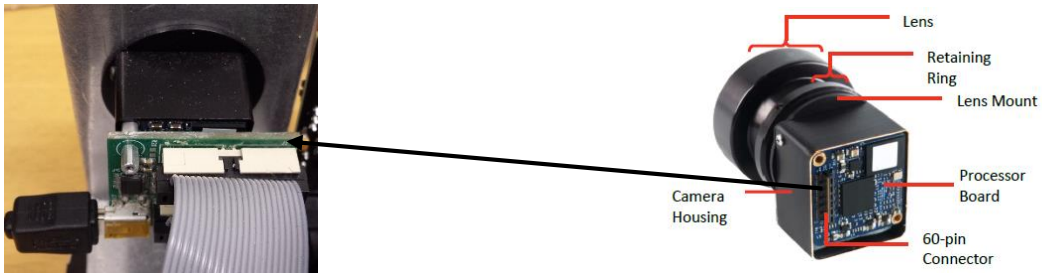

Figure 1. Camera interface board and cables

When colorization is disabled, the digital output video is 8 bit or 14 bit. Figure 2 shows that 8-bit video is coming after Automatic Gain Control (AGC) process whereas 14-bit video is coming before AGC process. It is important to note for configuration that in 8-bits, BDSI_D13 is MSB and BDSI_D06 is LSB.

Controlling the camera through FTDI

The output from the base configuration can be controlled with DRC control software. In our case, FTDI is used for sending the commands to control the camera as shown in Figure 3. In the software, RS232 serial, with right combination of COM port and Baud rate of 57600 has been used to establish connection with camera since these are default parameters.

The frame format is always 320 columns by 240 rows of progressive scan (4:3)

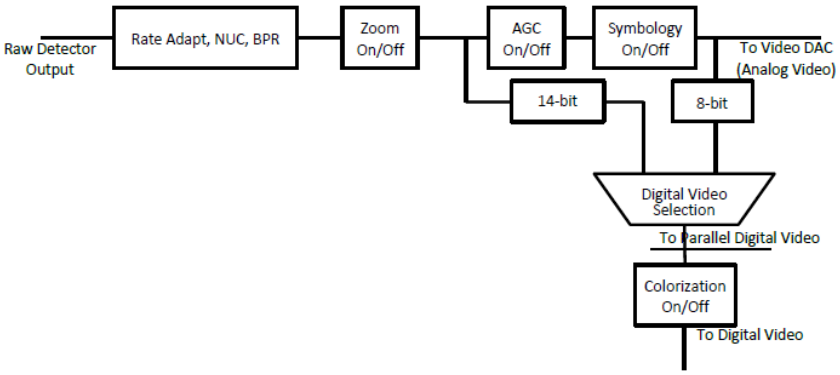

Figure 2. Thermal cam block diagram for video output

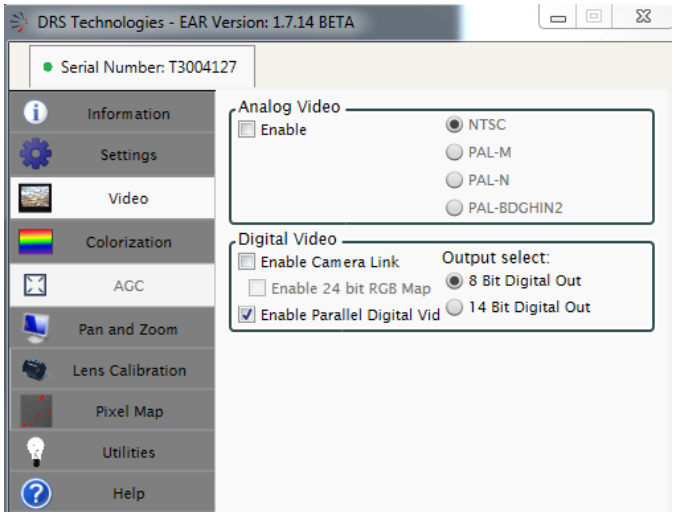

Figure 3. Control interface from DRS

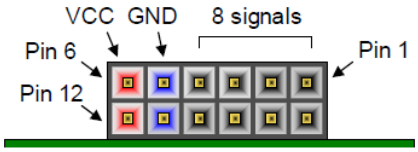

Figure 20. PMOD Connectors- Front view as loaded on PCB

Pmod JA	Pmod JB	Pmod JC	Pmod JD	Pmod XDAC
JA1: B13	JP1: G14	JC1: K2	JD1: H4	JXADC1: A13
JA2: F14	JB2: P15	JC2: E7	JD2: H1	JXADC2: A15
JA3: D17	JB3: V11	JC3: J3	JD3: G1	JXADC3: B16
JA4: E17	JB4: V15	JC4: J4	JD4: G3	JXADC4: B18
JA7: G13	JB7: K16	JC7: K1	JD7: H2	JXADC7: A14
JA8: C17	JB8: R16	JC8: E6	JD8: G4	JXADC8: A16
JA9: D18	JB9: T9	JC9: J2	JD9: G2	JXADC9: B17
JA10: E18	JB10: U11	JC10: G6	JD10: F3	JXADC10: A18

Figure 4. Nexus4 board pins configurations for PMODs. Snapshot from digilent document "Nexys4™ FPGA Board Reference Manual"

Thermal camera PINS configuration with Nexus4 board, italic text for 8-bits for POST_AGC data

Nexus4/ PMOD JC (UCF)	**Interface board/ J5 on Camera side J1**	**Nexus4/ PMOD JD (UCF)**	**Interface board/ J4 on Camera side J2**
K2	*BDSI_LSYNC*	H4	BDSI_D5
K1	*BDSI_PCLK*	H2	BDSI_D4
E7	*BDSI_D13*	*H1*	*BDSI_D7*
E6	BDSI_FSYNC	*G4*	*BDSI_D6*
J3	BDSI_D1	*G1*	*BDSI_D9*
J2	*BDSI_D12*	*G2*	*BDSI_D8*
J4	BDSI_D3	*G3*	*BDSI_D11*
G6	BDSI_D2	*F3*	*BDSI_D10*

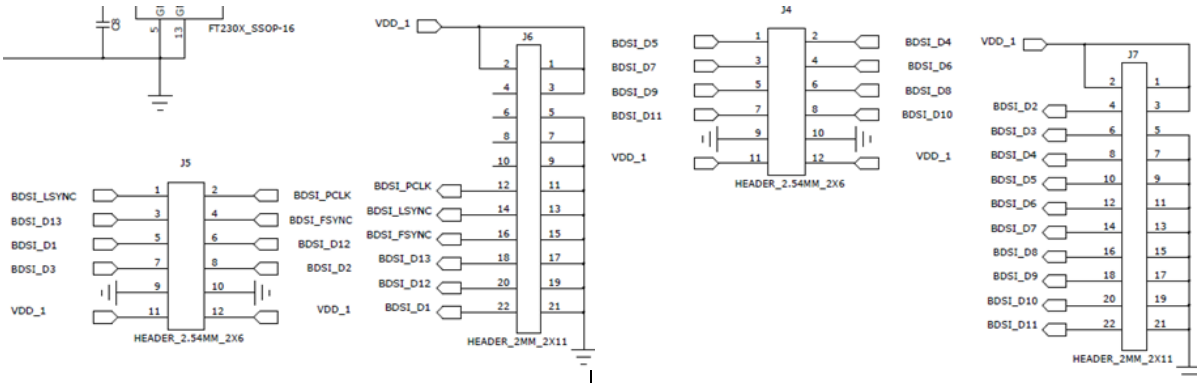

Figure 5. Thermal camera pins configuration schematic (Note: the PINS for J4 and J5 will appear flipped in original documents which needs to be corrected according to this document)

Visual Camera PINS configuration with Nexus4 board

Visual camera PINS configuration with Nexus4 board

Nexus4/ PMOD JA	Interface board/ J8	Nexus4/ PMOD JB	Interface board/ J9
B13	DOUT0	G14	DOUT_LSB0
G13	DOUT1	K16	DOUT_LSB1
F14	DOUT2	P15	LV
C17	DOUT3	R16	SDA
D17	DOUT4	V11	FV
D18	DOUT5	T9	SCL
E17	DOUT6	V15	PIX_CLK
E18	DOUT7		

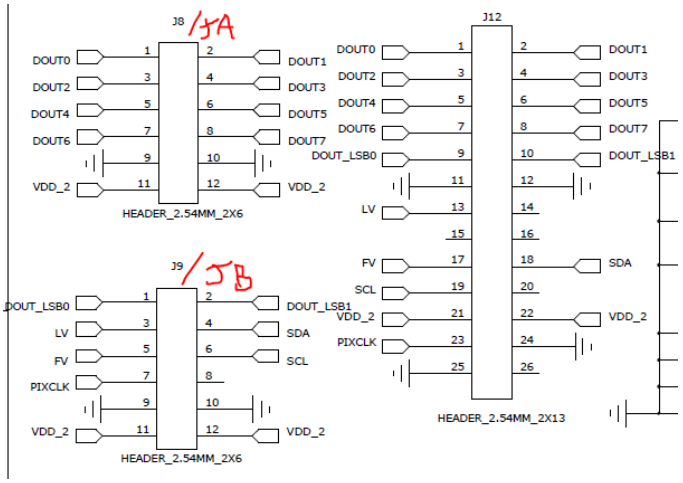

Figure 6. Visual camera pins configuration schematic